

P-Channel 30-V (D-S) MOSFET

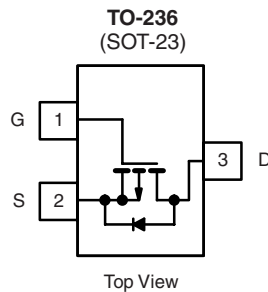
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^b
- 30	0.078 at $V_{GS} = - 10$ V	- 3.2
	0.130 at $V_{GS} = - 4.5$ V	- 2.5

FEATURES

- Halogen-free Option Available
- TrenchFET[®] Power MOSFET



RoHS
COMPLIANT



Si2307BDS (L7)*

* Marking Code

Ordering Information: Si2307BDS-T1-E3 (Lead (Pb)-free)
Si2307BDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted					
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage	V_{DS}	- 30		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150$ °C) ^b	I_D	$T_A = 25$ °C	- 3.2	- 2.5	A
		$T_A = 70$ °C	- 2.6	- 2.0	
Pulsed Drain Current ^a	I_{DM}	- 12			
Continuous Source Current (Diode Conduction) ^b	I_S	- 1.25	- 0.75		
Power Dissipation ^b	P_D	$T_A = 25$ °C	1.25	0.75	W
		$T_A = 70$ °C	0.8	0.48	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^b	R_{thJA}	80	100	°C/W
Maximum Junction-to-Ambient ^c		130	166	

Notes:

- Pulse width limited by maximum junction temperature.
- Surface Mounted on FR4 board, $t \leq 5$ s.
- Surface Mounted on FR4 board.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

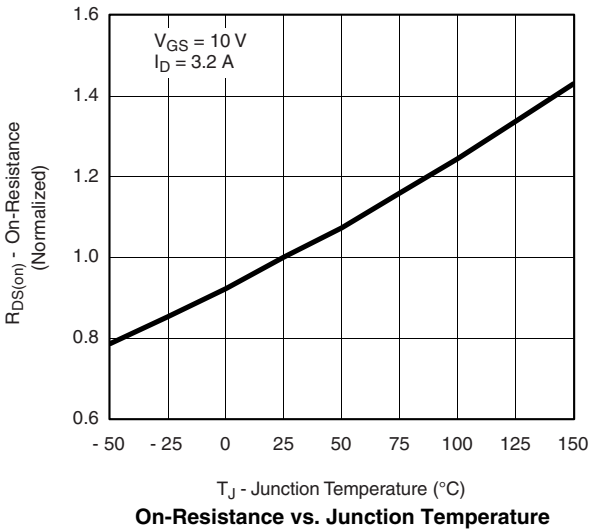
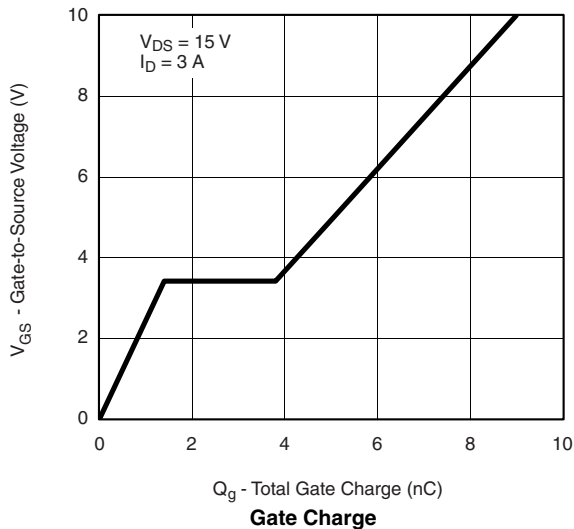
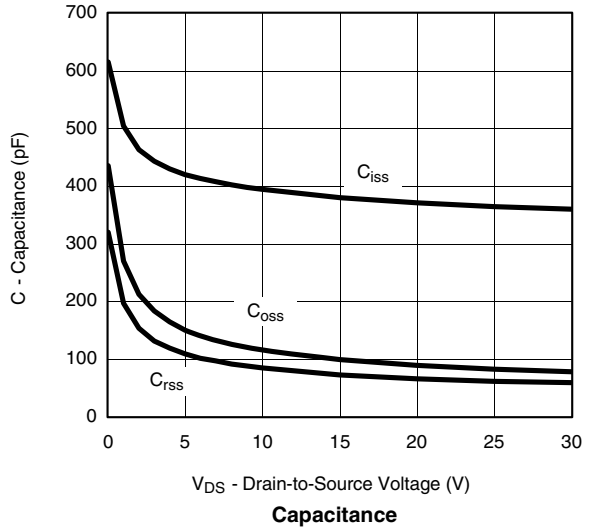
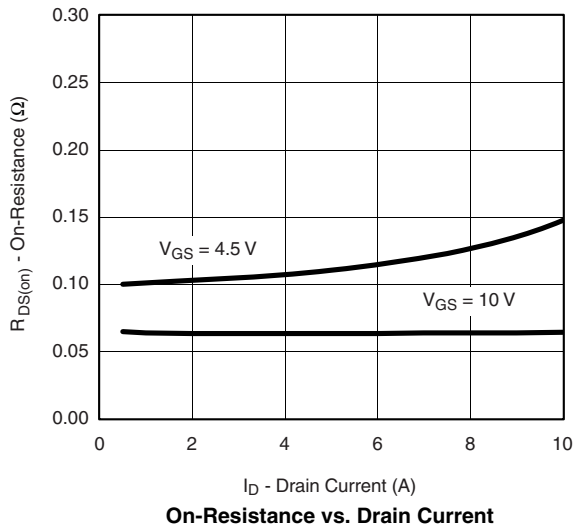
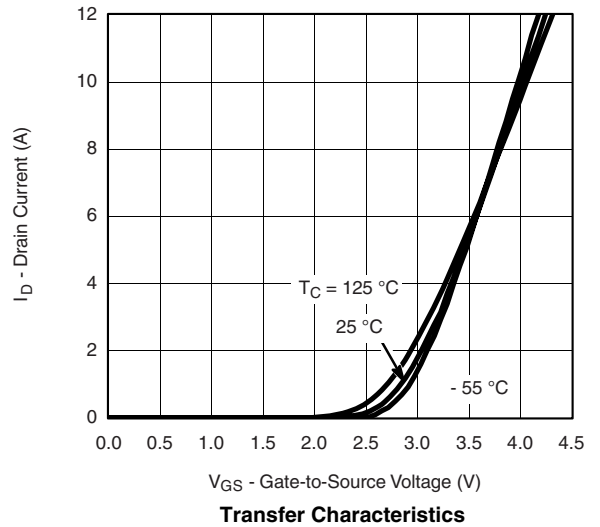
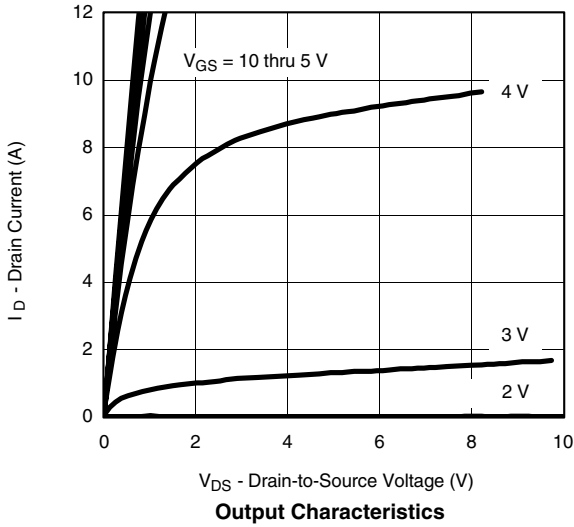
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -10\text{ }\mu\text{A}$	- 30			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1.0		- 3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -10\text{ V}, V_{GS} = -10\text{ V}$	- 6			A
Drain-Source On-Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -3.2\text{ A}$		0.063	0.078	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -2.5\text{ A}$		0.105	0.130	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -3.2\text{ A}$		5.0		S
Diode Forward Voltage	V_{SD}	$I_S = -0.75\text{ A}, V_{GS} = 0\text{ V}$		- 0.85	- 1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}$ $I_D \cong -1.7\text{ A}$		9.0	15	nC
Gate-Source Charge	Q_{gs}			1.4		
Gate-Drain Charge	Q_{gd}			2.4		
Gate Resistance	R_g	$f = 1.0\text{ MHz}$		8.0		Ω
Input Capacitance	C_{iss}	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		380		μF
Output Capacitance	C_{oss}			100		
Reverse Transfer Capacitance	C_{rss}			75		
Switching^c						
Turn-On Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong -1.0\text{ A}, V_{GEN} = -4.5\text{ V}$ $R_g = 6\text{ }\Omega$		9	20	ns
	t_r			12	20	
Turn-Off Time	$t_{d(off)}$			25	40	
	t_f			14	21	

Notes:

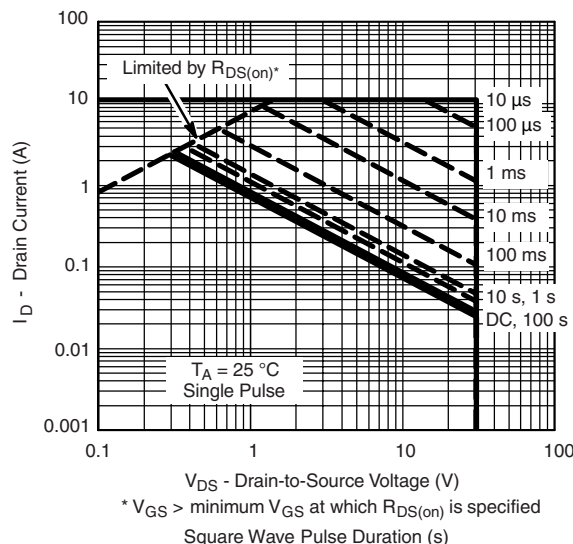
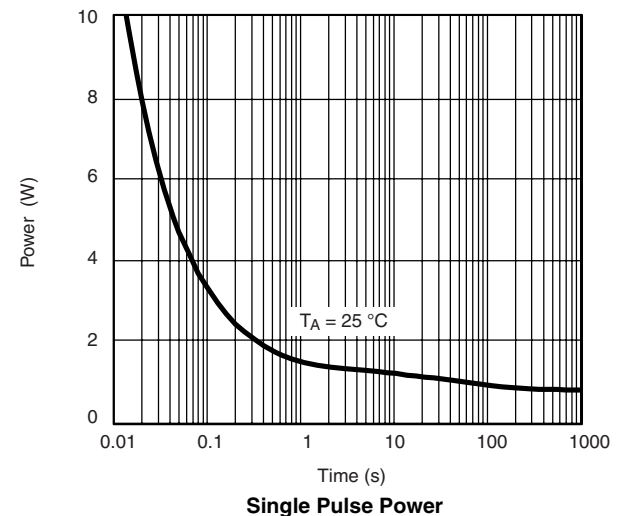
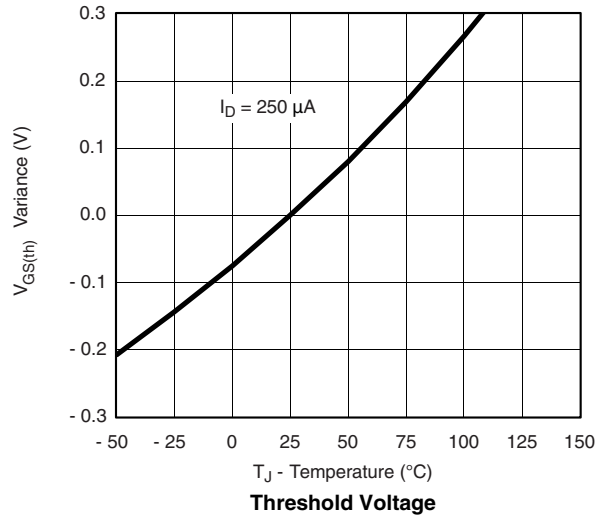
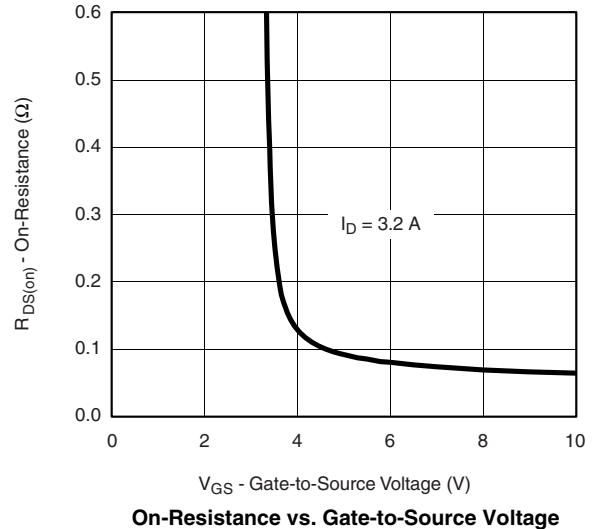
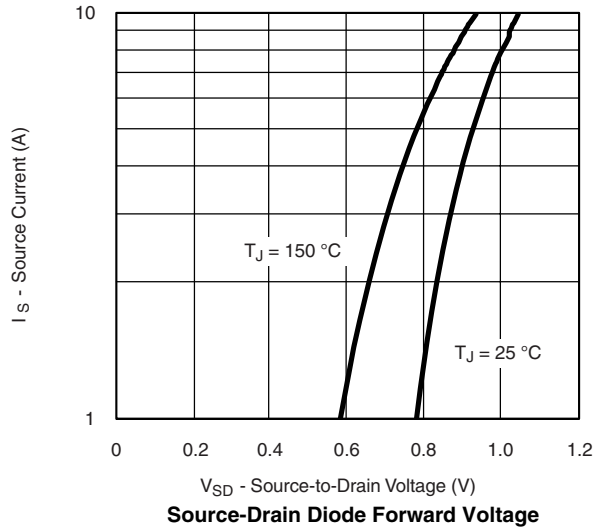
- a. Pulse test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. For DESIGN AID ONLY, not subject to production testing.
c. Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

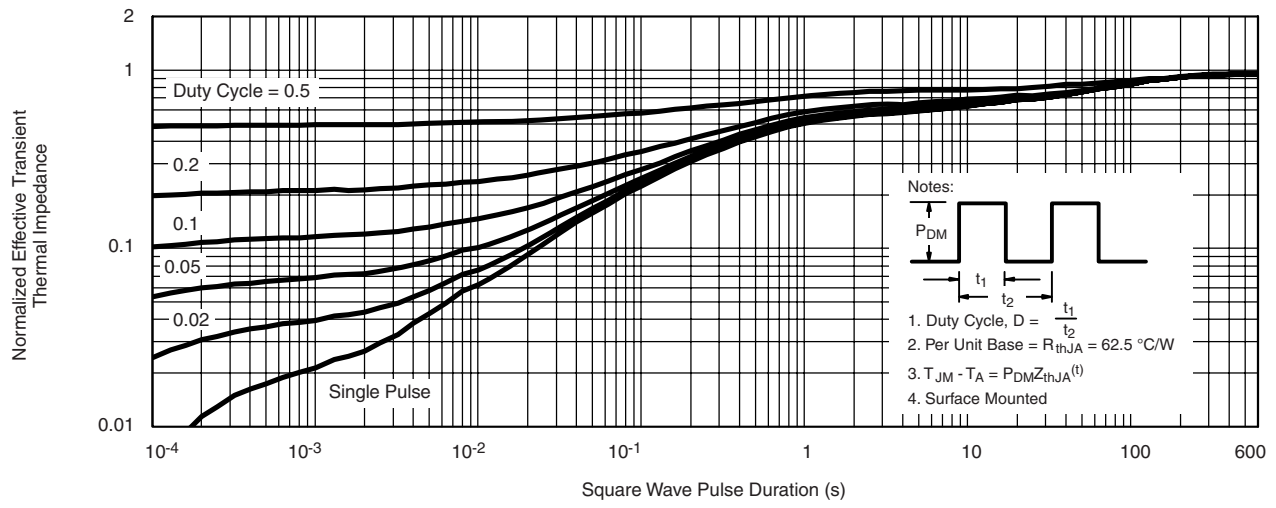
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72699>.

SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A ₁	0.01	0.10	0.0004	0.004
A ₂	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E ₁	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e ₁	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L ₁	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°

ECN: S-03946-Rev. K, 09-Jul-01
 DWG: 5479

Mounting LITTLE FOOT[®] SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint. In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the

ambient air. This pattern uses all the available area underneath the body for this purpose.



FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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