

74HC4060; 74HCT4060

14-stage binary ripple counter with oscillator

Rev. 4 — 10 February 2016

Product data sheet

1. General description

The 74HC4060; 74HCT4060 is a 14-stage ripple-carry counter/divider and oscillator with three oscillator terminals (RS, RTC and CTC), ten buffered parallel outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case, keep the oscillator pins (RTC and CTC) floating. The counter advances on the HIGH-to-LOW transition of RS. A HIGH level on MR clears all counter stages and forces all outputs LOW, independent of the other input conditions. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{cc}.

2. Features and benefits

- All active components on chip
- RC or crystal oscillator configuration
- Complies with JEDEC standard no. 7 A
- Input levels:
 - ◆ For 74HC4060: CMOS level
 - ◆ For 74HCT4060: TTL level
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

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4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4060D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4060D				
74HC4060DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4060DB				
74HC4060PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4060BQ	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal-enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4060BQ				

5. Functional diagram

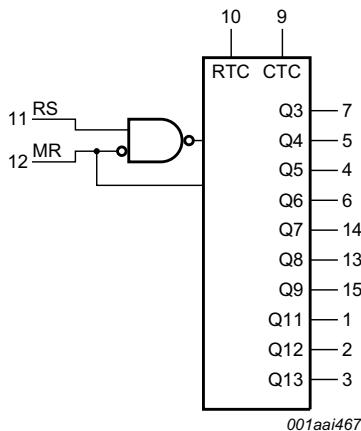


Fig 1. Logic symbol

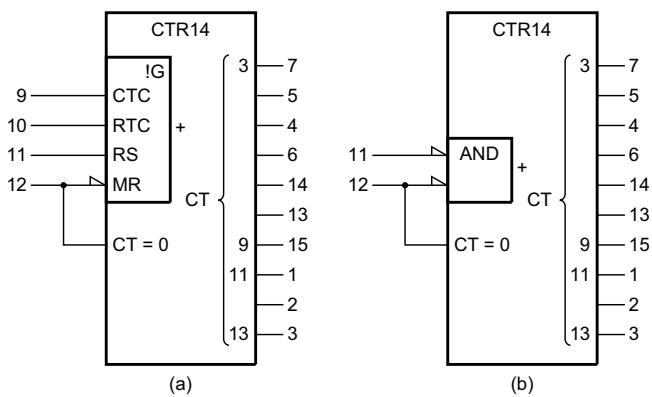


Fig 2. IEC logic symbol

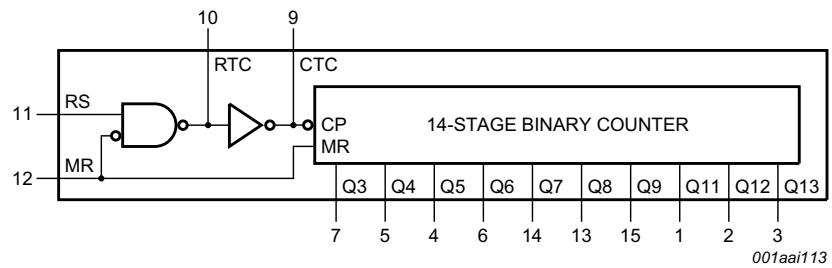


Fig 3. Functional diagram

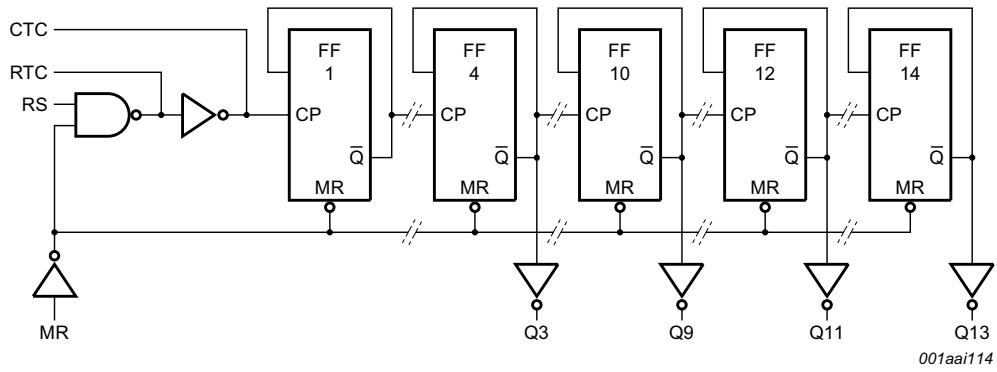


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

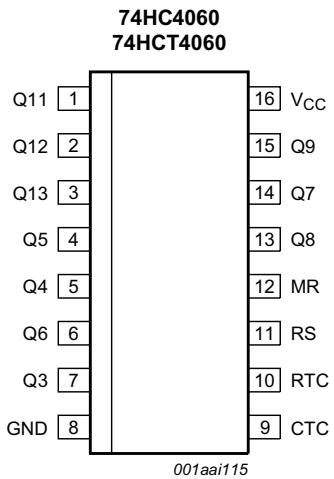


Fig 5. Pin configuration SO16 and (T)SSOP16

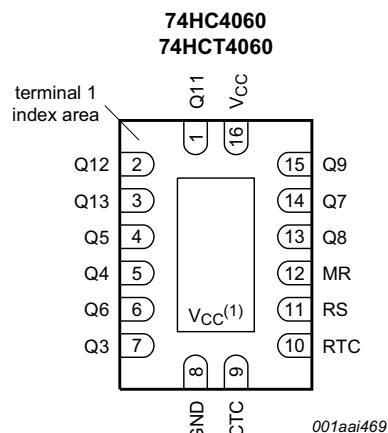


Fig 6. Pin configuration DHVQFN16

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to V_{CC}.

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11 to Q13	1, 2, 3	counter output
Q3 to Q9	7, 5, 4, 6, 14, 13, 15	counter output
GND	8	ground (0 V)
CTC	9	external capacitor connection
RTC	10	external resistor connection
RS	11	clock input /oscillator pin
MR	12	master reset input (active HIGH)
V _{CC}	16	supply voltage

7. Functional description

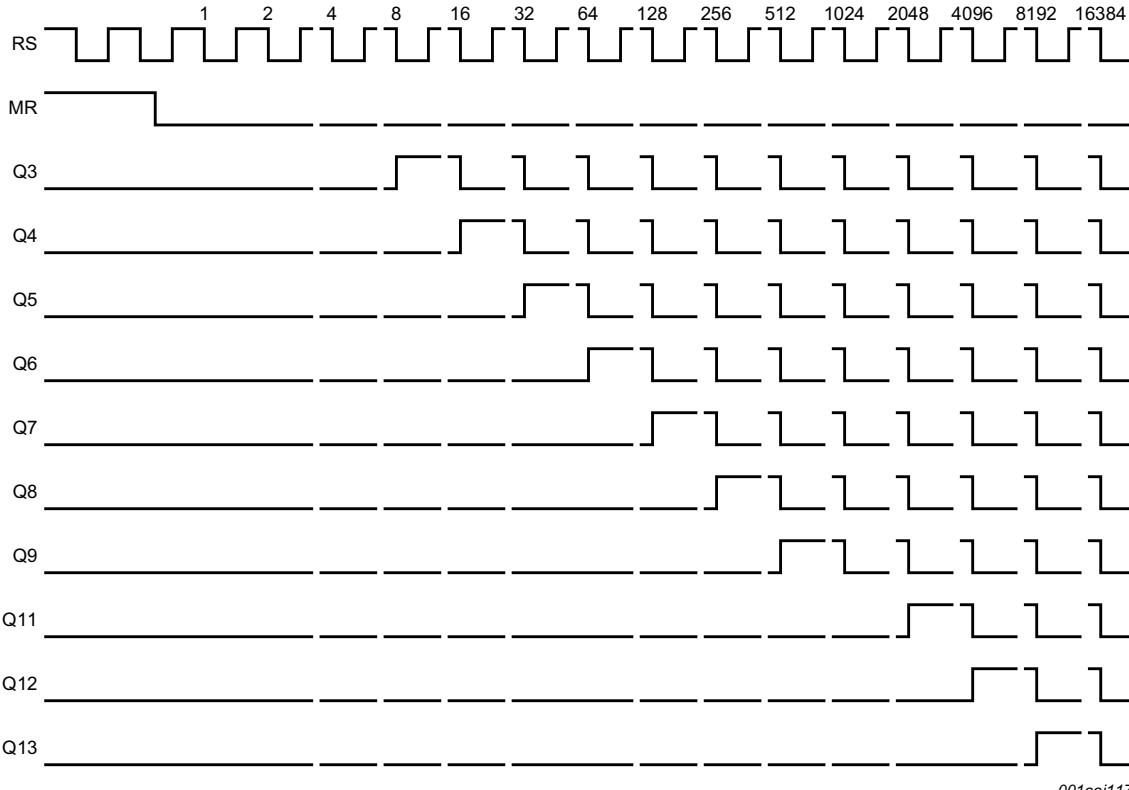


Fig 7. Timing diagram

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1]	-	±20 mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1]	-	±20 mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C

Table 3. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		SO16 package	[2]	-	500 mW
		(T)SSOP16 package	[3]	-	500 mW
		DHVQFN16 package	[4]	-	500 mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.[4] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 4. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4060			74HCT4060			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 5. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4060										
V _{IH}	HIGH-level input voltage	MR input								
		V _{CC} = 2.0 V	1.5	1.3	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.1	-	4.2	-	4.2	-	V
		RS input								
		V _{CC} = 2.0 V	1.7	-	-	1.7	-	1.7	-	V
		V _{CC} = 4.5 V	3.6	-	-	3.6	-	3.6	-	V
		V _{CC} = 6.0 V	4.8	-	-	4.8	-	4.8	-	V

Table 5. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IL}	LOW-level input voltage	MR input								
		V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
		RS input								
		V _{CC} = 2.0 V	-	-	0.3	-	0.3	-	0.3	V
		V _{CC} = 4.5 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 6.0 V	-	-	1.2	-	1.2	-	1.2	V
V _{OH}	HIGH-level output voltage	RTC output; RS = MR = GND								
		I _O = −20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = −2.6 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I _O = −3.3 mA; V _{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
		RTC output; RS = MR = V _{CC}								
		I _O = −20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = −0.65 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I _O = −0.85 mA; V _{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
		CTC output; RS = V _{IH} ; MR = V _{IL}								
		I _O = −3.2 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I _O = −4.2 mA; V _{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
		V _I = V _{IH} or V _{IL} ; except RTC output								
		I _O = −20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		V _I = V _{IH} or V _{IL} ; except RTC and CTC outputs								
		I _O = −4.0 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I _O = −5.2 mA; V _{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V

Table 5. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	RTC output; $RS = V_{CC}$; $MR = GND$								
		$I_O = 20 \mu A$; $V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A$; $V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A$; $V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 2.6 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$	-	-	0.26	-	0.33	-	0.4	V
		$I_O = 3.3 \text{ mA}$; $V_{CC} = 6.0 \text{ V}$	-	-	0.26	-	0.33	-	0.4	V
		CTC output; $RS = V_{IL}$; $MR = V_{IH}$								
		$I_O = 3.2 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$	-	-	0.26	-	0.33	-	0.4	V
		$I_O = 4.2 \text{ mA}$; $V_{CC} = 6.0 \text{ V}$	-	-	0.26	-	0.33	-	0.4	V
		$V_I = V_{IH}$ or V_{IL} ; except RTC output								
		$I_O = 20 \mu A$; $V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A$; $V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A$; $V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$V_I = V_{IH}$ or V_{IL} ; except RTC and CTC outputs								
		$I_O = 4.0 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$	-	-	0.26	-	0.33	-	0.4	V
		$I_O = 5.2 \text{ mA}$; $V_{CC} = 6.0 \text{ V}$	-	-	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

74HCT4060

V_{IH}	HIGH-level input voltage	MR input; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	[1]	2.0	-	-	2.0	-	2.0	-	V
		RS input; $V_{CC} = 4.5 \text{ V}$		3.6	-	-	3.6	-	3.6	-	V
V_{IL}	LOW-level input voltage	MR input; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	[1]	-	-	0.8	-	0.8	-	0.8	V
		RS input; $V_{CC} = 4.5 \text{ V}$		-	-	0.9	-	0.9	-	0.9	V

Table 5. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit	
			Min	Typ	Max	Min	Max	Min	Max		
V _{OH}	HIGH-level output voltage	RTC output; RS = MR = V _{CC}									
		I _O = −20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V	
		I _O = −0.65 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V	
		RTC output; RS = MR = GND									
		I _O = −20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V	
		I _O = −2.6 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V	
		CTC output; RS = V _{IH} ; MR = V _{IL}									
		I _O = −3.2 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V	
		V _I = V _{IH} or V _{IL} ; except RTC output									
		I _O = −20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; except RTC and CTC outputs									
		I _O = −4.0 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V	
		RTC output; RS = V _{CC} ; MR = GND									
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V	
		I _O = 2.6 mA; V _{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V	
		CTC output; RS = V _{IL} ; MR = V _{IH}									
		I _O = 3.2 mA; V _{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V	
		V _I = V _{IH} or V _{IL} ; except RTC output									
I _I	input leakage current	I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V	
		V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA	
		I _{CC}	V _I = V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A	-	-	8.0	-	80	-	160	µA
		ΔI _{CC}	per input pin; V _I = V _{CC} − 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A	-	40	144	-	180	-	196	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF	

[1] For HCT4060, only input MR (pin 12) has TTL input switching levels.

11. Dynamic characteristics

Table 6. Dynamic characteristics

GND = 0 V; $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4060										
t_{pd}	propagation delay	RS to Q3; see Figure 8 [1]								
		$V_{CC} = 2.0 \text{ V}$	-	99	300	-	375	-	450	ns
		$V_{CC} = 4.5 \text{ V}$	-	36	60	-	75	-	90	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	31	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	29	51	-	64	-	77	ns
		Qn to Qn+1; see Figure 9 [2]								
		$V_{CC} = 2.0 \text{ V}$	-	22	80	-	100	-	120	ns
		$V_{CC} = 4.5 \text{ V}$	-	8	16	-	20	-	24	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	6	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	14	-	17	-	20	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 10								
		$V_{CC} = 2.0 \text{ V}$	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5 \text{ V}$	-	20	35	-	44	-	53	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	16	30	-	37	-	45	ns
t_t	transition time	Qn; see Figure 8 [3]								
		$V_{CC} = 2.0 \text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	13	-	16	-	19	ns
t_w	pulse width	RS (HIGH or LOW); see Figure 8								
		$V_{CC} = 2.0 \text{ V}$	80	17	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	6	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	5	-	17	-	20	-	ns
		MR (HIGH); see Figure 10								
		$V_{CC} = 2.0 \text{ V}$	80	25	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	9	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	7	-	17	-	20	-	ns
		MR to RS; see Figure 10								
		$V_{CC} = 2.0 \text{ V}$	100	28	-	125	-	150	-	ns
t_{rec}	recovery time	$V_{CC} = 4.5 \text{ V}$	20	10	-	25	-	30	-	ns
		$V_{CC} = 6.0 \text{ V}$	17	8	-	21	-	26	-	ns

Table 6. Dynamic characteristics ...continuedGND = 0 V; $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f_{\max}	maximum frequency	RS; see Figure 8								
		$V_{CC} = 2.0 \text{ V}$	6	26	-	4.8	-	4	-	MHz
		$V_{CC} = 4.5 \text{ V}$	30	80	-	24	-	20	-	MHz
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	87	-	-	-	-	-	MHz
		$V_{CC} = 6.0 \text{ V}$	35	95	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$; [4] $V_{CC} = 5 \text{ V}; f_i = 1 \text{ MHz}$	-	40	-	-	-	-	-	pF

74HCT4060

t_{pd}	propagation delay	RS to Q3; see Figure 8 [1]										
		$V_{CC} = 4.5 \text{ V}$	-	33	66	-	83	-	99	ns		
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	31	-	-	-	-	-	ns		
		Qn to Qn+1; see Figure 9 [2]										
		$V_{CC} = 4.5 \text{ V}$	-	8	16	-	20	-	24	ns		
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	6	-	-	-	-	-	ns		
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 10										
		$V_{CC} = 4.5 \text{ V}$	-	21	44	-	55	-	66	ns		
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	18	-	-	-	-	-	ns		
t_t	transition time	Qn; see Figure 8 [3]										
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns		
t_w	pulse width	RS (HIGH or LOW); see Figure 8										
		$V_{CC} = 4.5 \text{ V}$	16	6	-	20	-	24	-	ns		
		MR (HIGH); see Figure 10										
		$V_{CC} = 4.5 \text{ V}$	16	6	-	20	-	24	-	ns		
t_{rec}	recovery time	MR to RS; see Figure 10										
		$V_{CC} = 4.5 \text{ V}$	26	13	-	33	-	39	-	ns		
f_{\max}	maximum frequency	RS; see Figure 8										
		$V_{CC} = 4.5 \text{ V}$	30	80	-	24	-	20	-	MHz		
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	88	-	-	-	-	-	MHz		

Table 6. Dynamic characteristics ...continuedGND = 0 V; C_L = 50 pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} − 1.5 V; ^[4] V_{CC} = 5 V; f_i = 1 MHz	-	40	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .[2] Q_{n+1} is the next Q_n output.[3] t_t is the same as t_{THL} and t_{TLH} .[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

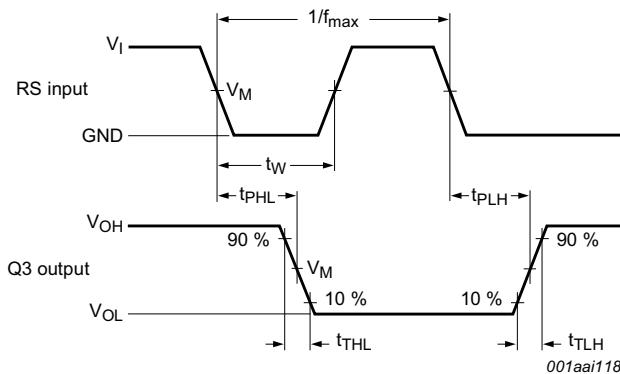
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

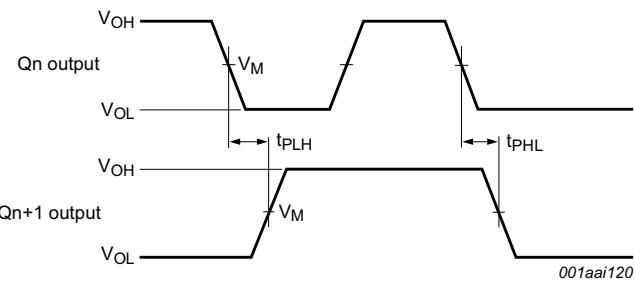
 f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms

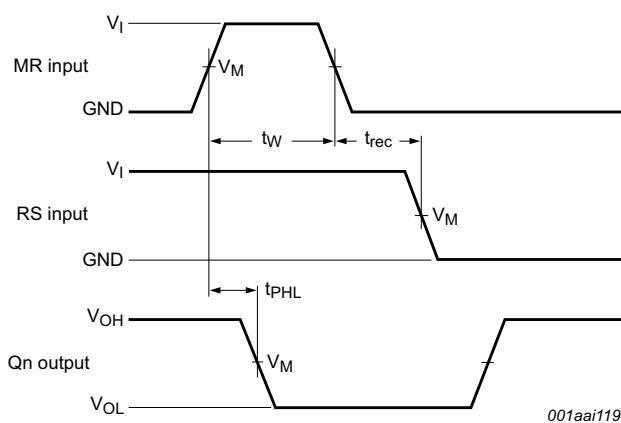
Measurement points are given in [Table 7](#). V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.**Fig 8. Waveforms showing the clock (RS) to output (Q3) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency**



Measurement points are given in [Table 7](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Waveforms showing the output Qn to output Qn+1 propagation delays



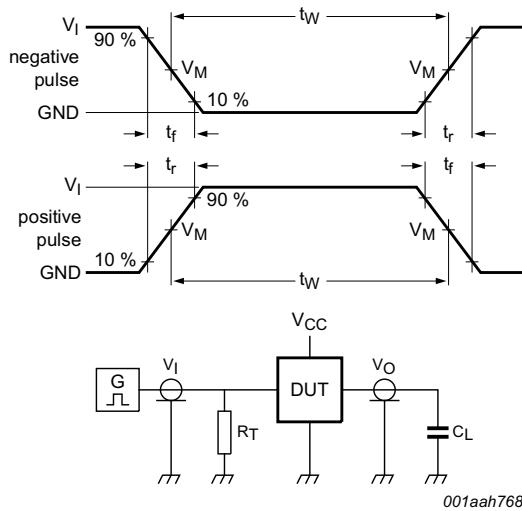
Measurement points are given in [Table 7](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. Waveforms showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (RS) recovery time

Table 7. Measurement points

Type	Input	Output
	V_M	V_M
74HC4060	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT4060	1.3 V	1.3 V



Test data is given in [Table 8](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 11. Test circuit for measuring switching times

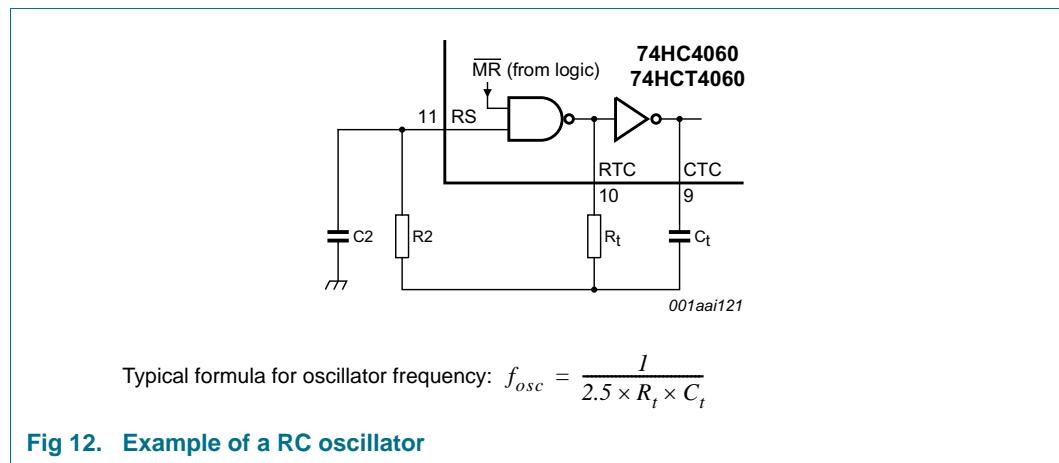
Table 8. Test data

Type	Input		Load
	V_I	t_r, t_f	
74HC4060	V_{CC}	6 ns	15 pF, 50 pF
74HCT4060	3 V	6 ns	15 pF, 50 pF

13. RC oscillator

13.1 Timing component limitations

The oscillator frequency is mainly determined by $R_t C_t$, provided $R_2 \approx 2R_t$ and $R_2 C_2 \ll R_t C_t$. The function of R_2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the ON resistance in series with it, which typically is 280Ω at $V_{CC} = 2.0$ V, 130Ω at $V_{CC} = 4.5$ V and 100Ω at $V_{CC} = 6.0$ V.



The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t > 50 \text{ pF}$, up to any practical value and $10 \text{ k}\Omega < R_t < 1 \text{ M}\Omega$.

In order to avoid start-up problems, $R_t \geq 1 \text{ k}\Omega$.

13.2 Typical crystal oscillator circuit

In Figure 13, R_2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R_2 should not be too large. A practical value for R_2 is $2.2 \text{ k}\Omega$.

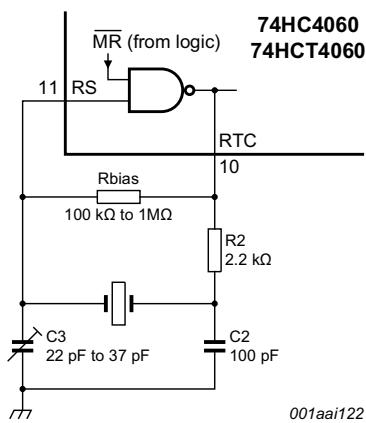
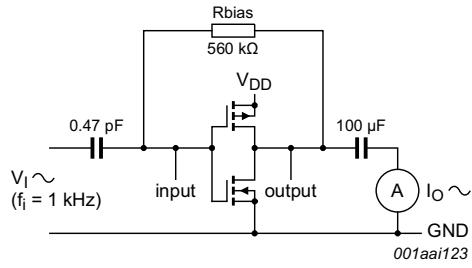


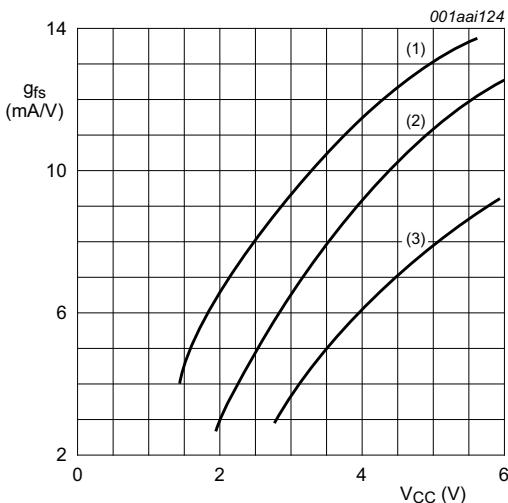
Fig 13. External component connection for a crystal oscillator



$g_{fs} = \Delta I_O / \Delta V_O$ at V_O is constant; $MR = \text{LOW}$.

See also [Figure 15](#).

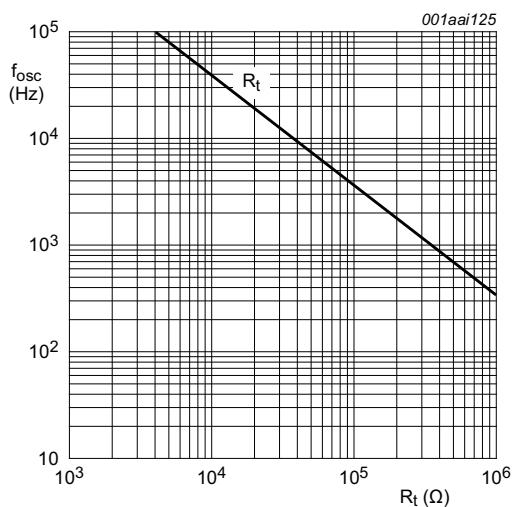
Fig 14. Test set-up for measuring forward transconductance



$T_{amb} = 25^\circ\text{C}$.

- (1) Maximum.
- (2) Typical.
- (3) Minimum.

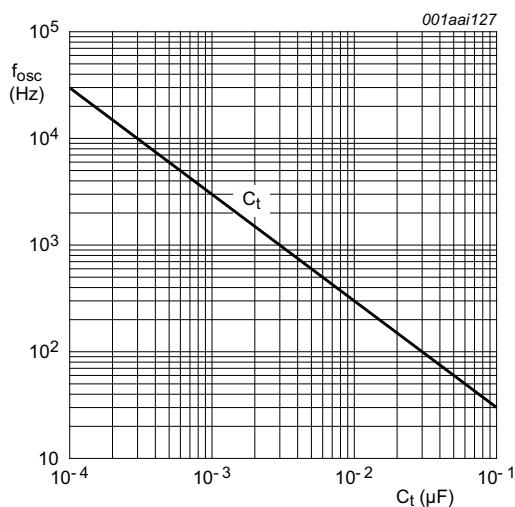
Fig 15. Typical forward transconductance as function of the supply voltage



V_{CC} = 2.0 V to 6.0 V; T_{amb} = 25 °C.

For R_t curve: C_t = 1 nF; $R2$ = 2 × R_t .

Fig 16. RC oscillator frequency as a function of R_t



V_{CC} = 2.0 V to 6.0 V; T_{amb} = 25 °C.

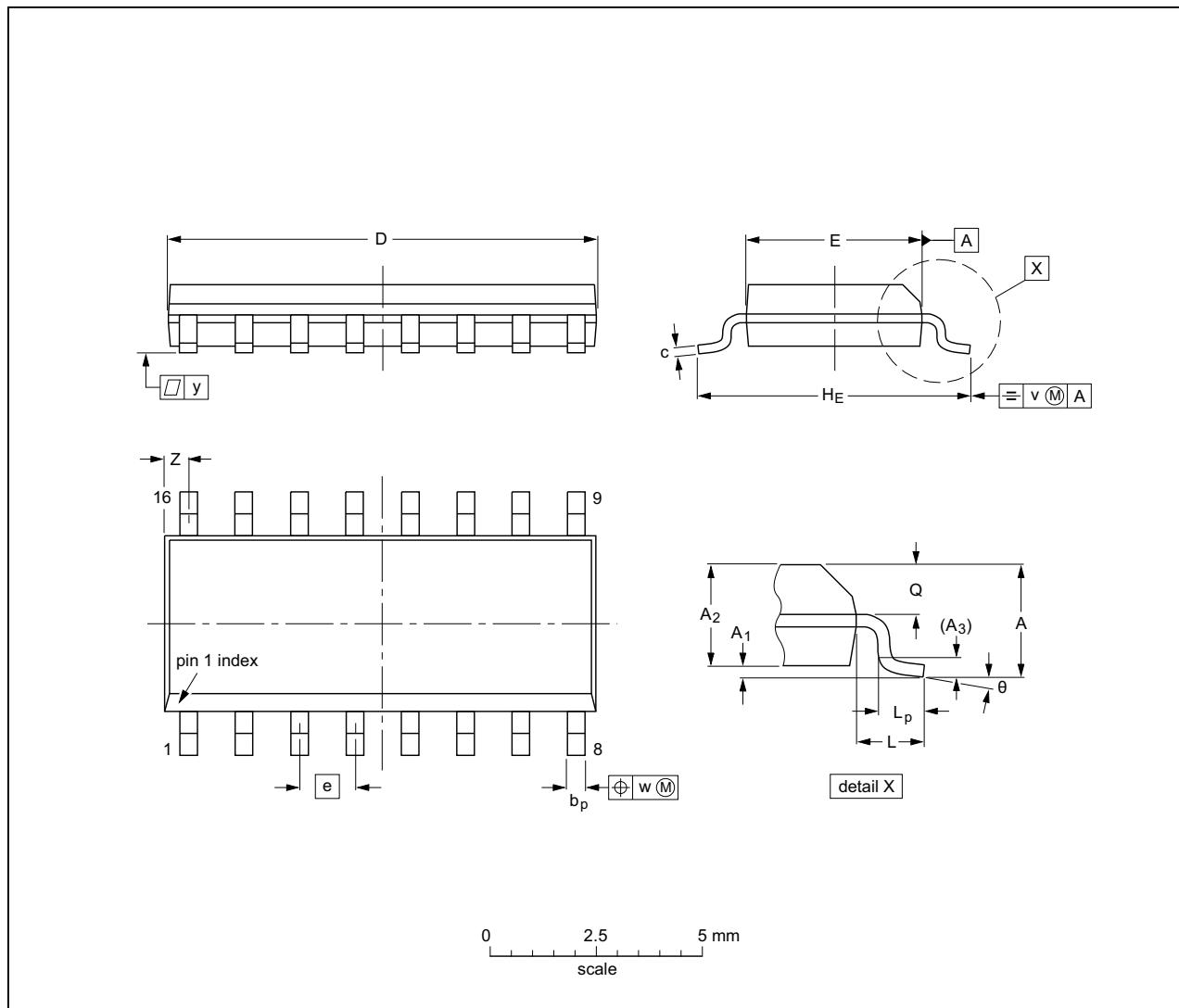
For C_t curve: R_t = 100 kΩ; $R2$ = 200 kΩ.

Fig 17. RC oscillator frequency as a function of C_t

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75 0.10	0.25 0.125	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 18. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

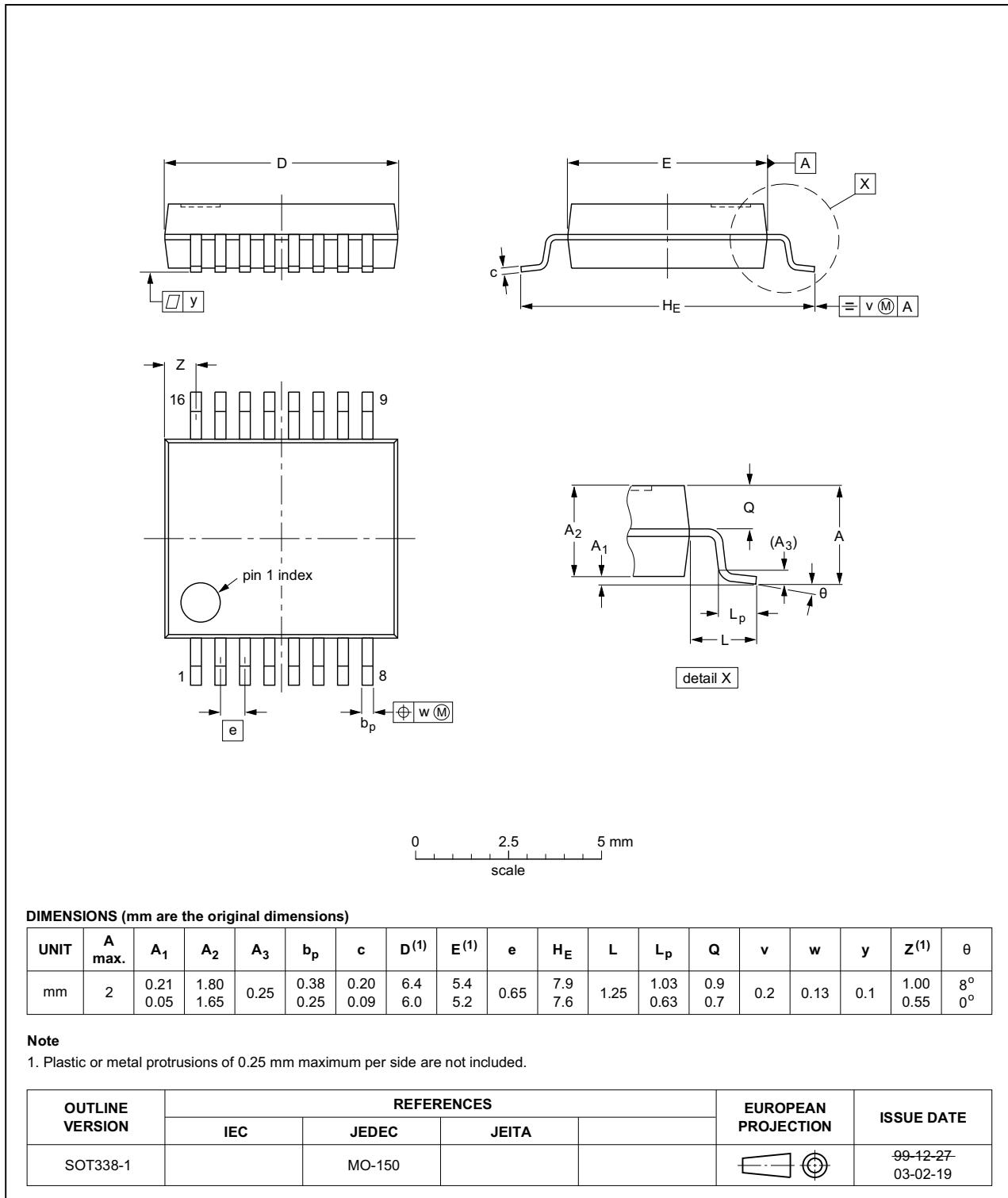


Fig 19. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

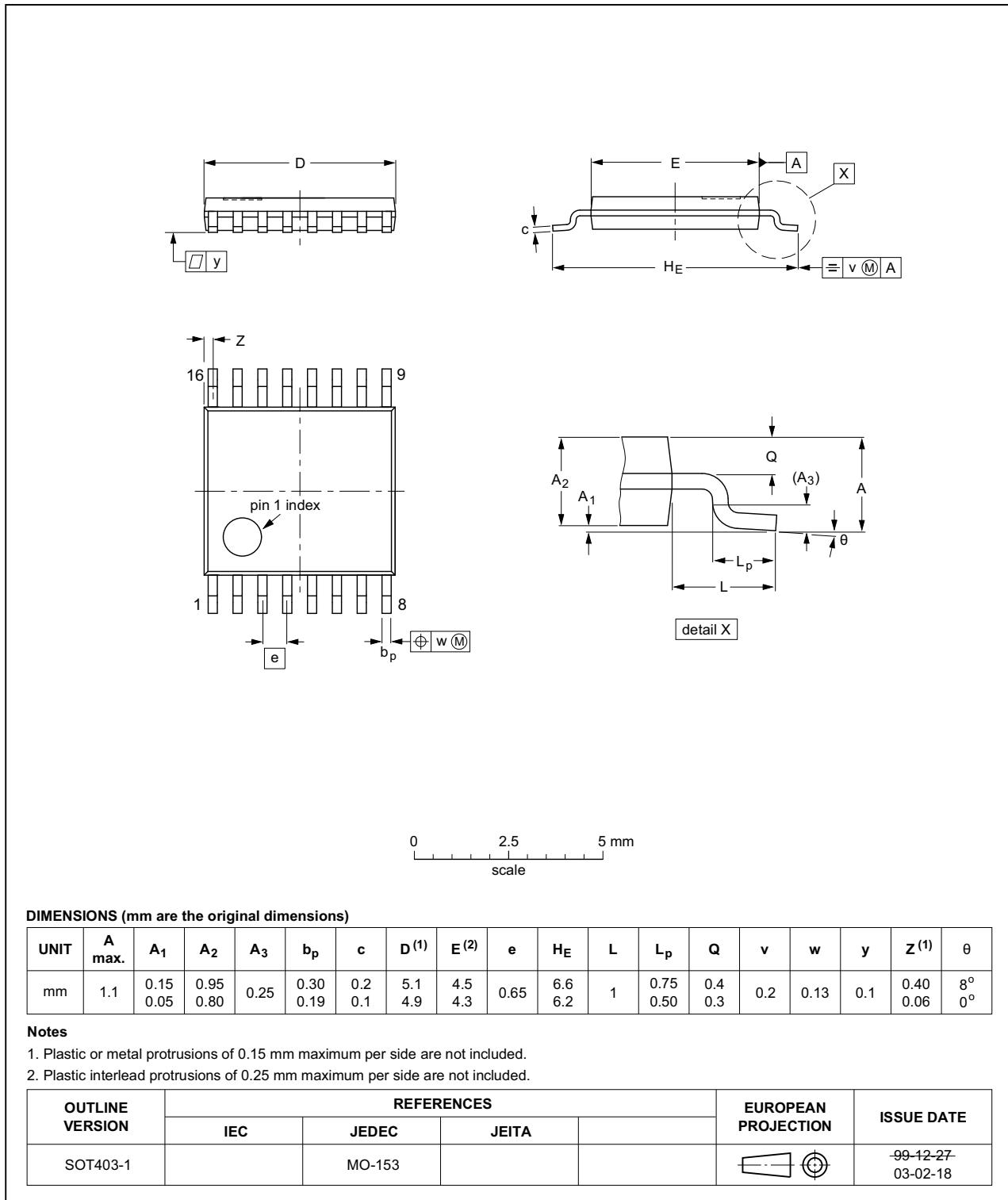


Fig 20. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

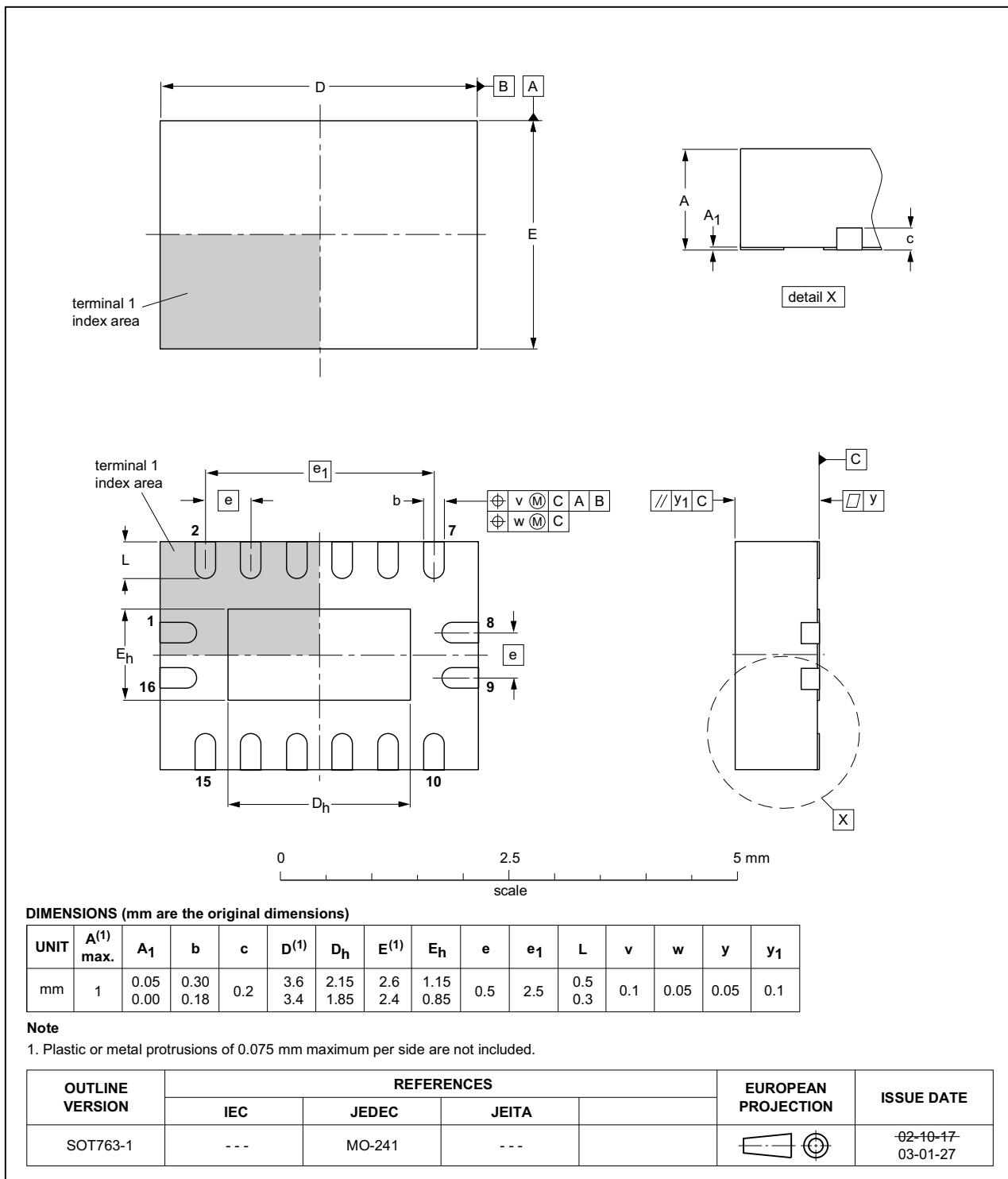


Fig 21. Package outline SOT763-1 (DHVQFN16)

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4060 v.4	20160210	Product data sheet	-	74HC_HCT4060 v.3
Modifications:	<ul style="list-style-type: none"> • Type numbers 74HC4060N and 74HCT4060N (SOT38-4) removed. • Table 5: HIGH and LOW input levels added for 74HCT4060. (errata) 			
74HC_HCT4060 v.3	20080714	Product data sheet	-	74HC_HCT4060_CNV v.2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 4: DHVQFN16 package added. • Section 8: derating values added for DHVQFN16 package. • Section 14: outline drawing added for DHVQFN16 package. 			
74HC_HCT4060_CNV v.2	19970901	Product specification	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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19. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	4
6.1	Pinning	4
6.2	Pin description	4
7	Functional description	5
8	Limiting values	5
9	Recommended operating conditions	6
10	Static characteristics	6
11	Dynamic characteristics	10
12	Waveforms	12
13	RC oscillator	15
13.1	Timing component limitations	15
13.2	Typical crystal oscillator circuit	15
14	Package outline	18
15	Abbreviations	22
16	Revision history	22
17	Legal information	23
17.1	Data sheet status	23
17.2	Definitions	23
17.3	Disclaimers	23
17.4	Trademarks	24
18	Contact information	24
19	Contents	25

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