

FEATURES

- Multi-rate up to 3.2Gbps operation
- Wide gain-bandwidth product
 - 38dB differential gain
 - 2GHz 3dB bandwidth
- Low noise 50Ω CML data outputs
 - 800mV_{pp} output swing
 - 60ps edge rates
 - 5ps_{RMS} typ. random jitter
 - 15ps_{pp} typ. deterministic jitter
- Chatter-free, Signal-Detect (SD) output
 - 4.6dB electrical hysteresis
 - OC-TTL output with internal 4.75kΩ pull-up resistor
- Programmable SD sensitivity using single external resistor
- Internal 50Ω data input termination
- TTL EN input allows feedback from SD
- Wide operating range
 - Single 3.3V ±10% or 5V ±10% power supply
 - -40°C to +85°C industrial temperature range
- Available in tiny 10-pin EPAD-MSOP and 16-pin MLF™ packages

APPLICATIONS

- 1.25Gbps and 2.5Gbps Gigabit Ethernet
- 1.062Gbps and 2.125Gbps Fibre Channel
- 155Mbps, 622Mbps, 1.25Gbps, and 2.5Gbps SONET/SDH
- Gigabit interface converter (GBIC)
- Small form factor (SFF) and small form factor pluggable (SFP) transceivers
- Parallel 10G Ethernet
- High-gain line driver and line receiver

DESCRIPTION

The SY88843V low-power limiting post amplifier is designed for use in fiber-optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88843V quantizes these signals and outputs typically 800mV_{pp} voltage-limited waveforms.

The SY88843V operates from a single +3.3V ±10% or +5V ±10% power supply, over an industrial temperature range of -40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 3.2Gbps and as small as 10mVp-p can be amplified to drive devices with CML inputs or AC-coupled PECL inputs.

The SY88843V incorporates a signal detect (SD), open-collector TTL output with internal 4.75kΩ pull-up resistor. A programmable, loss-of-signal level set pin (SDLVL) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold set by SDLVL and de-asserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a loss of signal condition. EN asserts the true output signal without removing the input signal. Typically 4.6dB SD hysteresis is provided to prevent chattering.

Please see Micrel's website at www.micrel.com for a complete selection of optical module ICs. The following table summarizes the differences between devices in Micrel's latest family of Limiting Amplifiers.

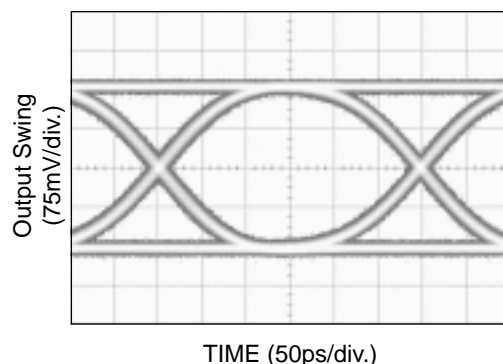
All support documentation can be found on Micrel's web site at www.micrel.com.

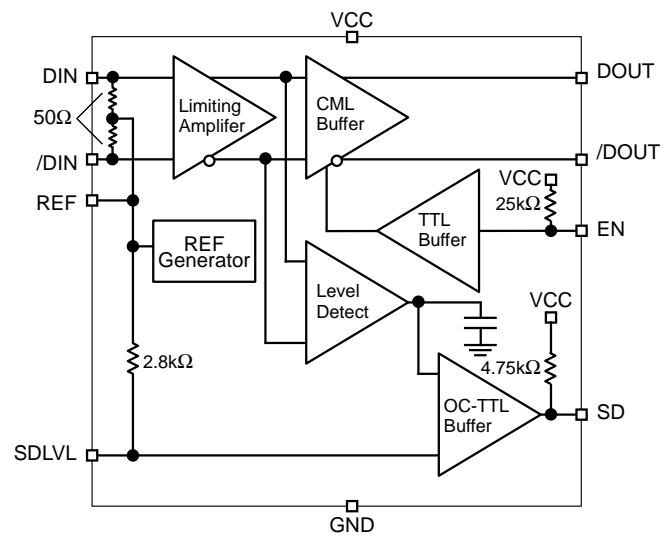
| Part Number | Integrated 50Ω Input Termination | LOS or SD | Active LOW or HIGH Enable |
|-------------|----------------------------------|-----------|---------------------------|
| SY88773V | No | LOS | LOW |
| SY88823V | No | SD | HIGH |
| SY88843V | Yes | SD | HIGH |
| SY88973V | Yes | LOS | LOW |

Table 1. Limiting Amplifiers Selection Guide

TYPICAL PERFORMANCE

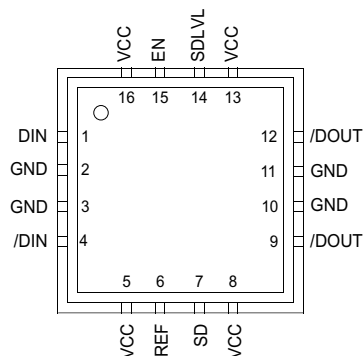
3.3V, 25°C, 10mV_{pp} Input
@3.2Gbps 2³¹-1 PRBS, R_{LOAD} = 50Ω to V_{CC}



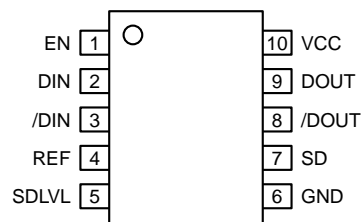
FUNCTIONAL BLOCK DIAGRAM

PACKAGE/ORDERING INFORMATION

Ordering Information⁽¹⁾



16-Pin MLF™ (MLF-16)



10-Pin EPAD-MSOP (K10-2)

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|--------------------------------|--------------|-----------------|--------------------------------------|------------------|
| SY88843VKI | K10-2 | Industrial | 843V | Sn-Pb |
| SY88843VKITR ⁽²⁾ | K10-2 | Industrial | 843V | Sn-Pb |
| SY88843VMI | MLF-16 | Industrial | 843V | Sn-Pb |
| SY88843VMITR ⁽²⁾ | MLF-16 | Industrial | 843V | Sn-Pb |
| SY88843VEY ⁽³⁾ | K10-2 | Industrial | 843V with Pb-Free bar-line indicator | Pb-Free Matte-Sn |
| SY88843VEYTR ^(2, 3) | K10-2 | Industrial | 843V with Pb-Free bar-line indicator | Pb-Free Matte-Sn |
| SY88843VMG ⁽³⁾ | MLF-16 | Industrial | 843V with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY88843VMGTR ^(2, 3) | MLF-16 | Industrial | 843V with Pb-Free bar-line indicator | Pb-Free NiPdAu |

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

| Pin Number (MSOP) | Pin Number (MLF™) | Pin Name | Type | Pin Function |
|-------------------|-----------------------------|-------------|--|--|
| 1 | 15 | EN | TTL Input: Default is high. | Enable: De-asserts true data output when low. Incorporates 25k Ω pull-up to VCC. |
| 2, 3 | 1, 4 | DIN, /DIN | Differential Data Input | Differential data input. Each pin internally terminates to REF through 50 Ω . |
| 4 | 6 | REF | | Reference Voltage: Bypass with 0.01 μF low ESR capacitor from REF to VCC to stabilize SDLVL and REF. |
| 5 | 14 | SDLVL | Input: Default is maximum sensitivity. | Signal Detect Level Set: A resistor from this pin to VCC sets the threshold for the data input amplitude at which the SD output will be asserted. |
| 6 Exposed Pad | 2, 3, 10, 11 Exposed Pad | GND | Ground | Device ground. Exposed pad must be soldered (or equivalent) to the same potential as the ground pins. |
| 7 | 7 | SD | Open Collector TTL Output with internal 4.75k Ω pull-up resistor | Signal Detect: Asserts high when the data input amplitude rises above the threshold set by SDLVL. |
| 8, 9 | 9, 12 | DOUT, /DOUT | Differential CML Output | Differential data output. |
| 10 | 5, 8, 13, 16 | VCC | Power Supply | Positive power supply. Bypass with 0.1 μF 0.01 μF low ESR capacitors. 0.01 μF capacitors should be as close as possible to VCC pins. |

Absolute Maximum Ratings⁽¹⁾

| | |
|---------------------------------------|---|
| Supply Voltage (V_{CC}) | 0V to +7.0V |
| EN, SDLVL Voltage | 0 to V_{CC} |
| REF Current | ± 1 mA |
| SD Current | ± 5 mA |
| DOUT, /DOUT Current | ± 25 mA |
| DIN, /DIN Current | ± 10 mA |
| Storage Temperature (T_S) | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 20 sec.) | 260°C |

Operating Ratings⁽²⁾

| | |
|---|---|
| Supply Voltage (V_{CC}) | +3.0V to +3.6V or +4.5V to +5.5V |
| Ambient Temperature (T_A) | -40°C to $+85^\circ\text{C}$ |
| Junction Temperature (T_J) | -40°C to $+120^\circ\text{C}$ |
| Package Thermal Resistance ⁽³⁾ | |
| MLF TM | |
| θ_{JA} (Still-Air) | 61°C/W |
| ψ_{JB} | 38°C/W |
| EPAD-MSOP | |
| θ_{JA} (Still-Air) | 38°C/W |
| ψ_{JB} | 22°C/W |

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.0\text{V}$ to 3.6V or 4.5V to 5.5V , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; typical values at $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------|-------------------------------|----------------------------|----------------|----------------|----------------|----------|
| I_{CC} | Power Supply Current | 3.3V, Note 4 5V, Note 4 | | 28 30 | 42 45 | mA mA |
| | Power Supply Current | 3.3V, Note 5 5V, Note 5 | | 45 47 | 62 65 | mA mA |
| V_{REF} | REF Voltage | | | $V_{CC}-1.3$ | | V |
| SDLVL | SDLVL Voltage Range | | V_{REF} | | V_{CC} | V |
| V_{OH} | DOUT, /DOUT HIGH Voltage | Note 6 | $V_{CC}-0.020$ | $V_{CC}-0.005$ | V_{CC} | V |
| V_{OL} | DOUT, /DOUT LOW Voltage | 3.3V, Note 6 5V, Note 6 | $V_{CC}-0.475$ | $V_{CC}-0.400$ | $V_{CC}-0.350$ | V |
| | | | $V_{CC}-0.510$ | $V_{CC}-0.400$ | $V_{CC}-0.350$ | V |
| V_{OFFSET} | Differential Output Offset | Note 6 | | | ± 80 | mV |
| Z_O | Single-Ended Output Impedance | | 40 | 50 | 60 | Ω |
| Z_I | Single-Ended Input Impedance | | 40 | 50 | 60 | Ω |

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.0\text{V}$ to 3.6V or 4.5V to 5.5V , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|-----------------------|----------------------------|------|-----|----------|---------------|
| V_{OH} | SD Output HIGH Level | Sourcing 100 μA | 2.4 | | V_{CC} | V |
| V_{OL} | SD Output LOW Level | Sinking 2mA | | | 0.5 | V |
| V_{IH} | EN Input HIGH Voltage | | 2.0 | | | V |
| V_{IL} | EN Input LOW Voltage | | | | 0.8 | V |
| I_{IH} | EN Input HIGH Current | $V_{IN} = 2.7\text{V}$ | | | 20 | μA |
| | | $V_{IN} = V_{CC}$ | | | 100 | μA |
| I_{IL} | EN Input LOW Current | $V_{IN} = 0.5\text{V}$ | -0.3 | | | mA |

Notes:

1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes the use of 4-layer PCB. Exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.
4. Excludes current of CML output stage. See "Detailed Description."
5. Total device current with no output load.
6. Output levels are based on a 50 Ω to V_{CC} load impedance. If the load impedance is different, the output level will be changed. Amplifier is in limiting mode.

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.0V$ to $3.6V$ or $4.5V$ to $5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $R_{LOAD} = 50\Omega$ to V_{CC} ; typical values at $V_{CC} = 3.3V$, $T_A = 25^{\circ}C$.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------|---------------------------------------|--|------------|------------|-------------|---------------------------------------|
| PSRR | Power Supply Rejection Ratio | | | 35 | | dB |
| t_r, t_f | Output Rise/Fall Time (20% to 80%) | Note 7 | | 60 | 120 | ps |
| t_{JITTER} | Deterministic Random | Note 8 | | 15 5 | | ps _{PP} ps _{RMS} |
| V_{ID} | Differential Input Voltage Swing | | 10 | | 1800 | mV _{PP} |
| V_{OD} | Differential Output Voltage Swing | 3.3V, Note 7 5V, Note 7 | 700 700 | 800 800 | 950 1020 | mV _{PP} mV _{PP} |
| HYS | SD Hysteresis | Note 9 | 2 | 4.6 | 8 | dB |
| t_{OFF} | SD Release Time | | | 0.1 | 0.5 | μs |
| t_{ON} | SD Assert Time | | | 0.2 | 0.5 | μs |
| V_{SR} | SD Sensitivity Range | Note 10 | 10 | | 35 | mV _{PP} |
| B_{-3dB} | -3dB Bandwidth | | | 2.0 | | GHz |
| $A_{V(Diff)}$ | Differential Voltage Gain | | 32 | 38 | | dB |
| S_{21} | Single-Ended Small-Signal Gain | | 26 | 32 | | dB |

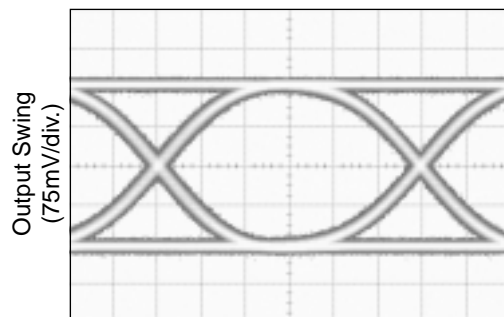
Notes:

7. Amplifier in limiting mode. Input is a 200MHz square wave, $t_i < 300ps$.
8. Deterministic jitter measured using 2.488Gbps K28.5 pattern, $V_{ID} = 10mV_{pp}$. Random jitter measured using 2.488Gbps K28.7 pattern, $V_{ID} = 10mV_{pp}$.
9. Electrical signal.
10. This is the detectable range of input amplitudes that can de-assert SD. The input amplitude to assert SD is 2–8dB higher than the de-assert amplitude. See "Typical Operating Characteristics" for graphs showing how to choose a particular V_{SDLVL} or R_{SDLVL} for a particular SD de-assert, and its associated assert, amplitude. If increased SD sensitivity and hysteresis are required, an application note entitled "Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers" is available at http://www.micrel.com/product-info/app_hints+notes.shtml.

TYPICAL OPERATING CHARACTERISTICS

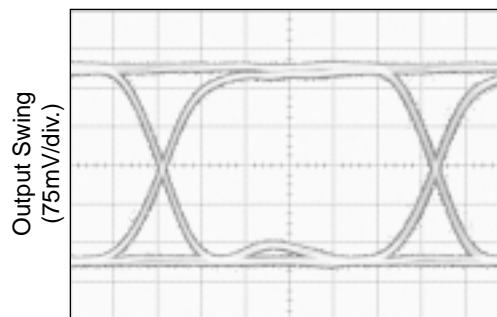
$V_{CC} = 3.3V$, $T_A = 25^\circ C$, $R_{LOAD} = 50\Omega$ to V_{CC} , unless otherwise stated.

10mV_{pp} Input @3.2Gbps 2³¹-1 PRBS



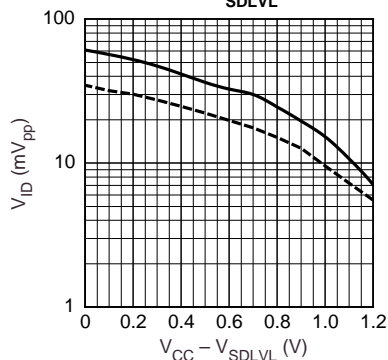
TIME (50ps/div.)

1.8V_{pp} Input @3.2Gbps 2³¹-1 PRBS

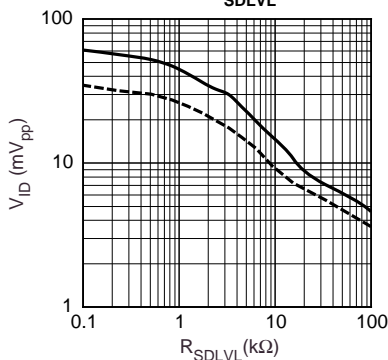


TIME (50ps/div.)

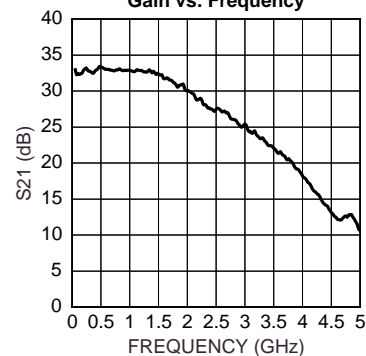
V_{ID} to Assert/De-assert SD
vs. V_{SDLVL}



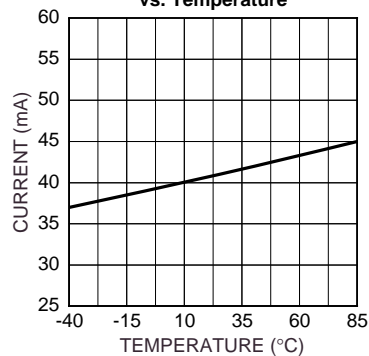
V_{ID} to Assert/De-assert SD
vs. R_{SDLVL}



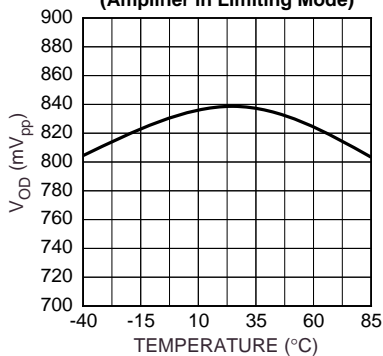
Single-Ended Small-Signal
Gain vs. Frequency



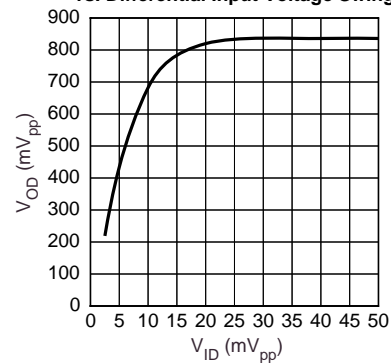
Power Supply Current
vs. Temperature



Differential Output Voltage
Swing vs. Temperature
(Amplifier in Limiting Mode)



Differential Output Voltage Swing
vs. Differential Input Voltage Swing



DETAILED DESCRIPTION

The SY88843V low-power, limiting post amplifier operates from a single $+3.3V \pm 10\%$ or $+5V \pm 10\%$ power supply, over an industrial temperature range of -40°C to $+85^{\circ}\text{C}$. Signals with data rates up to 3.2Gbps and as small as 10mV_{PP} can be amplified. Figure 1 shows the allowed input voltage swing. The SY88843V generates an SD output, providing feedback to EN for output stability. SDLVL sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

The SY88843V's inputs are internally terminated with 50Ω to REF. Unless unaffected by this internal termination scheme, upstream devices need to be AC-coupled to the SY88843V's inputs. Figure 2 shows a simplified schematic of the input structure.

The high sensitivity of the input amplifier detects and amplifies as small as 10mV_{PP}. The input amplifier allows input signals as large as 1800mV_{PP}. Input signals are linearly amplified with a typically 38dB differential voltage gain. Since it is a limiting amplifier, the SY88843V outputs typically 800mV_{PP} voltage-limited waveforms for input signals that are greater than 10mV_{PP}. Applications requiring the SY88843V to operate with high gain should have the upstream TIA placed as close as possible to the SY88843V's input pins to ensure the device's best performance of the device.

Output Buffer

The SY88843V's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to VCC or equivalent for each output pin provides buffer termination. Figure 3 shows a simplified schematic of the output structure and includes an appropriate termination method. Of course, driving a downstream device with a CML input that is internally terminated with 50Ω to VCC eliminates the need for external termination. As noted in the previous section, the amplifier outputs, typically 800mV_{PP}, waveforms across 25Ω total loads. The output buffer, thus, switches typically 16mA tail-current. Figure 4 shows the power supply current measurement which excludes the 16mA tail-current.

Signal Detect

The SY88843V incorporates a chatter-free, SD open-collector TTL output with internal 4.75kΩ pull-up resistor as shown in Figure 5. SD is used to determine that the input amplitude large enough to be considered a valid input. SD asserts high if the input amplitude rises above the threshold set by SDLVL and de-asserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a loss-of-signal condition. EN de-asserts low the true output signal without removing the input signals. Typically, 4.6dB SD hysteresis is provided to prevent chattering.

Signal Detect-Level Set

A programmable, signal-detect level set pin sets the threshold of the input amplitude detection. Connecting an external resistor between VCC and SDLVL sets the voltage at SDLVL. This voltage ranges from V_{CC} to V_{REF}. The external resistor creates a voltage divider between V_{CC} and REF as shown in Figure 6. If desired, an appropriate external voltage may be applied rather than using a resistor. The relationship between V_{SDLVL} and R_{SDLVL} is given by:

$$V_{\text{SDLVL}} = V_{\text{CC}} - 1.3 \frac{R_{\text{SDLVL}}}{R_{\text{SDLVL}} + 2.8}$$

where voltages are in volts and resistances are in kΩ.

The smaller the external resistor, which implies a smaller voltage difference from SDLVL to VCC, the lower the SD sensitivity. Hence, larger input amplitude is required to assert SD. The "Typical Operating Characteristics" section contains graphs showing the relationship between the input amplitude detection sensitivity and V_{SDLVL} or R_{SDLVL}.

Hysteresis

The SY88843V provides typically 4.6dB SD electrical hysteresis. By definition, a power ratio measured in dB is $10\log(\text{power ratio})$. Power is calculated as V_{IN}^2/R for an electrical signal. Hence, the same ratio can be stated as $20\log(\text{voltage ratio})$. While in linear mode, the electrical voltage input changes linearly with the optical power and the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. The SY88843V provides typically 2.3dB SD optical hysteresis. As the SY88843V is an electrical device, this datasheet refers to hysteresis in electrical terms. With 4.6dB SD hysteresis, a voltage factor of 1.7 is required to assert SD.

Hysteresis and Sensitivity Improvement

If increased SD sensitivity and hysteresis are required, an application note entitled "Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers" is available at http://www.micrel.com/product-info/app_hints+notes.shtml.

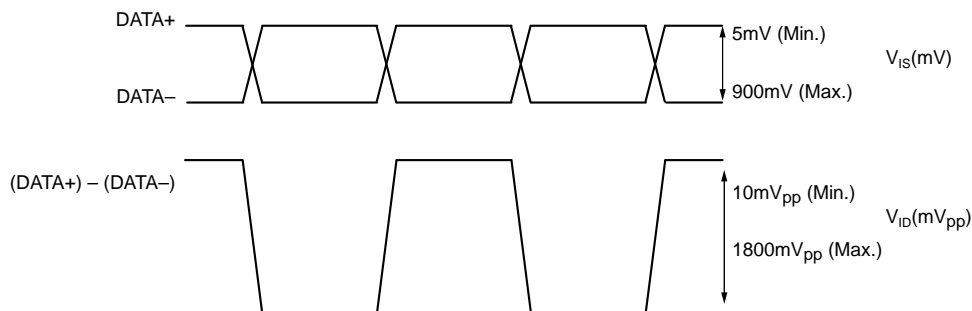
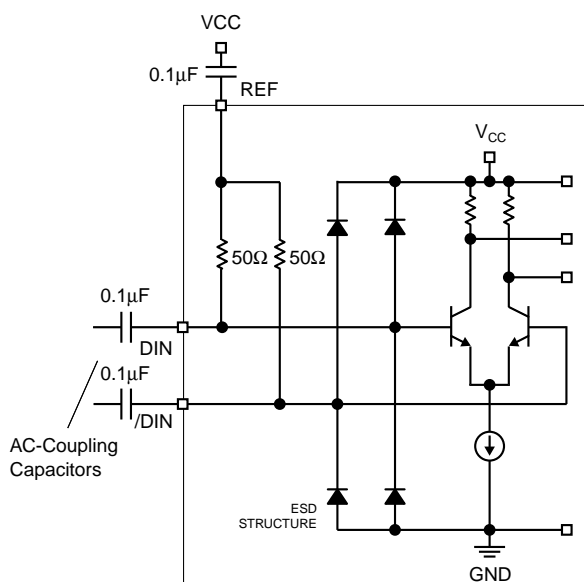
Figure 1. V_{IS} and V_{ID} Definition

Figure 2. Input Structure

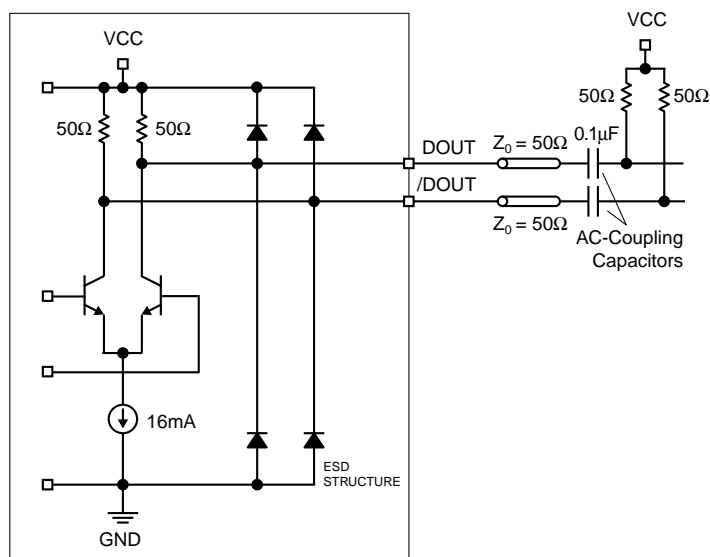


Figure 3. Output Structure

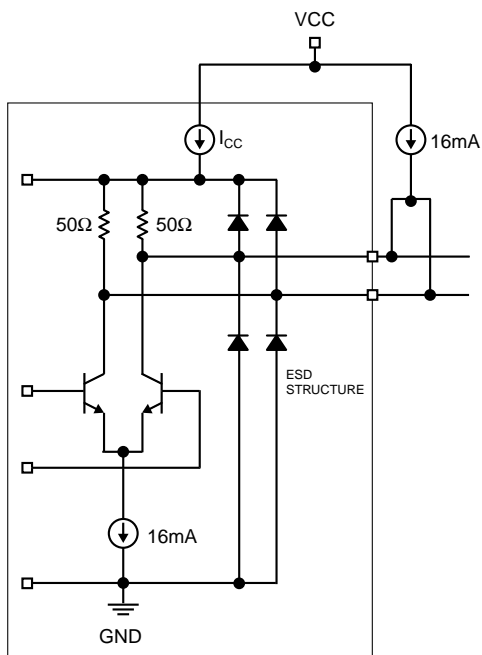


Figure 4. Power Supply Current Measurement

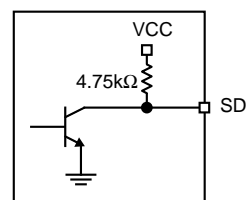
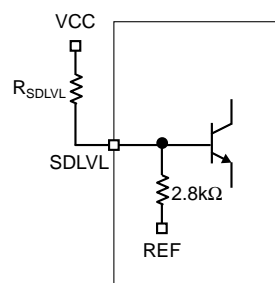
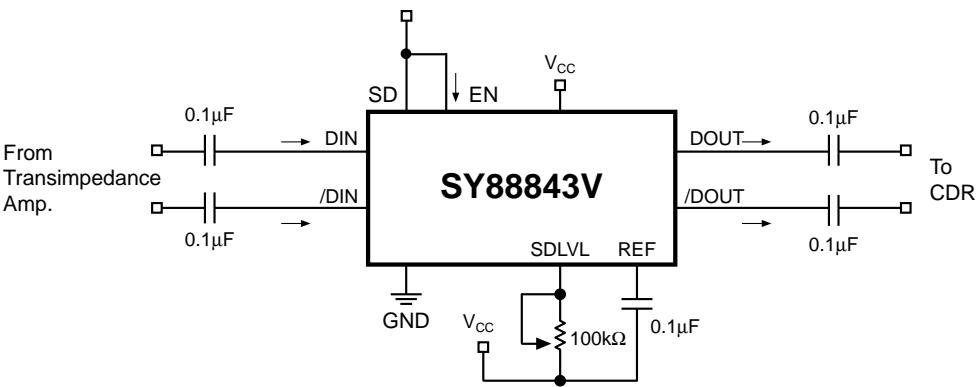


Figure 5. SD Output Structure

Figure 6. SD_{LVL} Setting Circuit

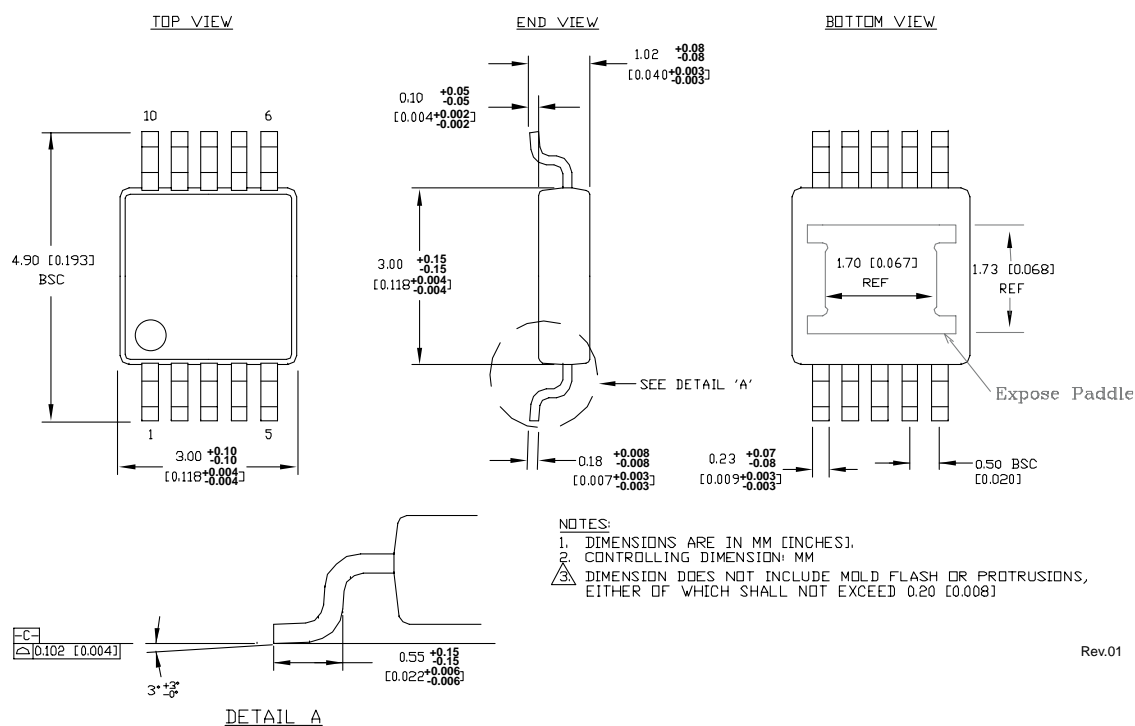
TYPICAL APPLICATIONS CIRCUIT



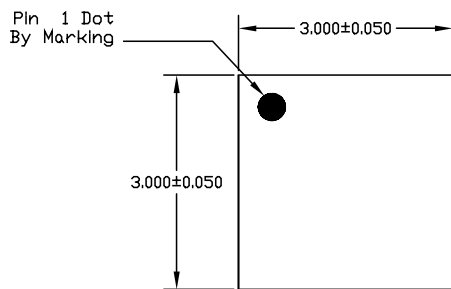
RELATED PRODUCT AND SUPPORT DOCUMENTATION

| Part Number | Function | Data Sheet Link |
|-------------------|---|---|
| SY88773V | 3.3V/5V 3.2Gbps CML Low-Power, Limiting Post Amplifier w/ TTL LOS | http://www.micrel.com/_PDF/HBW/sy88773v.pdf |
| SY88823V | 3.3V/5V 3.2Gbps CML Low-Power, Limiting Post Amplifier w/ TTL SD | http://www.micrel.com/_PDF/HBW/sy88823v.pdf |
| SY88843V | 3.3V/5V 3.2Gbps CML Low-Power, Limiting Post Amplifier w/ TTL SD | http://www.micrel.com/_PDF/HBW/sy88843v.pdf |
| SY88973V | 3.3V/5V 3.2Gbps CML Low-Power, Limiting Post Amplifier w/ TTL LOS | http://www.micrel.com/_PDF/HBW/sy88973v.pdf |
| Application Notes | Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers | http://www.micrel.com/product-info/app_hints+notes.shtml |

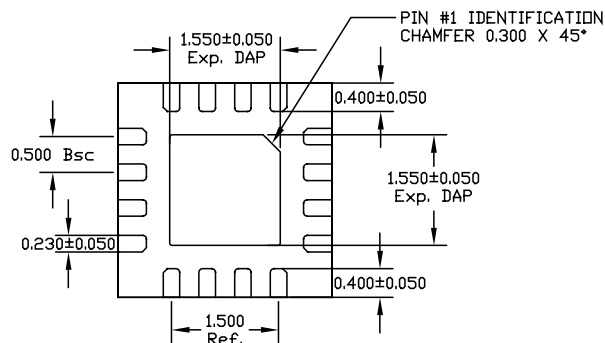
10 LEAD EPAD-MSOP (K10-2)



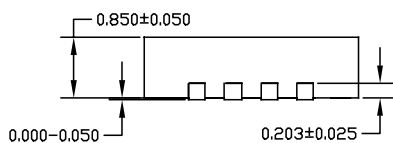
16-PIN *Micro*LEADFRAME™ (MLF-16)



TOP VIEW



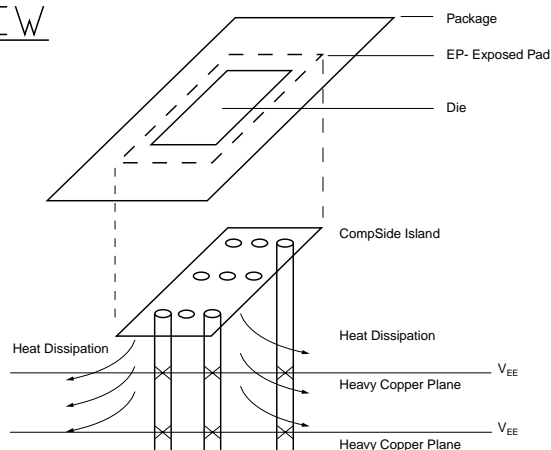
BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin MLF™ Package (Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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