

SNx4AHCT08 Quadruple 2-Input Positive-AND Gates

1 Features

- Inputs are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Servers
- Network Switches
- PCs and Notebooks
- Electronic Points of Sale

4 Simplified Schematic



3 Description

The SNx4AHCT08 devices are quadruple 2-input positive-AND gates. These devices perform the Boolean function $Y = A \times B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------|
| SNx4AHCT08 | SOIC (14) | 8.65 mm × 3.91 mm |
| | SSOP (14) | 6.20 mm × 5.30 mm |
| | SOP (14) | 12.60 mm × 5.30 mm |
| | TSSOP (14) | 5.00 mm × 4.40 mm |
| | VQFN (14) | 3.50 mm × 3.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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5 Revision History

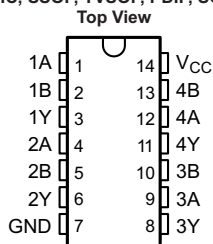
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision M (July 2014) to Revision N | Page |
|--|-------------|
| • Added T_J , Junction temperature | 4 |
| • Updated V_{IH} and V_{IL} MIN and MAX values | 4 |

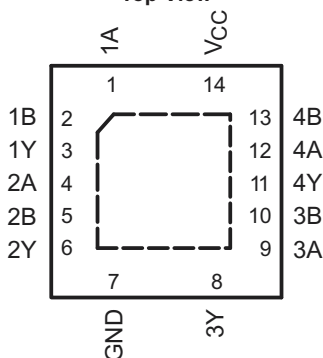
| Changes from Revision L (October 1995) to Revision M | Page |
|--|-------------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted Ordering Information table. | 1 |
| • Added Military Disclaimer to Features list. | 1 |
| • Added Applications. | 1 |
| • Added Pin Functions table | 3 |
| • Added ESD Ratings table. | 4 |
| • Changed MAX operating temperature to 125°C in Recommended Operating Conditions table. | 4 |
| • Added Thermal Information table. | 5 |
| • Added Typical Characteristics section | 6 |
| • Added Detailed Description section | 8 |
| • Added Application and Implementation section | 9 |
| • Added Power Supply Recommendations and Layout sections | 10 |

6 Pin Configuration and Functions

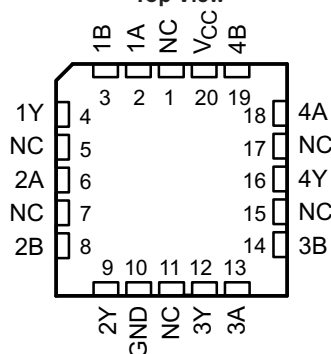
SN54AHCT08 . . . J or W Package
 14-Pin CDIP or CFP
SN74AHCT08 . . . D, DB, DGV, N, NS, or PW Package
 14-Pin SOIC, SSOP, TVSOP, PDIP, SO, or TSSOP



SN74AHCT08 . . . RGY Package
 14-Pin VQFN
 Top View



SN54AHCT08 . . . FK Package
 20-Pin LCCC
 Top View



NC – No internal connection

Pin Functions

| NAME | PIN | | | | I/O | DESCRIPTION |
|-----------------|-----------------------|-----|------------|----|-----|---------------|
| | SN74AHCT08 | | SN54AHCT08 | | | |
| | D, DB, DGV, N, NS, PW | RGY | J, W | FK | | |
| 1A | 1 | 1 | 1 | 2 | I | 1A Input |
| 1B | 2 | 2 | 2 | 3 | I | 1B Input |
| 1Y | 3 | 3 | 3 | 4 | O | 1Y Output |
| 2A | 4 | 4 | 4 | 6 | I | 2A Input |
| 2B | 5 | 5 | 5 | 8 | I | 2B Input |
| 2Y | 6 | 6 | 6 | 9 | O | 2Y Output |
| 3Y | 8 | 8 | 8 | 12 | O | 3Y Output |
| 3A | 9 | 9 | 9 | 13 | I | 3A Input |
| 3B | 10 | 10 | 10 | 14 | I | 3B Input |
| 4Y | 11 | 11 | 11 | 16 | O | 4Y Output |
| 4A | 12 | 12 | 12 | 18 | I | 4A Input |
| 4B | 13 | 13 | 13 | 19 | I | 4B Input |
| GND | 7 | 7 | 7 | 10 | — | Ground Pin |
| NC | — | — | — | 1 | — | No Connection |
| | | | | 5 | | |
| | | | | 7 | | |
| | | | | 11 | | |
| | | | | 15 | | |
| V _{CC} | 14 | 14 | 14 | 20 | — | Power Pin |

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|---|-------------------------------------|--|-----------------------|------|----|
| V _{CC} | Supply voltage range | -0.5 | 7 | V | |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 7 | V | |
| V _O | Output voltage range ⁽²⁾ | -0.5 | V _{CC} + 0.5 | V | |
| I _{IK} | Input clamp current | V _I < 0 | | -20 | mA |
| I _{OK} | Output clamp current | V _O < 0 or V _O > V _{CC} | | ±20 | mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | ±25 | mA |
| Continuous current through V _{CC} or GND | | | | ±50 | mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C | |
| T _J | Junction temperature | | 150 | °C | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | SN54AHCT08 | | SN74AHCT08 | | UNIT |
|-----------------|------------------------------------|------------|-----------------|------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -8 | | -8 | mA |
| I _{OL} | Low-level output current | | 8 | | 8 | mA |
| Δt/Δv | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI Application Report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74AHCT08 | | | | UNIT |
|-------------------------------|--|------------|-----------|-------------|----------|------|
| | | D (SOIC) | DB (SSOP) | DGV (TVSOP) | N (PDIP) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 97.5 | 109.5 | 133.3 | 59.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 58.7 | 62.1 | 55.6 | 47.3 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 51.8 | 56.9 | 66.3 | 39.5 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 22.6 | 22.6 | 7.8 | 32.4 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 51.6 | 56.3 | 56.6 | 39.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AHCT08 | | SN74AHCT08 | | UNIT |
|---------------------------------|---|-----------------|-----------------------|-----|------|------------|-------------------|------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | V | |
| | I _{OH} = -8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | | | 0.1 | | 0.1 | 0.1 | V | |
| | I _{OL} = 8 mA | | | | 0.36 | | 0.44 | 0.44 | | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 ⁽¹⁾ | ±1 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 2 | | 20 | 20 | μA | |
| ΔI _{CC} ⁽²⁾ | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | 1.35 | | 1.5 | 1.5 | mA | |
| C _i | V _I = V _{CC} or GND | 5 V | | 4 | 10 | | | 10 | pF | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

7.6 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54AHCT08 | | SN74AHCT08 | | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|------------------|--------------------|------------------|--------------------|------------------|------------------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | Y | C _L = 15 pF | | 5 ⁽¹⁾ | 6.9 ⁽¹⁾ | 1 ⁽¹⁾ | 8 ⁽¹⁾ | 1 | 8 | ns |
| t _{PHL} | | | | | | | 5 ⁽¹⁾ | 6.9 ⁽¹⁾ | 1 ⁽¹⁾ | 8 ⁽¹⁾ | |
| t _{PLH} | A or B | Y | C _L = 50 pF | | 5.5 | 7.9 | 1 | 9 | 1 | 9 | ns |
| t _{PHL} | | | | | | | 5.5 | 7.9 | 1 | 9 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.7 Noise Characteristics

 $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}^{(1)}$

| PARAMETER | | SN74AHCT08 | | | UNIT |
|-------------|--|------------|------|------|------|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | -0.4 | -0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | 4.4 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

(1) Characteristics are for surface-mount packages only.

7.8 Operating Characteristics

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------|-----------------------------|-----|------|
| C_{pd} | No load, $f = 1\text{ MHz}$ | 18 | pF |

7.9 Typical Characteristics

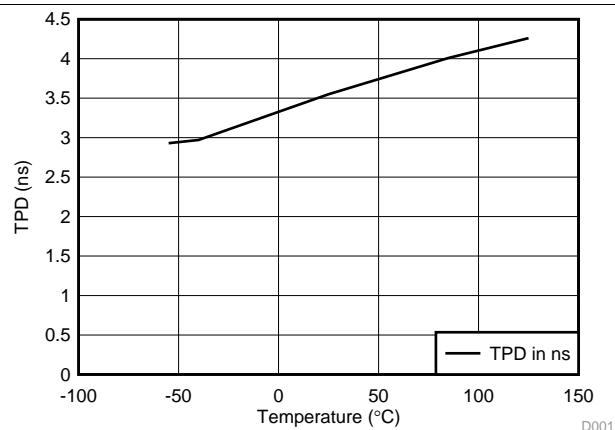
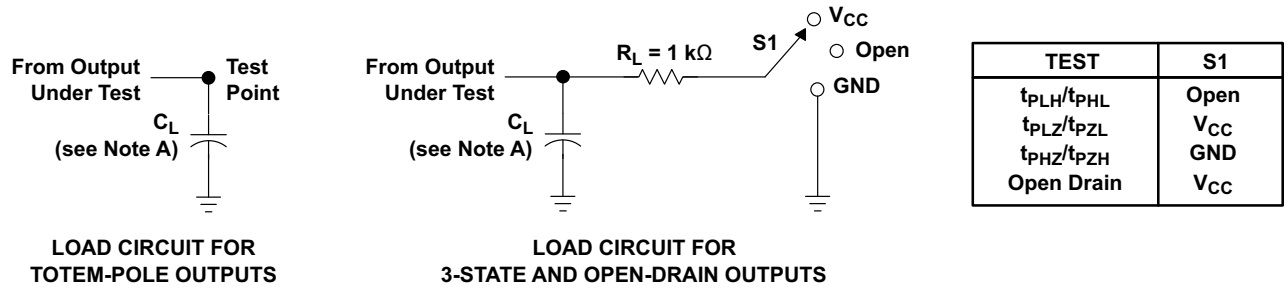


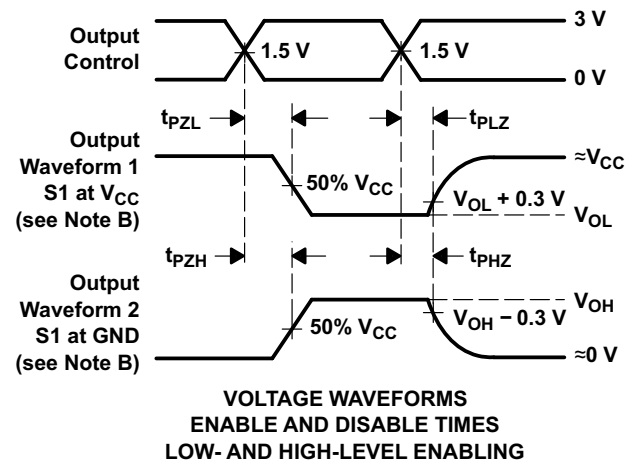
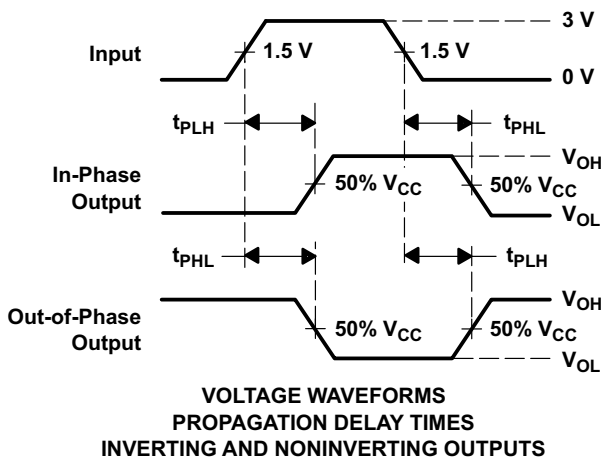
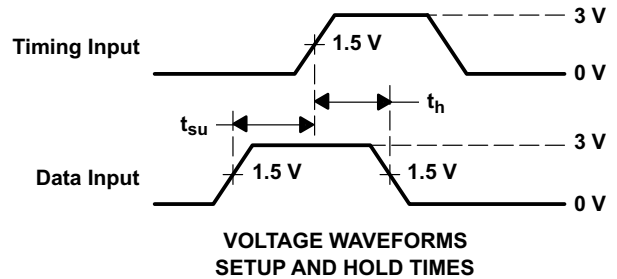
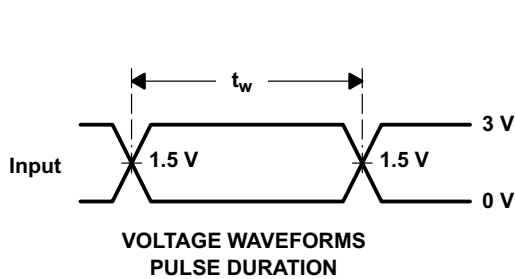
Figure 1. TPD vs Temperature

8 Parameter Measurement Information



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SNx4AHCT08 devices are quadruple 2-input positive-AND gates with low drive that will produce slow rise and fall times. This slow transition reduces ringing on the output signal. The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when $V_{CC} = 0$ V.

9.2 Functional Block Diagram



9.3 Feature Description

- Slow rise and fall time on outputs allow for low-noise outputs
- TTL inputs allow up translation from 3.3 V to 5 V

9.4 Device Functional Modes

[Table 1](#) is the function table for the SNx4AHCT08.

**Table 1. Function Table
(Each Gate)**

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | H | H |
| L | X | L |
| X | L | L |

10 Application and Implementation

10.1 Application Information

The SNx4AHCT08 devices are low-drive CMOS devices that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The TTL inputs can accept voltages down to 3.3 V and translate up to 5 V.

10.2 Typical Application

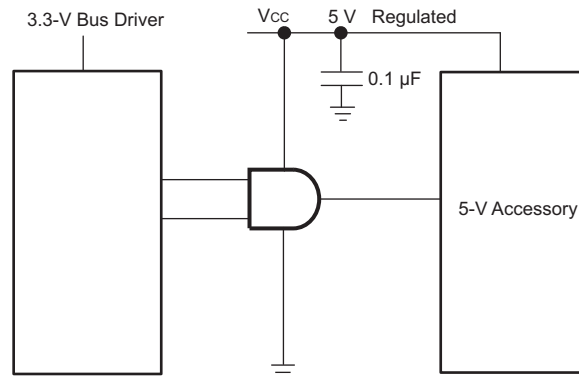


Figure 3. Typical Application Diagram

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended input conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified High and low levels: See $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend output conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part
 - Outputs should not be pulled above V_{CC}

10.2.3 Application Curves

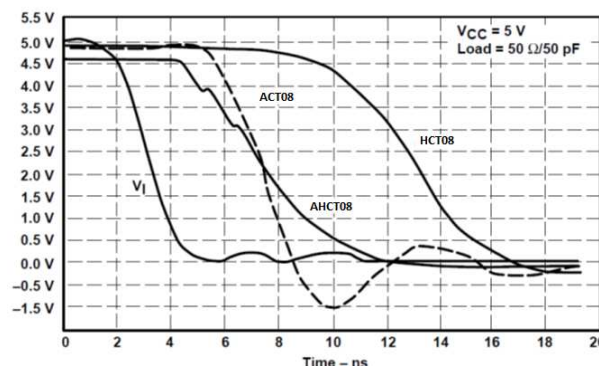


Figure 4. Switching Characteristics Comparison

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 5](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

12.2 Layout Example

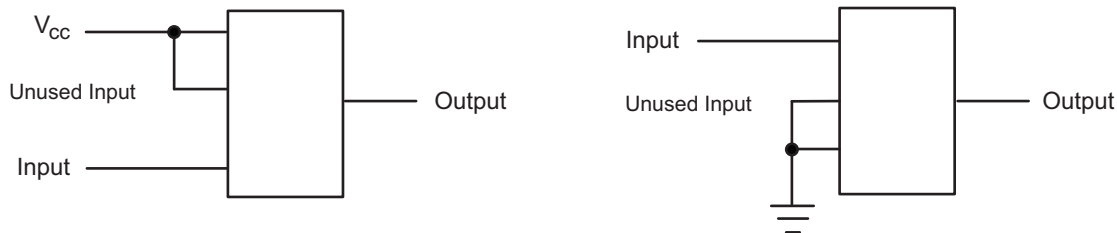


Figure 5. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54AHCT08 | Click here | Click here | Click here | Click here | Click here |
| SN74AHCT08 | Click here | Click here | Click here | Click here | Click here |

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|--------------------------------------|----------------------|--------------|--|-------------------------|
| 5962-9682101Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9682101Q2A SNJ54AHCT 08FK | Samples |
| 5962-9682101QCA | ACTIVE | CDIP | J | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9682101QC A SNJ54AHCT08J | Samples |
| 5962-9682101QDA | ACTIVE | CFP | W | 14 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9682101QD A SNJ54AHCT08W | Samples |
| 5962-9682101VDA | ACTIVE | CFP | W | 14 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9682101VD A SNV54AHCT08W | Samples |
| SN74AHCT08D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT08 | Samples |
| SN74AHCT08DBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB08 | Samples |
| SN74AHCT08DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT08 | Samples |
| SN74AHCT08DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT08 | Samples |
| SN74AHCT08DGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB08 | Samples |
| SN74AHCT08DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT08 | Samples |
| SN74AHCT08DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT08 | Samples |
| SN74AHCT08N | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -40 to 125 | SN74AHCT08N | Samples |
| SN74AHCT08NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT08 | Samples |
| SN74AHCT08PW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB08 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| SN74AHCT08PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | HB08 | Samples |
| SN74AHCT08PWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB08 | Samples |
| SN74AHCT08RGYR | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HB08 | Samples |
| SN74AHCT08RGYRG4 | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HB08 | Samples |
| SNJ54AHCT08FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9682101Q2A SNJ54AHCT08FK | Samples |
| SNJ54AHCT08J | ACTIVE | CDIP | J | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9682101QC A SNJ54AHCT08J | Samples |
| SNJ54AHCT08W | ACTIVE | CFP | W | 14 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9682101QD A SNJ54AHCT08W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHCT08, SN54AHCT08-SP, SN74AHCT08 :

- Catalog: [SN74AHCT08](#), [SN54AHCT08](#)

- Enhanced Product: [SN74AHCT08-EP](#), [SN74AHCT08-EP](#)

- Military: [SN54AHCT08](#)

- Space: [SN54AHCT08-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHCT08DGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT08DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHCT08DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHCT08NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHCT08PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT08PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT08PWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT08RGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHCT08DGVR | TVSOP | DGV | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74AHCT08DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74AHCT08DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74AHCT08NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AHCT08PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74AHCT08PWR | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74AHCT08PWRG4 | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74AHCT08RGYR | VQFN | RGY | 14 | 3000 | 367.0 | 367.0 | 35.0 |

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - △ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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