Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

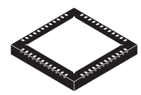
To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

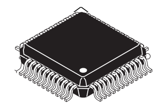
Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

Document Number: MC9RS08LA8
Rev. 2, 1/2012

MC9RS08LA8



48 QFN
Case 1975
7 mm^2



48 LQFP
Case 932
7 mm^2

MC9RS08LA8

Features:

- 8-Bit RS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 2.7 V to 5.5 V across temperature range of –40°C to 85°C
  - Subset of HC08 instruction set with added BGND instruction
- On-Chip Memory
  - 8 KB flash read/program/erase over full operating voltage and temperature
  - 256-byte random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to flash contents
- Power-Saving Modes
  - Wait and stop
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 1 MHz to 16 MHz
  - Internal clock source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; supports bus frequencies up to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
  - **LCD** — Up to 8 × 21 or 4 × 25 segments; compatible with 5 V or 3 V LCD glass displays using on-chip charge pump; functional in wait, stop modes for very low power LCD operation; frontplane and backplane pins multiplexed with GPIO functions; selectable frontplane and backplane configurations
  - **ADC** — 6-channel, 10-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop; fully functional from 2.7 V to 5.5 V.
  - **TPM** — One 2-channel 16-bit timer/pulse-width modulator (TPM) module
  - **SCI** — One 2-channel serial communications interface module with optional 13-bit break; LIN extensions
  - **SPI** — One serial peripheral interface module in 8-bit data length mode with a receive data buffer hardware match function
  - **ACMP** — Analog comparator with option to compare to internal reference
  - **MTIM** — One 8-bit modulo timer
  - **KBI** — 8-pin keyboard interrupt module
  - **RTI** — One real-time interrupt module with optional reference clock.
- Input/Output
  - 33 GPIOs including 1 output only pin and 1 input only pin.
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins.
- Package Options
  - 48-pin QFN
  - 48-pin LQFP

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	10/9/2008	Initial public released.
2	1/30/2012	Updated the case number of 48-pin QFN to 1975; updated 48-pin QFN case outline drawing.

Related Documentation

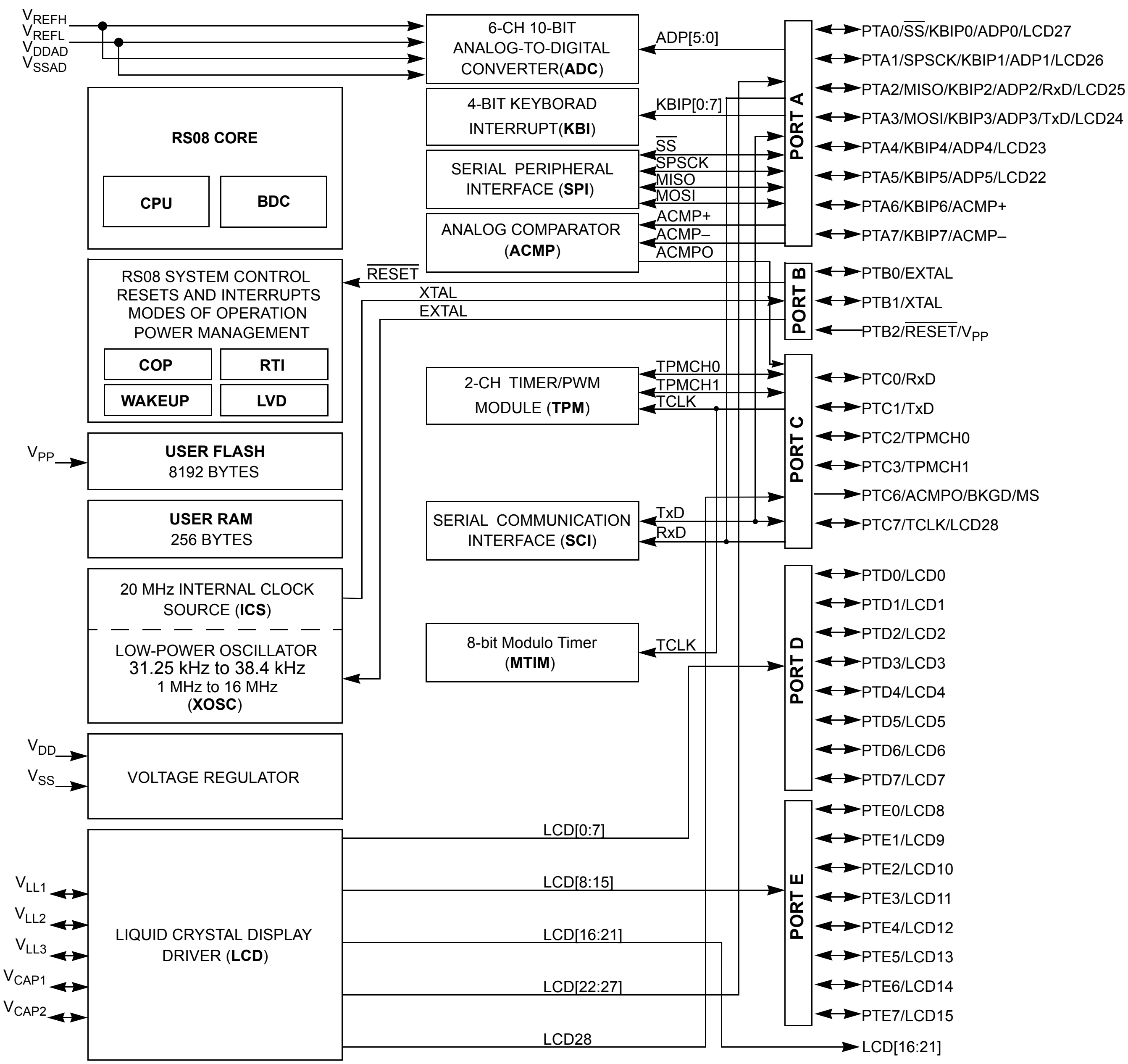
Find the most current versions of all documents at: http://www.freescale.com

Reference Manual **(MC9RS08LA8RM)**

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9RS08LA8 MCU.



NOTES:
1. PTB2/RESET/V_{PP} is an input only pin when used as port pin
2. PTC6/ACMPO/BKGD/MS is an output only pin

Figure 1. MC9RS08LA8 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08LA8 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number	<-- Lowest **Priority** --> Highest					
48	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**	**Alt 5**
1	PTD7					LCD7
2	PTD6					LCD6
3	PTD5					LCD5
4	PTD4					LCD4
5	PTD3					LCD3
6	PTD2					LCD2
7	PTD1					LCD1
8	PTD0					LCD0
9						V_{CAP1}
10						V_{CAP2}
11						V_{LL1}
12						V_{LL2}
13						V_{LL3}
14	PTA6	KBIP6	ACMP+			
15	PTA7	KBIP7	ACMP–			
16				V_{SSAD}/V_{REFL}		
17				V_{DDAD}/V_{REFH}		
18	PTB0			EXTAL		
19	PTB1			XTAL		
20				V_{DD}		
21				V_{SS}		
22	PTB2		RESET	V_{PP}		
23	PTC0		RxD			
24	PTC1		TxD			
25	PTC2		TPMCH0			
26	PTC3		TPMCH1			
27	PTC6	ACMPO	BKGD	MS		
28	PTC7		TCLK			LCD28
29	PTA0	SS	KBIP0	ADP0		LCD27
30	PTA1	SPSCK	KBIP1	ADP1		LCD26
31	PTA2	MISO	KBIP2	RxD	ADP2	LCD25

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number	<-- Lowest **Priority** --> Highest					
48	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**	**Alt 5**
32	PTA3	MOSI	KBIP3	TxD	ADP3	LCD24
33	PTA4		KBIP4	ADP4		LCD23
34	PTA5		KBIP5	ADP5		LCD22
35						LCD21
36						LCD20
37						LCD19
38						LCD18
39						LCD17
40						LCD16
41	PTE7					LCD15
42	PTE6					LCD14
43	PTE5					LCD13
44	PTE4					LCD12
45	PTE3					LCD11
46	PTE2					LCD10
47	PTE1					LCD9
48	PTE0					LCD8

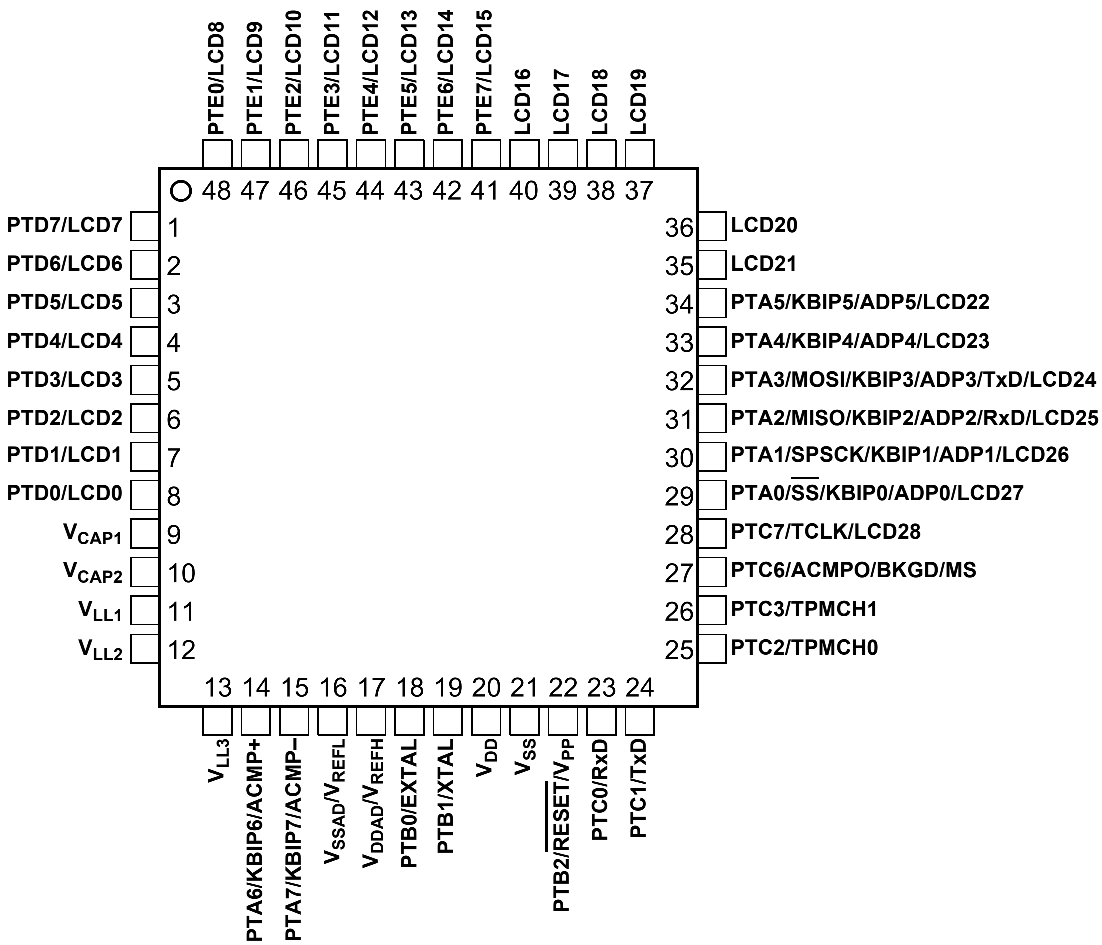


Figure 2. MC9RS08LA8 Series in 48-Pin QFN/LQFP Package

3 Electrical Characteristics

This chapter contains electrical and timing specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	2.7 to 5.5	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{RESET}/V_{PP}$ pin which is internally clamped to V_{SS} only.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than IDD, the injection current may flow out of VDD and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_{JMAX}	105	°C
Thermal resistance Single layer board 48-pin LQFP 48-pin QFN Four layer board 48-pin LQFP 48-pin QFN	θ_{JA}	 71 84 49 28	°C/W

The average chip-junction temperature (TJ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts chip internal power

$P_{I/O}$ = Power dissipation on input and output pins user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between PD and TJ (if PI/O is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (PD)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation A-3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.4 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85°C	I_{LAT}	±100[2]	—	mA
	Latch-up current at T_A = 85°C	I_{LAT}	±75[3]	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.
2 These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of ±100 mA.
3 This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to ±75 mA.

3.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient)

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	P	Supply voltage (run, wait and stop modes) 0 < f_{Bus} <10 MHz	V_{DD}	2.7	—	5.5	V
2	D	Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	0.8[1]	—	—	V
3	P	Low-voltage Detection threshold (V_{DD} falling)	V_{LVD}	—	1.8	—	V
4	C	Power on RESET (POR) voltage	V_{POR}	0.9	1.4	1.7	V
5	P	Input high voltage (V_{DD} > 5V) (all digital inputs)	V_{IH}	0.70 × V_{DD}	—	—	V
6	P	Input high voltage (2.7 V ≤ V_{DD} ≤ 5 V) (all digital inputs)	V_{IH}	0.85 × V_{DD}	—	—	V
7	P	Input low voltage (V_{DD} > 5 V) (all digital inputs)	V_{IL}	—	—	0.30 × V_{DD}	V
8	P	Input low voltage (2.7 V ≤ V_{DD} ≤ 5 V) (all digital inputs)	V_{IL}	—	—	0.30 × V_{DD}	V
9	C	Input hysteresis (all digital inputs)	V_{hys}	0.06 × V_{DD}	—	—	V
10	P	Input leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input only pins	|IIn|	—	0.025	1.0	μA
11	P	High impedance (off-state) leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input/output	|IOZ|	—	0.025	1.0	μA
12	C	Internal pullup/pulldown resistors[2](all port pins)	R_{PU}	20	45	65	kΩ
13	P	Output high voltage (all ports)[3,4] I_{OH} = –5 mA (V_{DD} ≥ 4.5 V) I_{OH} = –3 mA (V_{DD} ≥ 3 V)	V_{OH}	V_{DD} – 0.8	—	—	V
14	C	Maximum total I_{OH} for all port pins	|IOHT|	—	—	100	mA

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
15	P	Output low voltage (port A)[4] I_{OL} = 5 mA ($V_{DD} \geq$ 4.5 V) I_{OL} = 3 mA ($V_{DD} \geq$ 3 V)	V_{OL}	—	—	0.8 0.8	V
16	C	Maximum total I_{OL} for all port pins	I_{OLT}	—	—	100	mA
17	C	dc injection current[5,6,7] $V_{In} < V_{SS}$, $V_{In} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins		— —	— —	0.2 0.8	mA mA
18	C	Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

1 This parameter is characterized and not tested on each device.

2 Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

3 The I_{OH} is for high output drive strength.

4 It is tested under high output drive strength only.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{RESET}/V_{PP}$ which is internally clamped to V_{SS} only

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 This parameter is characterized and not tested on each device.

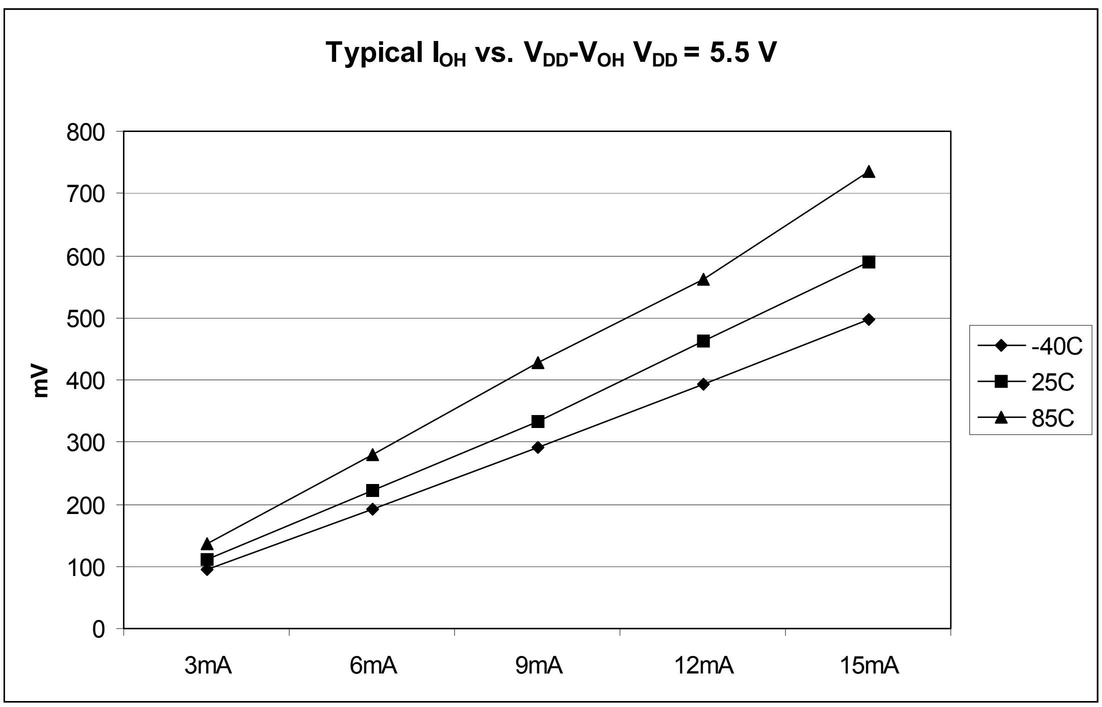


Figure 3. Typical I_{OH} vs. V_{DD}-V_{OH} (V_{DD} = 5.5 V)

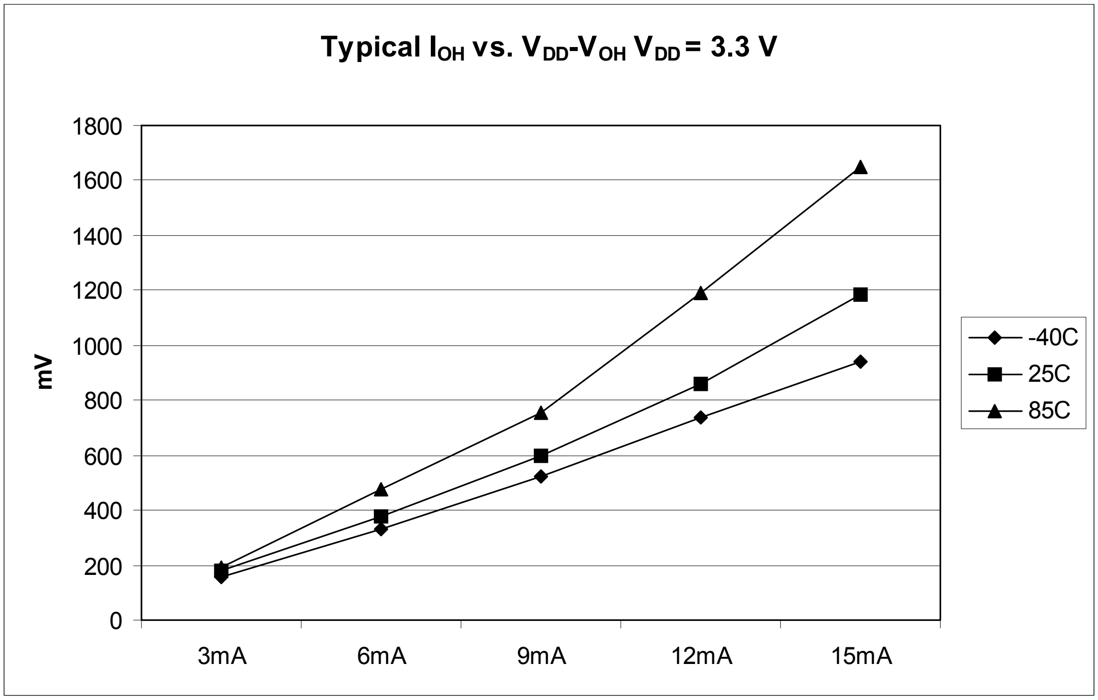


Figure 4. Typical I_{OH} vs. V_{DD}-V_{OH} (V_{DD} = 3.3 V)

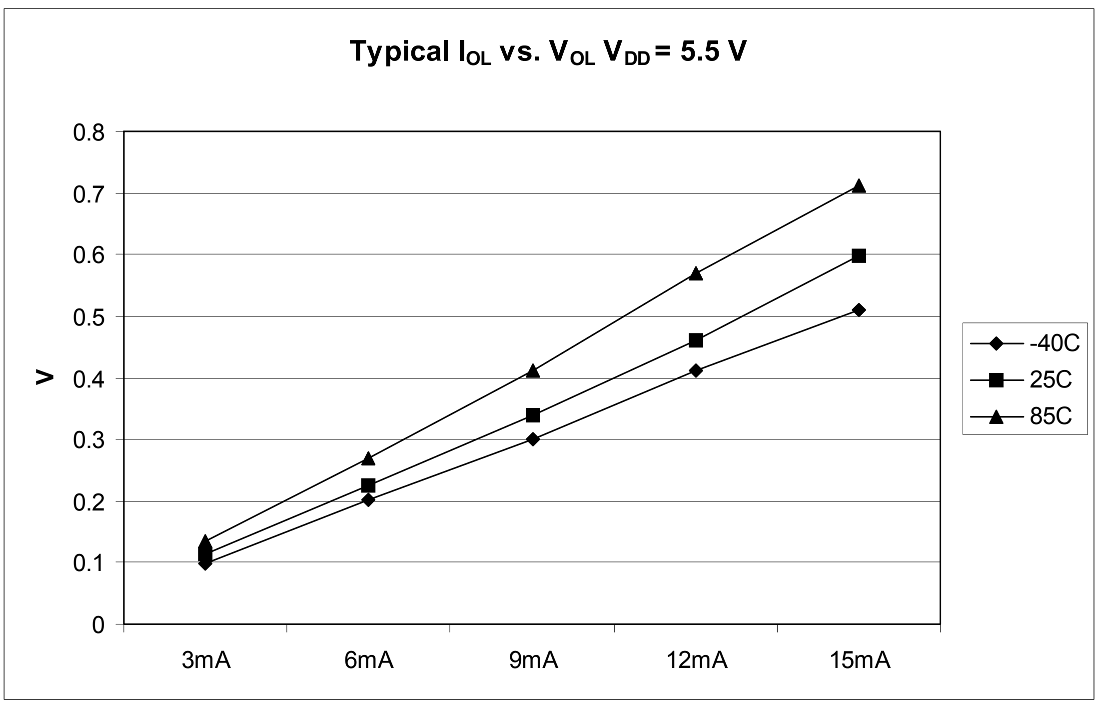


Figure 5. Typical I_{OL} vs. V_{OL} (V_{DD} = 5.5 V)

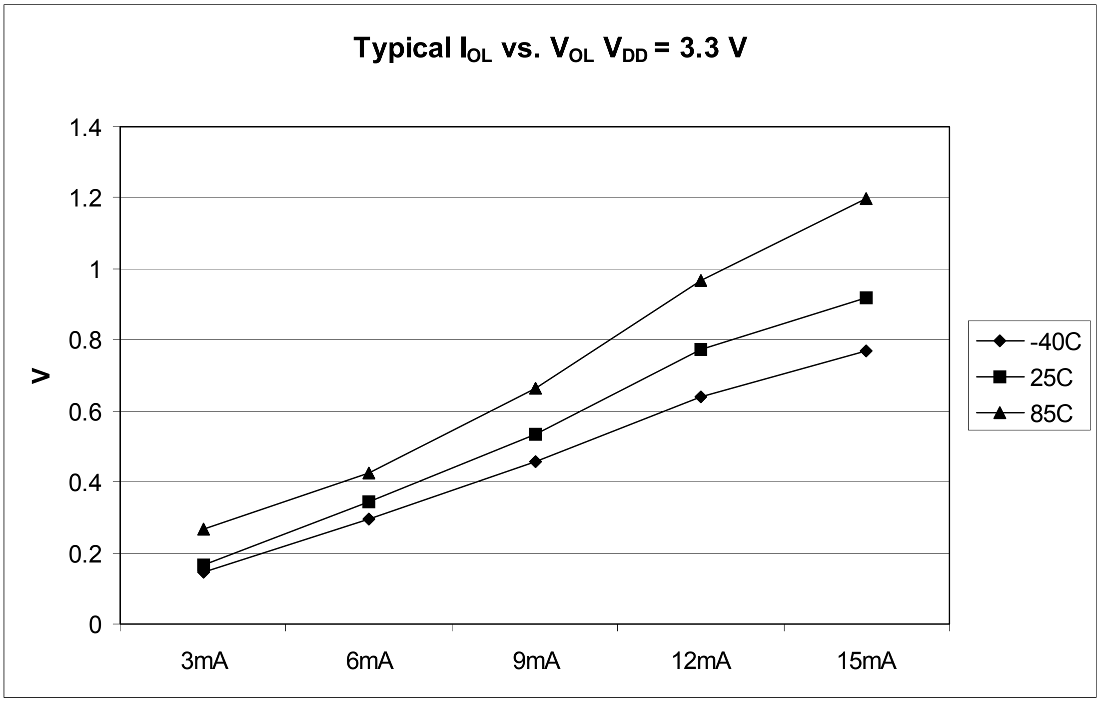


Figure 6. Typical I_{OL} vs. V_{OL} (V_{DD} = 3.3 V)

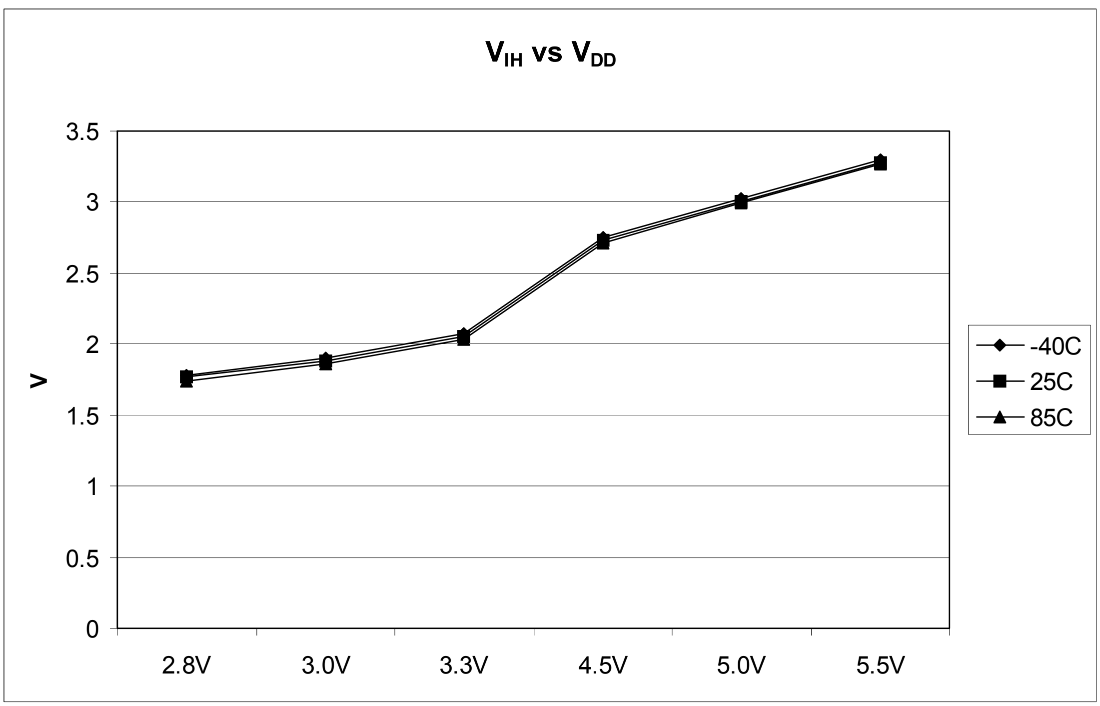


Figure 7. Typical V_{DD} vs. V_{IH}

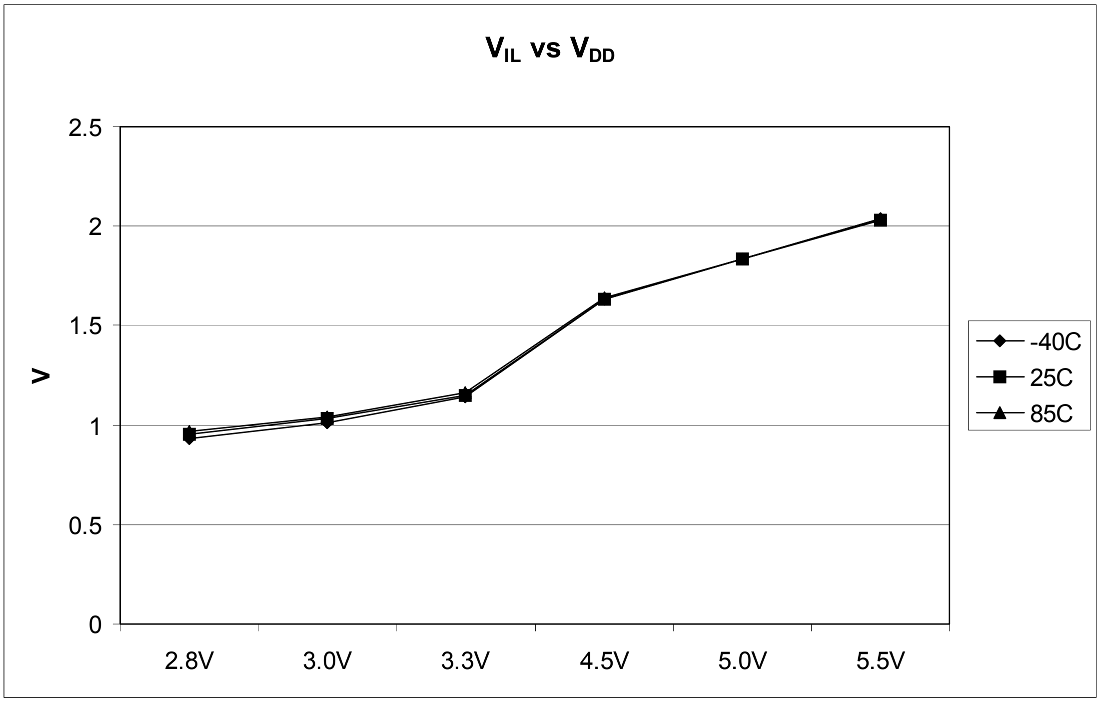


Figure 8. Typical V_{DD} vs. V_{IL}

3.6 Supply Current Characteristics

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Unit
1	P	Run supply current[2] measured at (f_{Bus} = 10 MHz)	RI_{DD10}	5	3.71	mA
				3.3	3.68	mA
				3	3.67	mA
				2.7	3.66	mA
2	P	Wait mode supply current	WI_{DD1}	5	1.37	mA
				3.3	1.37	mA
				3	1.37	mA
				2.7	1.36	mA
3	P	Stop mode supply current	SI_{DD}	5	1.40	µA
				3.3	1.35	µA
				3	1.31	µA
				2.7	1.25	µA
4	C	ADC adder from stop[3]	—	5	125.45	µA
				3.3	122.04	µA
				3	121.59	µA
				2.7	121.22	µA
5	C	ACMP adder from stop (ACME = 1)	—	5	21	µA
				3	18.5	µA

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Unit
6	C	RTI adder from stop with 1 kHz clock source enabled[4]	—	5	2.4	μA
				3	1.9	μA
8	C	LVI adder from stop (LVDE = 1 and LVDSE = 1)	—	5	70	μA
				3	65	μA

1 Typicals are measured at 25 °C.
2 Does not include any dc loads on port pins
3 Required asynchronous ADC clock and LVD to be enabled.
4 Most customers are expected to find that auto-wakeup from stop can be used instead of the higher current wait mode. Wait mode typical is 1.37 mA at 5 V and 3 V with f_{Bus} = 10 MHz.

3.7 External (XOSC) and Internal (ICS) Oscillator Characteristics

Reference Figure 9 for crystal or resonator circuit.

Table 9. External Oscillator Specifications (Temperature Range = –40 to 85°C Ambient)

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Oscillator crystal or resonator (EREFS = 1) Low range, (IREFS = x) High range, FLL bypassed external (CLKS = 10, IREFS = x) High range, FLL engaged external (CLKS = 00, IREFS = 0)	 f_{lo} f_{hi_byp} f_{hi_eng}	 32 1 1	 — — —	 38.4 10 10	 kHz MHz MHz
Load capacitors	C_1 C_2	See Note [2]			
Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F		 10 1		 MΩ MΩ
Series resistor Low range Low Gain (HGO = 0) High Gain (HGO = 1) High range Low Gain (HGO = 0) High Gain (HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 10 20	 — — — — — —	kΩ
Crystal start-up time [3, 4] Low range High range	 t_{CSTL} t_{CSTH}	 — —	 500 4	 — —	ms
Square wave input clock frequency (EREFS = 0) FLL bypass external (CLKS = 10) FLL engaged external (CLKS = 00)	f_{extal}	 0 0.03125	 — —	 20 5	MHz
Average internal reference frequency - untrimmed	f_{int_ut}	25	31.25	41.66	kHz
Average internal reference frequency - trimmed	f_{int_t}	31.25	31.25	39.0625	kHz
DCO output frequency range - untrimmed	f_{dco_ut}	12.8	16	21.33	MHz
DCO output frequency range - trimmed	f_{dco_t}	16	16	20	MHz
Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco\_res\_t}$	—	—	±0.2	$\%f_{dco}$
Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	—	±2	$\%f_{dco}$
FLL acquisition time [3,5]	$t_{acquire}$	—	—	1	ms
Long term Jitter [6] of DCO output clock (averaged over 2ms interval)	C_{Jitter}	—	—	0.6	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 See crystal or resonator manufacturer's recommendation.

3 This parameter is characterized and not tested on each device.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[6] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

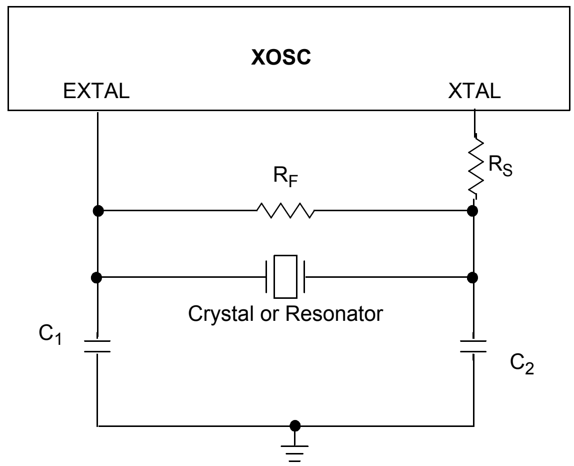


Figure 9. Typical Crystal or Resonator Circuit

3.8 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.8.1 Control Timing

Table 10. Control Timing

Parameter	Symbol	Min	Typical	Max	Unit
Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	0	—	10	MHz
Real time interrupt internal oscillator period	t_{RTI}	700	1000	1300	µs
External $\overline{\text{RESET}}$ pulse width[1]	t_{extrst}	150	—	—	ns
KBI pulse width[2]	t_{KBIPW}	1.5 t_{cyc}	—	—	ns
KBI pulse width in stop[1]	t_{KBIPWS}	100	—	—	ns
Port rise and fall time (load = 50 pF)[3] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	11 35	— —	ns

[1] This is the shortest pulse that is guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

[2] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

[3] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

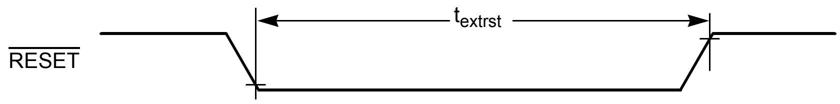


Figure 10. Reset Timing

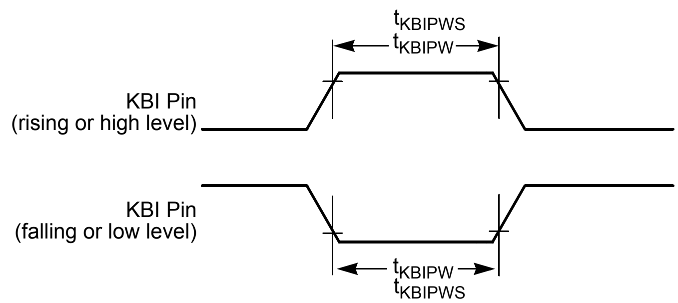


Figure 11. KBI Pulse Width

3.8.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM/MTIM Input Timing

Function	Symbol	Min	Max	Unit
External clock frequency	f_{TCLK}	0	f_{Bus}1/4	MHz
External clock period	t_{TCLK}	4	—	t_{CYC}
External clock high time	t_{clkh}	1.5	—	t_{CYC}
External clock low time	t_{clkl}	1.5	—	t_{CYC}
Input capture pulse width	f_{ICPW}	1.5	—	t_{CYC}

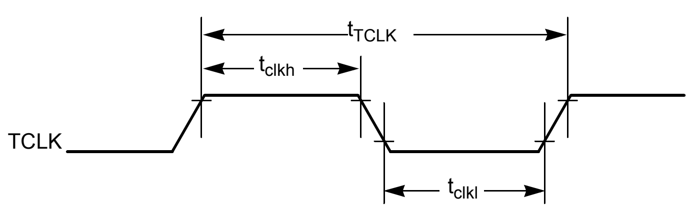


Figure 12. Timer External Clock

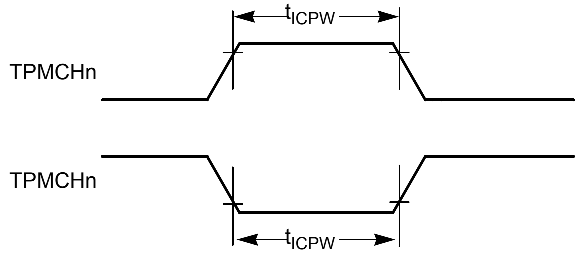


Figure 13. Timer Input Capture Pulse

3.9 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{DD}	2.7	—	5.5	V
Supply current (active)	I_{DDAC}	—	20	35	µA
Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
Analog input offset voltage[1]	V_{AIO}	—	20	40	mV
Analog Comparator hysteresis[1]	V_H	3.0	9.0	15.0	mV
Analog source impedance	R_{AS}	—	—	10	kΩ
Analog input leakage current	I_{ALKG}	—	—	1.0	µA
Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	µs
Analog Comparator bandgap reference voltage	V_{BG}	1.208	1.208	1.208	V

1 These data are characterized but not production tested. Measurements are made with the device entered STOP mode.

3.10 Internal Clock Source Characteristics

Table 13. Internal Clock Source Specifications

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Average internal reference frequency — untrimmed	f_{int_ut}	25	31.25	41.66	kHz
Average internal reference frequency — trimmed	f_{int_t}	31.25	39.0625[2]	39.0625	kHz
DCO output frequency range — untrimmed	f_{dco_ut}	12.8	16	21.33	MHz
DCO output frequency range — trimmed	f_{dco_t}	16	20[3]	20	MHz
Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco\_res\_t}$	—	—	0.2	%fdco
Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	—	2	%fdco
FLL acquisition time[4,5]	$t_{acquire}$	—	—	1	ms
Stop recovery time (FLL wakeup to previous acquired frequency) IREFSTEN = 0 IREFSTEN = 1	t_{wakeup}	—	 100 86	—	µs

1 Data in typical column was characterized at 3.0 V and 5.0 V, 25 °C or is typical recommended value.
2 This value has been trimmed to 39.0625 kHz when out of factory
3 This value has been trimmed to 20 MHz when out of factory

[4] This parameter is characterized and not tested on each device.

[5] This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBILP) to FLL enabled (FEI, FBI).

3.11 ADC Characteristics

Table 14. 5 Volt 10-bit ADC Operating Conditions

Characteristic	Conditions	Symbol	Min	Typical[1]	Max	Unit
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V
	Delta to V_{DD} ($V_{DD} – V_{DDAD}$)[2]	ΔV_{DDAD}	–100	0	100	mV
Ground voltage	Delta to V_{SS} ($V_{SS} – V_{SSAD}$)[2]	ΔV_{SSAD}	–100	0	100	mV
Ref voltage high	—	V_{REFH}	2.7	V_{DDAD}	V_{DDAD}	V
Ref voltage low	—	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V
Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF
Input resistance	—	R_{ADIN}	—	3	5	kΩ
Analog source resistance external to MCU	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	— —	— —	5 10	kΩ
	8-bit mode (all valid f_{ADCK})		—	—	10	
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz
	Low power (ADLPC = 1)		0.4	—	4.0	

[1] Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] DC potential difference.

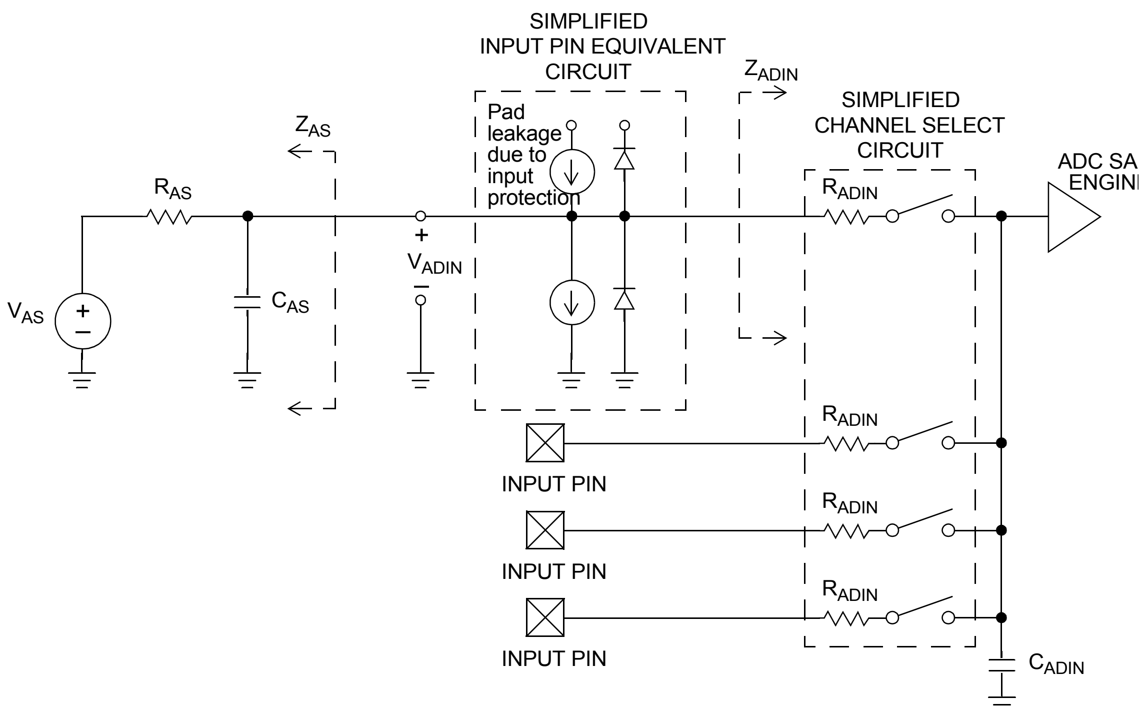


Figure 14. ADC Input Impedance Equivalency Diagram

Table 15. 10-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

Characteristic	Conditions	C	Symbol	Min	Typical[1]	Max	Unit
Supply current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	133	—	µA
Supply current ADLPC=1 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	218	—	µA
Supply current ADLPC=0 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	327	—	µA
Supply current ADLPC=0 ADLSMP=0 ADCO=1	$V_{DDAD} \le 5.5$ V	P	I_{DDAD}	—	0.582	1	mA
Supply current	Stop, Reset, Module Off		I_{DDAD}	—	0.011	1	µA
ADC asynchronous clock source	High Speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low Power (ADLPC = 1)			1.25	2	3.3	

Table 15. 10-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$) (continued)

Characteristic	Conditions	C	Symbol	Min	Typical[1]	Max	Unit
Conversion time (Including sample time)	Short Sample (ADLSMP = 0)	P	t_{ADC}	—	20	—	ADCK cycles
	Long Sample (ADLSMP = 1)			—	40	—	
Sample time	Short Sample (ADLSMP = 0)	P	t_{ADS}	—	3.5	—	ADCK cycles
	Long Sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted error	10-bit mode	P	E_{TUE}	—	±1	±2.5	LSB[2]
	8-bit mode			—	±0.5	±1.0	
Differential non-linearity	10-bit mode	P	DNL	—	±0.5	±1.0	LSB[2]
	8-bit mode			—	±0.3	±0.5	
	Monotonicity and no-missing-code guaranteed						
Integral non-linearity	10-bit mode	C	INL	—	±0.5	±1.0	LSB[2]
	8-bit mode			—	±0.3	±0.5	
Zero-scale error	10-bit mode	P	E_{ZS}	—	±0.5	±1.5	LSB[2]
	8-bit mode			—	±0.5	±0.5	
Full-scale error $V_{ADIN} = V_{DDA}$	10-bit mode	P	E_{FS}	—	±0.5	±1.5	LSB[2]
	8-bit mode			—	±0.5	±0.5	
Quantization error	10-bit mode	D	E_Q	—	—	±0.5	LSB[2]
	8-bit mode			—	—	±0.5	
Input leakage error pad leakage[3] * R_{AS}	10-bit mode	D	E_{IL}	—	±0.2	±2.5	LSB[2]
	8-bit mode			—	±0.1	±1	

[1] Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] 1 LSB = $(V_{REFH} – V_{REFL})/2^N$

[3] Based on input pad leakage current. Refer to pad electrical.

3.12 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.12.1 Control Timing

Table 16. Control Timing

Characteristic	Symbol	Min	Typical	Max	Unit
Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	DC	—	10	MHz
Real time interrupt internal oscillator period	t_{RTI}	700	1000	1300	μs

Table 16. Control Timing (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
External $\overline{RESET}$ pulse width[1]	t_{extrst}	150		—	ns
KBI pulse width[2]	t_{KBIPW}	1.5 t_{cyc}		—	ns
KBI pulse width in stop[1]	t_{KBIPWS}	100		—	ns
Port rise and fall time (load = 50 pF)[3] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	11 35	— —	ns

1 This is the shortest pulse that is guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

2 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

3 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

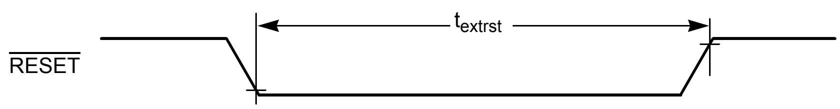


Figure 15. Reset Timing

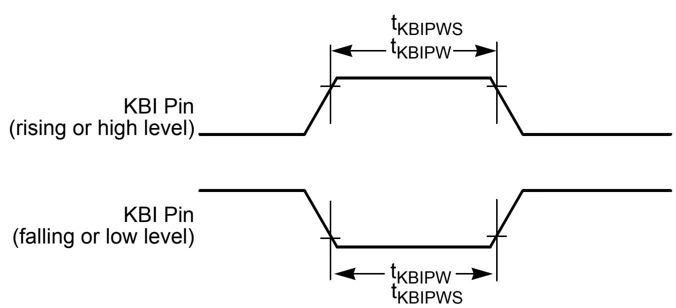


Figure 16. KBI Pulse Width

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

Table 17. Flash Characteristics

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Supply voltage for program/erase	V_{DD}	2.7	—	5.5	V
Program/Erase voltage	V_{PP}	11.8	12	12.2	V
V_{PP} current Program Mass erase	I_{VPP_prog} I_{VPP_erase}	— —	— —	200 100	µA µA
Supply voltage for read operation 0 < f_{Bus} < 10 MHz	V_{Read}	2.7	—	5.5	V

Table 17. Flash Characteristics (continued)

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Byte program time	t_{prog}	20	—	40	µs
Mass erase time	t_{me}	500	—	—	ms
Cumulative program HV time[2]	t_{hv}	—	—	8	ms
Total cumulative HV time (total of t_{me} & t_{hv} applied to device)	t_{hv_total}	—	—	2	hours
HVEN to program setup time	t_{pgs}	10	—	—	µs
PGM/MASS to HVEN setup time	t_{nvs}	5	—	—	µs
HVEN hold time for PGM	t_{nvh}	5	—	—	µs
HVEN hold time for MASS	t_{nvh1}	100	—	—	µs
V_{PP} to PGM/MASS setup time	t_{vps}	20	—	—	ns
HVEN to V_{PP} hold time	t_{vph}	20	—	—	ns
V_{PP} rise time[3]	t_{vrs}	200	—	—	ns
Recovery time	t_{rcv}	1	—	—	µs
Program/erase endurance T_L to T_H = –40 °C to 85 °C	—	1000	—	—	cycles
Data retention	t_{D_ret}	15	—	—	years

1 Typicals are measured at 25 °C.

2 t_{hv} is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

3 Fast V_{PP} rise time may potentially trigger the ESD protection structure, which may result in over current flowing into the pad and cause permanent damage to the pad. External filtering for the V_{PP} power source is recommended. An example V_{PP} filter is shown in Figure 17.

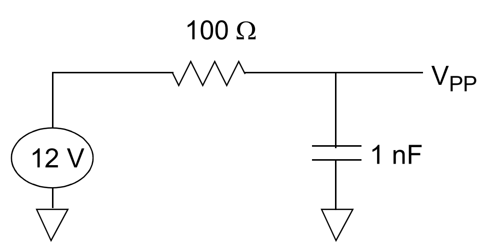
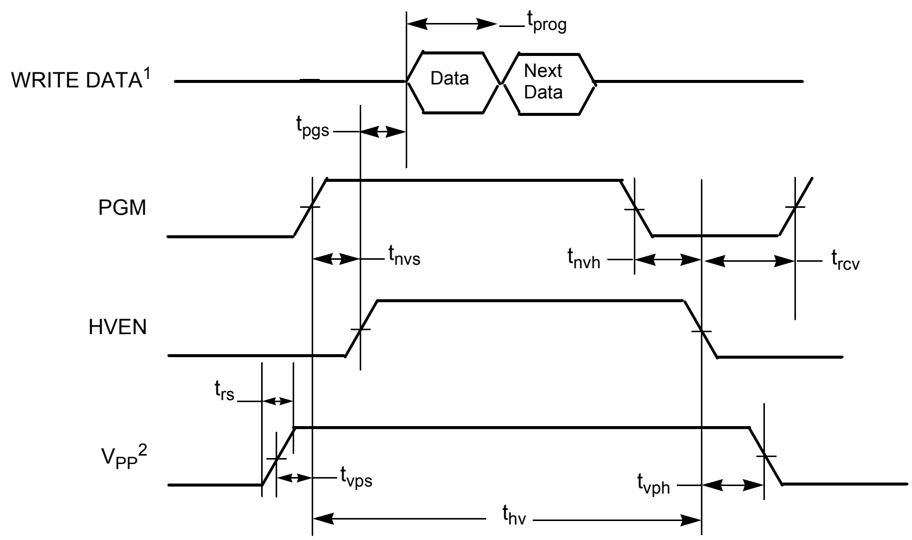


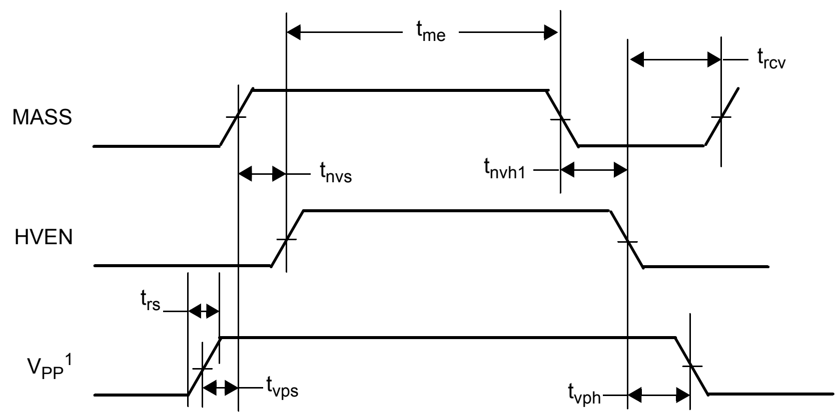
Figure 17. Example V_{PP} Filtering



1 Next Data applies if programming multiple bytes in a single row, refer to *MC9RS08LA8 Series Reference Manual*.

2 V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 18. Flash Program Timing

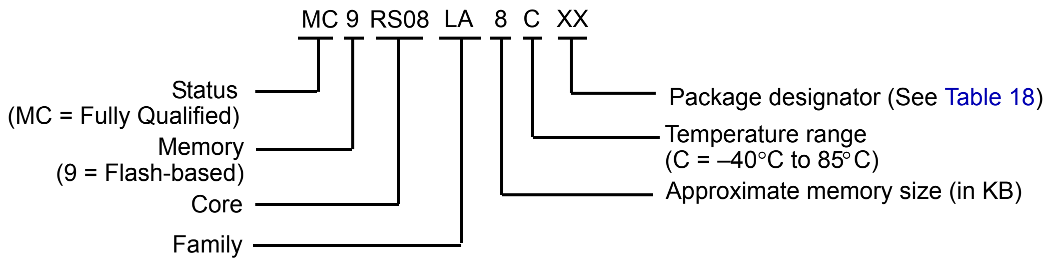


1 V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 19. Flash Mass Erase Timing

4 Ordering Information

This section contains ordering information for MC9RS08LA8 devices. See below for an example of the device numbering system.



5 Package Information and Mechanical Drawings

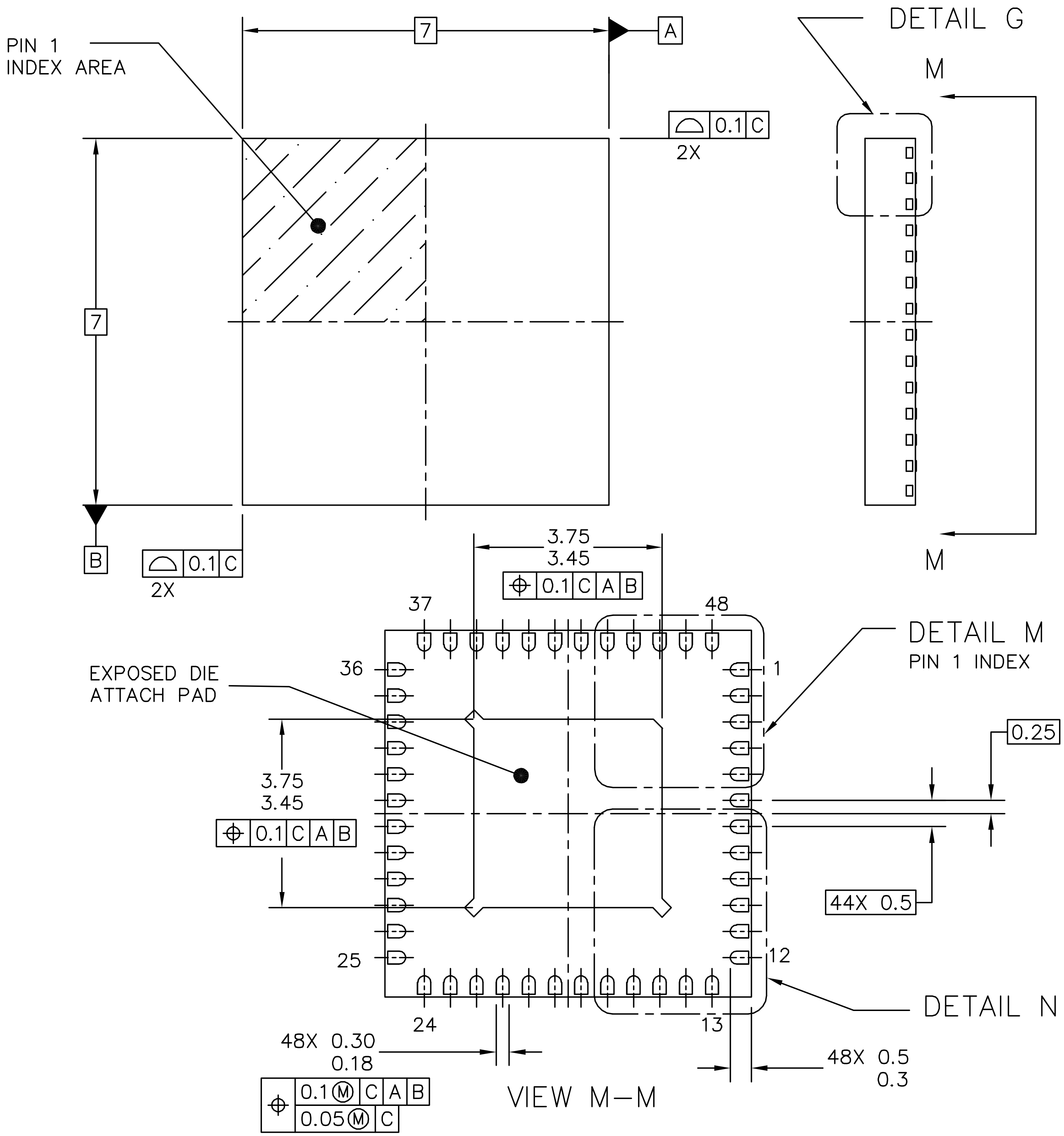
Table 18 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9RS08LA8 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

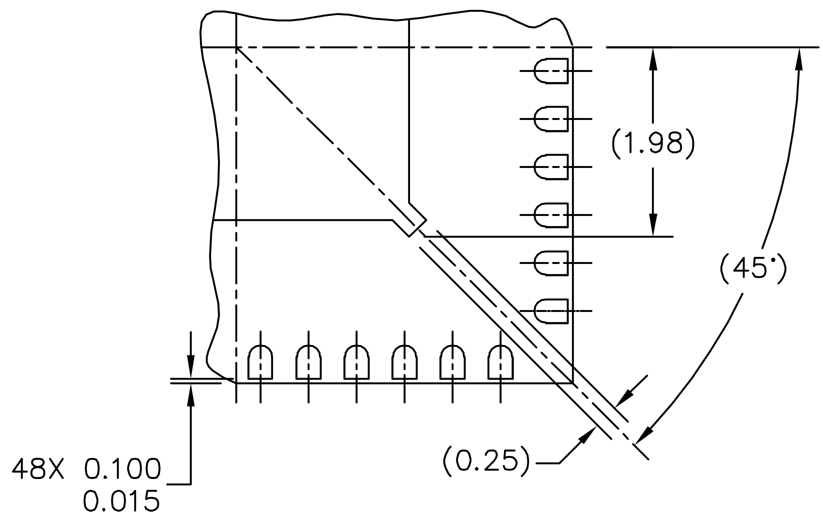
- Click on the appropriate link in Table 18, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 18) in the “Enter Keyword” search box at the top of the page.

Table 18. Device Numbering System

Device Number	Memory		Package		
	FLASH	RAM	Type	Designator	Document No.
MC9RS08LA8	8 KB	256 bytes	48-Pin QFN	FT	98ARL10606D
			48-Pin LQFP	LF	98ASH00962A

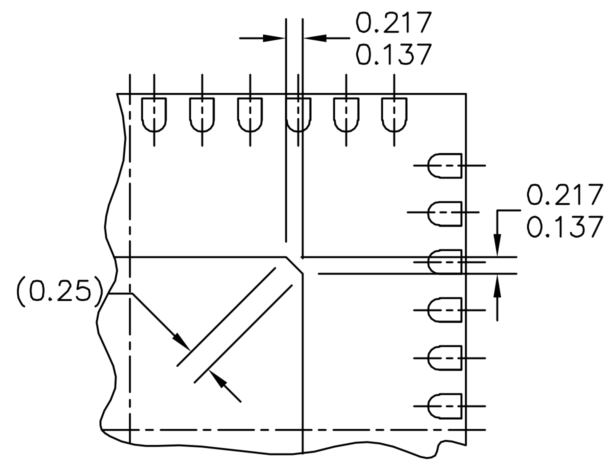


MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARL10606D	REV: 0
	CASE NUMBER: 1975–01	29 AUG 2007
	STANDARD: JEDEC–MO–220 VKKD–2	



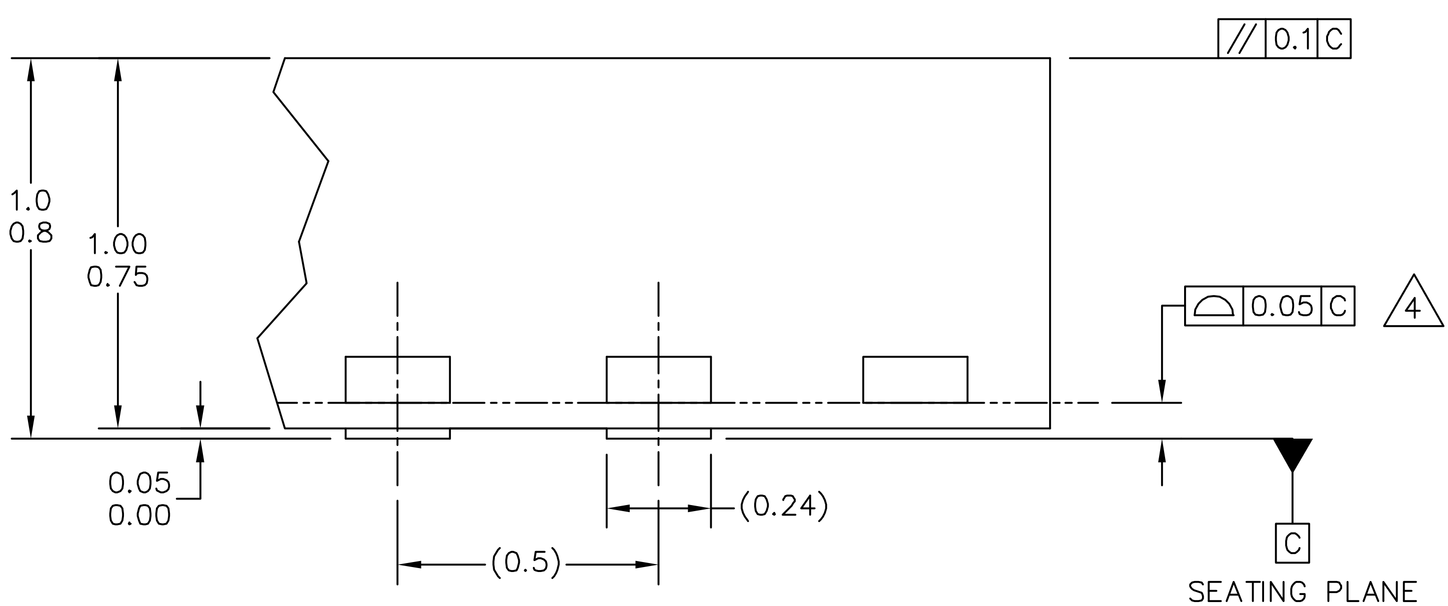
DETAIL N

PREFERRED CORNER CONFIGURATION



DETAIL M

PREFERED PIN 1 BACKSIDE IDENTIFIER



DETAIL G

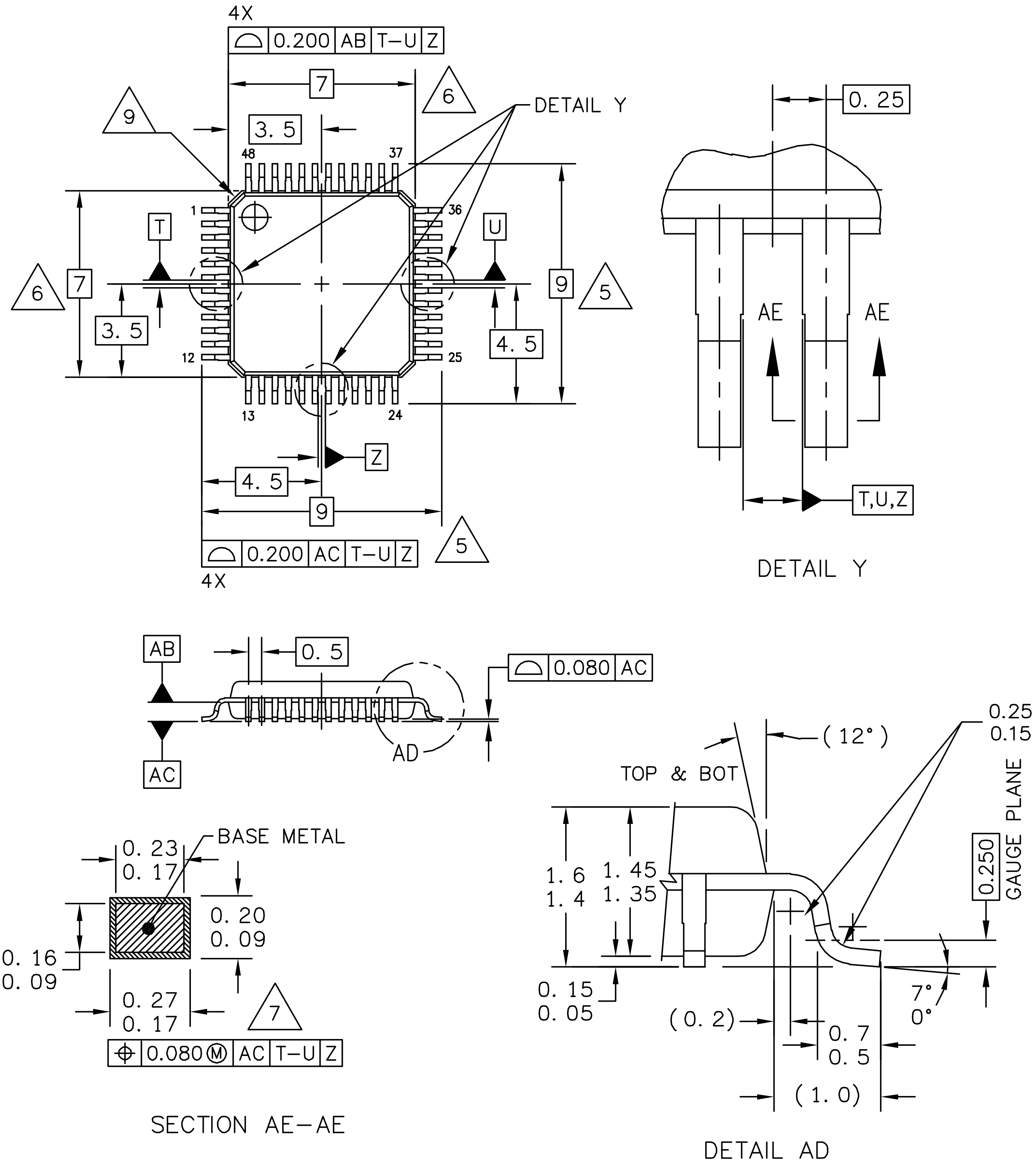
VIEW ROTATED 90° CW

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARL10606D	REV: O
	CASE NUMBER: 1975-01	29 AUG 2007
	STANDARD: JEDEC-MO-220 VKKD-2	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARL10606D	REV: O
	CASE NUMBER: 1975–01	29 AUG 2007
	STANDARD: JEDEC–MO–220 VKKD–2	



MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:
LQFP, 48 LEAD, 0. 50 PITCH
(7. 0 X 7. 0 X 1. 4)

DOCUMENT NO: 98ASH00962A

REV: G

CASE NUMBER: 932–03

14 APR 2005

STANDARD: JEDEC MS–026–BBC

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.

△5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.

△6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.

△7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.

8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.

△9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A	REV: G
	CASE NUMBER: 932–03	14 APR 2005
	STANDARD: JEDEC MS–026–BBC	

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Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
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Document Number: MC9RS08LA8
Rev. 2
1/2012