

# RF Power LDMOS Transistor

## N-Channel Enhancement-Mode Lateral MOSFET

This 1.26 W RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 728 to 3600 MHz.

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQ} = 90$  mA,  $P_{out} = 1.26$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.<sup>(1)</sup>

### 2100 MHz

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	21.6	23.2	9.1	-42.0	-11
2140 MHz	21.8	23.0	9.0	-41.5	-15
2170 MHz	21.7	22.6	8.7	-41.7	-15

### 2300 MHz

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2300 MHz	21.2	23.6	9.0	-40.9	-10
2350 MHz	21.6	22.6	8.6	-40.0	-22
2400 MHz	20.7	21.0	8.3	-40.1	-9

### 2600 MHz

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2500 MHz	19.6	22.0	9.8	-44.8	-7
2600 MHz	21.0	22.7	9.4	-41.4	-15
2700 MHz	19.6	21.2	8.9	-39.7	-5

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQ} = 80$  mA,  $P_{out} = 1.26$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.<sup>(1)</sup>

### 700 MHz

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
728 MHz	24.3	25.5	9.3	-44.0	-12
748 MHz	24.3	24.7	9.4	-43.9	-12
768 MHz	24.3	23.8	9.5	-43.6	-12

### 3500 MHz

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
3400 MHz	14.7	15.8	9.0	-44.9	-7
3500 MHz	16.0	16.8	9.0	-44.9	-8
3600 MHz	15.0	17.4	8.6	-44.2	-4

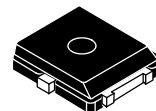
1. All data measured in fixture with device soldered to heatsink.

### Features

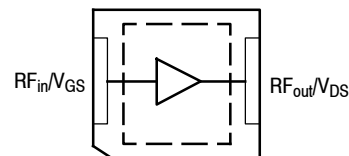
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Universal Broadband Driven Device with Internal RF Feedback

## AFT27S010NT1

728–3600 MHz, 1.26 W AVG., 28 V  
AIRFAST RF POWER LDMOS  
TRANSISTOR



PLD-1.5W  
PLASTIC



(Top View)

Note: The center pad on the backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature Range	$T_C$	-40 to +150	°C
Operating Junction Temperature Range (1,2)	$T_J$	-40 to +150	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 1.3 W CW, 28 Vdc, $I_{DQ} = 90$ mA, 2140 MHz	$R_{\theta JC}$	3.5	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 12.1$ $\mu\text{Adc}$ )	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_D = 90$ mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.5	1.8	2.3	Vdc
Drain-Source On-Voltage ( $V_{GS} = 6$ Vdc, $I_D = 121$ mAdc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rtf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rtf>. Select Documentation/Application Notes - AN1955.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ} = 90\text{ mA}$ , $P_{out} = 1.26\text{ W Avg.}$ , $f = 2170\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	$G_{ps}$	20.0	21.7	—	dB
Drain Efficiency	$\eta_D$	18.5	21.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-40.6	-37.9	dBc
Input Return Loss	IRL	—	-14	-9	dB

**Load Mismatch** (In Freescale Test Fixture, 50 ohm system)  $I_{DQ} = 90\text{ mA}$ ,  $f = 2140\text{ MHz}$ 

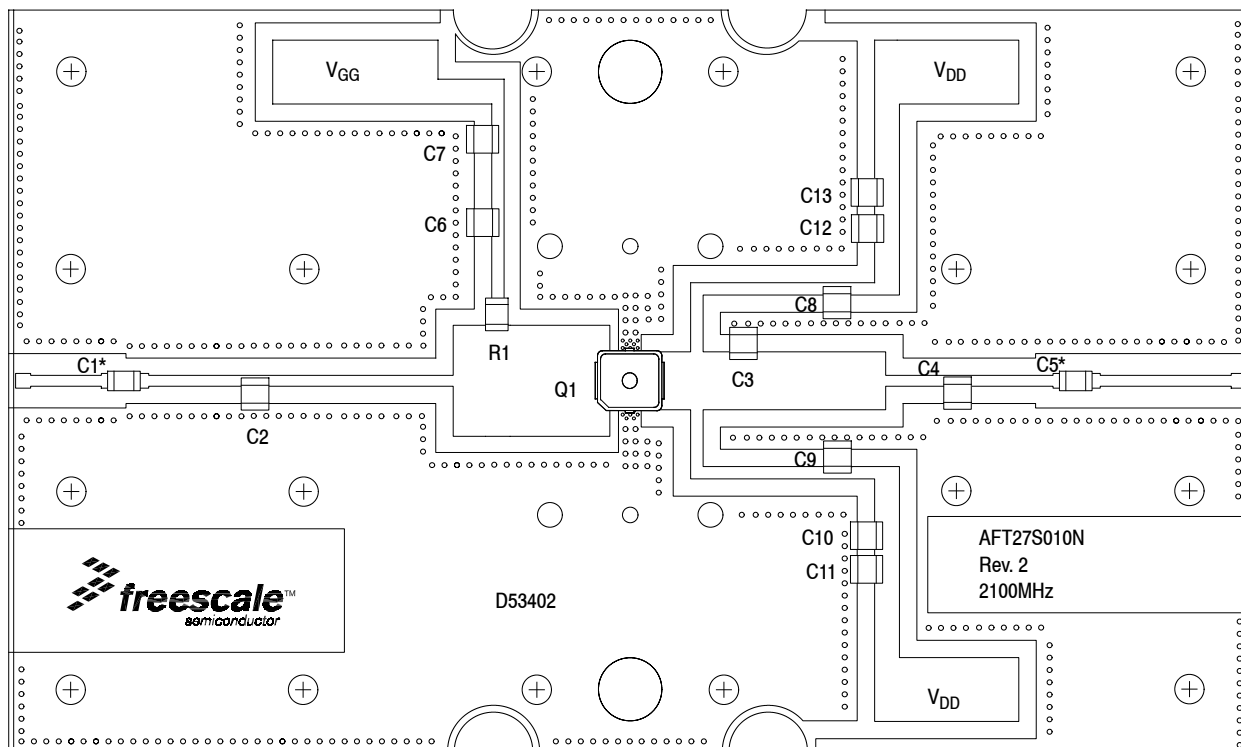
VSWR 5:1 at 32 Vdc, 13.9 W CW Output Power (3 dB Input Overdrive from 10 W CW Rated Power)	No Device Degradation
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**Typical Performance** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 90\text{ mA}$ , 2110–2170 MHz Bandwidth

$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	10	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz frequency range.)	$\Phi$	—	-12.6	—	°
VBW Resonance Point (IMD Seventh Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	120	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 1.26\text{ W Avg.}$	$G_F$	—	0.20	—	dB
Gain Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )	$\Delta G$	—	0.011	—	dB/°C
Output Power Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )	$\Delta P1dB$	—	0.004	—	dB/°C

**Table 6. Ordering Information**

Device	Tape and Reel Information	Package
AFT27S010NT1	T1 Suffix = 1000 Units, 16 mm Tape Width, 7-inch Reel	PLD-1.5W



\*C1 and C5 are mounted vertically.

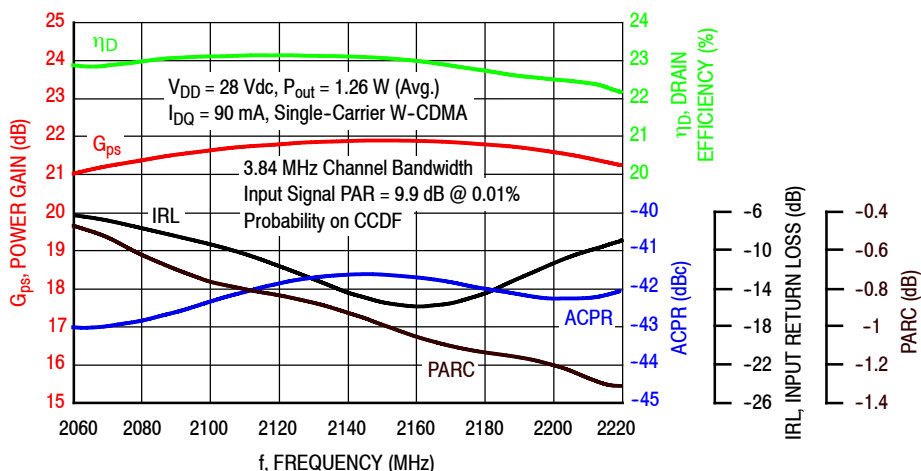
NOTE: All data measured in fixture with device soldered to heatsink.

**Figure 2. AFT27S010NT1 Test Circuit Component Layout — 2110-2170 MHz**

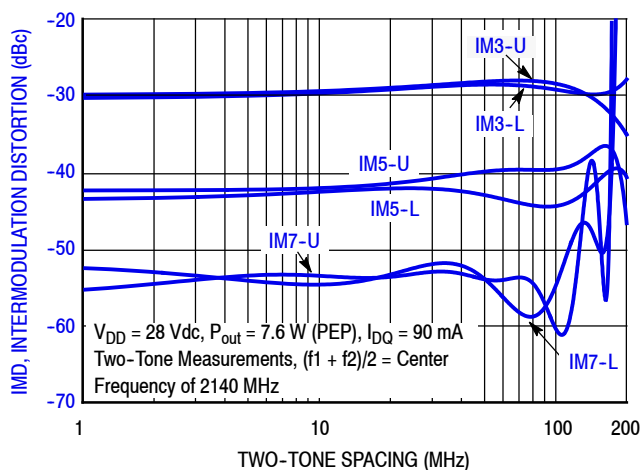
**Table 7. AFT27S010NT1 Test Circuit Component Designations and Values — 2110-2170 MHz**

Part	Description	Part Number	Manufacturer
C1, C5, C6, C8, C9	9.1 pF Chip Capacitors	ATC100B9R1JT500XT	ATC
C2	1.1 pF Chip Capacitor	ATC100B1R1JT500XT	ATC
C3	2.0 pF Chip Capacitor	ATC100B2R0JT500XT	ATC
C4	1.0 pF Chip Capacitor	ATC100B1R0JT500XT	ATC
C7, C10, C11, C12, C13	10 $\mu$ F Chip Capacitors	GRM32ER61H106KA12L	Murata
Q1	RF Power LDMOS Transistor	AFT27S010NT1	Freescale
R1	2.37 $\Omega$ Chip Resistor	CRCW12062R37FKEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D53402	MTL

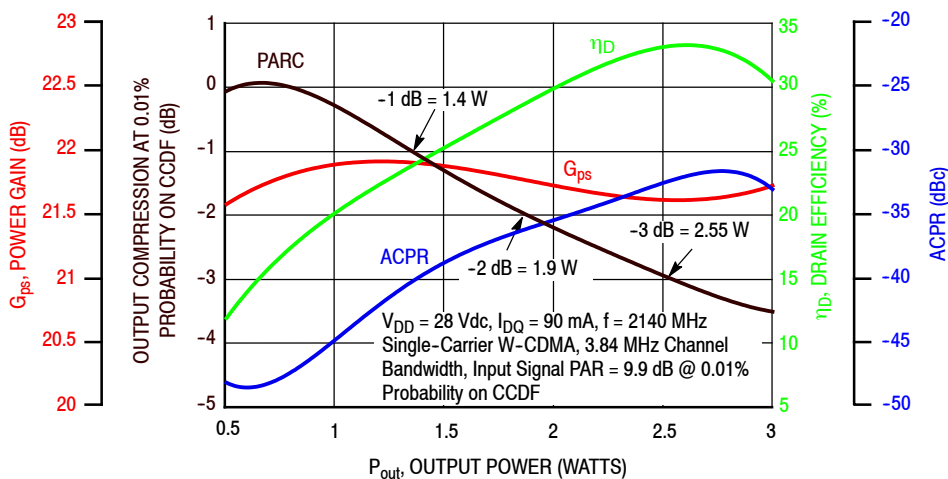
### TYPICAL CHARACTERISTICS — 2110-2170 MHz



**Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 1.26$  W Avg.**

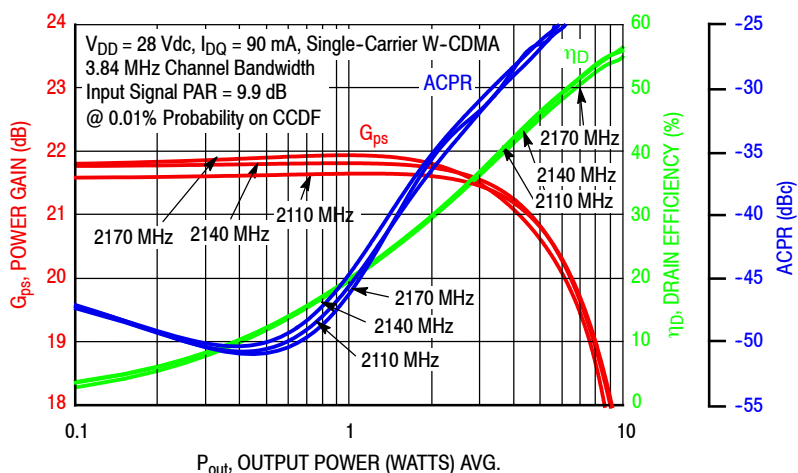


**Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing**

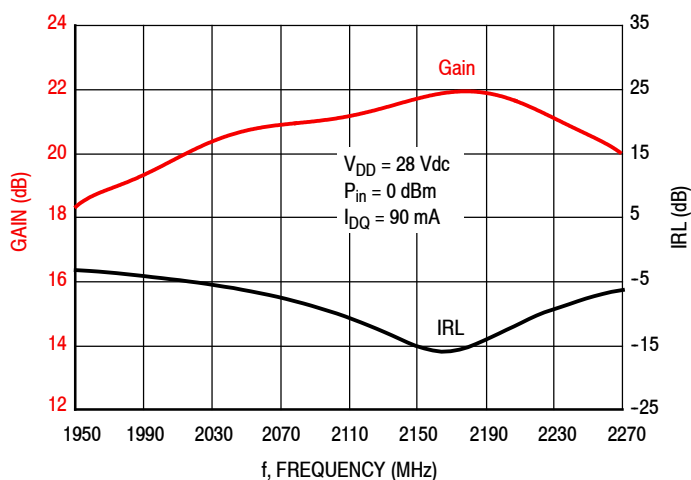


**Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

### TYPICAL CHARACTERISTICS — 2110-2170 MHz



**Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 7. Broadband Frequency Response**

**Table 8. Load Pull Performance — Maximum Power Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQ} = 87$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2110	1.23 - j0.107	0.698 + j0.572	5.85 + j3.49	21.0	41.2	13	60.2	-12
2140	1.08 - j0.422	0.877 + j0.537	5.79 + j3.28	20.8	41.2	13	59.5	-13
2170	1.12 - j0.0337	1.26 + j0.455	5.57 + j3.12	20.7	41.1	13	60.1	-11

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2110	1.23 - j0.107	0.592 + j0.741	6.75 + j2.96	18.7	42.0	16	59.6	-18
2140	1.08 - j0.422	0.807 + j0.78	6.62 + j2.72	18.5	42.0	16	58.6	-20
2170	1.12 - j0.0337	1.25 + j0.806	6.47 + j2.61	18.4	42.0	16	59.8	-17

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 9. Load Pull Performance — Maximum Drain Efficiency Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQ} = 87$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2110	1.23 - j0.107	0.609 + j0.446	3.56 + j6.04	22.7	39.7	9	67.5	-20
2140	1.08 - j0.422	0.736 + j0.434	3.63 + j5.62	22.4	39.9	10	66.6	-21
2170	1.12 - j0.0337	1.03 + j0.312	3.37 + j5.39	22.5	39.6	9	67.3	-19

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2110	1.23 - j0.107	0.512 + j0.627	3.80 + j5.81	20.5	40.5	11	67.3	-29
2140	1.08 - j0.422	0.671 + j0.667	3.77 + j5.41	20.3	40.6	11	65.9	-31
2170	1.12 - j0.0337	1.05 + j0.666	3.83 + j5.15	20.2	40.6	12	67.1	-27

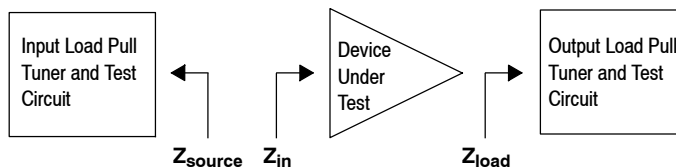
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.



### P1dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

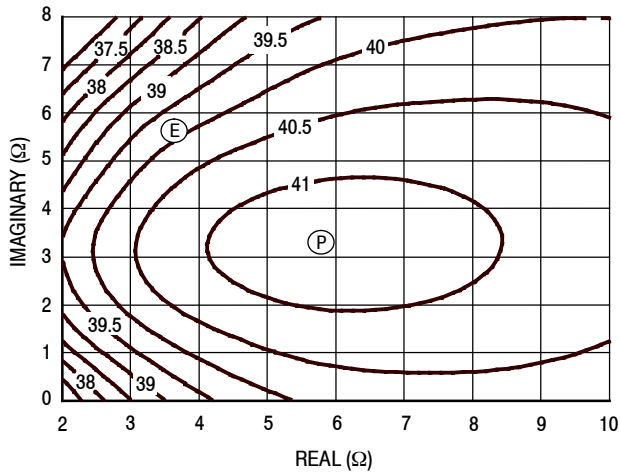


Figure 8. P1dB Load Pull Output Power Contours (dBm)

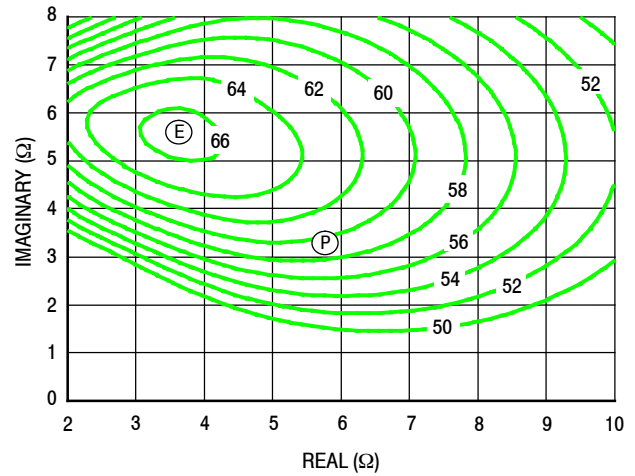


Figure 9. P1dB Load Pull Efficiency Contours (%)

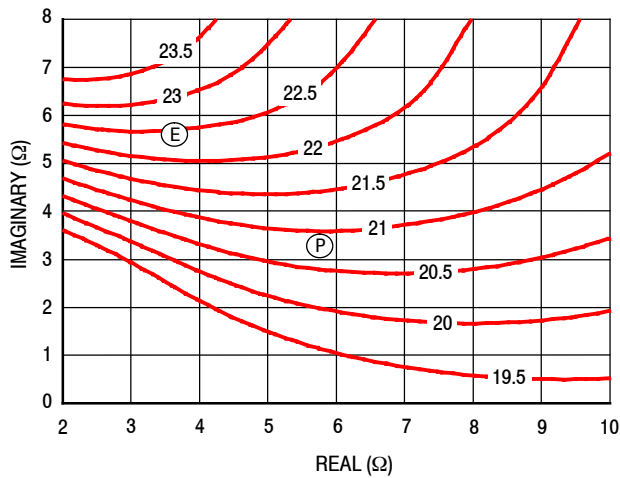


Figure 10. P1dB Load Pull Gain Contours (dB)

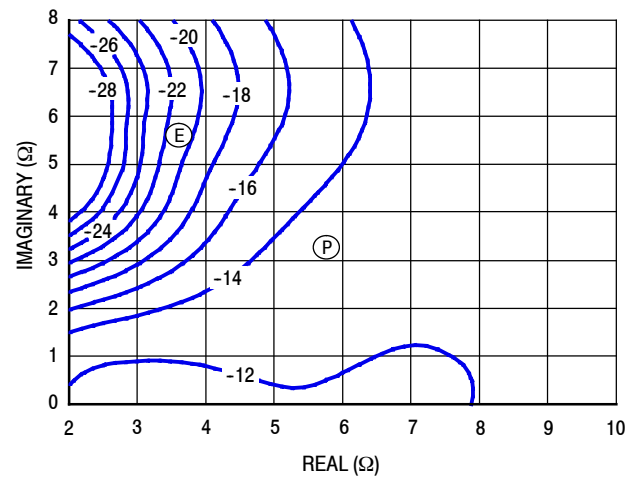


Figure 11. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power



### P3dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

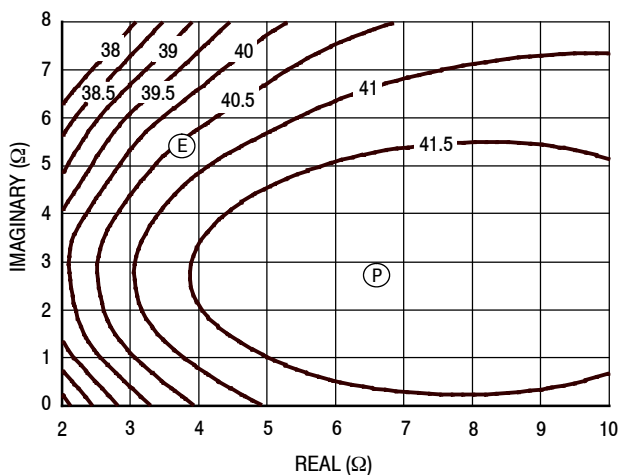


Figure 12. P3dB Load Pull Output Power Contours (dBm)

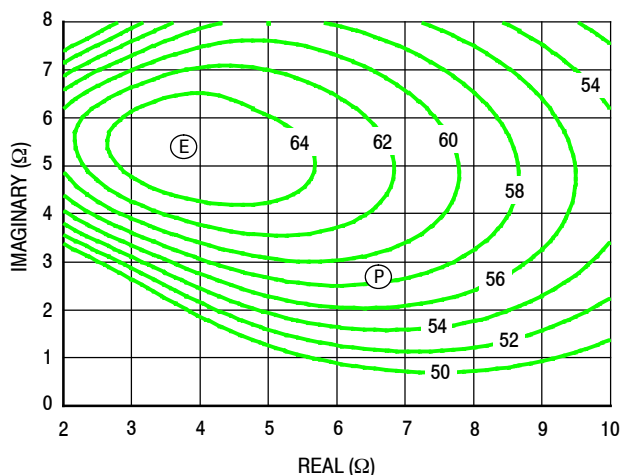


Figure 13. P3dB Load Pull Efficiency Contours (%)

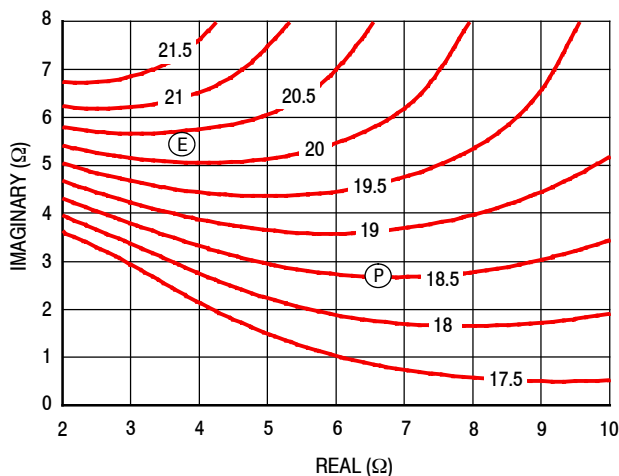


Figure 14. P3dB Load Pull Gain Contours (dB)

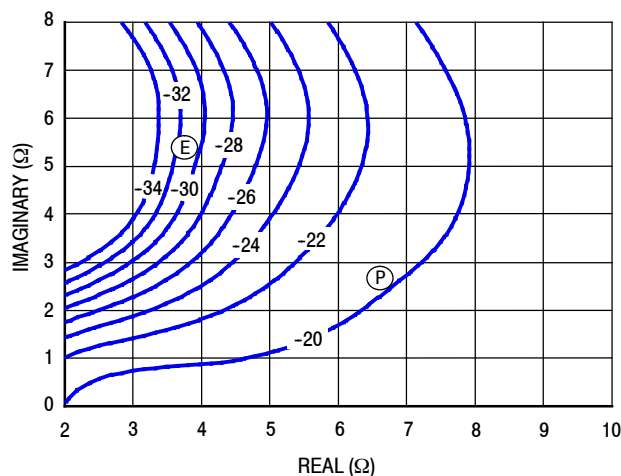
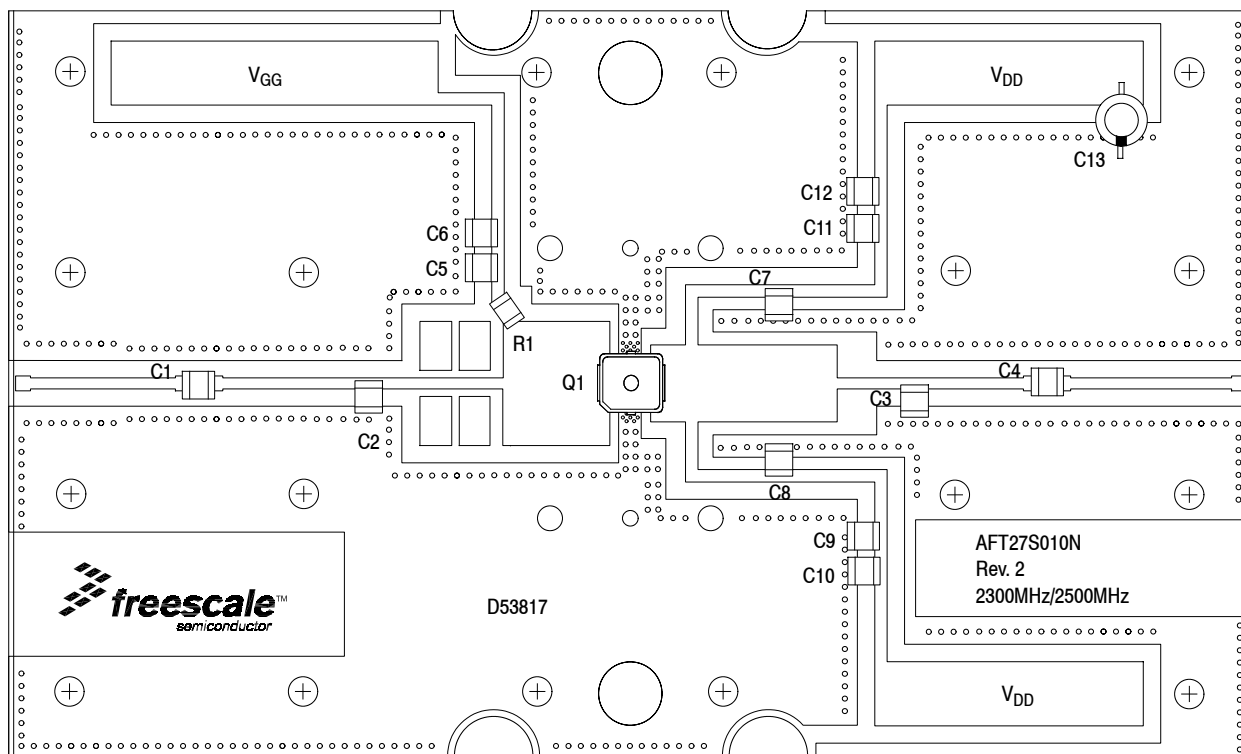


Figure 15. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

2500-2700 MHz



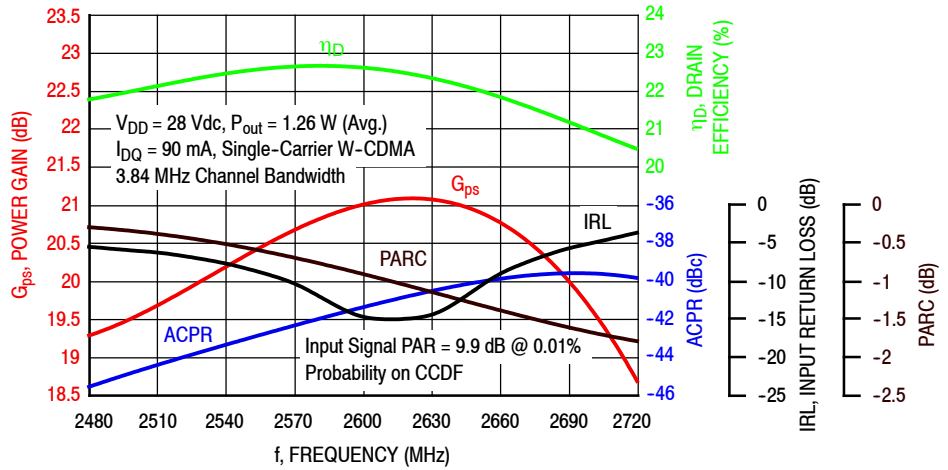
NOTE: All data measured in fixture with device soldered to heatsink.

Figure 16. AFT27S010NT1 Test Circuit Component Layout — 2500-2700 MHz

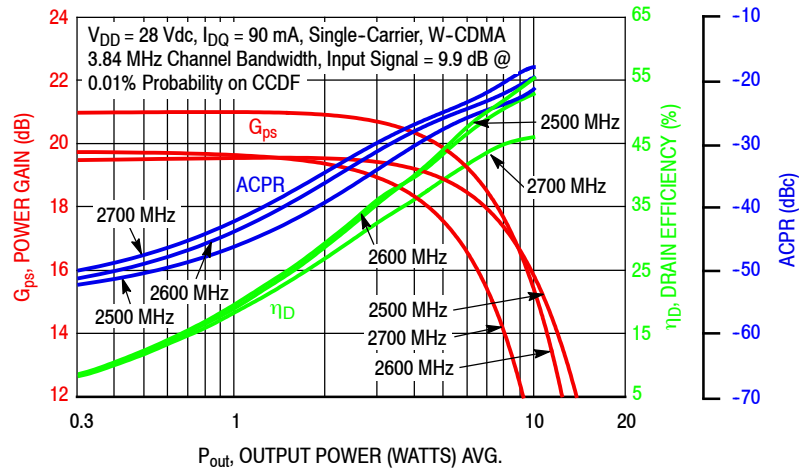
Table 10. AFT27S010NT1 Test Circuit Component Designations and Values — 2500-2700 MHz

Part	Description	Part Number	Manufacturer
C1, C4, C5, C7, C8	6.8 pF Chip Capacitors	ATC100B6R8JT500XT	ATC
C2	1.2 pF Chip Capacitor	ATC100B1R2JT500XT	ATC
C3	1 pF Chip Capacitor	ATC100B1R0JT500XT	ATC
C6, C9, C10, C11, C12	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
C13	220 μF, 50 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
Q1	RF Power LDMOS Transistor	AFT27S010NT1	Freescale
R1	4.75 Ω Chip Resistor	CRCW12064R75FKEA	Vishay
PCB	Rogers RO4350B, 0.020", ε <sub>r</sub> = 3.66	D53817	MTL

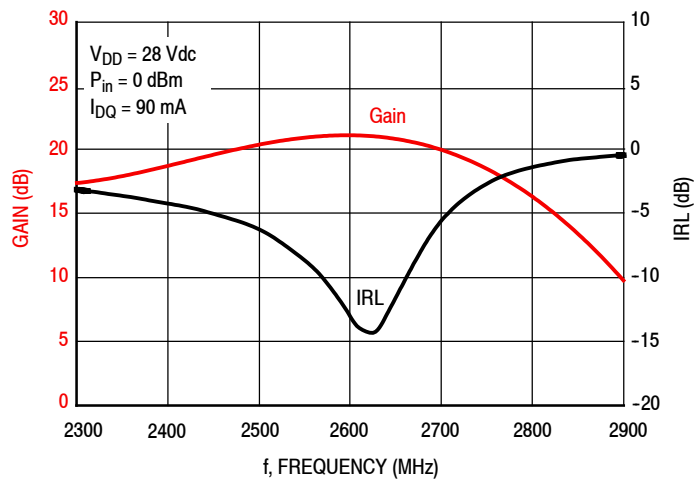
### TYPICAL CHARACTERISTICS — 2500-2700 MHz



**Figure 17. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 1.26$  W Avg.**

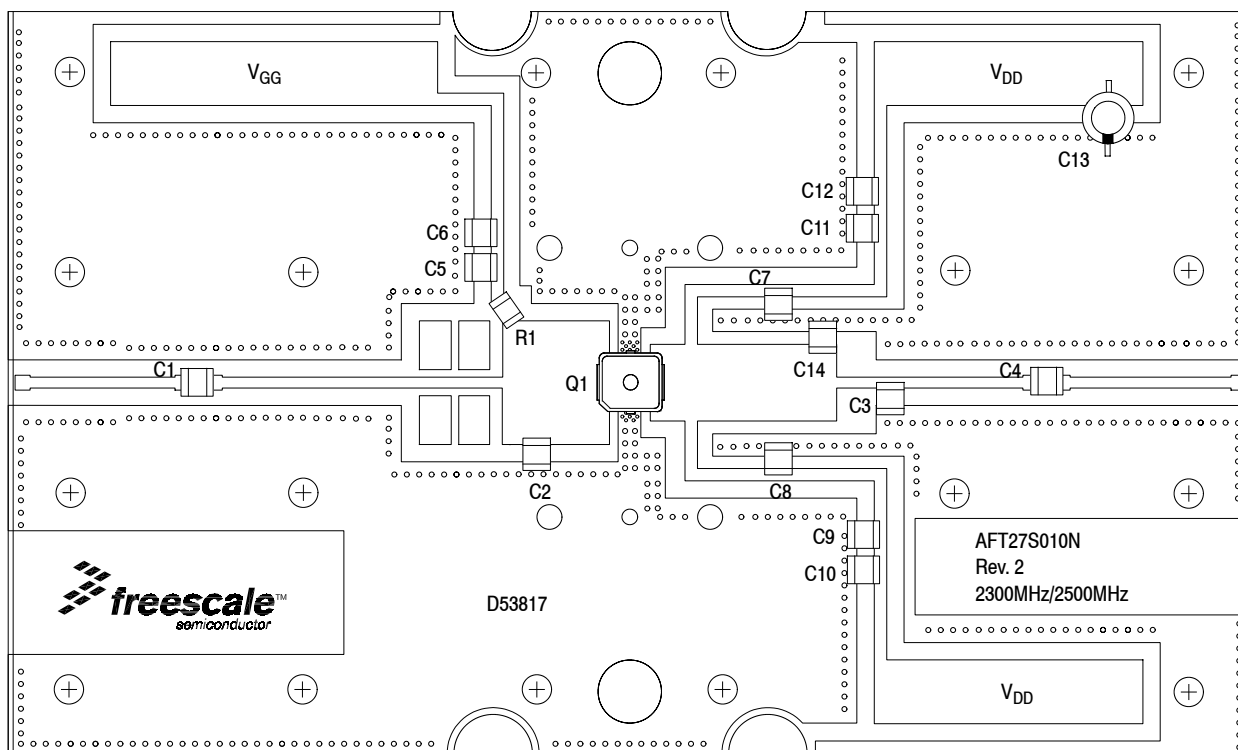


**Figure 18. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 19. Broadband Frequency Response**

2300-2400 MHz



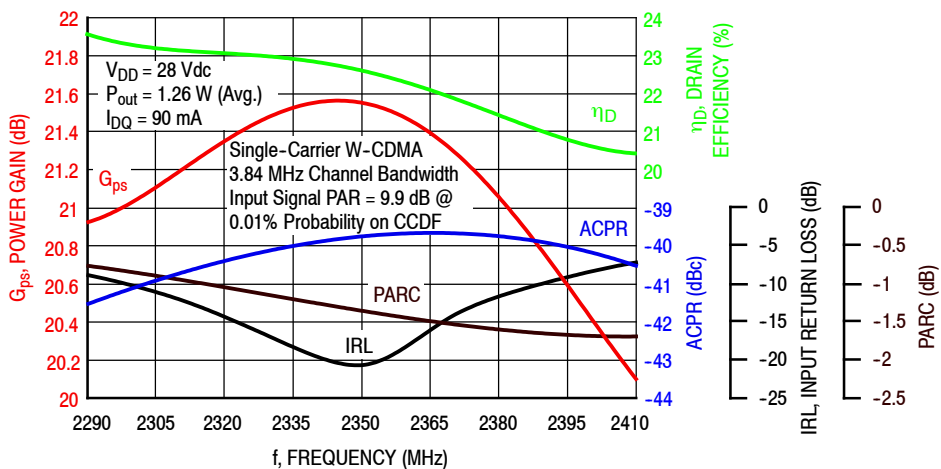
NOTE: All data measured in fixture with device soldered to heatsink.

Figure 20. AFT27S010NT1 Test Circuit Component Layout — 2300-2400 MHz

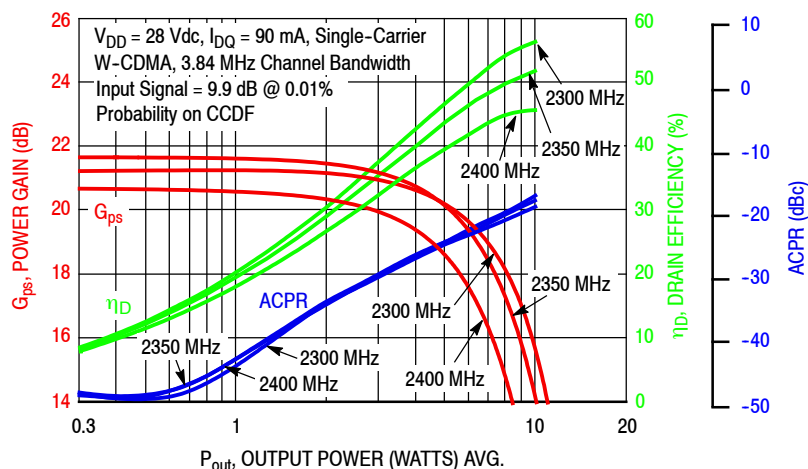
Table 11. AFT27S010NT1 Test Circuit Component Designations and Values — 2300-2400 MHz

Part	Description	Part Number	Manufacturer
C1, C4, C5, C7, C8	6.8 pF Chip Capacitors	ATC100B6R8JT500XT	ATC
C2, C14	1 pF Chip Capacitors	ATC100B1R0JT500XT	ATC
C3	1.2 pF Chip Capacitor	ATC100B1R2JT500XT	ATC
C6, C9, C10, C11, C12	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
C13	220 μF, 50 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
Q1	RF Power LDMOS Transistor	AFT27S010NT1	Freescale
R1	4.75 Ω, Chip Resistor	CRCW12064R75FKEA	Vishay
PCB	Rogers RO4350B, 0.020", ε <sub>r</sub> = 3.66	D53817	MTL

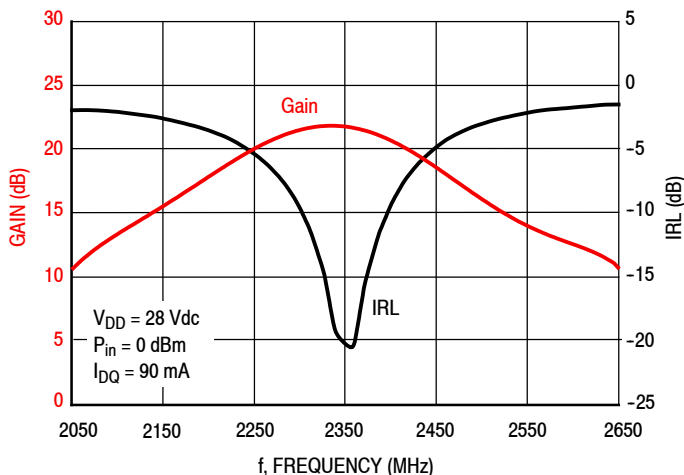
### TYPICAL CHARACTERISTICS — 2300-2400 MHz



**Figure 21. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 1.26$  W Avg.**



**Figure 22. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 23. Broadband Frequency Response**

**Table 12. Load Pull Performance — Maximum Power Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 87 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2300	1.12 - j1.10	0.995 + j1.38	5.39 + j2.23	20.1	40.9	12	55.9	-12
2400	1.06 - j1.59	0.948 + j1.96	5.09 + j1.86	19.8	40.9	12	55.1	-12
2500	1.00 - j1.60	1.29 + j1.95	4.51 + j1.56	19.2	40.8	12	55.8	-10
2600	0.985 - j3.50	0.743 + j3.66	4.81 + j1.10	19.0	41.3	13	56.2	-14
2690	1.10 - j3.13	1.48 + j2.98	4.14 + j0.987	19.0	41.0	13	57.5	-12

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2300	1.12 - j1.10	0.919 + j1.64	6.28 + j1.74	17.8	41.7	15	55.0	-19
2400	1.06 - j1.59	0.861 + j2.23	5.86 + j1.41	17.5	41.7	15	54.4	-19
2500	1.00 - j1.60	1.37 + j2.32	5.40 + j1.17	16.9	41.7	15	55.8	-17
2600	0.985 - j3.50	0.579 + j3.82	5.37 + j0.912	16.9	42.0	16	55.8	-22
2690	1.10 - j3.13	1.74 + j3.43	5.04 + j0.759	16.8	41.8	15	57.1	-18

(1) Load impedance for optimum P1dB power. (2) Load impedance for optimum P3dB power.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 13. Load Pull Performance — Maximum Drain Efficiency Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 87 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

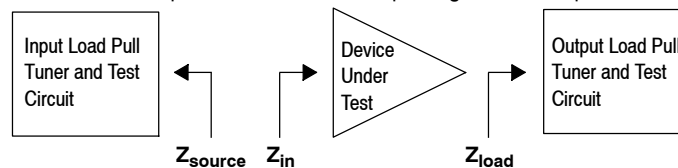
f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2300	1.12 - j1.10	0.855 + j1.22	3.36 + j4.23	21.6	39.8	9	61.9	-20
2400	1.06 - j1.59	0.829 + j1.80	3.34 + j3.53	21.2	39.9	10	60.4	-19
2500	1.00 - j1.60	1.04 + j1.82	3.21 + j3.00	20.8	40.0	10	61.1	-16
2600	0.985 - j3.50	0.709 + j3.49	3.17 + j2.53	20.0	40.5	11	60.7	-20
2690	1.10 - j3.13	1.14 + j2.91	2.87 + j2.16	20.4	40.2	10	62.0	-18

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2300	1.12 - j1.10	0.803 + j1.51	3.96 + j4.10	19.4	40.7	12	61.1	-27
2400	1.06 - j1.59	0.757 + j2.07	3.70 + j3.45	19.1	40.6	12	59.8	-27
2500	1.00 - j1.60	1.15 + j2.18	3.58 + j2.94	18.7	40.8	12	61.2	-24
2600	0.985 - j3.50	0.556 + j3.73	4.15 + j2.29	17.8	41.5	14	59.7	-26
2690	1.10 - j3.13	1.43 + j3.33	3.40 + j2.01	18.2	41.1	13	61.7	-25

(1) Load impedance for optimum P1dB efficiency. (2) Load impedance for optimum P3dB efficiency.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.


### P1dB - TYPICAL LOAD PULL CONTOURS — 2500 MHz

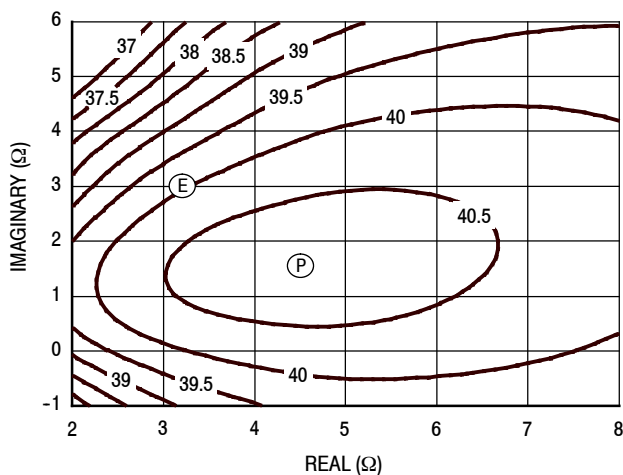


Figure 24. P1dB Load Pull Output Power Contours (dBm)

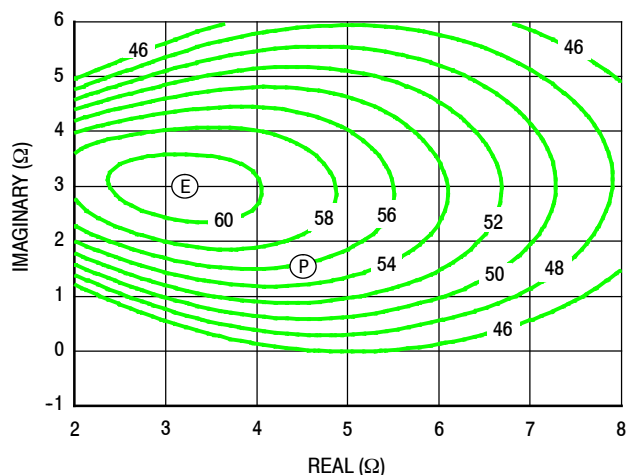


Figure 25. P1dB Load Pull Efficiency Contours (%)

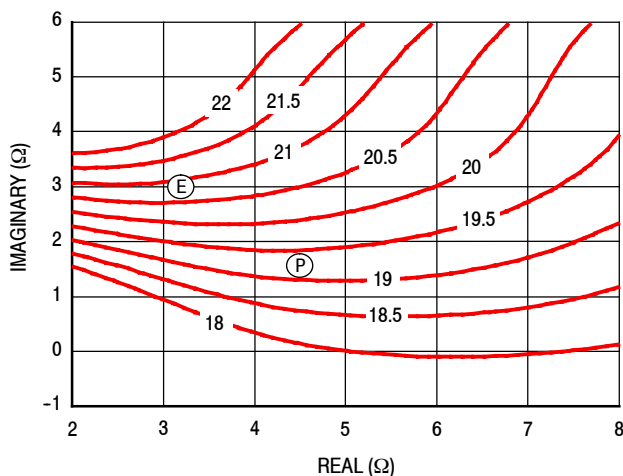


Figure 26. P1dB Load Pull Gain Contours (dB)

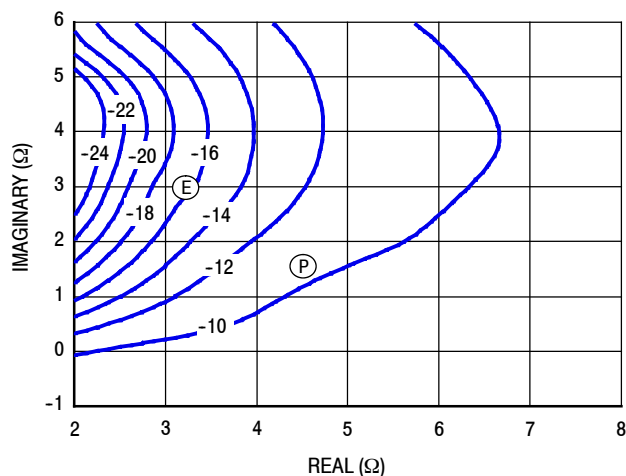


Figure 27. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB - TYPICAL LOAD PULL CONTOURS — 2500 MHz

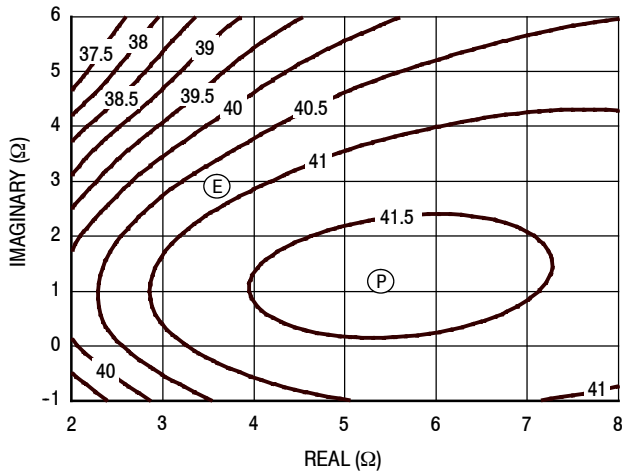


Figure 28. P3dB Load Pull Output Power Contours (dBm)

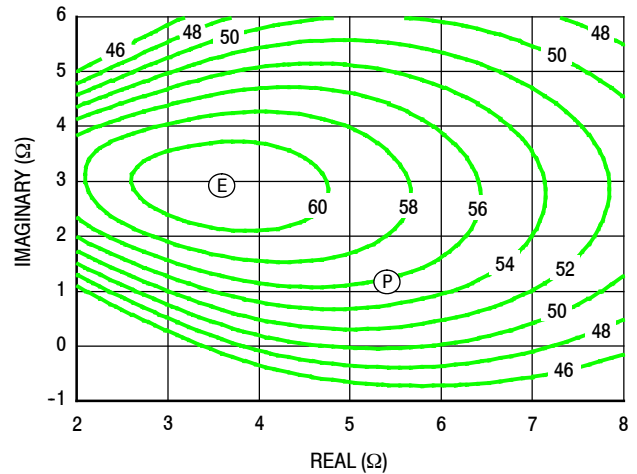


Figure 29. P3dB Load Pull Efficiency Contours (%)

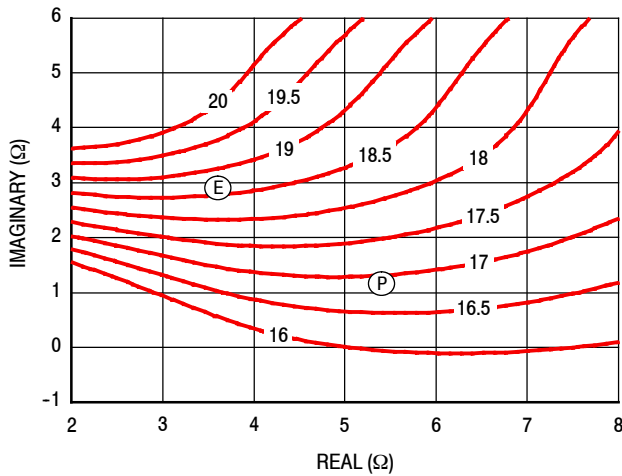


Figure 30. P3dB Load Pull Gain Contours (dB)

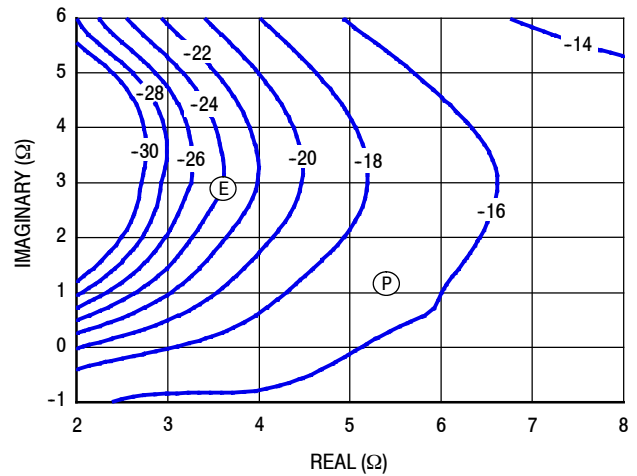


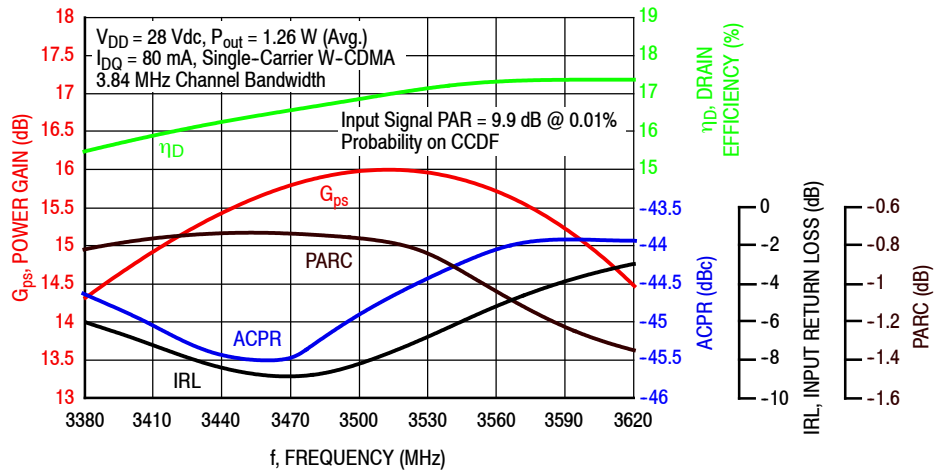
Figure 31. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

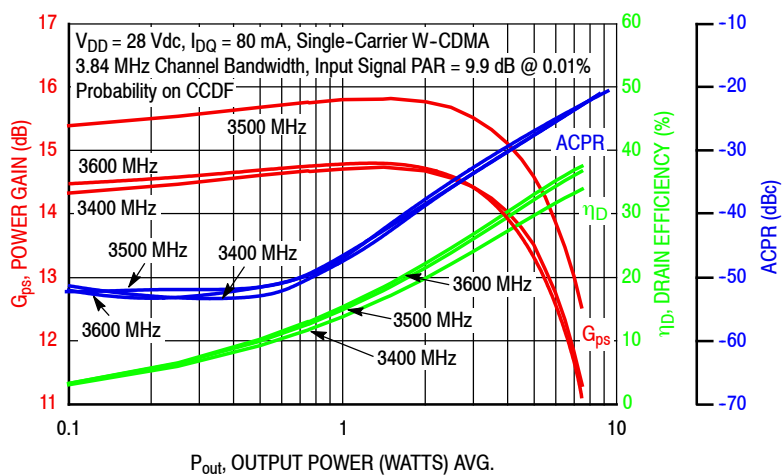
- Gain
- Drain Efficiency
- Linearity
- Output Power



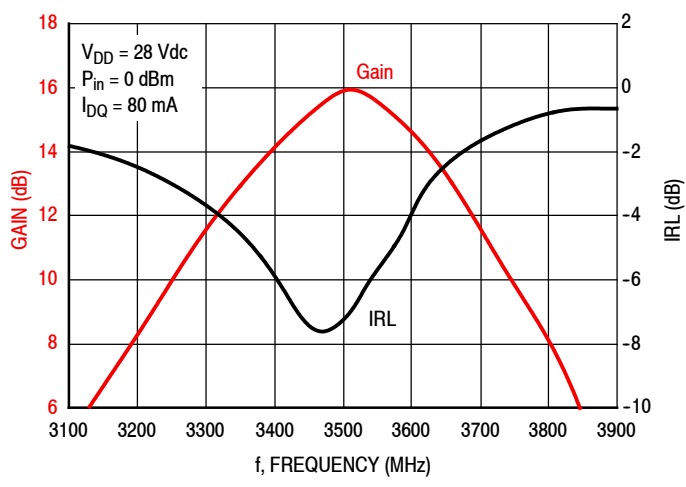
### TYPICAL CHARACTERISTICS — 3400-3600 MHz



**Figure 32. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 1.26 \text{ W Avg.}$**

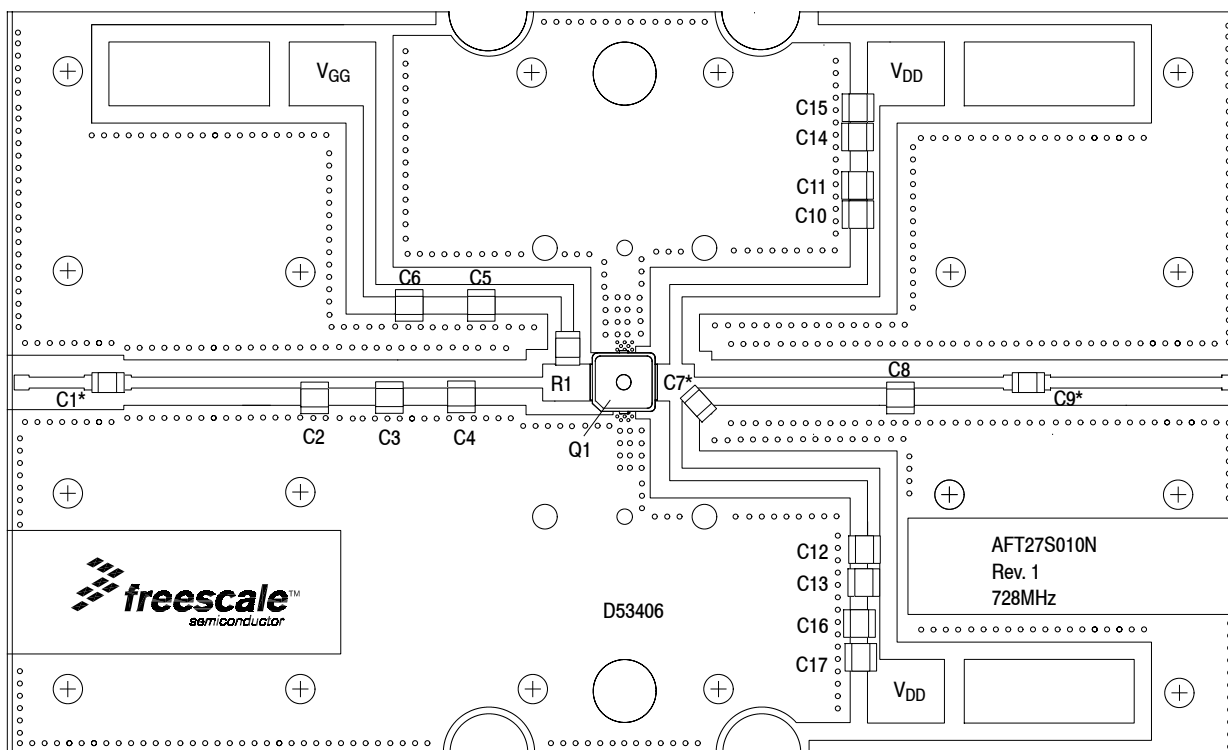


**Figure 33. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 34. Broadband Frequency Response**

728-768 MHz



\*C1, C7 and C9 are mounted vertically.

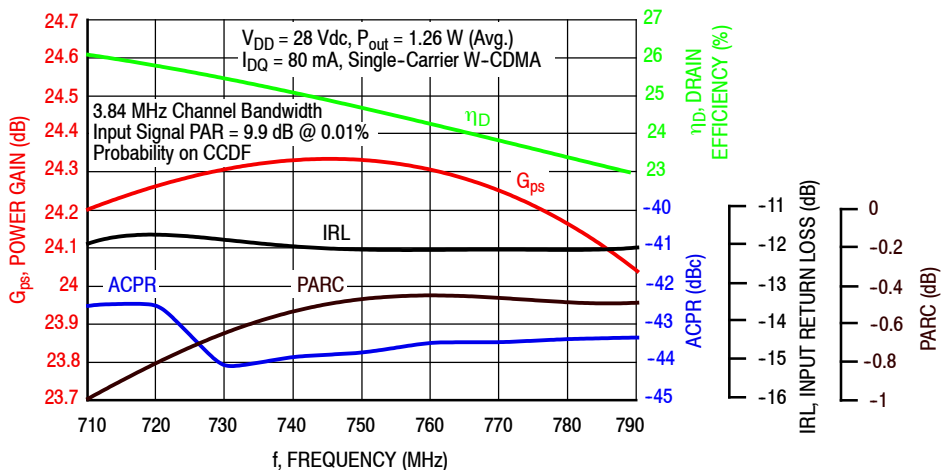
NOTE: All data measured in fixture with device soldered to heatsink.

Figure 35. AFT27S010NT1 Test Circuit Component Layout — 728-768 MHz

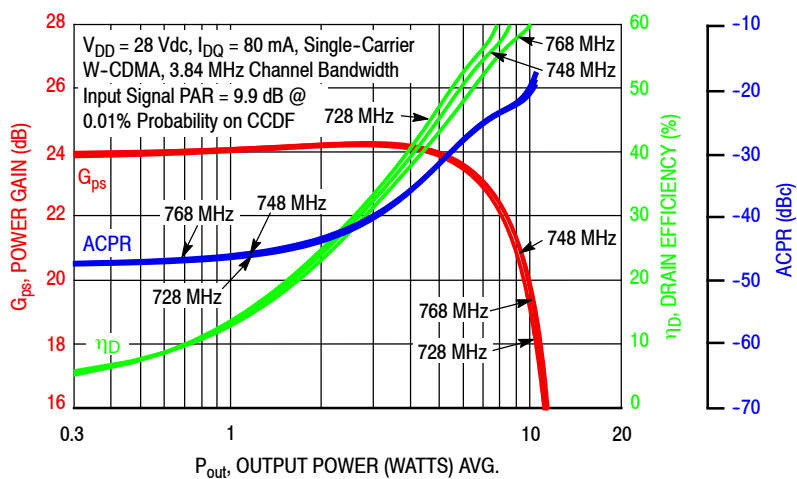
Table 14. AFT27S010NT1 Test Circuit Component Designations and Values — 728-768 MHz

Part	Description	Part Number	Manufacturer
C1, C9	82 pF Chip Capacitors	ATC100B820JT500XT	ATC
C2	3.9 pF Chip Capacitor	ATC100B3R9JT500XT	ATC
C3	1.7 pF Chip Capacitor	ATC100B1R7JT500XT	ATC
C4	2.7 pF Chip Capacitor	ATC100B2R7JT500XT	ATC
C5, C10, C11, C12, C13	33 pF Chip Capacitors	ATC100B330JT500XT	ATC
C6, C14, C15, C16, C17	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
C7	3.9 pF Chip Capacitor	ATC100B3R9JT500XT	ATC
C8	0.5 pF Chip Capacitor	ATC100B0R5JT500XT	ATC
Q1	RF Power LDMOS Transistor	AFT27S010NT1	Freescale
R1	10 Ω Chip Resistor	CWCR120610R0JNEA	Vishay
PCB	Rogers RO4350B, 0.020", ε <sub>r</sub> = 3.66	D53406	MTL

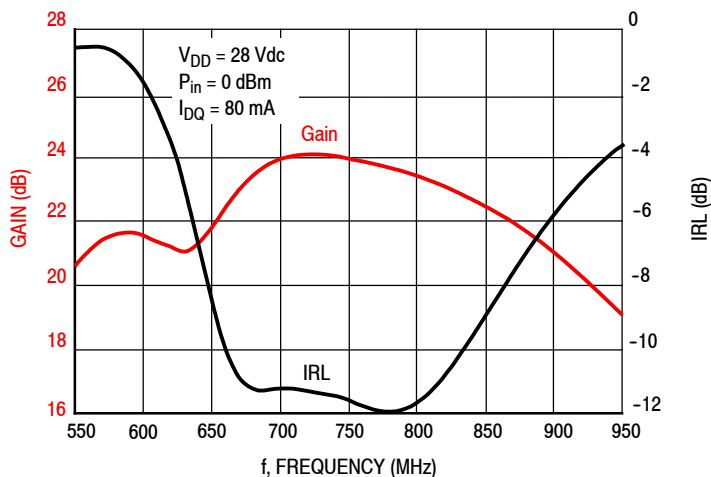
### TYPICAL CHARACTERISTICS — 728-768 MHz



**Figure 36. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 1.26 \text{ W Avg.}$**



**Figure 37. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 38. Broadband Frequency Response**

**Table 15. Load Pull Performance — Maximum Power Tuning**
 $V_{DD} = 28$  Vdc,  $I_{DQ} = 81$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
728	$2.05 + j12.1$	$1.72 - j11.7$	$15.1 + j6.07$	27.2	41.3	14	59.8	-15
748	$2.04 + j11.1$	$1.69 - j11.2$	$14.6 + j5.90$	27.0	41.5	14	60.2	-15
768	$1.94 + j10.5$	$1.69 - j10.8$	$14.6 + j5.49$	26.7	41.5	14	60.1	-14

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
728	$2.05 + j12.1$	$1.53 - j11.7$	$16.1 + j4.43$	24.7	42.3	17	61.9	-17
748	$2.04 + j11.1$	$1.50 - j11.3$	$15.1 + j4.52$	24.6	42.4	17	61.7	-17
768	$1.94 + j10.5$	$1.46 - j10.9$	$14.8 + j4.54$	24.5	42.4	17	61.7	-16

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 $Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{in}$  = Impedance as measured from gate contact to ground.

 $Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 16. Load Pull Performance — Maximum Drain Efficiency Tuning**
 $V_{DD} = 28$  Vdc,  $I_{DQ} = 81$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
728	$2.05 + j12.1$	$1.97 - j10.7$	$18.5 + j16.4$	27.9	39.7	9	68.4	-13
748	$2.04 + j11.1$	$1.81 - j9.83$	$16.7 + j20.1$	28.6	38.9	8	68.5	-14
768	$1.94 + j10.5$	$1.83 - j9.69$	$17.4 + j18.0$	28.3	39.5	9	69.2	-14

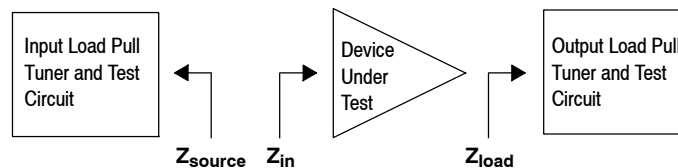
f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
728	$2.05 + j12.1$	$1.69 - j10.8$	$18.3 + j18.6$	26.1	40.3	11	73.7	-14
748	$2.04 + j11.1$	$1.58 - j10.4$	$17.5 + j17.5$	26.4	40.5	11	77.4	-14
768	$1.94 + j10.5$	$1.51 - j9.87$	$15.8 + j19.1$	26.8	40.0	10	72.8	-15

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 $Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{in}$  = Impedance as measured from gate contact to ground.

 $Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.


### P1dB - TYPICAL LOAD PULL CONTOURS — 748 MHz

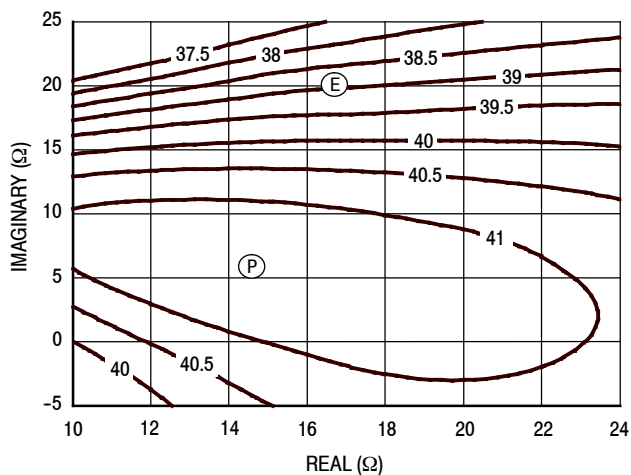


Figure 39. P1dB Load Pull Output Power Contours (dBm)

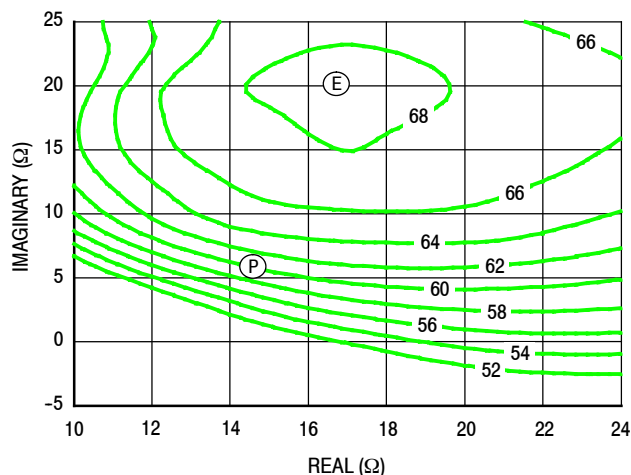


Figure 40. P1dB Load Pull Efficiency Contours (%)

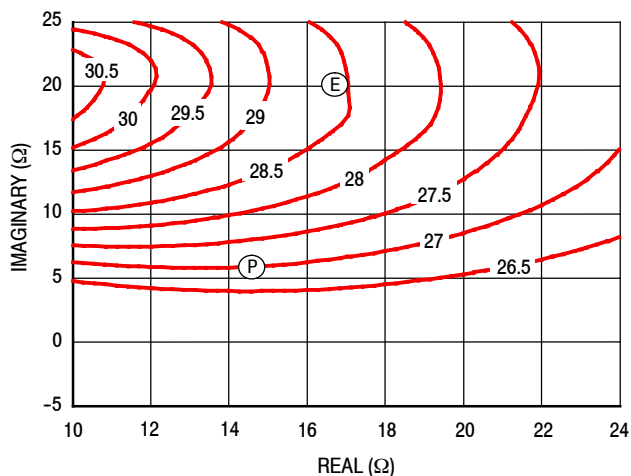


Figure 41. P1dB Load Pull Gain Contours (dB)

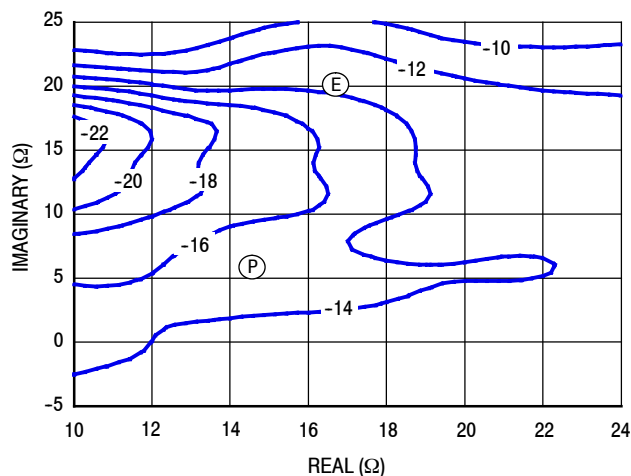


Figure 42. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB - TYPICAL LOAD PULL CONTOURS — 748 MHz

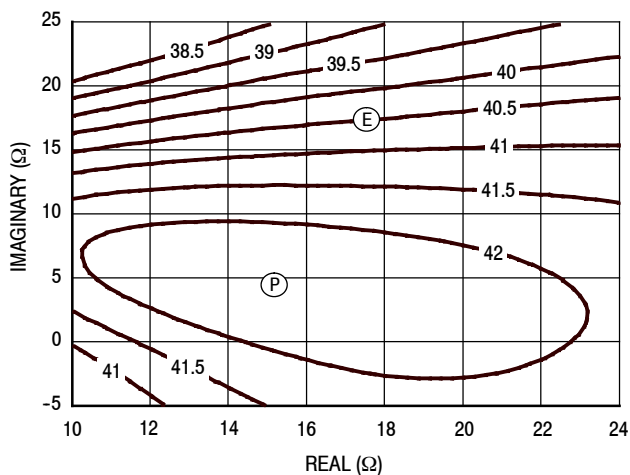


Figure 43. P3dB Load Pull Output Power Contours (dBm)

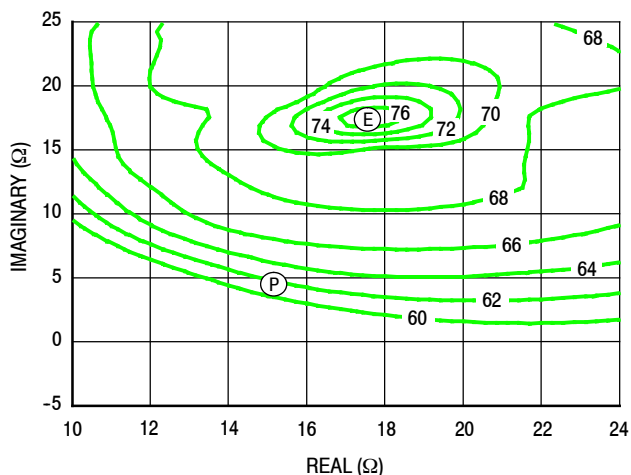


Figure 44. P3dB Load Pull Efficiency Contours (%)

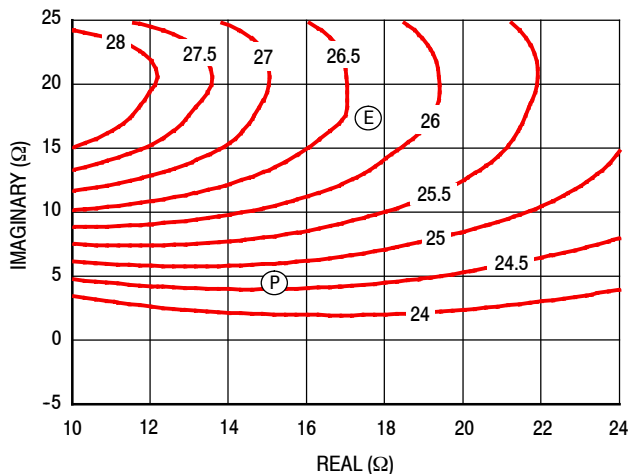


Figure 45. P3dB Load Pull Gain Contours (dB)

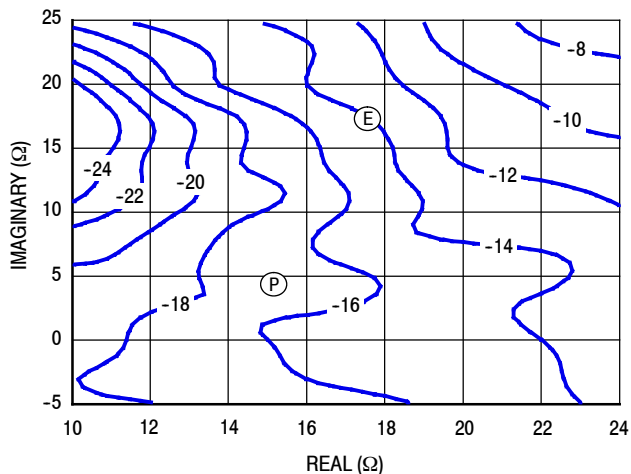


Figure 46. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

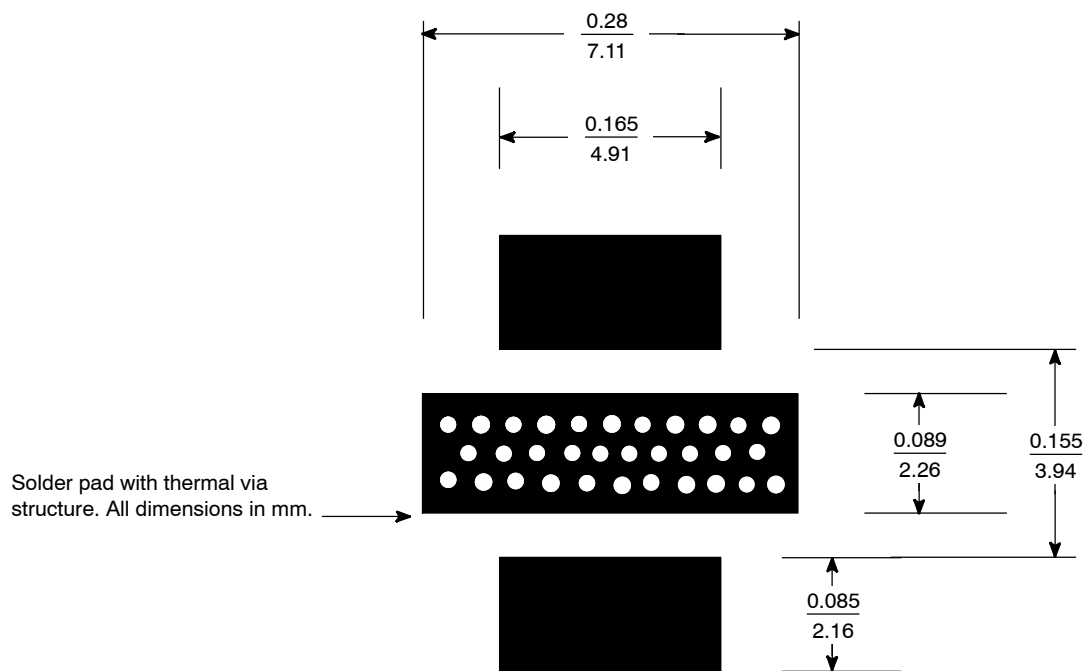
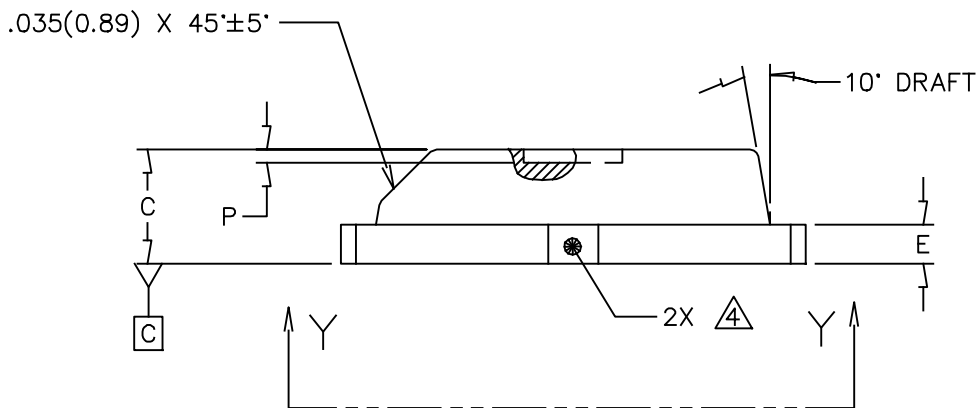
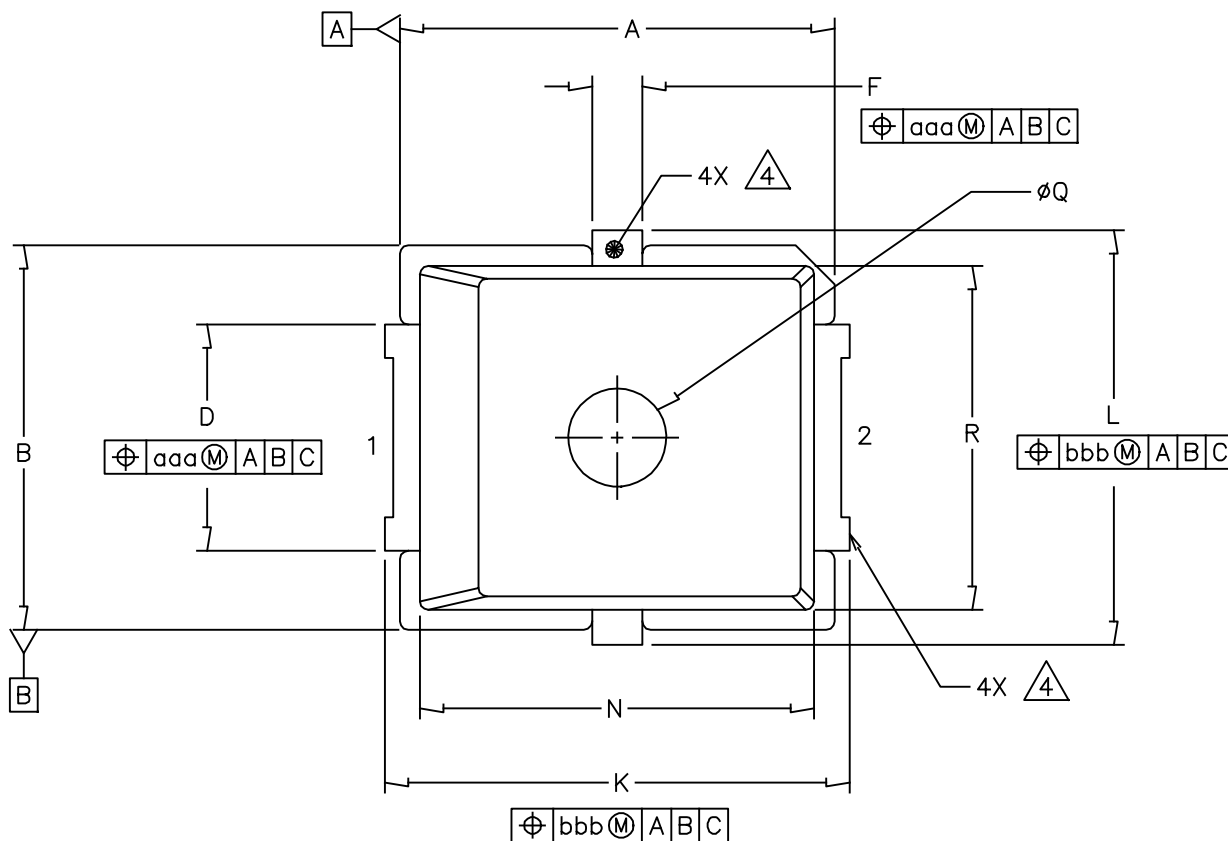


Figure 47. PCB Pad Layout for PLD-1.5W



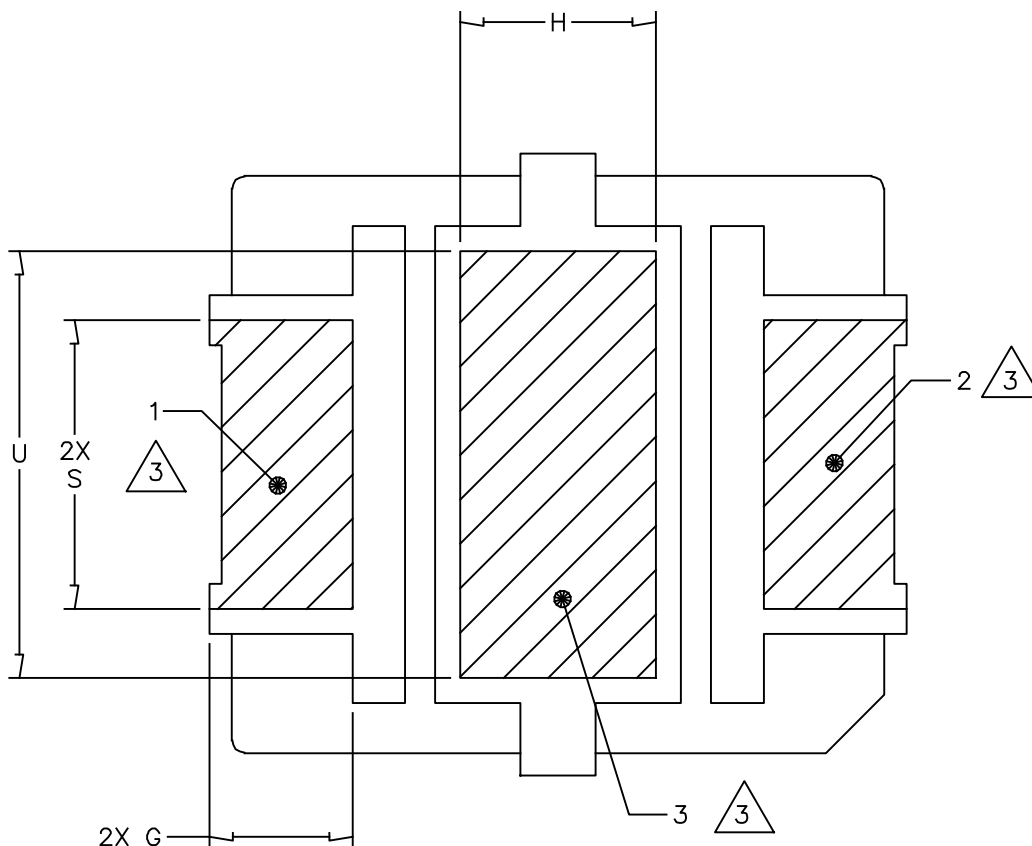
Figure 48. Product Marking

### PACKAGE DIMENSIONS



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		CASE NUMBER: 2297-01		14 JUN 2012	
		STANDARD: NON-JEDEC			





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	CASE NUMBER: 2297-01	14 JUN 2012	
	STANDARD: NON-JEDEC		

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3. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA. DIMENSIONS G, S, H AND U REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA.

4. THESE SURFACES ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.255	.265	6.48	6.73	Q	.055	.063	1.40	1.60
B	.225	.235	5.72	5.97	R	.200	.210	5.08	5.33
C	.065	.072	1.65	1.83	S	.110	—	2.79	—
D	.130	.150	3.30	3.81	U	.156	—	3.96	—
E	.021	.026	0.53	0.66	aaa	.004		0.10	
F	.026	.044	0.66	1.12	bbb	.005		0.13	
G	.038	—	0.97	—					
H	.069	—	1.75	—					
J	.160	.180	4.06	4.57					
K	.273	.285	6.93	7.24					
L	.245	.255	6.22	6.48					
N	.230	.240	5.84	6.10					
P	.000	.008	0.00	0.20					
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TITLE:  PLD-1.5W					DOCUMENT NO: 98ASA00476D			REV: 0	
					CASE NUMBER: 2297-01			14 JUN 2012	
					STANDARD: NON-JEDEC				

Refer to the following resources to aid your design process.

**Application Notes**

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

**Software**

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

**Development Tools**

- Printed Circuit Boards

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

**REVISION HISTORY**

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2013	<ul style="list-style-type: none"> <li>• Initial Release of Data Sheet</li> </ul>
1	Sept. 2014	<ul style="list-style-type: none"> <li>• Tape and Reel information: corrected tape width information from 13-inch reel to 7-inch reel to reflect actual reel size, p. 1</li> <li>• Changed operating frequency from 728–2700 MHz to 728–3600 MHz due to expanded device frequency capability resulting from additional test data, p. 1</li> </ul>
2	Nov. 2014	<ul style="list-style-type: none"> <li>• Added 3400–3600 MHz performance information as follows:               <ul style="list-style-type: none"> <li>- Typical Frequency Band table, p. 1</li> <li>- Fig. 32, Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ <math>P_{out} = 1.26\text{ W Avg.}</math>, p. 17</li> <li>- Fig. 33, Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power, p. 17</li> <li>- Fig. 34, Broadband Frequency Response, p. 17</li> </ul> </li> </ul>
3	Dec. 2015	<ul style="list-style-type: none"> <li>• Table 1, Maximum Ratings: corrected operating junction temperature range upper limit, p. 2</li> <li>• Table 5, Electrical Characteristics, On Characteristics <math>V_{DS(on)}</math>: updated <math>I_D</math> unit of measure to mA<sub>dc</sub> to reflect actual unit of measure, p. 2</li> <li>• Added Ordering Information Table 6, p. 3</li> </ul>

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