DESCRIPTION

Demonstration circuit 906A features the LTC®4306IUFD, a 4-channel, 2-wire I2C bus and SMBus compatible multiplexer having bus buffers that provide capacitive isolation between the upstream bus and downstream buses. Through software control, the LTC4306IUFD connects the upstream 2-wire bus to any desired combination of downstream buses. Each bus can be pulled up to a supply voltage ranging from 2.2V to 5.5V, independent of the LTC4306IUFD supply voltage. The downstream buses are also provided with ALERT1B – ALERT4B inputs for fault reporting.

Programmable timeout circuitry disconnects the downstream buses if the bus is stuck low. When activated, rise time accelerators source currents into the 2-wire bus pins during rising edges to reduce rise time. Two general purpose input/output (GPIO) pins can be configured as inputs, open-drain outputs or push-pull outputs. Green LED's D3 and D2 light up when GPIO1 and GPIO2, respectively, are low. Driving the ENABLE pin low restores all device features to their default states. Three address pins provide 27 distinct addresses.

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
V_{CC} Voltage Operating Range		2.7V – 5.5V
Bus Pull-up Supply Voltage Range (V_{BUS1}-V_{BUS4})		2.2V – 5.5V
2-Wire Bus Frequency Range		0 - 400kHz
Bus Stuck Low Disconnect Times	V_{CC} = 2.7V - 5.5V	7.5ms, 15ms, 30ms options all times +/-16.7% feature can also be disabled
Bus Buffer V_{OL} Offset Voltage	R_{BUS} = 10K	100mV (maximum)
Rise Time Accelerator Pull-up Current	V_{CC} = 3.3V	5.5mA (typical)
	V_{CC} = 5V	9mA (typical)
ALERTB and READY Output V_{OL} Voltages	V_{CC} = 2.7V - 5.5V; I_{ALERTB} = I_{READY} = 3mA	0.4V (maximum)

OPERATING PRINCIPLES

For operation with the DC906A, connect the host controller's SDA and SCL pins to the LTC4306IUFD's SDAIN and SCLIN pins (hereafter referred to as the upstream bus), and connect the upstream bus supply of 2.7V to 5.5V to Vcc (as shown in Figure 1). The host controller on the upstream side first addresses and configures the LTC4306IUFD to connect the upstream bus to one or more of the four downstream buses. Communications between the upstream and downstream components are then established and a host controller on any bus can then control the LTC4306IUFD.

Use turrets VBUS1-VBUS4 and jumpers JP1-JP4 to pull up the downstream buses to supply voltages different than VCC (i.e., to provide level-shifting). For

example, in Figure1, JP1 is set to the right position and a supply voltage is connected between VBUS1 and ground. Voltages on VBUS1-VBUS4 must range between 2.2V and 5.5V. To connect a downstream bus's pull-up supply to VCC, set its jumper to the left position.

Additional configurations include enabling and disabling the rise time accelerators on the backplane side and/or the card side, setting the GPIO's to open-drain output, push-pull output, or input mode, setting or resetting the GPIO's outputs, disabling the Bus Stuck Low disconnect feature or setting the disconnect time to 7.5ms, 15ms, 30ms. A host controller can also read the internal registers of the LTC4306IUFD to determine the settings of these features as well as fault statuses. All of these features are accessed by sending commands on the 2-wire bus.

The ENABLE pin, when pulled low, resets the LTC4306IUFD to its registers default state and disables communication to it. Communication can be reestablished when ENABLE is released high. Therefore, set jumper JP5 to the left position for normal operation, and set it to the right position to disable the LTC4306IUFD.

Slave devices that are capable of fault reporting and that are located on downstream buses 1-4 should connect their fault pins to ALERT1B-ALERT4B, respectively. The LTC4306IUFD passes downstream faults to the upstream host by pulling down on the ALERTB pin, so this host's fault input should be connected to the LTC4306IUFD ALERTB pin.

When the upstream bus is connected to one or more downstream buses, the READY pin voltage is pulled up to V_{CC}. When the upstream bus is disconnected from all downstream buses, the READY voltage is low (~0.2V).

On the DC906A, the board's default setting for jumpers JP6, JP7 and JP8 is the center position, which sets the address of the LTC4306IUFD to $(1001\ 010)_2$. To set a different address, configure the jumpers according to Table 1 of the data sheet (note: left position = H, middle position = NC, right position = L; default = NC for all three jumpers).

QUICK START PROCEDURE

Demonstration circuit 906A is easy to set up to evaluate the performance of the LTC4306IUFD. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

KEY NOTES: a. Do not activate rise time accelerators on buses whose pull-up supply voltages are lower than VCC. b. Make sure logic low voltages forced on all clock and data pins are < 0.4V. c. When activating multiple downstream buses that are powered from separate supply voltages, make sure that the LTC4306IUFD's VCC voltage is less than or equal to the lowest downstream bus pull-up supply voltage.

1. Jumpers JP1-JP4 choose the pull-up supply voltages VBUS1 – VBUS4 for downstream buses 1-4. For unused buses and buses pulled up to VCC, set the jumpers in the left position. To pull up a downstream bus to a different voltage than VCC, set its jumper to the right position, and connect the supply voltage to the appropriate turret on the left side of the board.
2. Set jumper J5 in the left position to enable communication to the LTC4306IUFD.
3. Configure jumpers JP6 – JP8 to set the desired 2-wire bus address for the LTC4306IUFD according to Table 1 on page 13 of the datasheet (note: left position = H, middle position = NC, right position = L; default = NC for all three jumpers).
4. Connect a cable from 6-pin header J2 to a board containing the master device(s).
5. Connect a 20-pin ribbon cable from J1 to a board that contains downstream slave devices. Note: the downstream buses can contain masters, but the original command to connect must come from a

master connected to the upstream SDAIN/SCLIN bus.

6. Connect power supplies to VCC and, if required, one or more of VBUS1 – VBUS4.

7. Turn on the power supplies.

   NOTE: Make sure that the power supply voltages do not exceed 5.5V.

8. Use the SMBus Read Byte and Write Byte protocols in conjunction with the register definitions on pages 8 and 9 of the datasheet to experiment with the LTC4306IUFD's features and to establish upstream-downstream communications between the master and slave devices.

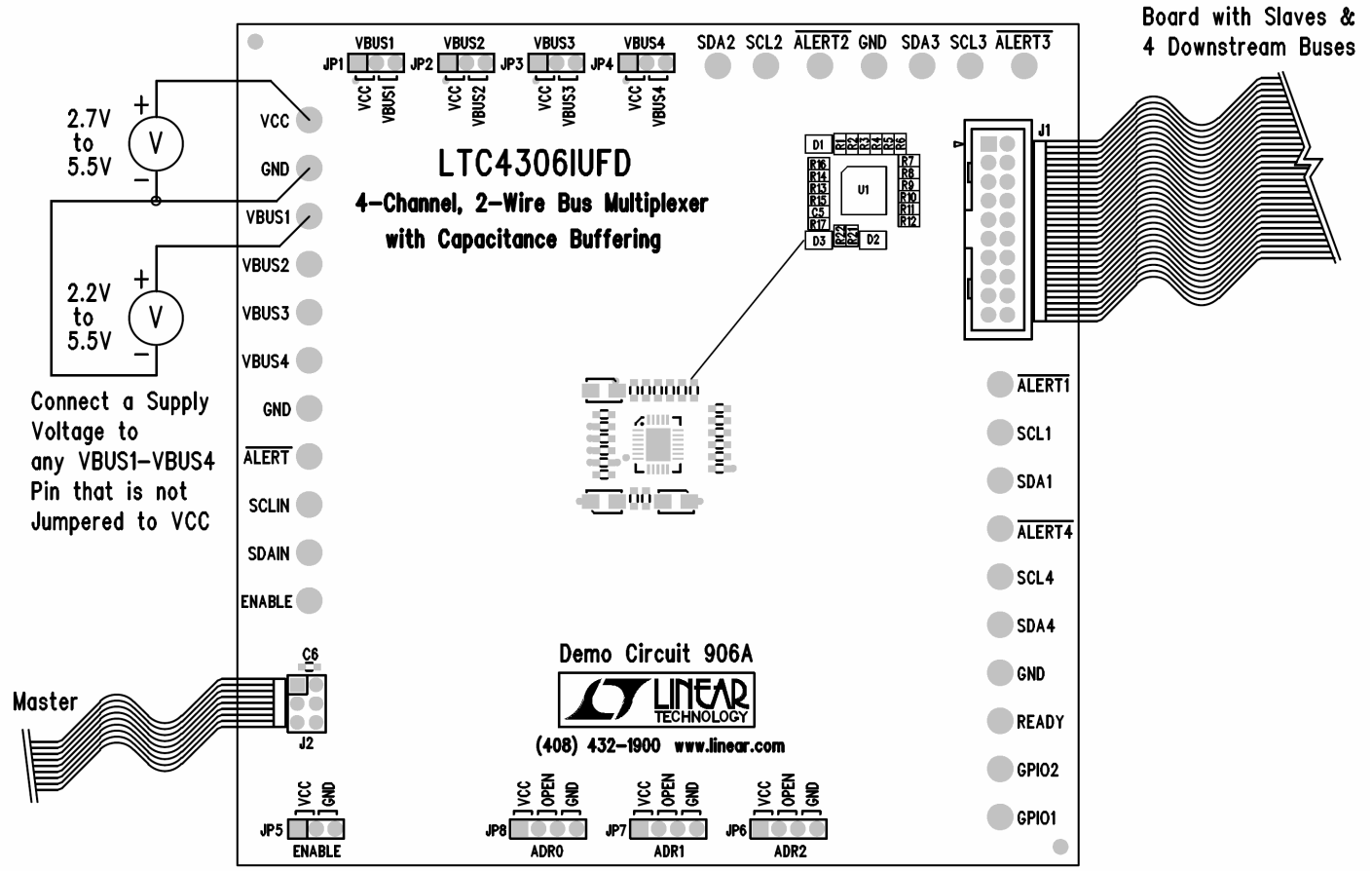
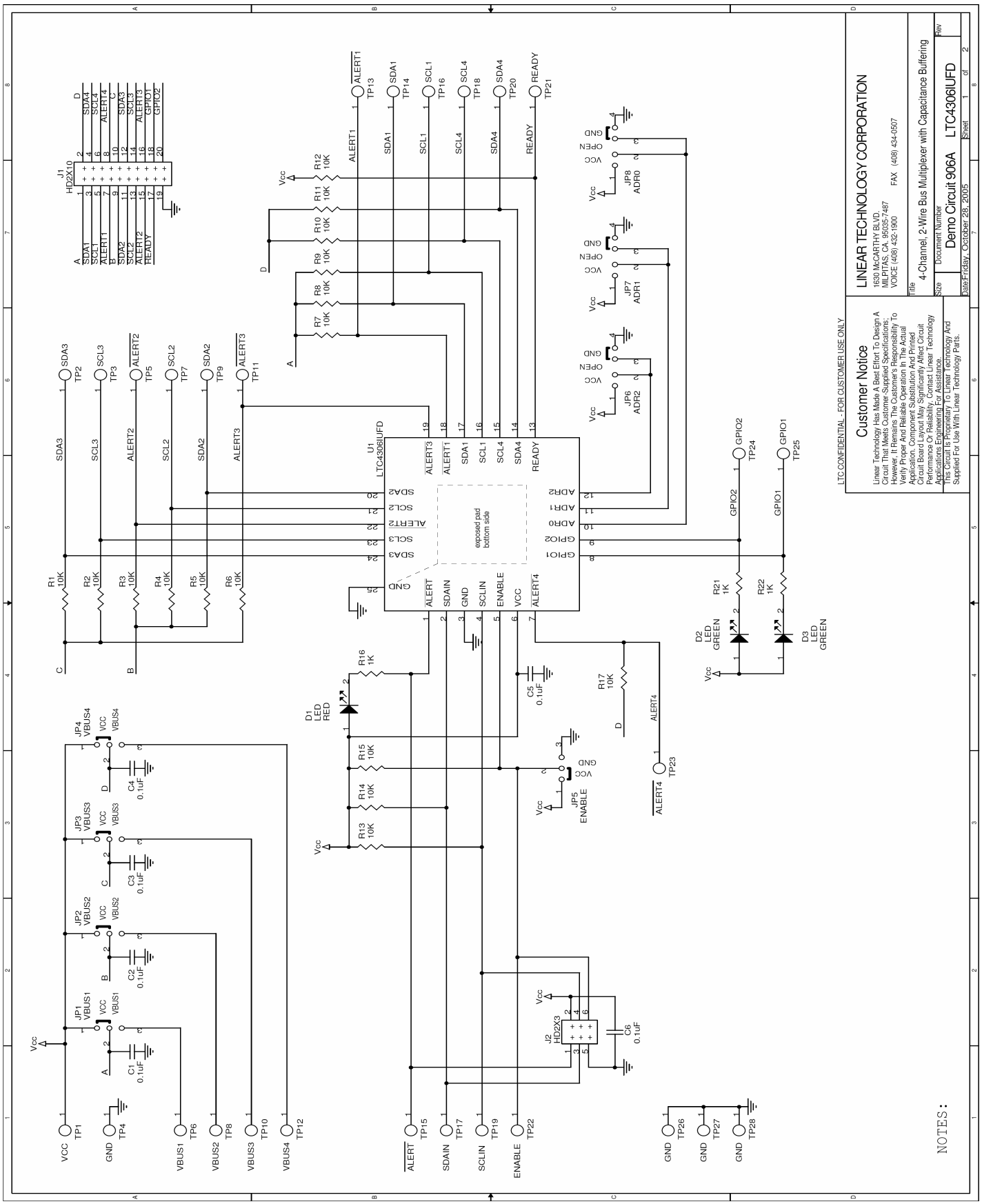


Figure 1. Proper Measurement Equipment Setup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This Circuit Is Proprietary To Linear Technology And Supplied For Use With Linear Technology Parts.
Title
4-Channel, 2-Wire Bus Multiplexer with Capacitance Buffering
Size
Document Number
Demo Circuit 906A
LTC4306IUFD
Rev
Date: Friday, October 28, 2005
Sheet 1 of 2
U1
LTC4306IUFD
exposed pad
bottom side
J1
HD2X10
J2
HD2X3
JP1 VBUS1
JP2 VBUS2
JP3 VBUS3
JP4 VBUS4
JP5 ENABLE
JP6 ADR2
JP7 ADR1
JP8 ADR0
D1 LED RED
D2 LED GREEN
D3 LED GREEN
NOTES: