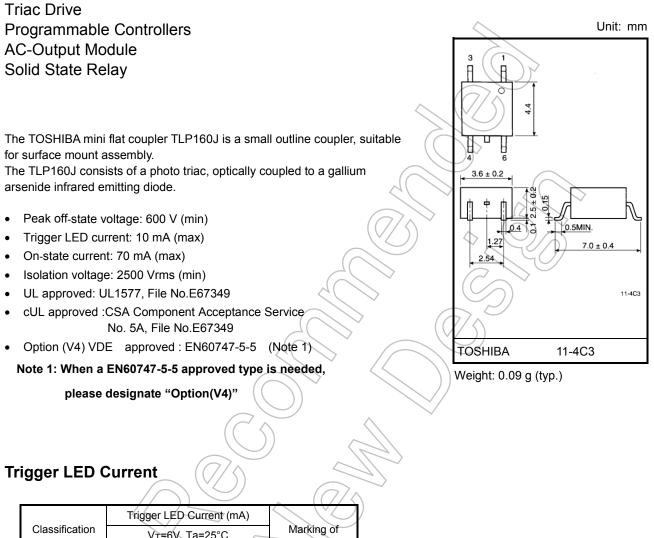
TLP160J

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TOSHIBA Photocoupler GaAs Ired & Photo-Triac

TLP160J



	Trigger LED C	$\langle \rangle \rangle \rangle \rangle \rangle \rangle$	
Classification (Note 1)	V _T =6V, T	a=25°C	Marking of Classification
	Min	Max	
(IFT7)		7.0	M
Standard	\sim	10	T7, blank
	\frown		

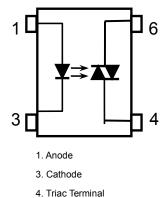
Note 1:Ex.(IFT7); TLP160J (IFT7)

Note: Application type name for certification test, please

use standard product type name, i.e.

TLP160J(IFT7): TLP160J

Pin Configurations (top view)



6. Triac Terminal

Start of commercial production 1988-04

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit		
Forward current		lF	50	mA		
	Forward current derating (Ta ≥ 53°C)		ΔI _F / °C	-0.7	mA / °C	
	Peak forward current (100 µs pulse, 100 pps)		lfp	1	A	
LED	Reverse voltage	Reverse voltage		5	v	
	Diode power dissipation		PD	100	mW	\bigcirc
	Diode power dissipation derating (Ta \ge 53°C)		ΔP _D /°C	-1.4	mW/°C	\sim
	Junction temperature		Tj	125	°C	\mathcal{O}
	Off-state output terminal voltage		Vdrm	600	X	
	On-state RMS current	Ta=25°C	IT(RMS)	70	mA	
		Ta=70°C		40		
	On-state current derating (Ta ≥ 25°C)		ΔI _T / °C	-0.67	mA / °C	
Detector	Peak on-state current (100µs pulse, 120pps)		ITP	(2^2)	A	$\langle \rangle$
Dete	Peak nonrepetitive surge current (P _W =10ms)		Ітѕм	1.2	A <	$\sum O$
	Output power dissipation		Po	200	mW	
	Output power dissipation derating (Ta \ge 25°C)		ΔP ₀ /°C	-2.0	mW / °C	9
	Junction temperature		(T)	115 ((/°C)	
Storage temperature range		Tstg	-55 to 125	Ŷ		
Operat	ting temperature range		Topr	-40 to 100	°C	
Lead s	oldering temperature (10 s)		T _{sol}	260	°C	
Isolatic	on voltage (AC, 1 minute, R	H. ≤ 60%) (Note 1)	BVS	2500	Vrms	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Device considered a two terminal device: Pins 1 and 3 shorted together and pins 4 and 6 shorted together.

Recommended Operating Conditions

Characteristic	Symbol	Min	Тур.	Max	Unit
Supply voltage	VAC	-	-	240	Vac
Forward current	lF	15	20	25	mA
Peak on-state current	ITP	-	-	1	А
Operating temperature	T _{opr}	-25		85	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Electrical Characteristics (Ta = 25°C)

	Characteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
	Forward voltage	VF	IF = 10 mA	1.0	1.15	1.3	V
LED	Reverse current	IR	V _R = 5 V	_	_	10	μA
	Capacitance	CT	VF = 0 V, f = 1 MHz	\nearrow	30	—	pF
	Peak off-state current	IDRM	V _{DRM} = 600 V		10	1000	nA
	Peak on-state voltage	VTM	I _{TM} = 70 mA	X))1.7	2.8	V
for	Holding current	Ін	(0	75	1.0	_	mA
Detector	Critical rate of rise of off-state voltage	dv / dt	V _{in} = 240 Vrms, Ta = 85°C (Fig.1)	\bigcirc	500	_	V / µs
	Critical rate of rise of commutating voltage	dv / dt(c)	IT = 15 mA, Vin = 60 Vrms (Eig.1)	_	0.2		V / µs
oupled Electrical Characteristics (Ta = 25°C)							

Coupled Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Trigger LED current	IFT	V _T = 6 ∀	()	> 5	10	mA
Capacitance input to output	Cs	Vs = 0 V, f = 1 MHz	$\sim_{\mathcal{P}}$	0.8	_	pF
Isolation resistance	Rs	Vs = 500 V, R.H. ≤ 60%	1×10 ¹²	10 ¹⁴	_	Ω
	BVS	AC, 60 s	2500	—	_	Vrms
Isolation voltage		AC, 1 s, in oil	—	5000	_	viins
		DC, 60 s, in oil	—	5000	_	Vdc
Turn-on time	ton	$V_D = 6 \rightarrow 4V, R_L = 100\Omega$ IF = rated IFT × 1.5	_	30	100	μs

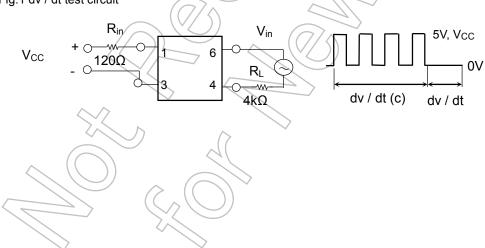
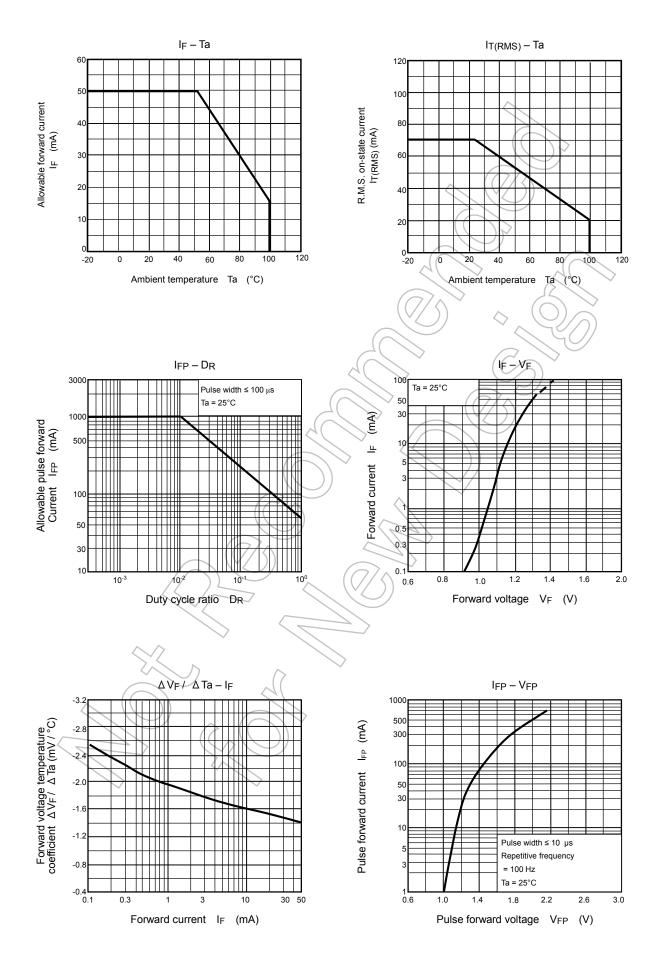
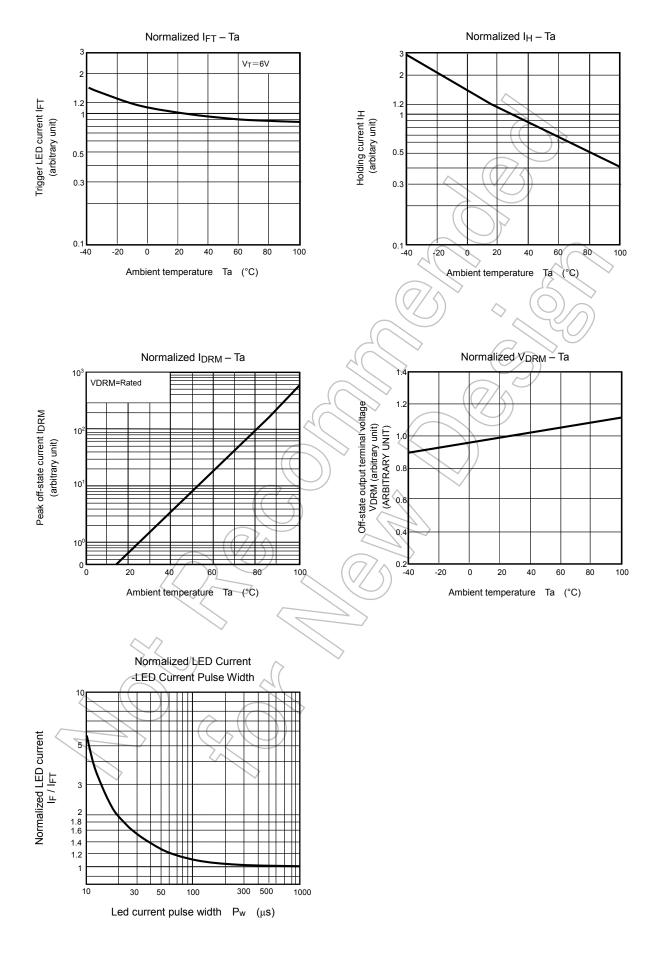


Fig.1 dv / dt test circuit

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