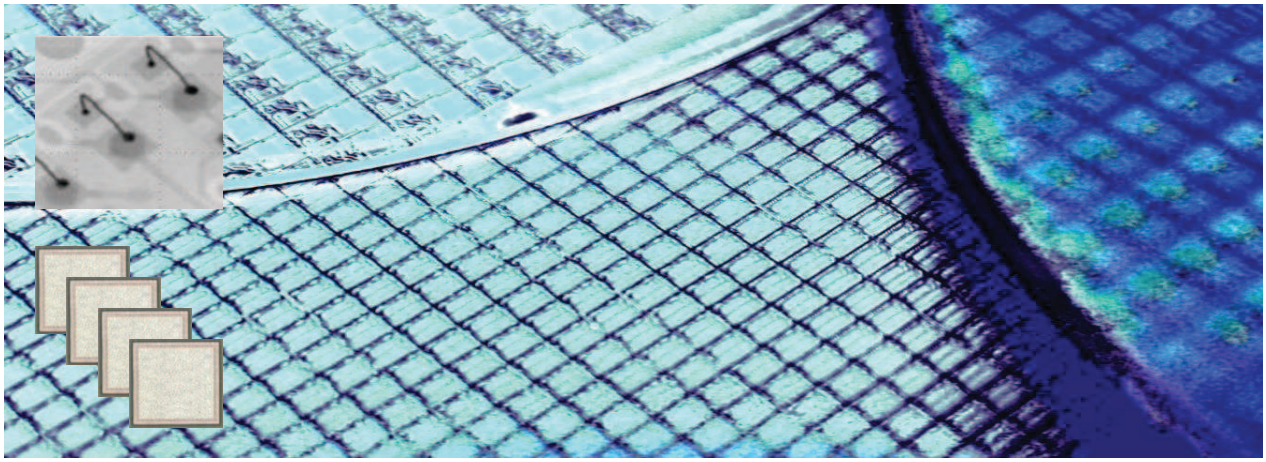
WTSC144.xxx – Wire Bonding Temperature Silicon Vertical Capacitor

Rev 3.1



Key features

- **Full compatible to monolithic ceramic capacitors**
- **Ultra high stability of capacitance value:**
  - **Temperature ±1.5% (-55°C to +200°C)**
  - **Voltage <0.1%/Volts**
  - **Negligible capacitance loss through ageing**
- **Custom sizes, values, shapes, tolerances and higher voltage**
- **Low leakage current down to 100pA**
- **Low profile**

Key applications

- **Any demanding applications,** such as medical, aerospace, automotive industrial…
- **Applicable for standard wire bonding approach** (ball and wedge)
- **Decoupling / Filtering / Charge pump (i.e: Pacemakers / defibrillators)**
- **High reliability applications**
- **Downsizing**

Thanks to the unique IPDiA Silicon capacitor technology, most of the problems encountered in demanding applications can be solved.

The capacitor integration capability (up to 250nF/mm^2) allows **smaller footprint** than ceramic alternative to answer strong volumes constraints.

This technology provides industry leading performances relative to the **capacitor stability** over the full -55°C/+200°C temperature with a **TC<1.5%.**

WTSC are dedicated to applications where **reliability** up to **200°C** is the main parameter.

The IPDiA technology is the most appropriate solution for Chip On Board, Chip On Foil, Chip On Glass, Chip On Ceramic, flip chip and embedded applications, when designers are looking at **utmost decoupling behaviours.**

This Silicon based technology is ROHS compliant and compatible with lead free reflow soldering process.

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Electrical specification

Unit	Capacitance value	10	15	22	33	47	68
	1pF	10pF: 935.144.522.210 935.144.528.210	15pF: 935.144.528.215	22pF: 935.144.528.222	33pF: 935.144.528.233	47pF: 935.144.528.247	68pF: 935.144.528.268
	10pF	100pF: 935.144.522.310 935.144.521.310	150pF: 935.144.522.315 935.144.528.315	220pF: 935.144.528.322	330pF: 935.144.528.333	*Contact IPDIA Sales*	680pF: 935.144.521.368
	0.1nF	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*
	1nF	10nF: 935.144.620.510	*Contact IPDIA Sales*	22nF: 935.144.827.522 935.144.624.522	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*
	10nF	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*

Parameters	Value
Capacitance range	*10pF to 22nF*
Capacitance tolerances	*±15%(*)*
Operating temperature range	*-55 to 200 °C(*)*
Storage temperatures	*- 70 to 215 °C*
Temperature coefficient	*±1.5%, from -55 to +200°C*
Breakdown Voltage (BV)	*90, 50, 30VDC(*)*
Capacitance variation versus RVDC	*0.1 % /V (from 0 V to RVDC)*
Equivalent Serial Inductor (ESL)	*Max 100 pH*
Equivalent Serial Resistor (ESR)	*Max 100 mΩ*
Insulation resistance	*100GΩ @16V,25°C 20GΩ @16V,200°C*
Aging	*Negligible, < 0.001% / 1000h*
Reliability	*FIT<0.017 parts / billions hours, RVDC, from -55 to +200°C*
Capacitor height	*Max 250µm (*)*

(*) Other values on request

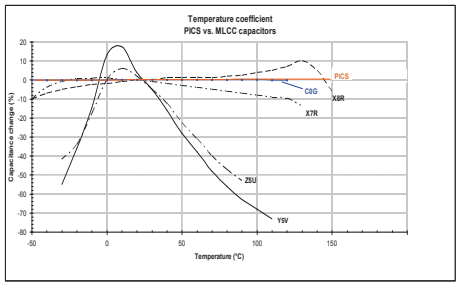


Fig.1 Capacitance change versus temperature variation compared to alternative technologies

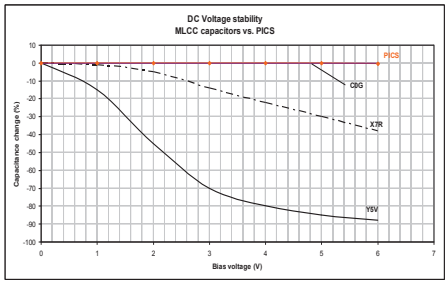


Fig.2 Capacitance change versus voltage variation compared to alternative

Part Number

935.144 **B.2** → Breakdown Voltage: 8= 30V, 6= 50V, 5= 90V

S. → Size: 0 = 0303, 1 = 0202, 2 = 0101, 3 = 0404, 4 = 0504, 5= 0302, 6 = 0503, 7 = 0402, 8 = 0201

U → Unit: 0 = 10 f, 1 = 0.1 p, 2 = 1 p, 3 = 10 p, 4 = 0.1 n, 5 = 1 n, 6 = 10 n, 7 = 0.1 µ, 8 = 1 µ, 9 = 10 µ

xx → Value (E6): 10, 15, 22, 33, 47, 68

i.e: 10nF/0303 case (WTSC type)
→ 935.144.620.510

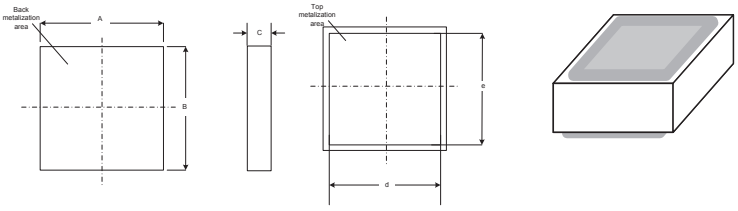
Termination & Outline

Termination

Outer electrodes in 3um Aluminum (Al/Si/Cu: 98.96%/1%/0;04%) or Nickel Gold electroless (Au:0.1um/Ni:5um), other finishings are available on request such as thin fine Gold Titanium (Au: 2um) or Copper (Cu:5um).
Applicable for standard wire bonding approach (ball and wedge).
Typical dimensions, all dimensions in mm.

Package outline

Typ.		0101	0201	0202	0303	0402	0404	0504
Comp. size	A	0.26 ±0.02	0.463 ±0.05	0.463 ±0.05	0.80 ±0.05	1.02 ±0.05	1.02 ±0.05	1.37 ±0.05
	B	0.26 ±0.02	0.26 ±0.02	0.463 ±0.05	0.80 ±0.05	0.463 ±0.05	1.02 ±0.05	1.02 ±0.05



Packaging

Tape and reel, tray, waffle pack or wafer delivery.

For more information, please visit: http://www.ipdia.com
To contact us, email to: sales@ipdia.com

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IPD Capacitor Assembly Set Up

Rev 1.0

Application Note

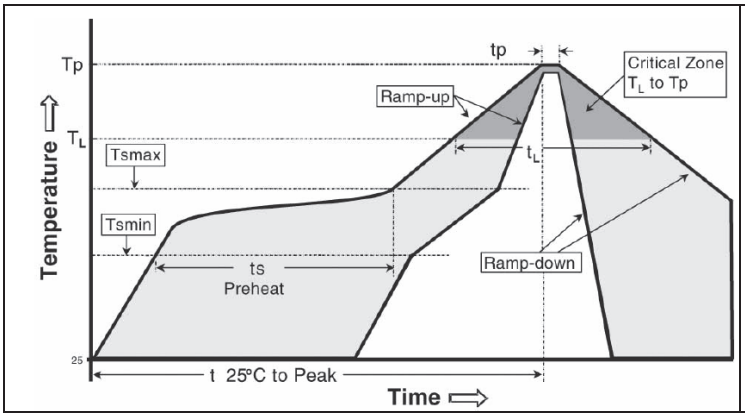
Outline

Silicon Capacitor for surface mounting device (SMD) assembly is a Wafer Level Chip Scale Packaging with the following features:

- Package dedicated to solve tombstoning effect of small SMD package;
- Package compatible with SMD assembly;
- Package without underfilling step;
- Interconnect available with various optional finishing for specific assembly.

Assembly consideration

- Standard pick & place equipment dedicated to WLCSP down to 400µm pitch.
- Solder paste type 3 in most cases of EIA size.
- Reflow has to be done with standard lead-free profile (for SAC alloys) or according to JEDEC recommendations J-STD 020D-01.



	Lead	Leadfree
	Tp: 235 °C	Tp: 260 °C
	TL: 183 °C	TL: 217 °C
	Ts min: 100 °C	Ts min: 150 °C
	Ts max: 150 °C	Ts max: 200 °C
	tL: 60-150 s	tL: 60-150 s

Process recommendation

After soldering, no solder paste should touch the side of the capacitor die as that might results in leakage currents due to remaining flux.

In order to use IPDiA standard capacitors within the JEDEC format and recommendation, the solder flux must be cleaned after reflow soldering step.
Notes: for a proper flux cleaning process, “rosin” flux type (R) or “water soluble” flux type (WS) is recommended for the solder printing material. “No clean” flux (NC) solder paste is not recommended.

In case the flux is not cleaned after the reflow soldering, the standard JEDEC would probably not be appropriate and the solder volume must be controlled:

- using smallest aperture design for the stencil, and using finer solder paste type 4 or 5 for a proper printing process.
- Mirroring pads would be the best recommendation

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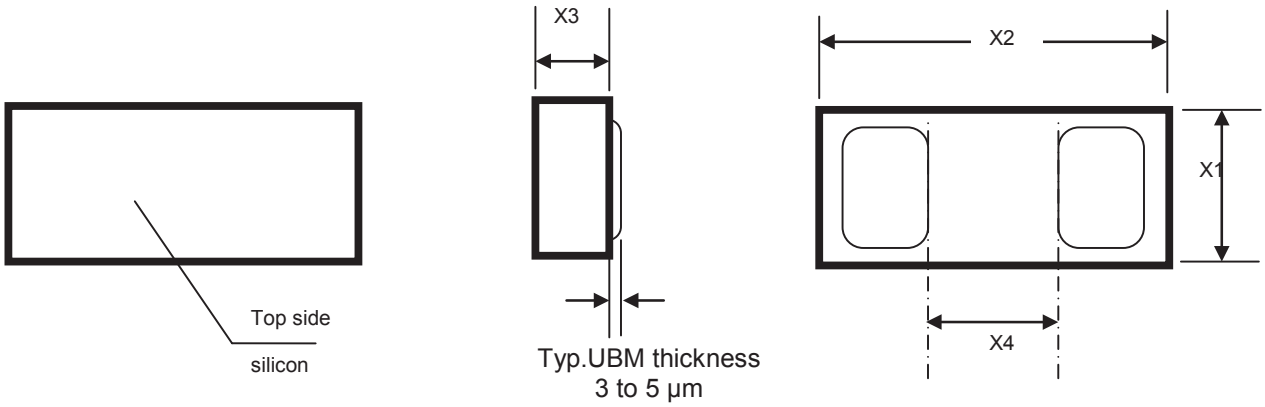
Pad recommendation

The capacitor is compatible with generic requirements for flip chip design (IPC7094).
Standard IPDiA 3D package can be compliant with established EIA size (0201, 0402, 0603, …).

Die size and land pattern dimensions is set up according to following range :

EIA size	0201	0402	0603	0805	1206	1812
Dimension max(X1 x X2) mm	0.86x0.66	1.26x0.76	1.86x1.16	2.26x1.46	3.46x1.86	4.76x3.66
Typical . die thickness X3 (mm)	0.1 or 0.4					
Typical pad size* (mm)	0.15x0.40	0.30x0.50	0.40x0.90	0.50x1.20	0.60x1.60	0.90x3.40
Typical pad separation (X4 mm)	0.3	0.4	0.8	1	2	2.7



After soldering, no solder paste should touch the side of the capacitor die as that might result in leakage currents due to remaining flux.

Manual Handling Considerations

These capacitors are designed to be mounted with a standard SMT line, using solder printing step, pick and place machine and a final reflow soldering step. In case of manual handling and mounting conditions, please follow below recommendations:

- Minimize mechanical pressure on the capacitors (use of a vacuum nozzle is recommended).
- Use of organic tip instead of metal tip for the nozzle.
- Minimize temperature shocks (Substrate pre-heating is recommended).
- No wire bonding on 0402 47nF, 0402 100nF, 1206 1µF and 1812 3,3µF

Process steps:

- On substrate, form the solder meniscus on each land pattern targeting 100 µm height after reflow (screen printing, dispensing solder paste or by wire soldering).
- Pick the capacitor from the tape & reel or the Gel Pack keeping backside visible using a vacuum nozzle and organic tip.
- Temporary place the capacitor on land pattern assuming the solder paste (Flux) will stick and maintain the capacitor.
- Reflow the assembly module with a dedicated thermal profile (see reflow recommendation profile).

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935144620510-T1O 935144620510-T3O