

TL7757 SUPPLY-VOLTAGE SUPERVISOR AND PRECISION VOLTAGE DETECTOR

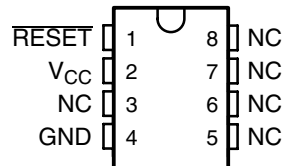
SLVS0411 – SEPTEMBER 1991 – REVISED AUGUST 2003

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Low Standby Current . . . 20 μ A
- RESET Output Defined When V_{CC} Exceeds 1 V
- Precision Threshold Voltage 4.55 V \pm 120 mV
- High Output Sink Capability . . . 20 mA
- Comparator Hysteresis Prevents Erratic Resets

description/ordering information

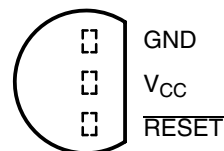
The TL7757 is a supply-voltage supervisor designed for use in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power up, when the supply voltage, V_{CC} , attains a value approaching 1 V, the RESET output becomes active (low) to prevent undefined operation. If the supply voltage drops below threshold voltage level (V_{IT-}), the RESET output goes to the active (low) level until the supply undervoltage fault condition is eliminated.

**D PACKAGE
(TOP VIEW)**

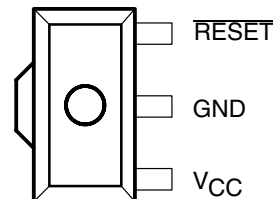


NC—No internal connection

**LP PACKAGE
(TOP VIEW)**



**PK PACKAGE
(TOP VIEW)**



GND is in electrical contact with the tab.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	SOIC (D)	Tube of 75	TL7757CD	7757C	
		Reel of 2500	TL7757CDR		
	TO226 / TO-92 (LP)	SOT (PK)	Reel of 1000	TL7757CPK	T7
			Reel of 2000	Bulk of 1000	TL7757CLP
TL7757CLPR					
-40°C to 85°C	SOIC (D)	Tube of 75	TL7757ID	7757I	
		Reel of 2500	TL7757IDR		
	TO226 / TO-92 (LP)	SOT (PK)	Bulk of 1000	TL7757ILP	TL7757I
			Reel of 2000	TL7757ILPR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

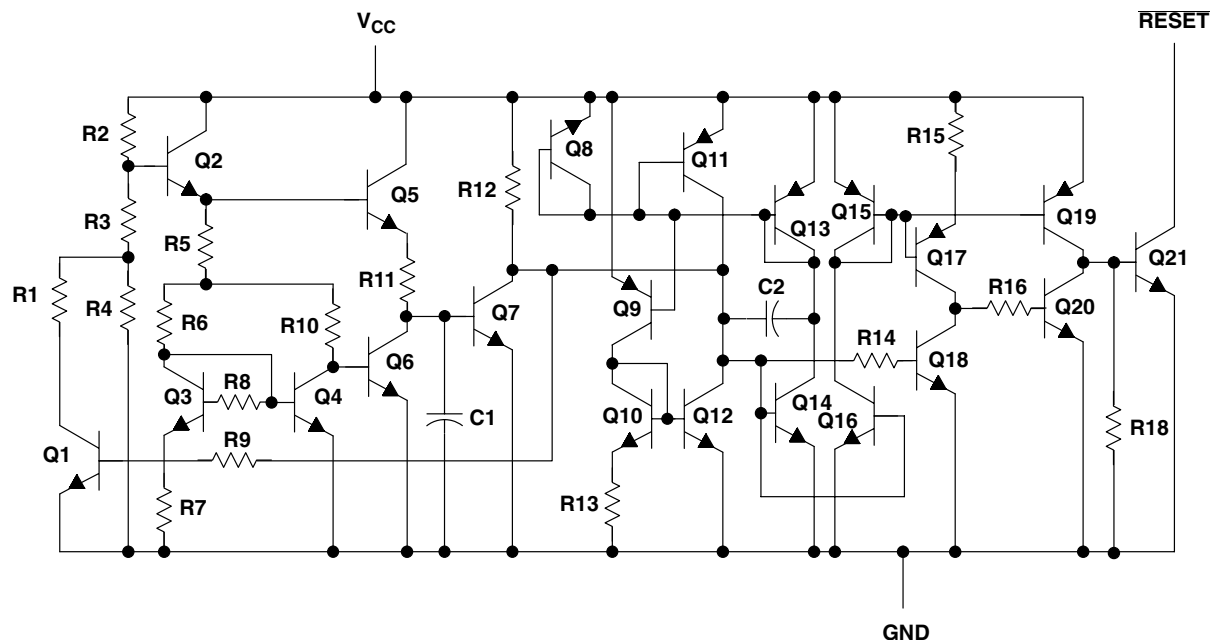
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TL7757 SUPPLY-VOLTAGE SUPERVISOR AND PRECISION VOLTAGE DETECTOR

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equivalent schematic



ACTUAL DEVICE COMPONENT COUNT	
Transistors	27
Resistors	20
Capacitors	2

absolute maximum ratings over operating junction temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	-0.3 V to 20 V
Off-state output voltage range (see Note 1)	-0.3 V to 20 V
Output current, I_O	30 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3):	
D package	97°C/W
LP package	140°C/W
PK package	52°C/W
Operating virtual junction temperature, T_J	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to network terminal ground.
 2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions

		MIN	MAX	UNIT	
V_{CC}	Supply voltage	1	7	V	
V_{OH}	High-level output voltage		15	V	
I_{OL}	Low-level output current		20	mA	
T_A	Operating free-air temperature	TL7757C	0	70	°C
		TL7757I	-40	85	

electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T_A	TL7757C			UNIT
			MIN	TYP	MAX	
V_{IT-}	Negative-going input threshold voltage at V_{CC}	25°C	4.43	4.55	4.67	V
		0°C to 70°C	4.4		4.7	
V_{hys}^\dagger	Hysteresis at V_{CC}	25°C	40	50	60	mV
		0°C to 70°C	30		70	
V_{OL}	Low-level output voltage $I_{OL} = 20$ mA, $V_{CC} = 4.3$ V	25°C		0.4	0.8	V
		0°C to 70°C			0.8	
I_{OH}	High-level output current $V_{CC} = 7$ V, $V_{OH} = 15$ V, See Figure 1	25°C			1	µA
		0°C to 70°C			1	
V_{res}^\ddagger	Power-up reset voltage $R_L = 2.2$ kΩ, V_{CC} slew rate ≤ 5 V/µs	25°C		0.8	1	V
		0°C to 70°C			1.2	
I_{CC}	Supply current $V_{CC} = 4.3$ V	25°C		1400	2000	µA
		0°C to 70°C			2000	
		$V_{CC} = 5.5$ V	0°C to 70°C			

[†] This is the difference between positive-going input threshold voltage, V_{IT+} , and negative-going input threshold voltage, V_{IT-} .

[‡] This is the lowest voltage at which RESET becomes active.

switching characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T_A	TL7757C			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output V_{CC} slew rate ≤ 5 V/µs, See Figures 2 and 3	25°C		3.4	5	µs
		0°C to 70°C			5	
t_{PHL}	Propagation delay time, high-to-low-level output See Figures 2 and 3	25°C		2	5	µs
		0°C to 70°C			5	
t_r	Rise time V_{CC} slew rate ≤ 5 V/µs, See Figures 2 and 3	25°C		0.4	1	µs
		0°C to 70°C			1	
t_f	Fall time See Figures 2 and 3	25°C		0.05	1	µs
		0°C to 70°C			1	
$t_{w(min)}$	Minimum pulse duration at V_{CC} for output response	25°C			5	µs
		0°C to 70°C			5	

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electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A	TL7757I			UNIT
			MIN	TYP	MAX	
V _{IT-} Negative-going input threshold voltage at V _{CC}		25°C	4.43	4.55	4.67	V
		-40°C to 85°C	4.4		4.7	
V _{hys} [†] Hysteresis at V _{CC}		25°C	40	50	60	mV
		-40°C to 85°C	30		70	
V _{OL} Low-level output voltage	I _{OL} = 20 mA, V _{CC} = 4.3 V	25°C		0.4	0.8	V
		-40°C to 85°C			0.8	
I _{OH} High-level output current	V _{CC} = 7 V, V _{OH} = 15 V, See Figure 1	25°C			1	μA
		-40°C to 85°C			1	
V _{res} [‡] Power-up reset voltage	R _L = 2.2 kΩ, V _{CC} slew rate ≤ 5 V/μs	25°C		0.8	1	V
		-40°C to 85°C			1.2	
I _{CC} Supply current	V _{CC} = 4.3 V	25°C		1400	2000	μA
		-40°C to 85°C			2100	
		-40°C to 85°C			40	

[†] This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.

[‡] This is the lowest voltage at which RESET becomes active.

switching characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A	TL7757I			UNIT
			MIN	TYP	MAX	
t _{PLH} Propagation delay time, low-to-high-level output	V _{CC} slew rate ≤ 5 V/μs, See Figures 2 and 3	25°C		3.4	5	μs
		-40°C to 85°C			5	
t _{PHL} Propagation delay time, high-to-low-level output	See Figures 2 and 3	25°C		2	5	μs
		-40°C to 85°C			5	
t _r Rise time	V _{CC} slew rate ≤ 5 V/μs, See Figures 2 and 3	25°C		0.4	1	μs
		-40°C to 85°C			1	
t _f Fall time	See Figures 2 and 3	25°C		0.05	1	μs
		-40°C to 85°C			1	
t _{w(min)} Minimum pulse duration at V _{CC} for output response		25°C			5	μs
		-40°C to 85°C			5	



PARAMETER MEASUREMENT INFORMATION

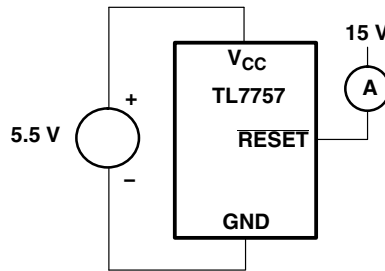
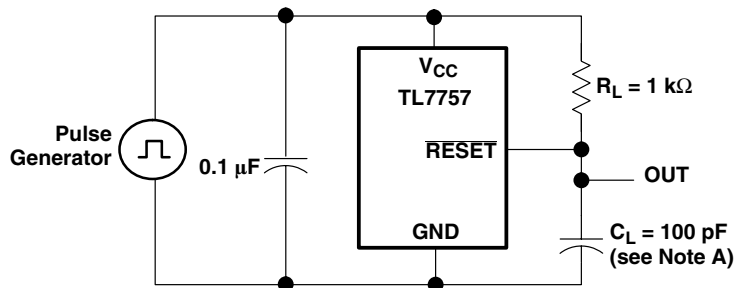
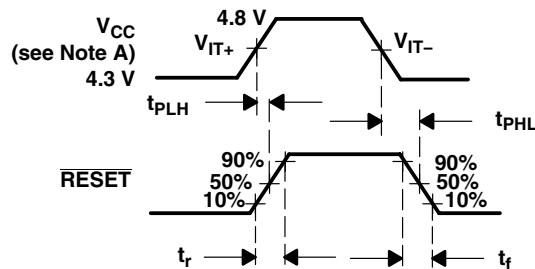


Figure 1. Test Circuit for Output Leakage Current



NOTE A: Includes jig and probe capacitance

Figure 2. Test Circuit for $\overline{\text{RESET}}$ Output Switching Characteristics



NOTE A: V_{CC} slew rate $\leq 5 \mu\text{s}$

Figure 3. Switching Diagram

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TYPICAL CHARACTERISTICS†

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**SUPPLY VOLTAGE
vs
RESET OUTPUT VOLTAGE**

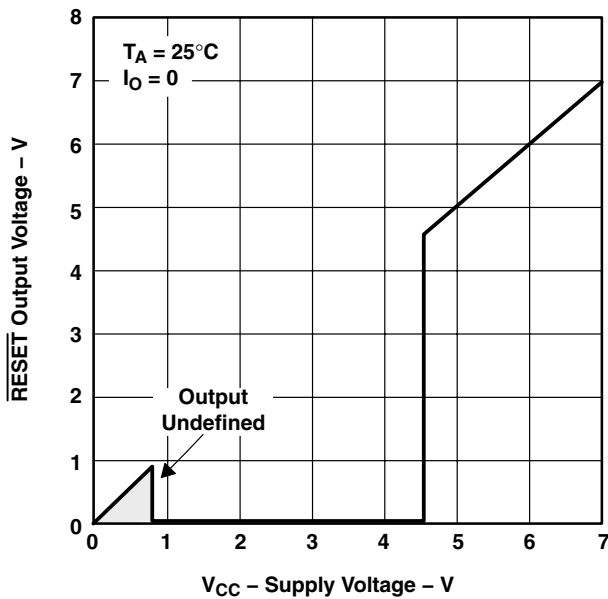


Figure 4

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

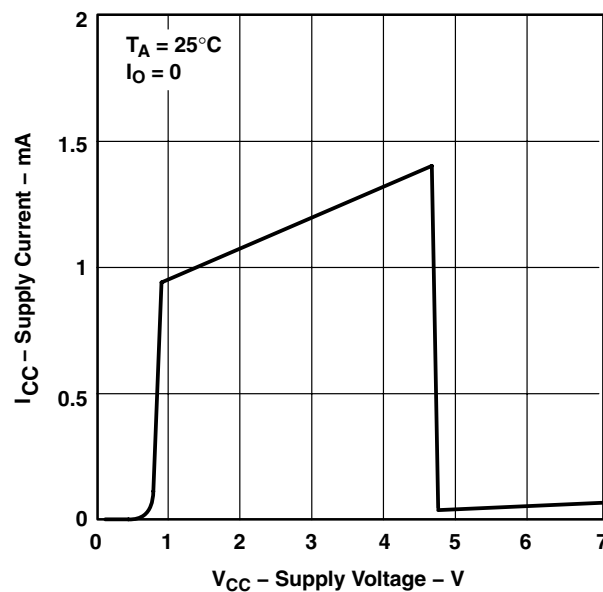


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

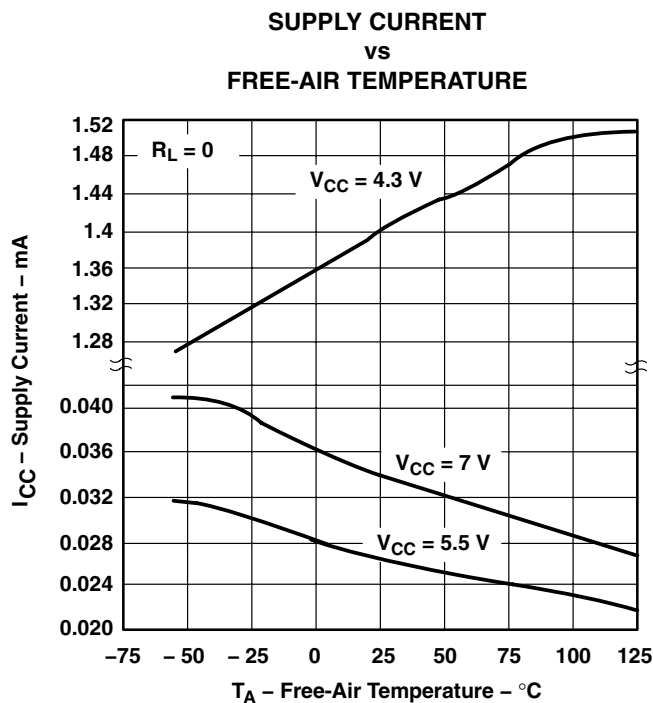


Figure 6

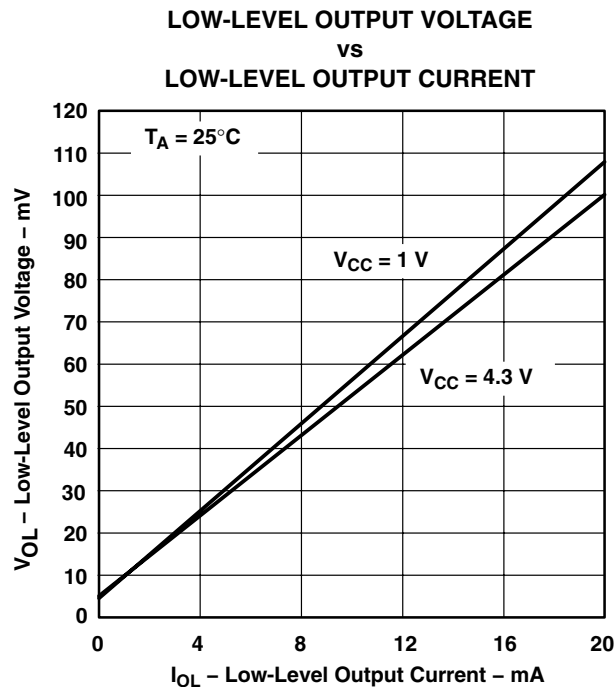


Figure 7

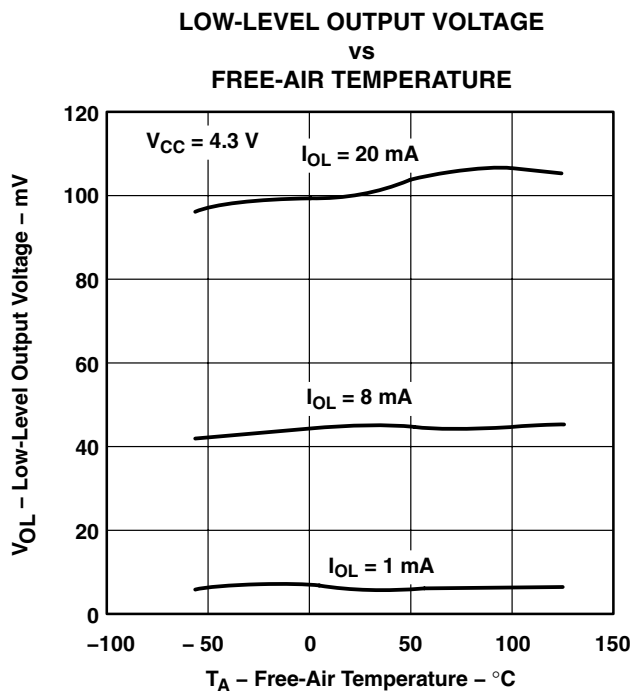


Figure 8

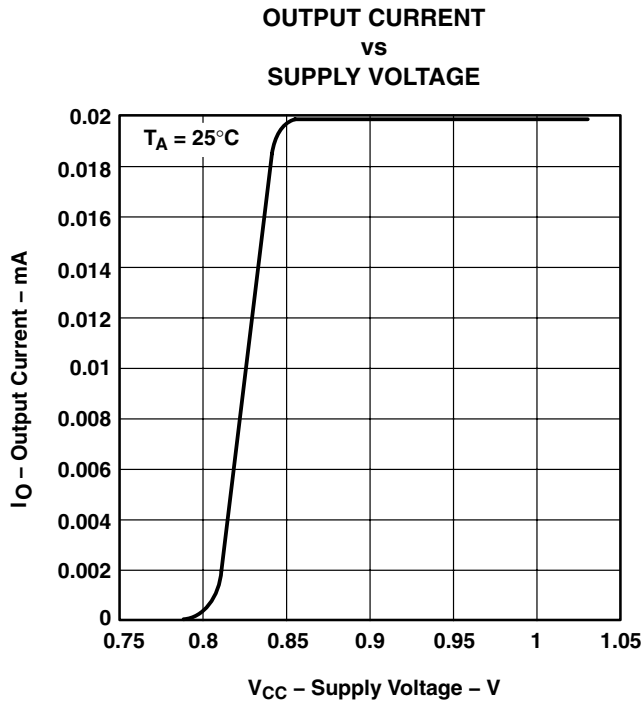


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

**INPUT THRESHOLD VOLTAGE
 (NEGATIVE-GOING V_{CC})
 vs
 FREE-AIR TEMPERATURE**

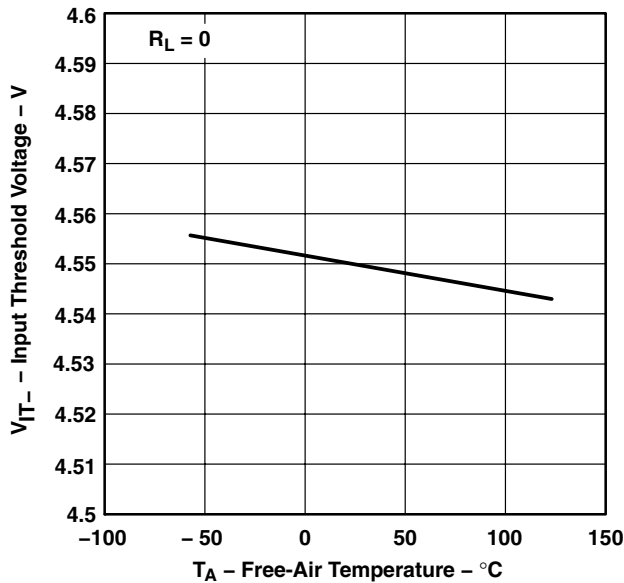


Figure 10

**POWER-UP RESET VOLTAGE
 vs
 FREE-AIR TEMPERATURE**

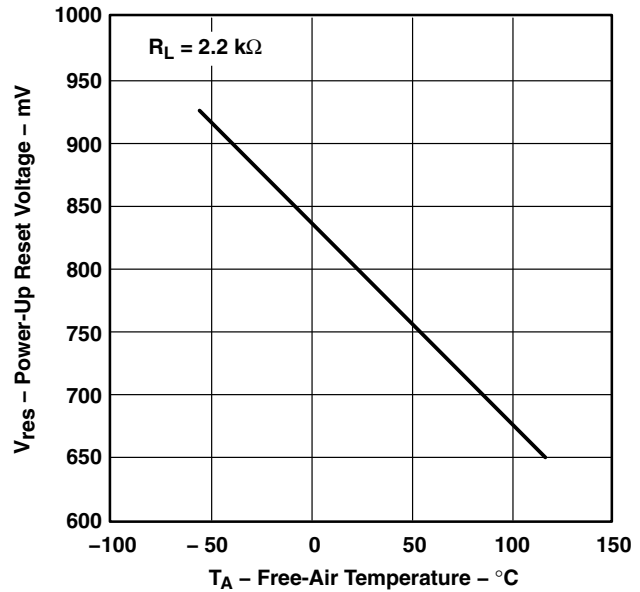


Figure 11

**POWER-UP RESET VOLTAGE
 AND SUPPLY VOLTAGE
 vs
 TIME**

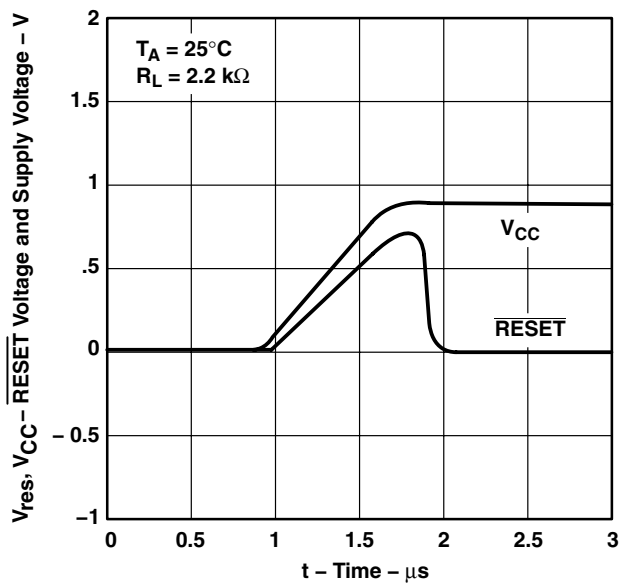


Figure 12

PROPAGATION DELAY TIME

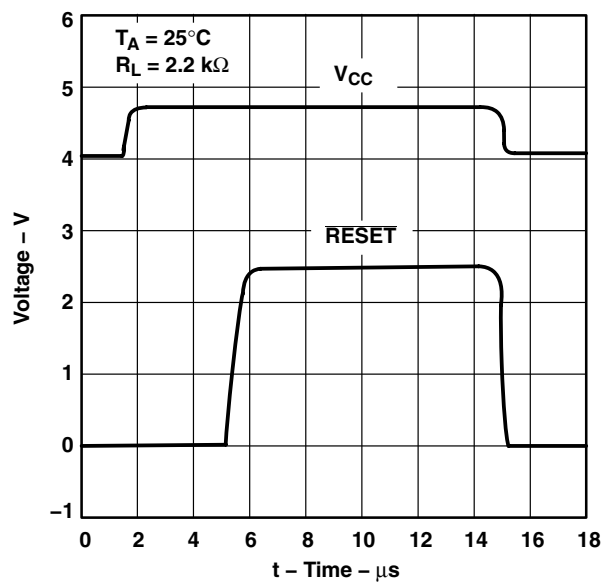
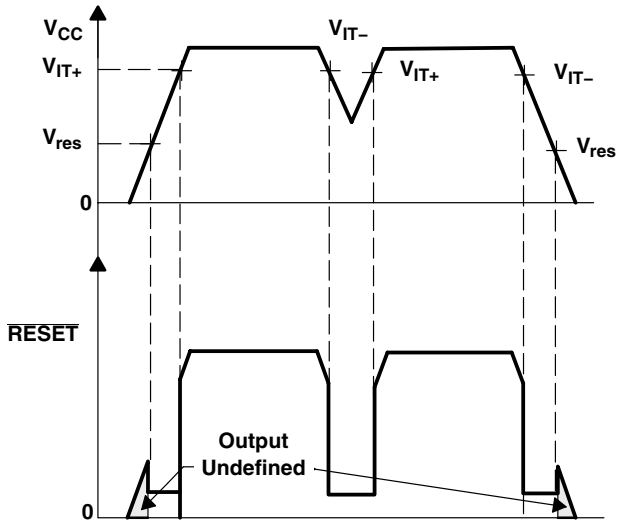


Figure 13

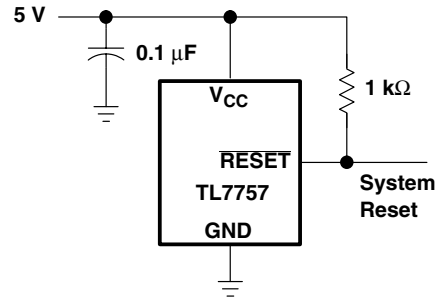
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

TYPICAL TIMING DIAGRAM



TYPICAL APPLICATION DIAGRAM



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7757CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	7757C	Samples
TL7757CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	7757C	Samples
TL7757CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	7757C	Samples
TL7757CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	SN	N / A for Pkg Type	0 to 70	TL7757C	Samples
TL7757CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	SN	N / A for Pkg Type	0 to 70	TL7757C	Samples
TL7757CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	SN	N / A for Pkg Type	0 to 70	TL7757C	Samples
TL7757CPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	0 to 70	T 7	Samples
TL7757CPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	0 to 70	T 7	Samples
TL7757ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7757I	Samples
TL7757IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7757I	Samples
TL7757ILP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85	TL7757I	Samples
TL7757ILPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85	TL7757I	Samples
TL7757ILPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85	TL7757I	Samples
TL7757IPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 85	7I	Samples
TL7757IPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 85	7I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7757CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7757CPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL7757IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7757IPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

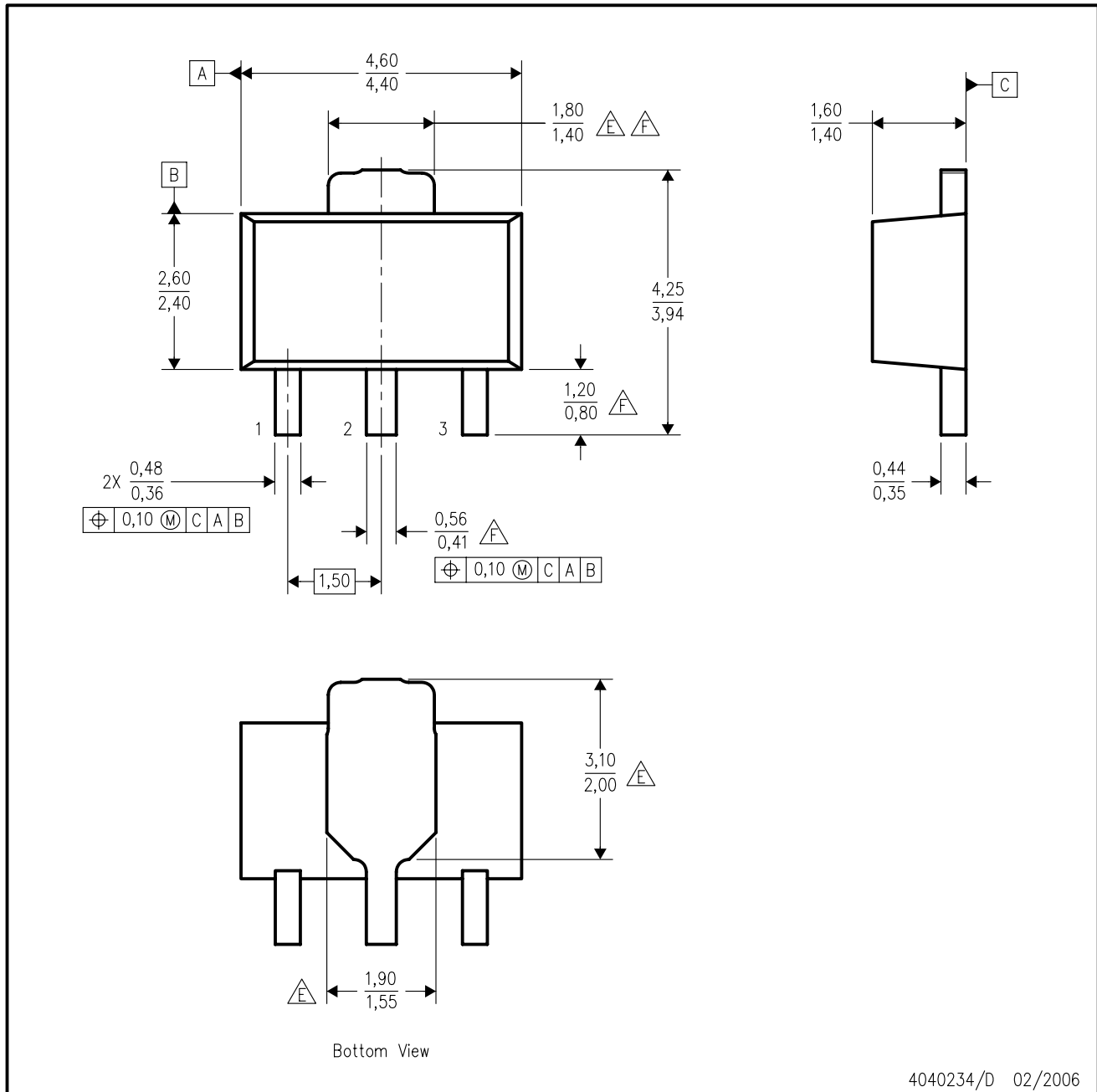


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7757CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7757CPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL7757IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7757IPK	SOT-89	PK	3	1000	340.0	340.0	38.0

PK (R-PSS0-F3)

PLASTIC SINGLE-IN-LINE PACKAGE



4040234/D 02/2006

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - The center lead is in electrical contact with the tab.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
- △E Thermal pad contour optional within these dimensions.
 △F Falls within JEDEC TO-243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

LP 3

TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040001-2/F

LP0003A



PACKAGE OUTLINE

TO-92 - 5.34 mm max height

TO-92



4215214/B 04/2017

NOTES:

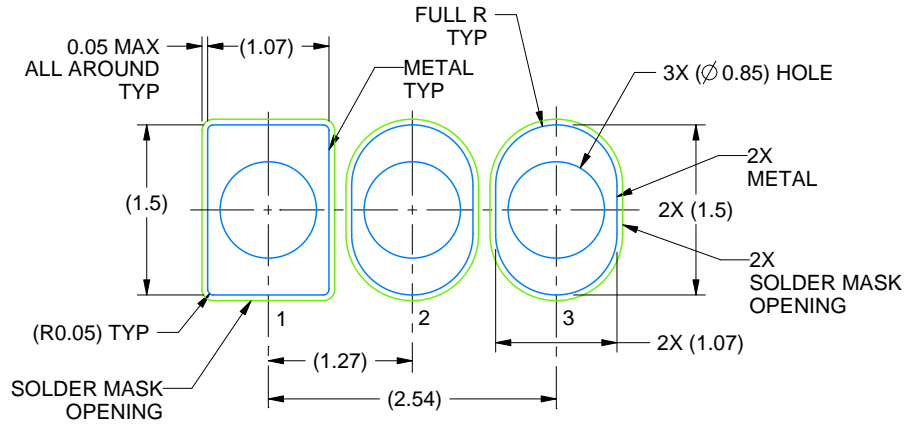
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
 - a. Straight lead option available in bulk pack only.
 - b. Formed lead option available in tape and reel or ammo pack.
 - c. Specific products can be offered in limited combinations of shipping medium and lead options.
 - d. Consult product folder for more information on available options.

EXAMPLE BOARD LAYOUT

LP0003A

TO-92 - 5.34 mm max height

TO-92



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

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TAPE SPECIFICATIONS

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

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