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November 2013

# FQD17N08L

# N-Channel QFET® MOSFET

80 V, 12.9 A, 100 mΩ

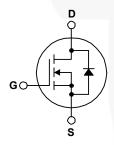
## **Description**

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, • 100% Avalanche Tested DC motor control, and variable switching power applications.

#### **Features**

- 12.9 A, 80 V,  $R_{DS(on)}$  = 100 m $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D = 6.45 A$
- Low Gate Charge (Typ. 8.8 nC)
- Low Crss (Typ. 29 pF)





## Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	FQD17N08LTM	Unit
$V_{DSS}$	Drain-Source Voltage	80	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)	12.9	Α
	- Continuous (T <sub>C</sub> = 100°C)	8.2	Α
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	51.6	Α
$V_{GSS}$	Gate-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	100	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	12.9	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) *	2.5	W
	Power Dissipation (T <sub>C</sub> = 25°C)	40	W
	- Derate above 25°C	0.32	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering, 1/8" from case for 5 seconds	300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FQD17N08LTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max. 3.13		
В	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

## **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD17N08LTM	FQD17N08L	DPAK	Tape and Reel	330 mm	16 mm	2500 units

## **Electrical Characteristics**

T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	80			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.08		V/°C
I <sub>DSS</sub>	Zoro Cato Valtago Prain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	μΑ
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 64 V, T <sub>C</sub> = 125°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0		2.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V, } I_{D} = 6.45 \text{ A}$ $V_{GS} = 5 \text{ V, } I_{D} = 6.45 \text{ A}$		0.076 0.090	0.100 0.115	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 6.45 A		11.7		S
Dynam	ic Characteristics			l	l	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,		400	520	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		120	155	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			29	37	pF
Switch	ing Characteristics		•		•	
t <sub>d(on)</sub>	Turn-On Delay Time			7	25	ns

	. •				
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 16.5 A,	 7	25	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$	 290	590	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	9	 20	50	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	 75	160	ns
$Q_g$	Total Gate Charge	V <sub>DS</sub> = 64 V, I <sub>D</sub> = 16.5 A,	 8.8	11.5	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 5 V	 2.0		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)	 5.4		nC

#### **Drain-Source Diode Characteristics and Maximum Ratings**

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I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		-		12.9	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		-		51.6	Α
$V_{SD}$	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 12.9 A	-		1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 16.5 A,		55		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs		85	//	nC

#### Notes:

- **Notes:** 1. Repetitive rating : pulse-width limited by maximum junction temperature. 2. L = 0.83 mH,  $I_{AS}$  = 12.9 A,  $V_{DD}$  = 25 V,  $R_G$  = 25  $\Omega$ , starting  $T_J$  = 25°C. 3.  $I_{SD} \le$  16.5 A, di/dt  $\le$  300 A/ $\mu$ s,  $V_{DD} \le$  BV $_{DSS}$ , starting  $T_J$  = 25°C. 4. Essentially independent of operating temperature.

# **Typical Characteristics**

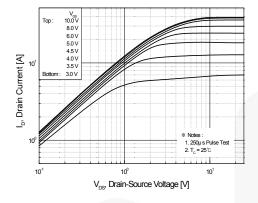


Figure 1. On-Region Characteristics

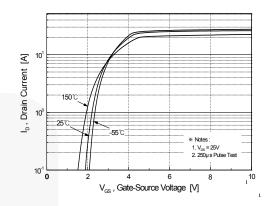


Figure 2. Transfer Characteristics

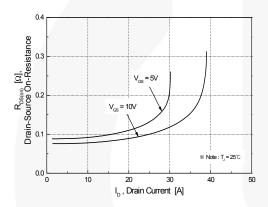


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

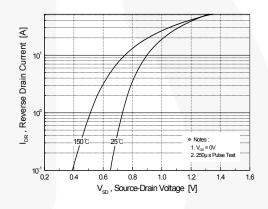


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

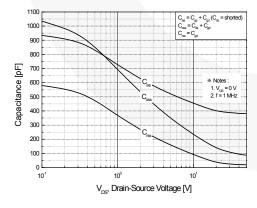


Figure 5. Capacitance Characteristics

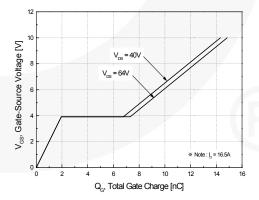


Figure 6. Gate Charge Characteristics

# 12 (Normalized) 10 (Normalized

Typical Characteristics (Continued)

3.0

3.0

2.5

(Normalized)

3.0

3.0

2.5

(Normalized)

3.0

3.0

3.0

3.0

4. Notes:

1. V<sub>os</sub> = 10 V

2. U<sub>c</sub> = 6.45 A

0.0

-100

-50

0.50

1.0

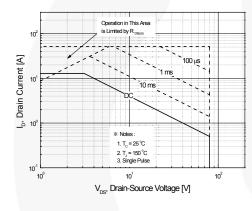
1.50

200

T<sub>1</sub>, Junction Temperature (<sup>2</sup>C)

Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature



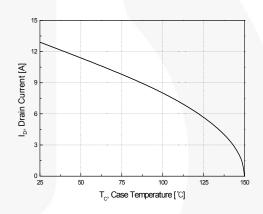


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

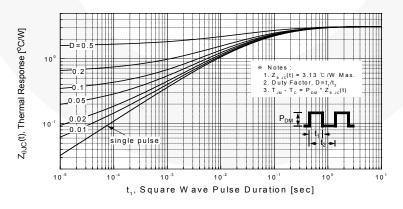


Figure 11. Transient Thermal Response Curve

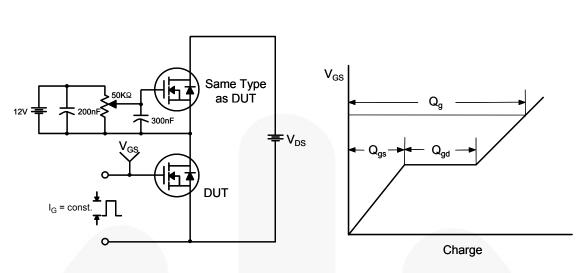


Figure 12. Gate Charge Test Circuit & Waveform

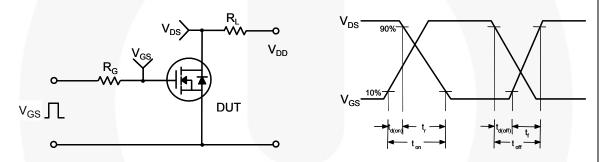


Figure 13. Resistive Switching Test Circuit & Waveforms

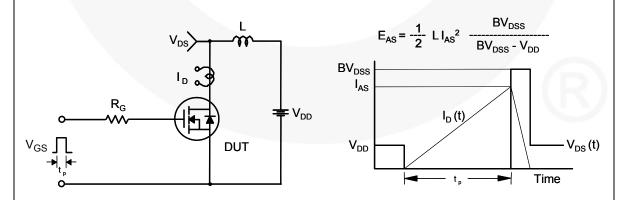
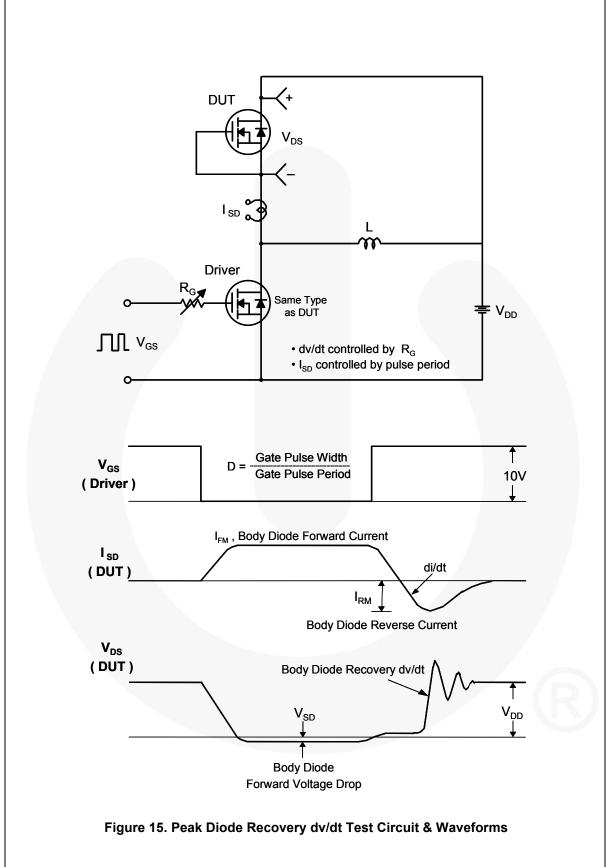
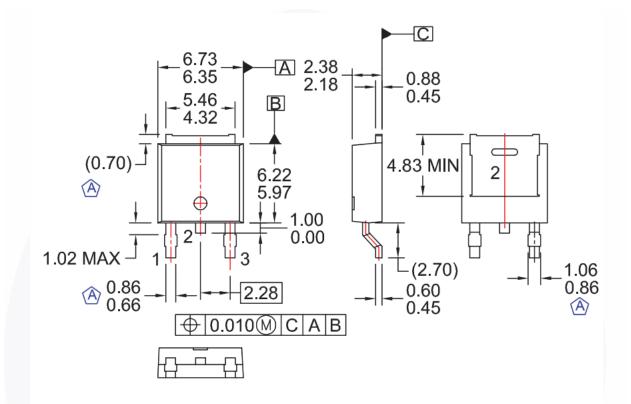


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



#### **Mechanical Dimensions**



NOTES: UNLESS OTHERWISE SPECIFIED

- (A) CONFORMS TO JEDEC TO-252 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- E) FORMERLY NAMED BD1733
- F) DRAWING FILE NAME: MKT-TO252D03REV1

Figure 16. TO-252 (D-PAK), Molded, 3-Lead, Jedec TO-252 VAR. AB, Surface Mount

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