TEXAS INSTRUMENTS

OPA316, OPA2316, OPA2316S, OPA4316

SBOS703F – APRIL 2014 – REVISED OCTOBER 2016

OPAx316 10-MHz, Low-Power, Low-Noise, RRIO, 1.8-V CMOS Operational Amplifier

1 Features

- Unity-Gain Bandwidth: 10 MHz
- Low I_Q: 400 µA/ch
- Wide Supply Range: 1.8 V to 5.5 V
- Low Noise: 11 nV/√Hz at 1 kHz
- Low Input Bias Current: ±5 pA
- Offset Voltage: ±0.5 mV
- Unity-Gain Stable
- Internal RFI-EMI Filter
- Shutdown Version: OPA2316S
- Extended Temperature Range: –40°C to +125°C

2 Applications

- Battery-Powered Instruments:
  - Consumer, Industrial, Medical
  - Notebooks, Portable Media Players
- Sensor Signal Conditioning
- Automotive Applications
- Barcode Scanners
- Active Filters
- Audio

3 Description

The OPAx316 family of single, dual, and quad operational amplifiers represents a new generation of general-purpose, low-power operational amplifiers. Featuring rail-to-rail input and output swings, low quiescent current (400 µA/ch typical) combined with a wide bandwidth of 10 MHz and very-low noise (11 nV/√Hz at 1 kHz) makes this family attractive for a variety of applications that require a good balance between cost and performance. The low input bias current supports those operational amplifiers to be used in applications with MΩ source impedances.

The robust design of the OPAx316 provide ease-of-use to the circuit designer—a unity-gain stable, integrated RFI-EMI rejection filter, no phase reversal in overdrive condition, and high electrostatic discharge (ESD) protection (4-kV HBM).

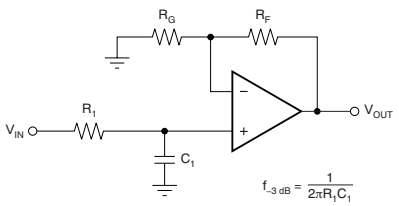
These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V). This latest addition of low-voltage CMOS operational amplifiers, in conjunction with the OPAx313 and OPAx314 provide a family of bandwidth, noise, and power options to meet the needs of a wide variety of applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA316	SC-70 (5)	1.25 mm × 2.00 mm
	SOT-23 (5)	1.60 mm × 2.90 mm
OPA2316	DFN (8)	3.00 mm × 3.00 mm
	MSOP, VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
OPA2316S	MSOP, VSSOP (10)	3.00 mm × 3.00 mm
	X2QFN (10)	1.50 mm × 2.00 mm
OPA4316	TSSOP (14)	4.40 mm × 5.00 mm
	SOIC (14)	8.65 mm × 3.91 mm

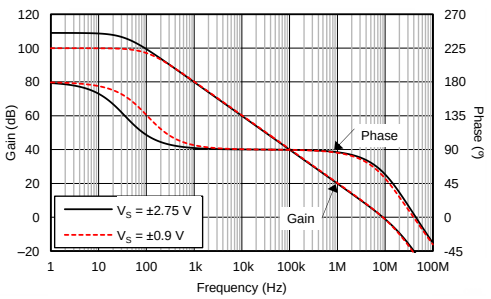
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Single-Pole, Low-Pass Filter



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Low-Supply Current (400 µA/ch) for 10-MHz Bandwidth



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (May 2016) to Revision F — **Page**

- Added SOIC (14) / OPA4316 body size information to *Device Information* table ... 1
- Added D package to PW package pinout drawing ... 4
- Added D (SOIC) thermal information to *Thermal Information*: OPA4316 table ... 8

Changes from Revision D (December 2014) to Revision E — **Page**

- Added new "*RUG*" package ... 1

Changes from Revision C (October 2014) to Revision D — **Page**

- Added *Shutdown* section to Electrical Characteristics table ... 10
- Added *Related Documentation* section ... 27

Changes from Revision B (August 2014) to Revision C — **Page**

- Updated devices and packages in *Device Information* table ... 1
- Added thermal information for OPA2316S and OPA4316 ... 7

Changes from Revision A (April 2014) to Revision B — **Page**

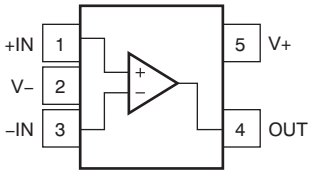
- Added OPA2316 to the *Device Information* table ... 1
- Added thermal information for OPA2316 ... 7
- Added channel separation to *Electrical Characteristics* ... 9
- Added GBP instead of UGB in the *Electrical Characteristics* ... 9
- Added Channel Separation vs Frequency plot ... 16

Changes from Original (April 2014) to Revision A **Page**

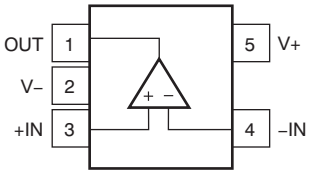
- Changed status from preview to production 1

5 Pin Configuration and Functions

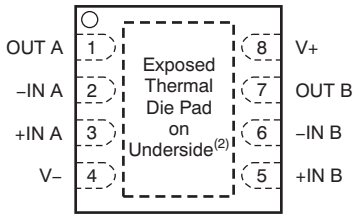
DCK Package
5-Pin SC70
Top View



DBV Package
5-Pin SOT-23
Top View



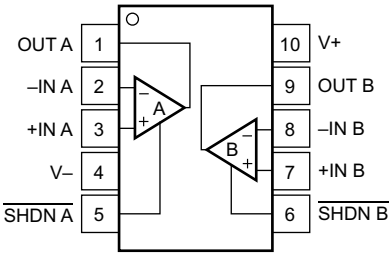
DRG Package
8-Pin DFN
Top View



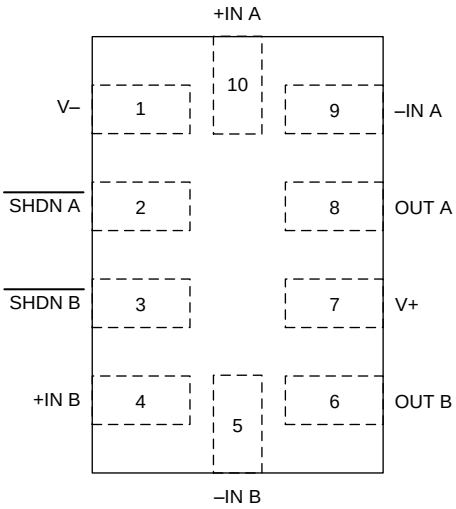
Pitch: 0.5 mm.

Connect thermal pad to V–. Pad size: 2.00 mm × 1.20 mm.

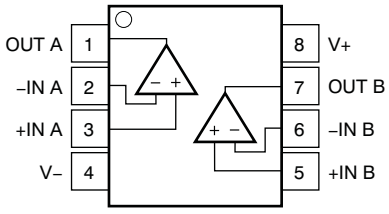
DGS Package
10-Pin MSOP
Top View



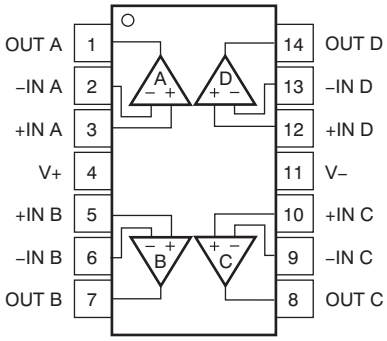
RUG Package
10-Pin QFN
Top View



D, DGK Packages
8-Pin MSOP, SO
Top View



D, PW Packages
14-Pin SOIC, TSSOP
Top View



Pin Functions

NAME	PIN							DESCRIPTION
	OPA316		OPA2316	OPA2316S		OPA4316		
	DBV	DCK	D, DGK, DRG	DGS	RUG	PW	D	
+IN	3	1	—	—	—	—	—	Noninverting input
+IN A	—	—	3	3	10	3	3	Noninverting input
+IN B	—	—	5	7	4	5	5	Noninverting input
+IN C	—	—	—	—	—	10	10	Noninverting input
+IN D	—	—	—	—	—	12	12	Noninverting input
–IN	4	3	—	—	—	—	—	Inverting input
–IN A	—	—	2	2	9	2	2	Inverting input
–IN B	—	—	6	8	5	6	6	Inverting input
–IN C	—	—	—	—	—	9	9	Inverting input
–IN D	—	—	—	—	—	13	13	Inverting input
OUT	1	4	—	—	—	—	—	Output
OUT A	—	—	1	1	8	1	1	Output
OUT B	—	—	7	9	6	7	7	Output
OUT C	—	—	—	—	—	8	8	Output
OUT D	—	—	—	—	—	14	14	Output
SHDN A	—	—	—	5	2	—	—	Shutdown (logic low), enable (logic high)
SHDN B	—	—	—	6	3	—	—	Shutdown (logic low), enable (logic high)
V+	5	5	8	10	7	4	4	Positive supply
V–	2	2	4	4	1	11	11	Negative supply or ground (for single-supply operation)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage				7	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	V
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted).

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
V_S	Supply voltage	1.8	5.5	V
	Specified temperature	–40	125	°C

6.4 Thermal Information: OPA316

THERMAL METRIC(1)		OPA316		UNIT
		DBV (SOT23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	221.7	263.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance(3)	144.7	75.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	49.7	51	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	26.1	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	49	50.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

Thermal Information: OPA316 (continued)

THERMAL METRIC(1)		OPA316		UNIT
		DBV (SOT23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance(7)	N/A	N/A	°C/W

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Thermal Information: OPA2316

THERMAL METRIC(1)		OPA2316			UNIT
		D (SO)	DGK (MSOP)	DRG (DFN)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	127.2	186.6	56.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance(3)	71.6	78.8	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	68.2	107.9	31	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	22	15.5	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	67.6	106.3	21.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance(7)	N/A	N/A	10.9	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.6 Thermal Information: OPA2316S

THERMAL METRIC(1)		OPA2316S		UNIT
		DGS (MSOP)	QFN (RUG)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	189.6	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance(3)	73.9	52	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	110.7	88	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	13.4	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	109.1	87	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance(7)	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.7 Thermal Information: OPA4316

THERMAL METRIC(1)		OPA4316		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	117.2	87.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance(3)	46.2	44.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	58.9	41.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	4.9	11.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	58.3	41.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance(7)	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.8 Electrical Characteristics

V_S (total supply voltage) = (V+) – (V–) = 1.8 V to 5.5 V.
at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.5	±2.5	mV
		V_S = 5 V, T_A = –40°C to 125°C			±3.5	mV
dV_{OS}/dT	Drift	V_S = 5 V, T_A = –40°C to 125°C		±2	±10	µV/°C
PSRR	vs power supply	V_S = 1.8 V – 5.5 V, V_{CM} = (V–)		±30	±150	µV/V
		V_S = 1.8 V – 5.5 V, V_{CM} = (V–), T_A = –40°C to 125°C			±250	µV/V
	Channel separation, dc	At dc		10		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	V_S = 1.8 V to 2.5 V	(V–) – 0.2		(V+)	V
		V_S = 2.5 V to 5.5 V	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V–) – 0.2 V < V_{CM} < (V+) – 1.4 V, T_A= –40°C to 125°C	70	86		dB
		V_S = 5.5 V, (V–) – 0.2 V < V_{CM} < (V+) – 1.4 V, T_A= –40°C to 125°C	76	90		dB
		V_S = 1.8 V, V_{CM} = –0.2 V to 1.8 V, T_A= –40°C to 125°C	57	72		dB
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V, T_A= –40°C to 125°C	65	80		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±5	±15	pA
		T_A= –40°C to 125°C			±15	nA
I_{OS}	Input offset current			±2	±15	pA
		T_A= –40°C to 125°C			±8	nA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		3		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 1 kHz		11		nV/√Hz
i_n	Input current noise density	f = 1 kHz		1.3		fA/√Hz
INPUT IMPEDANCE						
Z_{ID}	Differential			2 || 2		$10^{16}\Omega$ || pF
Z_{IC}	Common-mode			2 || 4		$10^{11}\Omega$ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ	94	100		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	104	110		dB
		V_S = 1.8 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 2 kΩ	90	96		dB
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ	100	106		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ, T_A= –40°C to 125°C	86			dB
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ, T_A= –40°C to 125°C	84			dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5 V, G = +1		10		MHz
φ_m	Phase margin	V_S = 5 V, G = +1		60		Degrees
SR	Slew rate	V_S = 5 V, G = +1		6		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF		1		µs
		To 0.01%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF		1.66		µs
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain = V_S		0.3		µs
THD + N	Total harmonic distortion + noise(1)	V_S = 5 V, V_O = 0.5 V_{RMS}, G = +1, f = 1 kHz		0.0008%		

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics (continued)

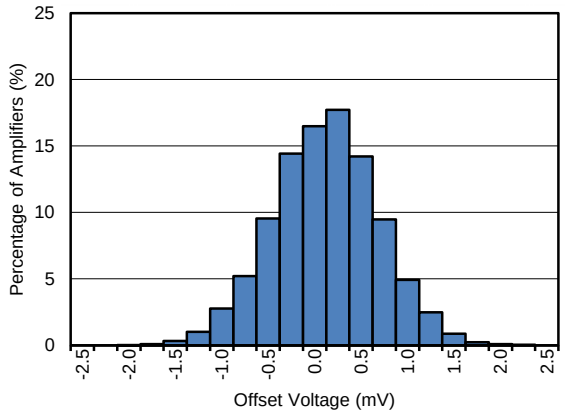
V_S (total supply voltage) = (V+) – (V–) = 1.8 V to 5.5 V.
at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 1.8 V, R_L = 10 kΩ, T_A= –40°C to 125°C			15	mV
		V_S = 5.5 V, R_L = 10 kΩ, T_A= –40°C to 125°C			30	mV
		V_S = 1.8 V, R_L = 2 kΩ, T_A= –40°C to 125°C			60	mV
		V_S = 5.5 V, R_L = 2 kΩ, T_A= –40°C to 125°C			120	mV
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		250		Ω
POWER SUPPLY						
V_S	Specified voltage		1.8		5.5	V
I_Q	Quiescent current per amplifier	V_S = 5 V, I_O = 0 mA, T_A= –40°C to 125°C		400	500	µA
	Power-on time	V_S = 0 V to 5.5 V		200		µs
SHUTDOWN (V_S = 1.8 V to 5.5 V)(2)						
I_{QSD}	Quiescent current, per device	All amplifiers disabled, $\overline{SHDN}$ = $V_{S–}$		0.01	1	µA
		One amplifier disabled (OPA2316S)		345		µA
V_{IH}	High voltage (enabled)	Amplifier enabled	(V+) – 0.5			V
V_{IL}	Low voltage (disabled)	Amplifier disabled			(V–) + 0.2	V
t_{ON}	Amplifier enable time(3)	Full shutdown, G = 1, V_{OUT} = 0.9 × V_S / 2(4)		13		µs
		Partial shutdown, G = 1, V_{OUT} = 0.9 × V_S / 2(4)		10		µs
t_{OFF}	Amplifier disable time(3)	G = 1, V_{OUT} = 0.1 × V_S / 2		5		µs
	$\overline{SHDN}$ pin input bias current (per pin)	V_{IH} = 5 V		3.5		pA
		V_{IL} = 0 V		2.5		pA
TEMPERATURE						
	Specified temperature		–40		125	°C
T_A	Operating temperature		–55		150	°C
T_{stg}	Storage temperature		–65		150	°C

(2) Ensured by design and characterization; not production tested.
(3) Enable time (t_{ON}) and disable time (t_{OFF}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(4) Full shutdown refers to the dual OPA2316S having both channels A and B disabled ($\overline{SHDN\_A}$ = $\overline{SHDN\_B}$ = $V_{S–}$). For partial shutdown, only one $\overline{SHDN}$ pin is exercised; in partial mode, the internal biasing and oscillator remain operational and the enable time is shorter.

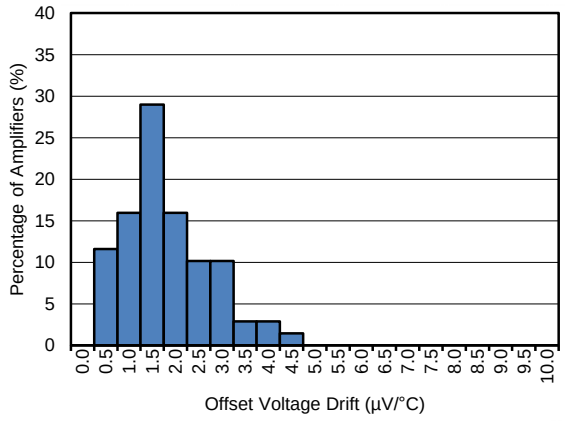
6.9 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



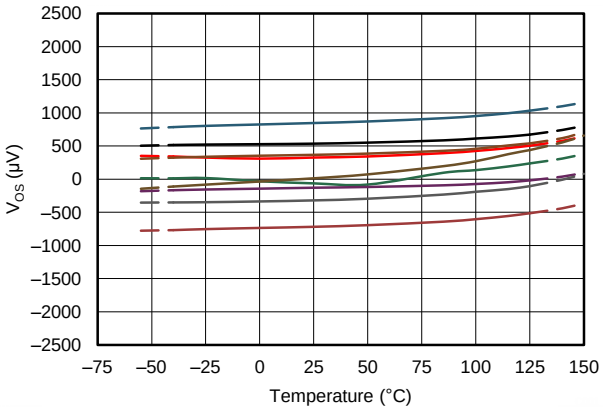
Distribution taken from 12551 amplifiers

Figure 1. Offset Voltage Production Distribution



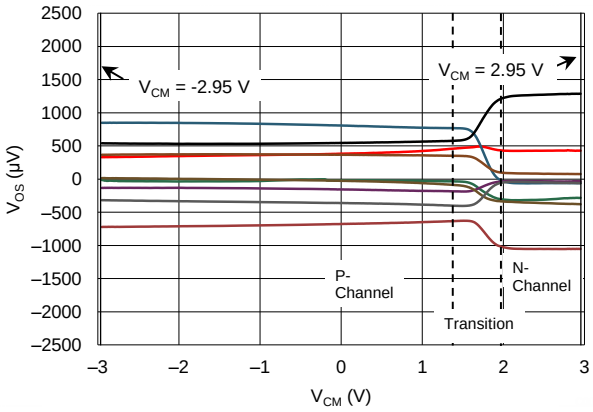
T_A = –40°C to +125°C, Distribution taken from 70 amplifiers

Figure 2. Offset Voltage Drift Distribution



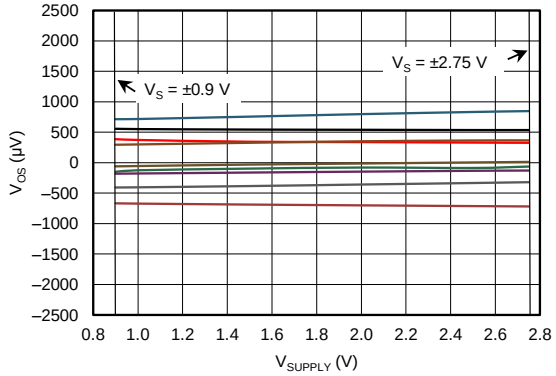
9 typical units shown

Figure 3. Offset Voltage vs Temperature



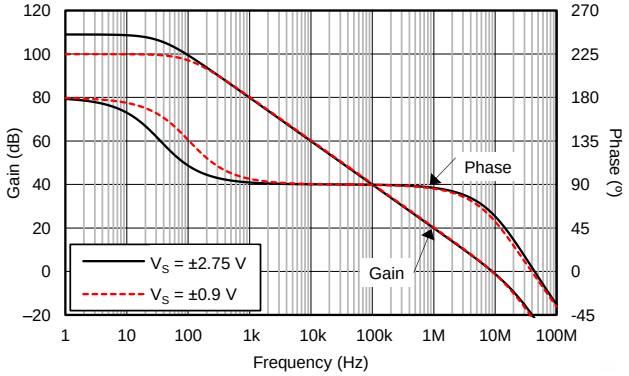
V+ = 2.75 V, V– = –2.75 V, 9 typical units shown

Figure 4. Offset Voltage vs Common-Mode Voltage



V+ = 0.9 V to 2.75 V, V– = –0.9 V to –2.75 V,
9 typical units shown

Figure 5. Offset Voltage vs Power Supply



V_{CM} < (V+) – 1.4 V

Figure 6. Open-Loop Gain and Phase vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

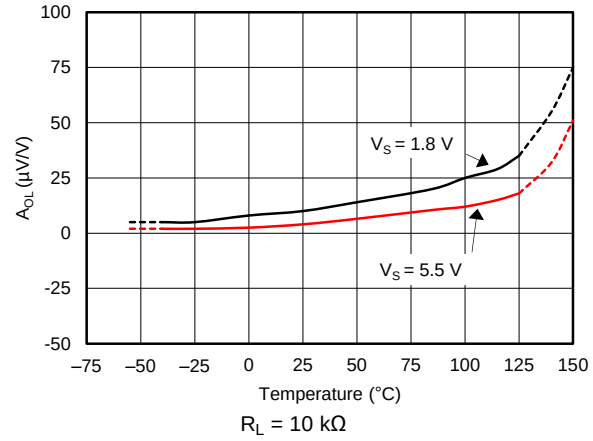


Figure 7. Open-Loop Gain vs Temperature

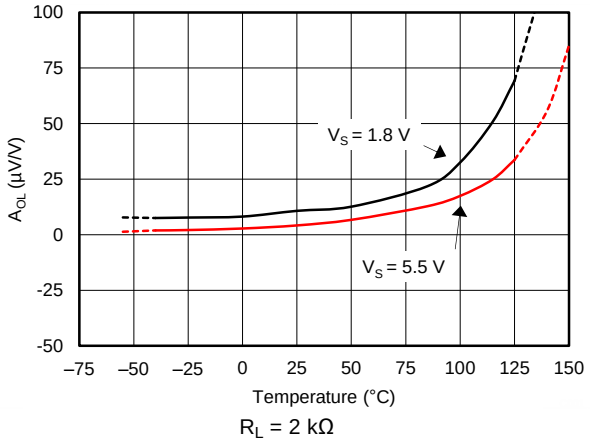


Figure 8. Open-Loop Gain vs Temperature

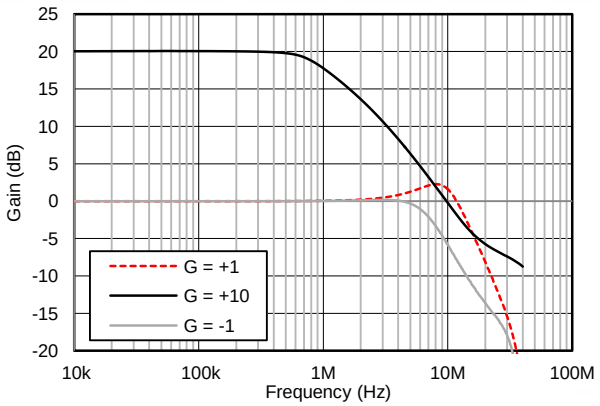


Figure 9. Closed-Loop Gain vs Frequency

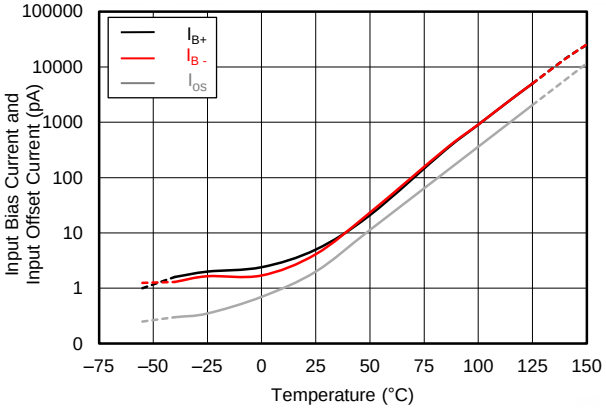


Figure 10. Input Bias and Offset Current vs Temperature

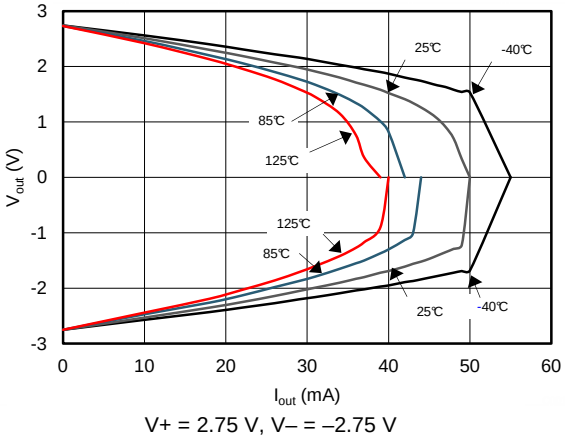


Figure 11. Output Voltage Swing vs Output Current

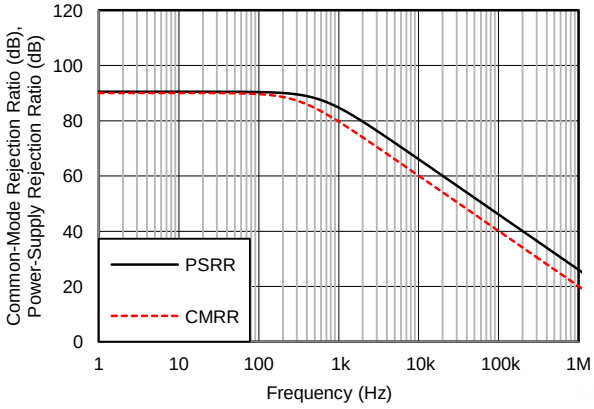


Figure 12. CMRR and PSRR vs Frequency (Referred to Input)

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

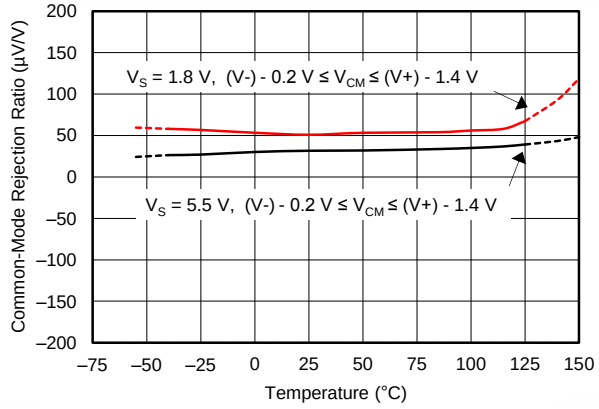


Figure 13. CMRR vs Temperature (Narrow Range)

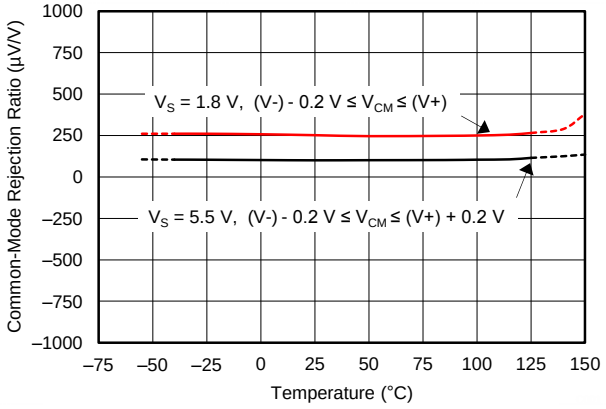


Figure 14. CMRR vs Temperature (Wide Range)

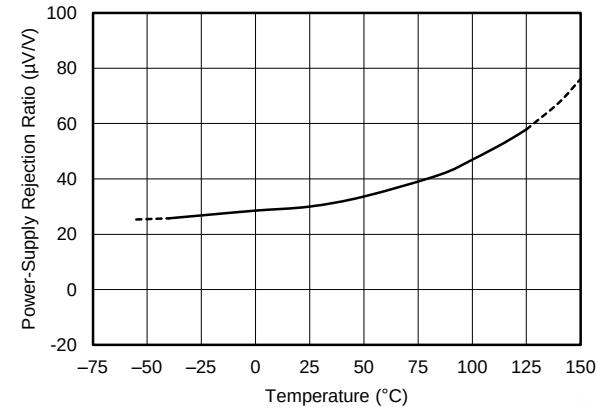


Figure 15. PSRR vs Temperature

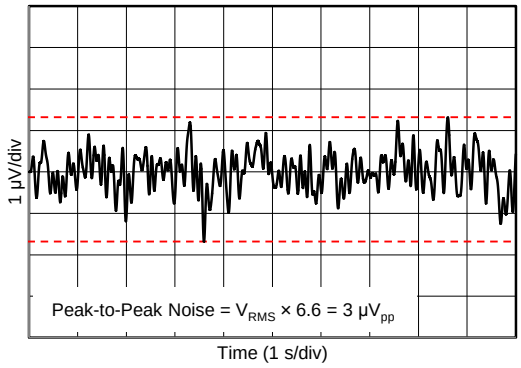


Figure 16. 0.1-Hz to 10-Hz Input Voltage Noise

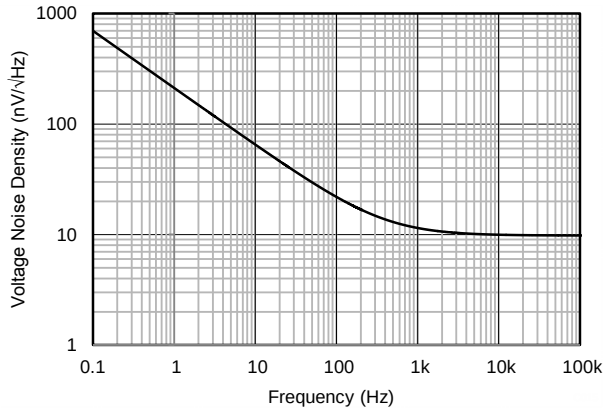


Figure 17. Input Voltage Noise Spectral Density vs Frequency

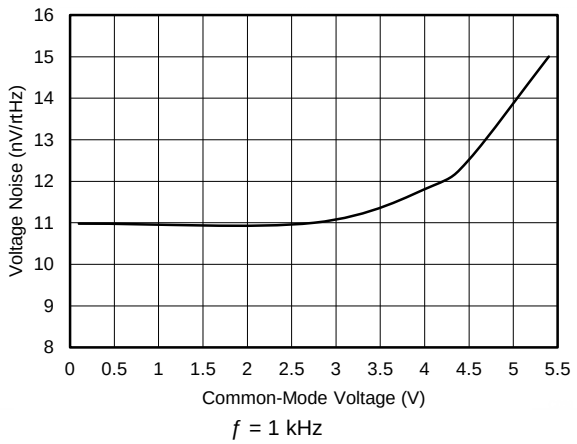
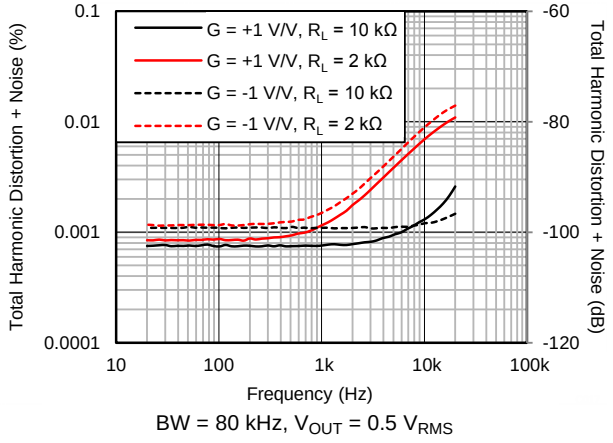


Figure 18. Input Voltage Noise vs Common-Mode Voltage

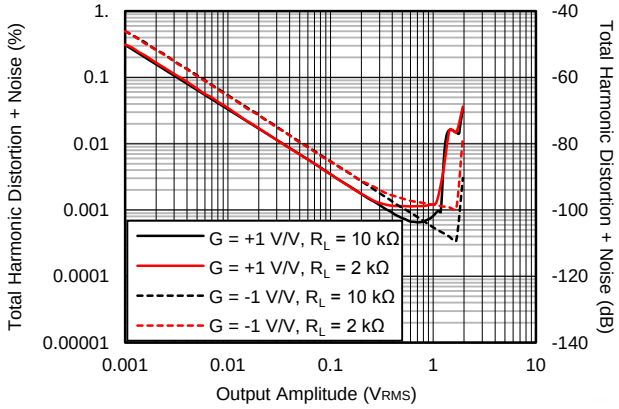
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



BW = 80 kHz, V_{OUT} = 0.5 V_{RMS}

Figure 19. THD + N vs Frequency



f = 1 kHz, BW = 80 kHz

Figure 20. THD + N vs Amplitude

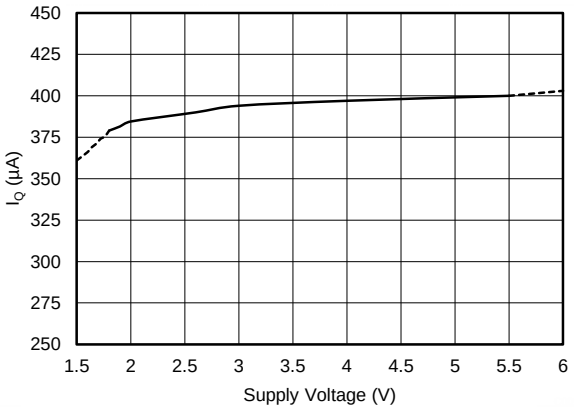


Figure 21. Quiescent Current vs Supply Voltage

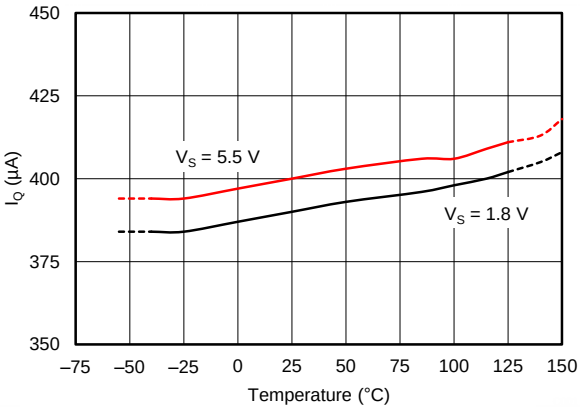


Figure 22. Quiescent Current vs Temperature

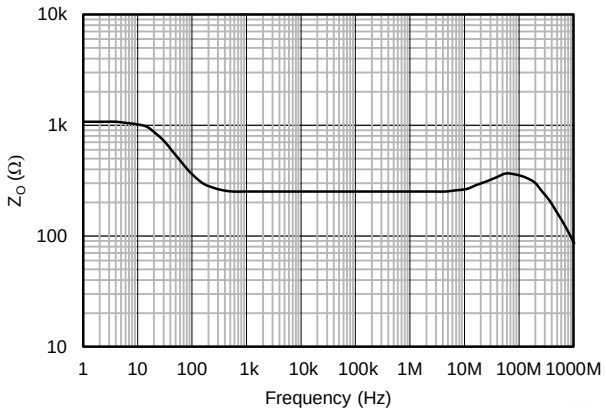
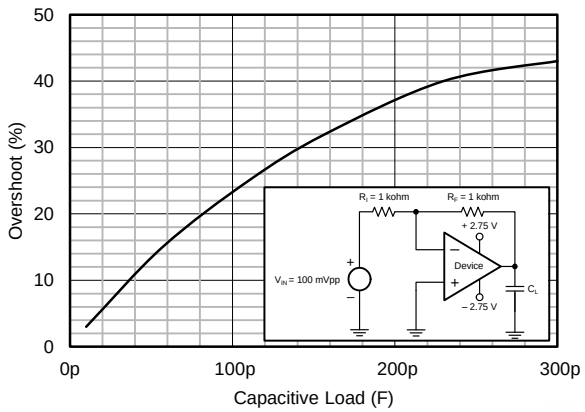


Figure 23. Open-Loop Output Impedance vs Frequency

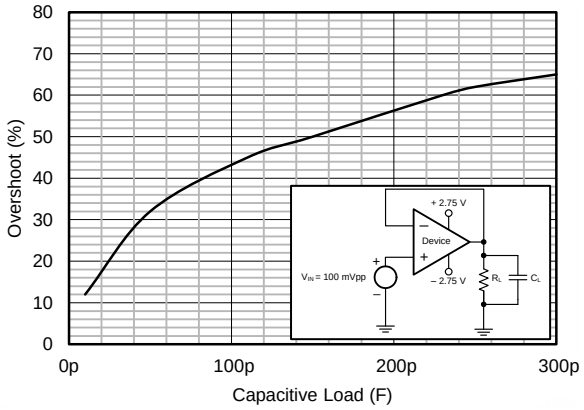


V+ = 2.75 V, V– = –2.75 V, G = –1 V/V

Figure 24. Small-Signal Overshoot vs Load Capacitance

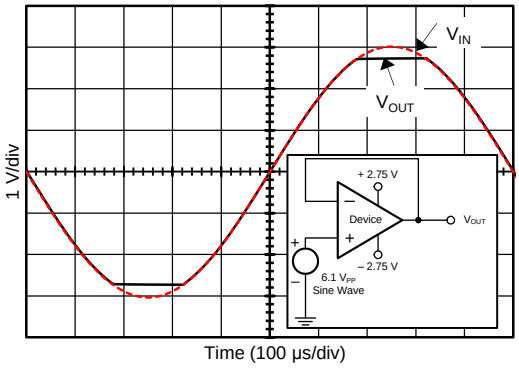
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



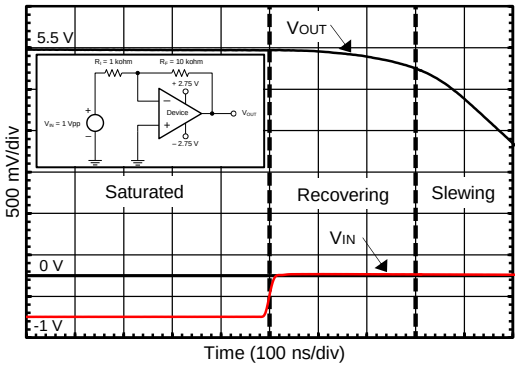
V+ = 2.75 V, V– = –2.75 V , G = +1 V/V, R_L = 1 kΩ

Figure 25. Small-Signal Overshoot vs Load Capacitance



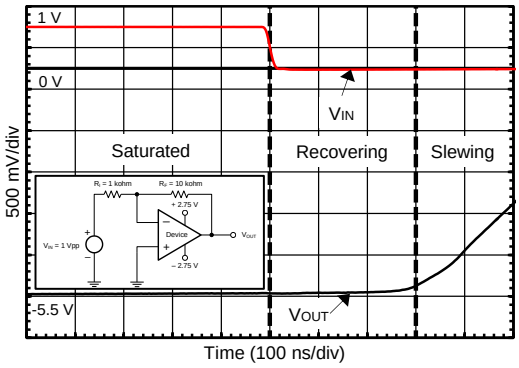
V+ = 2.75 V, V– = –2.75 V

Figure 26. No Phase Reversal



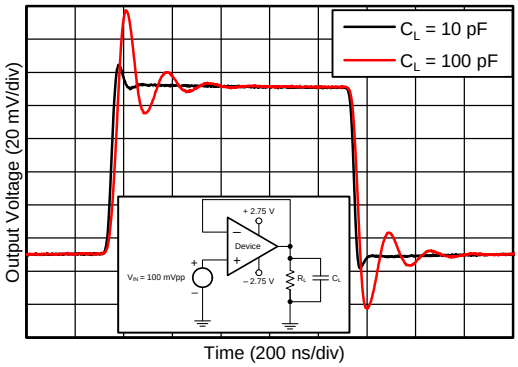
V+ = 2.75 V, V– = –2.75 V , G = –10 V/V

Figure 27. Positive Overload Recovery



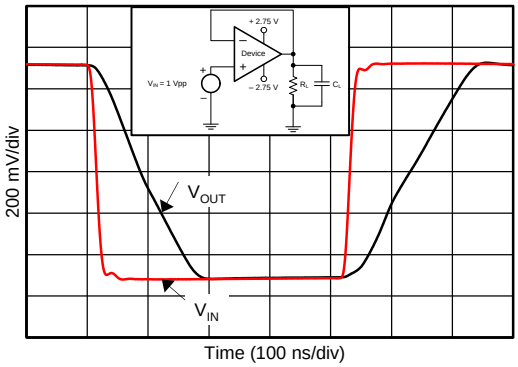
V+ = 2.75 V, V– = –2.75 V, G = –10 V/V

Figure 28. Negative Overload Recovery



V+ = 2.75 V, V– = –2.75 V, G = +1 V/V

Figure 29. Small-Signal Step Response

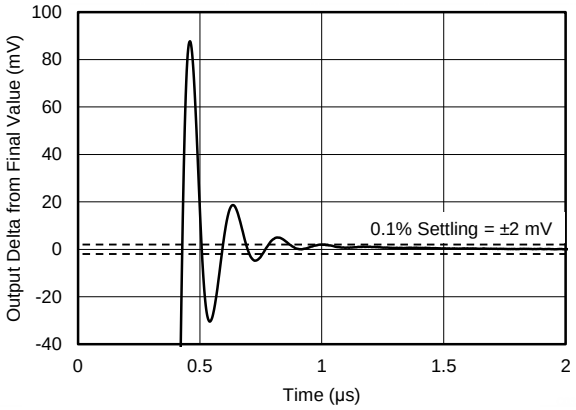


V+ = 2.75 V, V– = –2.75 V, C_L = 100 pF, G = +1 V/V

Figure 30. Large-Signal Step Response

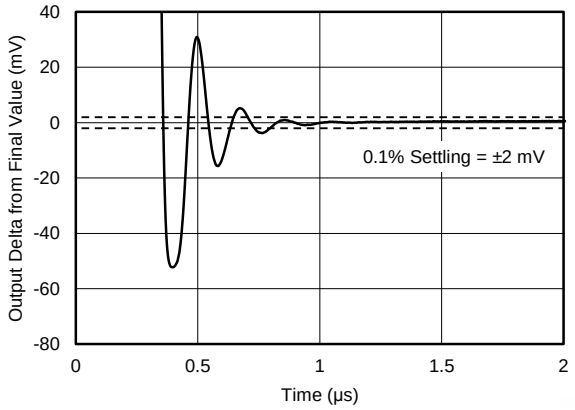
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



C_L = 100 pF, G = +1 V/V

Figure 31. Positive Large-Signal Settling Time



C_L = 100 pF, G = +1 V/V

Figure 32. Negative Large-Signal Settling Time

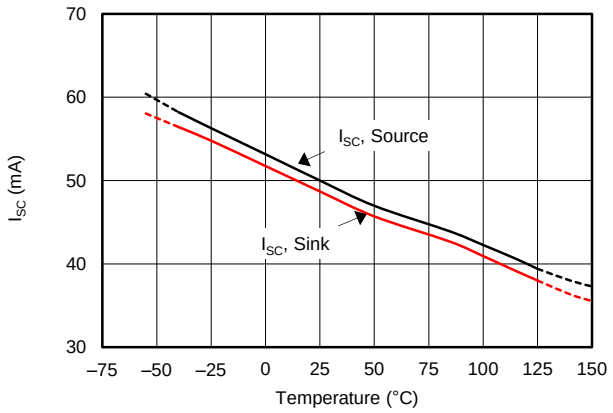


Figure 33. Short-Circuit Current vs Temperature

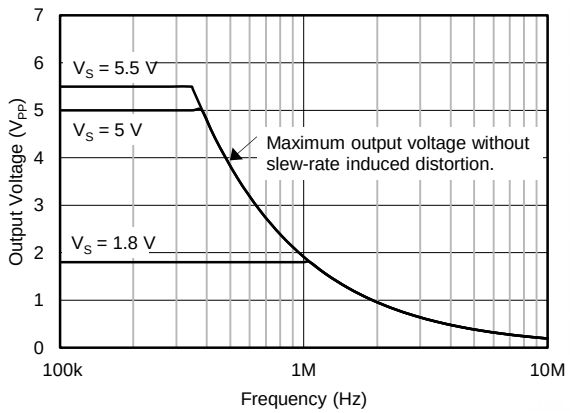
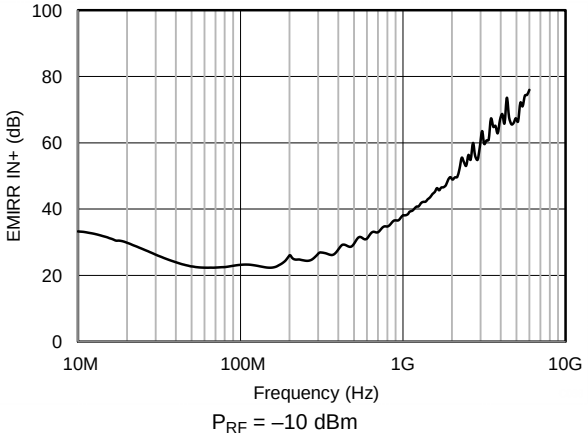
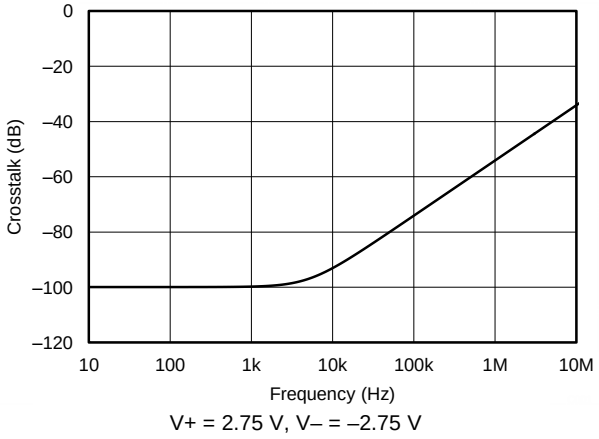


Figure 34. Maximum Output Voltage vs Frequency and Supply Voltage



P_{RF} = –10 dBm

Figure 35. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR IN+) vs Frequency



V+ = 2.75 V, V– = –2.75 V

Figure 36. Channel Separation vs Frequency

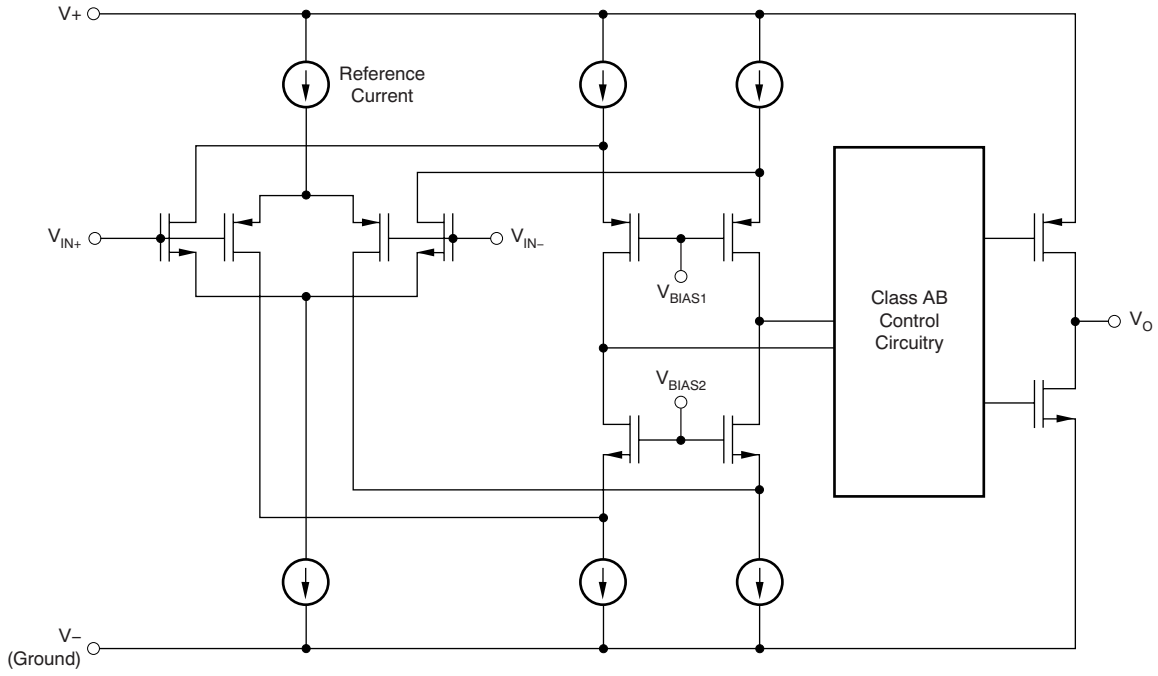
7 Detailed Description

7.1 Overview

The OPA316 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving less than or equal to 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails and allows the OPA316 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

The OPA316 family features 10-MHz bandwidth and 6-V/μs slew rate with only 400-μA supply current per channel, providing good ac performance at very-low power consumption. DC applications are well served with a very-low input noise voltage of 11 nV/√Hz at 1 kHz, low input bias current (5 pA), and an input offset voltage of 0.5 mV (typical).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPAx316 operational amplifiers are fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the *Typical Characteristics* graphs.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPAx316 series extends 200 mV beyond the supply rails for supply voltages greater than 2.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative

Feature Description (continued)

supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

7.3.3 Input and ESD Protection

The OPAx316 incorporates internal ESD protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in *Absolute Maximum Ratings*. Figure 37 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

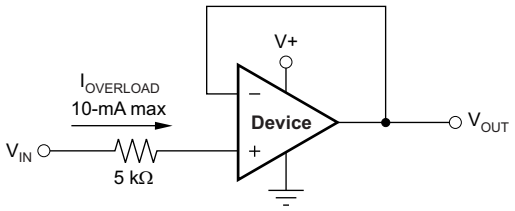


Figure 37. Input Current Protection

7.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the OPAx316 is specified in several ways so the user can select the best match for a given application, as shown in *Electrical Characteristics*. First, the data sheet gives the CMRR of the device in the common-mode range below the transition region [V_{CM} < (V+) – 1.4 V]. This specification is the best indicator of device capability when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at V_{CM} = –0.2 V to 5.7 V for V_S = 5.5 V. This last value includes the variations shown in Figure 4 through the transition region.

7.3.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The OPA316 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. This filter provides both common-mode and differential-mode filtering. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

TI developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared by the EMI immunity. Figure 35 illustrates the results of this testing on the OPA316 series. For more information, see *EMI Rejection Ratio of Operational Amplifiers* (SBOA128).

7.3.6 Rail-to-Rail Output

Designed as a low-power, low-noise operational amplifier, the OPAx316 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads of 10-kΩ, the output swings typically to within 30 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; see the typical characteristic graph *Output Voltage Swing vs Output Current* (Figure 11).

Feature Description (continued)

7.3.7 Capacitive Load and Stability

The OPAx316 is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the OPAx316 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (+1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. As a conservative best practice, designing for 25% overshoot (40° phase margin) provides improved stability over process variations. The equivalent series resistance (ESR) of some very-large capacitors (C_L greater than 1 μF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See the typical characteristic graphs, *Small-Signal Overshoot vs Capacitive Load* (Figure 24, G = –1 V/V) and *Small-Signal Overshoot vs Capacitive Load* (Figure 25, G = +1 V/V).

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10 Ω to 20 Ω) in series with the output, as shown in Figure 38. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

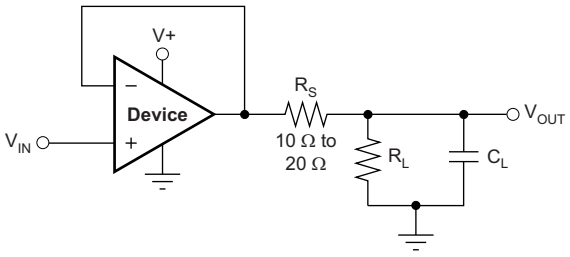


Figure 38. Improving Capacitive Load Drive

7.3.8 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx316 is approximately 300 ns.

7.3.9 DFN Package

The OPA2316 (dual version) device uses the DFN style package (also known as SON); this package is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes printed circuit board (PCB) space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is the low, 0.9-mm height. DFN packages are physically small, have a smaller routing area, improved thermal performance, reduced electrical parasitics, and use a pinout scheme that is consistent with other commonly-used packages, such as SOIC and MSOP). Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be simply mounted using standard PCB assembly techniques. See *QFN/SON PCB Attachment* (SLUA271) , and *Quad Flatpack No-Lead Logic Packages* (SCBA017).

Feature Description (continued)

NOTE

Connect the exposed lead frame die pad on the bottom of the DFN package to the most negative potential (V–).

7.4 Device Functional Modes

The OPA316, OPA2316, and OPA4316 devices are powered on when the supply is connected. The devices can be operated as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

The OPA2316S device has a SHDN (enable) pin function referenced to the negative supply voltage of the operational amplifier. A logic level high enables the operational amplifier. A valid logic high is defined as voltage [(V+) – 0.1 V], up to (V+), applied to the SHDN pin. A valid logic low is defined as [(V–) + 0.1 V], down to (V–), applied to the enable pin. The maximum allowed voltage applied to SHDN is 5.5 V with respect to the negative supply, independent of the positive supply voltage. Connect this pin to a valid high or a low voltage or driven, but not left as an open circuit.

The logic input is a high-impedance CMOS input. Both inputs are independently controlled. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 General Configurations

When receiving low-level signals, the device often requires limiting the bandwidth of the incoming signals into the system. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting pin of the amplifier, as Figure 39 shows.

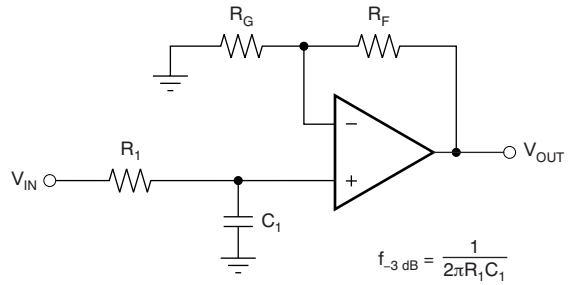


Figure 39. Single-Pole Low-Pass Filter

If even more attenuation is needed, the device requires a multiple-pole filter. The Sallen-Key filter can be used for this task, as Figure 40 shows. For best results, the amplifier must have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

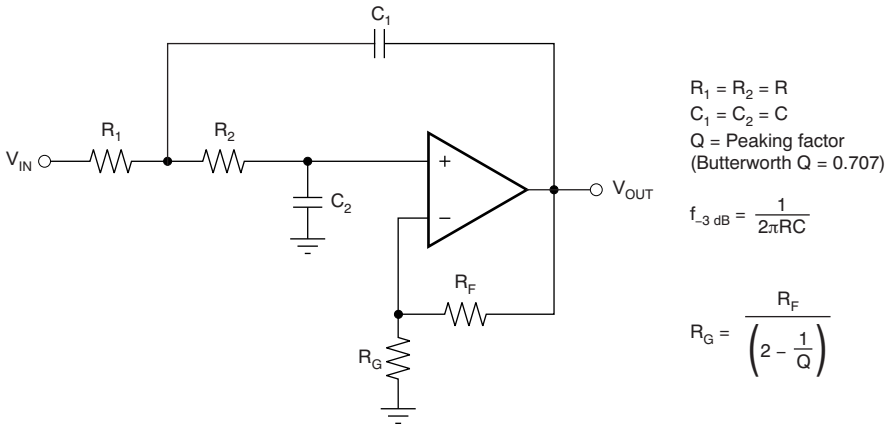


Figure 40. Two-Pole, Low-Pass, Sallen-Key Filter

8.2 Typical Application

Some applications require differential signals. Figure 41 shows a simple circuit to convert a single-ended input of 0.1 V to 2.4 V into a differential output of ±2.3 V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier functions as a buffer and creates a voltage, VOUT+. The second amplifier inverts the input and adds a reference voltage to generate VOUT–. VOUT+ and VOUT– range from 0.1 V to 2.4 V. The difference, VDIFF, is the difference between VOUT+ and VOUT– which makes the differential output voltage range 2.3 V.

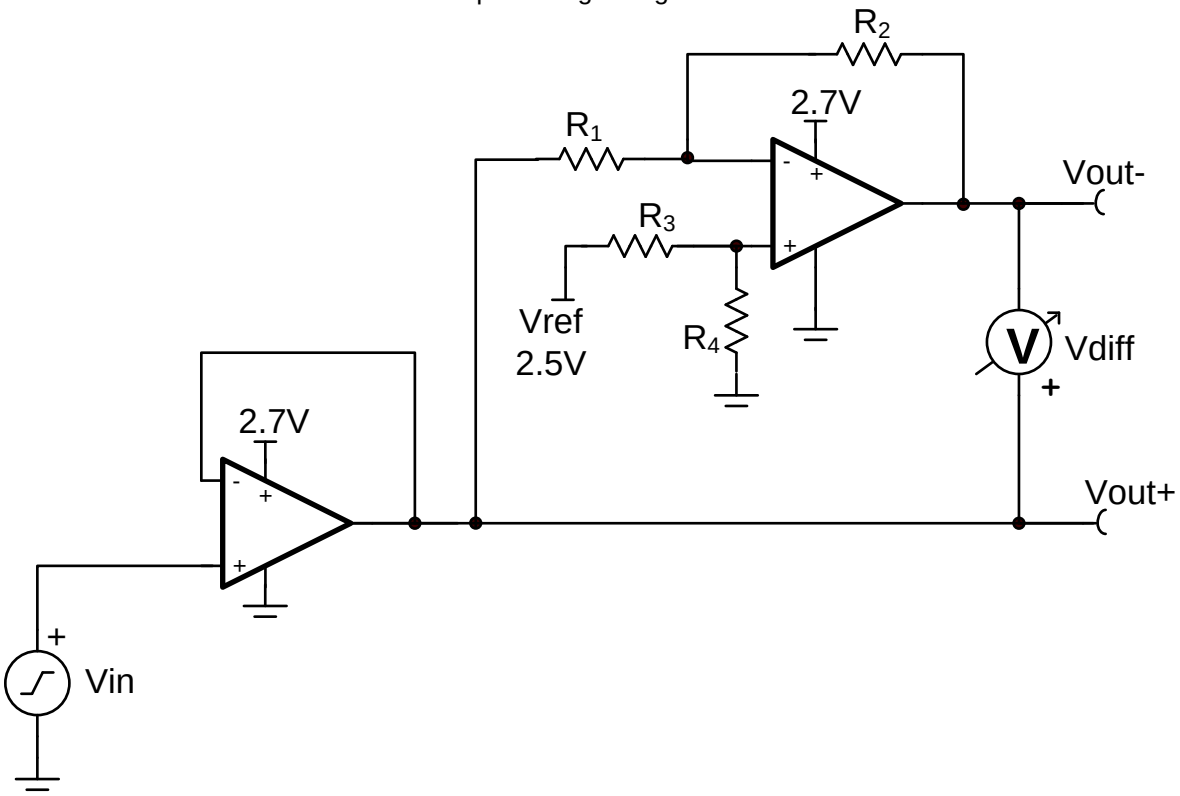


Figure 41. Schematic for a Single-Ended Input to Differential Output Conversion

8.2.1 Design Requirements

Table 1 lists the design requirements:

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Supply voltage	2.7 V
Reference voltage	2.5 V
Input voltage	0.1 V to 2.4 V
Output differential voltage	±2.3 V
Output common-mode voltage	1.25 V
Small-signal bandwidth	5 MHz

8.2.2 Detailed Design Procedure

The circuit in Figure 41 takes a single-ended input signal, VIN, and generates two output signals, VOUT+ and VOUT– using two amplifiers and a reference voltage, VREF. VOUT+ is the output of the first amplifier and is a buffered version of the input signal, VIN (as shown in Equation 1). VOUT– is the output of the second amplifier which uses VREF to add an offset voltage to VIN and feedback to add inverting gain. The transfer function for VOUT– is given in Equation 2.

$$V_{out+} = V_{in} \quad (1)$$

$$V_{out-} = V_{ref} \times \left(\frac{R_4}{R_3 + R_4} \right) \times \left(1 + \frac{R_2}{R_1} \right) - V_{in} \times \frac{R_2}{R_1} \quad (2)$$

The differential output signal, VDIFF, is the difference between the two single-ended output signals, VOUT+ and VOUT–. Equation 3 shows the transfer function for VDIFF. Using conditions in Equation 4 and Equation 5 and applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage, and the maximum output of each amplifier is equal to VREF. The differential output range is 2 × VREF. Furthermore, the common-mode voltage is one half of VREF, as shown in Equation 7.

$$V_{diff} = V_{out+} - V_{out-} = V_{in} \times \left(1 + \frac{R_2}{R_1} \right) - V_{ref} \times \left(\frac{R_4}{R_3 + R_4} \right) \times \left(1 + \frac{R_2}{R_1} \right) \quad (3)$$

$$V_{out+} = V_{in} \quad (4)$$

$$V_{out-} = V_{ref} - V_{in} \quad (5)$$

$$V_{diff} = 2 \times V_{in} - V_{ref} \quad (6)$$

$$V_{cm} = \left(\frac{V_{out+} + V_{out-}}{2} \right) = \frac{1}{2} V_{ref} \quad (7)$$

8.2.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common-mode input range and output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design, so the OPAx316 is selected because the bandwidth is greater than the target of 5 MHz. The bandwidth and power ratio makes this device power efficient and the low offset and drift ensure good accuracy for moderate precision applications.

8.2.2.2 Passive Component Selection

Because the transfer function of VOUT– is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design uses resistors with resistance values of 49.9 kΩ and tolerances of 0.1%. However, if the noise of the system is a key parameter, smaller resistance values (6 kΩ or lower) can be selected to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

8.2.3 Application Curves

The measured transfer functions in Figure 42, Figure 43, and Figure 44 are generated by sweeping the input voltage from 0.1 V to 2.4 V. The full input range is actually 0 V to 2.5 V, but is restricted by 0.1 V to maintain optimal linearity. For more details on this design and other alternative devices that can be used in place of the OPAx316, see (*Single-Ended Input to Differential Output Conversion Circuit Reference Design* (TIPD131).

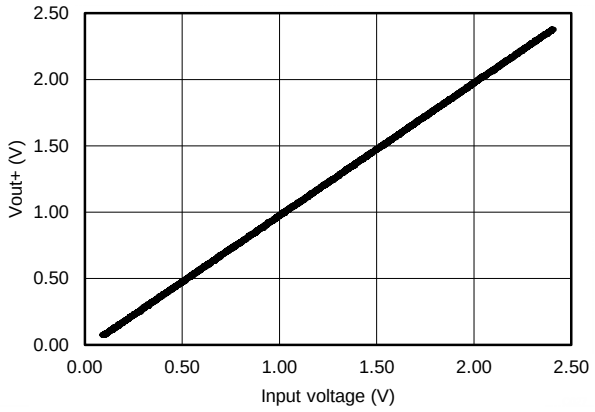


Figure 42. VOUT+ vs Input Voltage

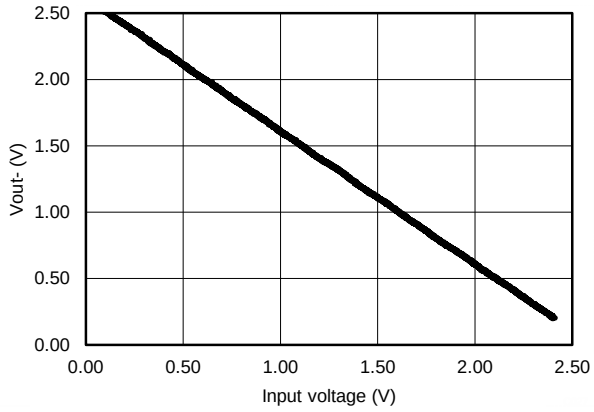


Figure 43. VOUT– vs Input Voltage

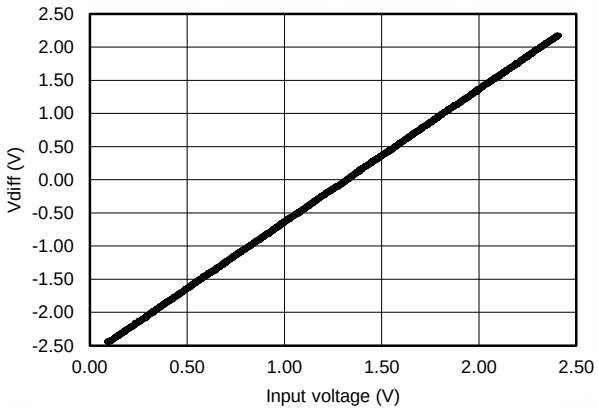


Figure 44. VDIFF vs Input Voltage

9 Power Supply Recommendations

The OPAx316 is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*) table.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more information on bypass capacitor placement, see *Layout Guidelines*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example* .
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

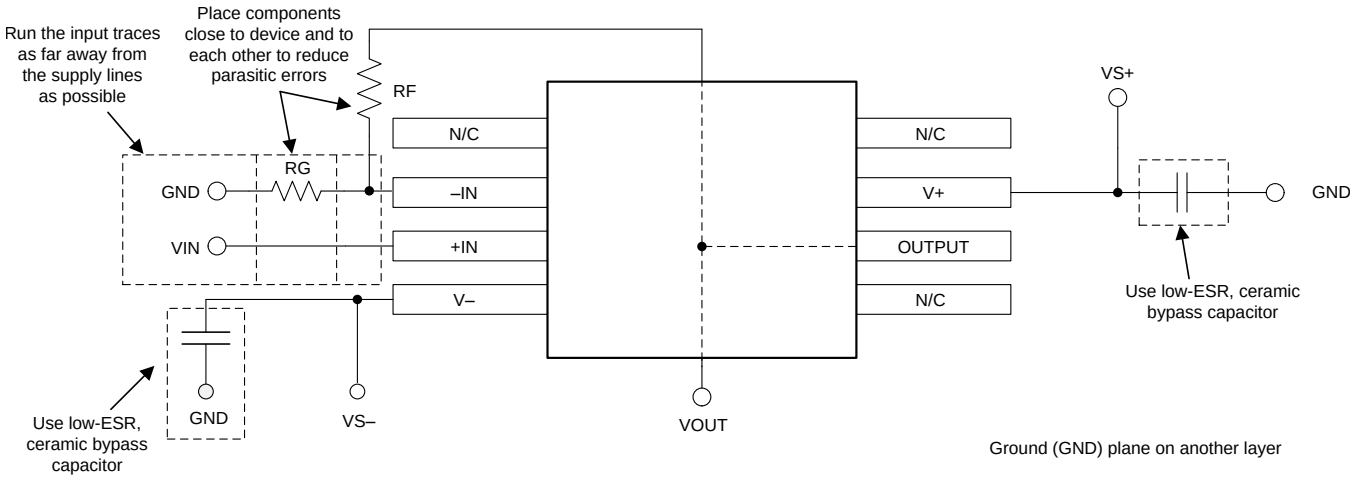


Figure 45. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *EMI Rejection Ratio of Operational Amplifiers* (SBOA128).
- *QFN/SON PCB Attachment* (SLUA271).
- *Quad Flatpack No-Lead Logic Packages* (SCBA017).
- *Single-Ended Input to Differential Output Conversion Circuit Reference Design* (TIPD131).
- *Circuit Board Layout Techniques* (SLOA089).

11.2 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA316	Click here	Click here	Click here	Click here	Click here
OPA2316	Click here	Click here	Click here	Click here	Click here
OPA2316S	Click here	Click here	Click here	Click here	Click here
OPA4316	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2316ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2316	Samples
OPA2316IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OVMQ	Samples
OPA2316IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OVMQ	Samples
OPA2316IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2316	Samples
OPA2316IDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SMD	Samples
OPA2316IDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SMD	Samples
OPA2316SIDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SMG	Samples
OPA2316SIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SMG	Samples
OPA2316SIRUGR	ACTIVE	X2QFN	RUG	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1QU	Samples
OPA2316SIRUGT	ACTIVE	X2QFN	RUG	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1QU	Samples
OPA316IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SLE	Samples
OPA316IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SLE	Samples
OPA316IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLD	Samples
OPA316IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLD	Samples
OPA4316ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4316D	Samples
OPA4316IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4316D	Samples
OPA4316IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4316	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4316IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4316	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

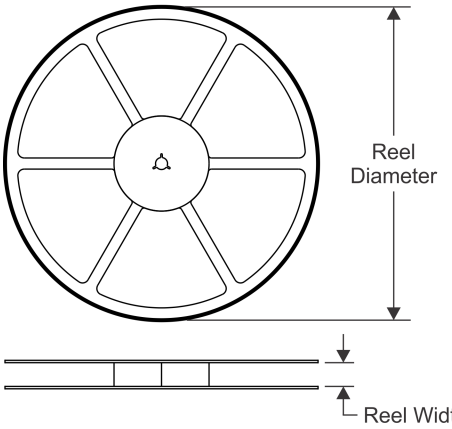
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

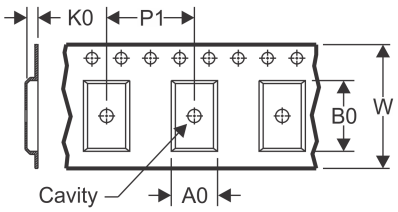
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

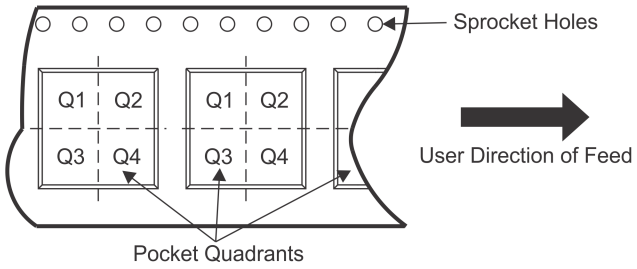


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

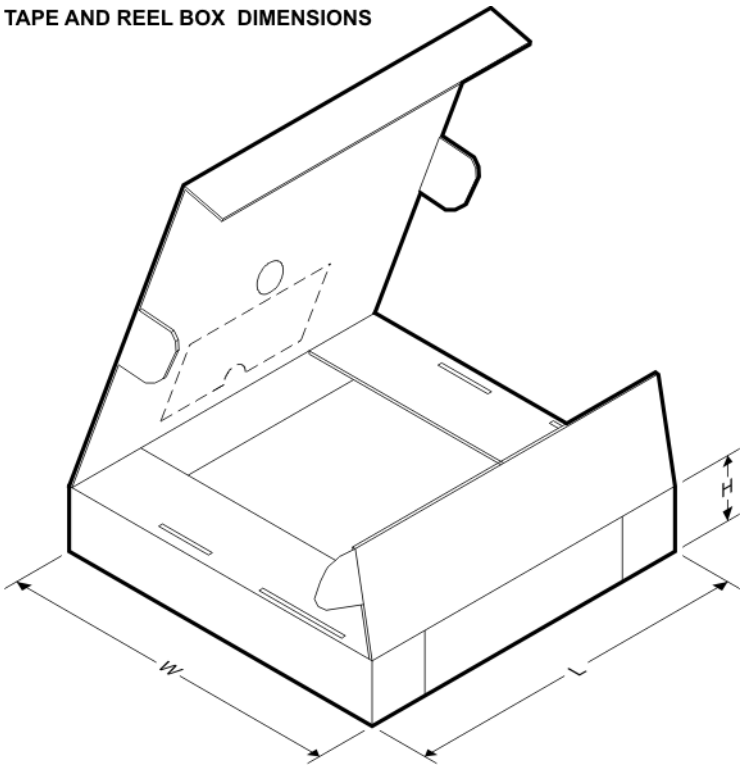
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2316IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2316IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2316IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2316IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2316SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2316SIRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
OPA2316SIRUGT	X2QFN	RUG	10	250	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
OPA316IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA316IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA316IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA316IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA4316IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4316IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

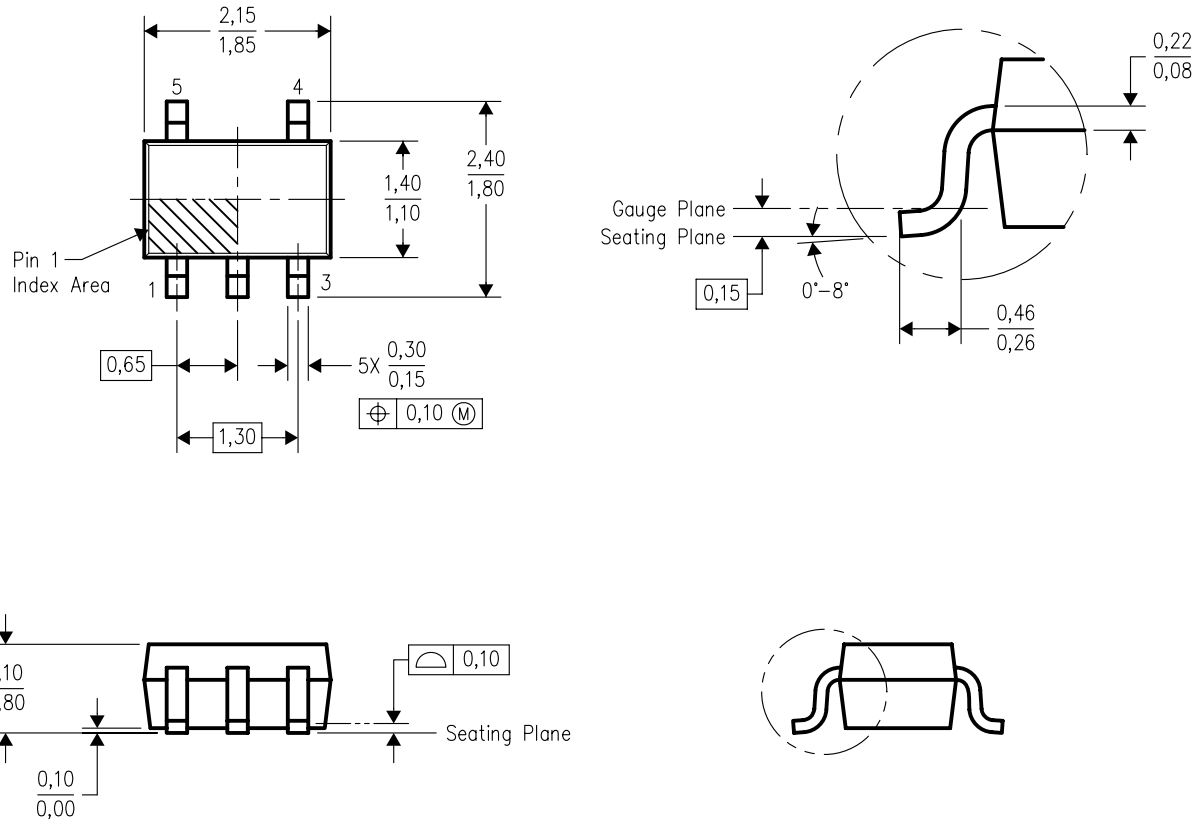
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2316IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2316IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2316IDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA2316IDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA2316SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
OPA2316SIRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
OPA2316SIRUGT	X2QFN	RUG	10	250	210.0	185.0	35.0
OPA316IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA316IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA316IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA316IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
OPA4316IDR	SOIC	D	14	2500	333.2	345.9	28.6
OPA4316IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

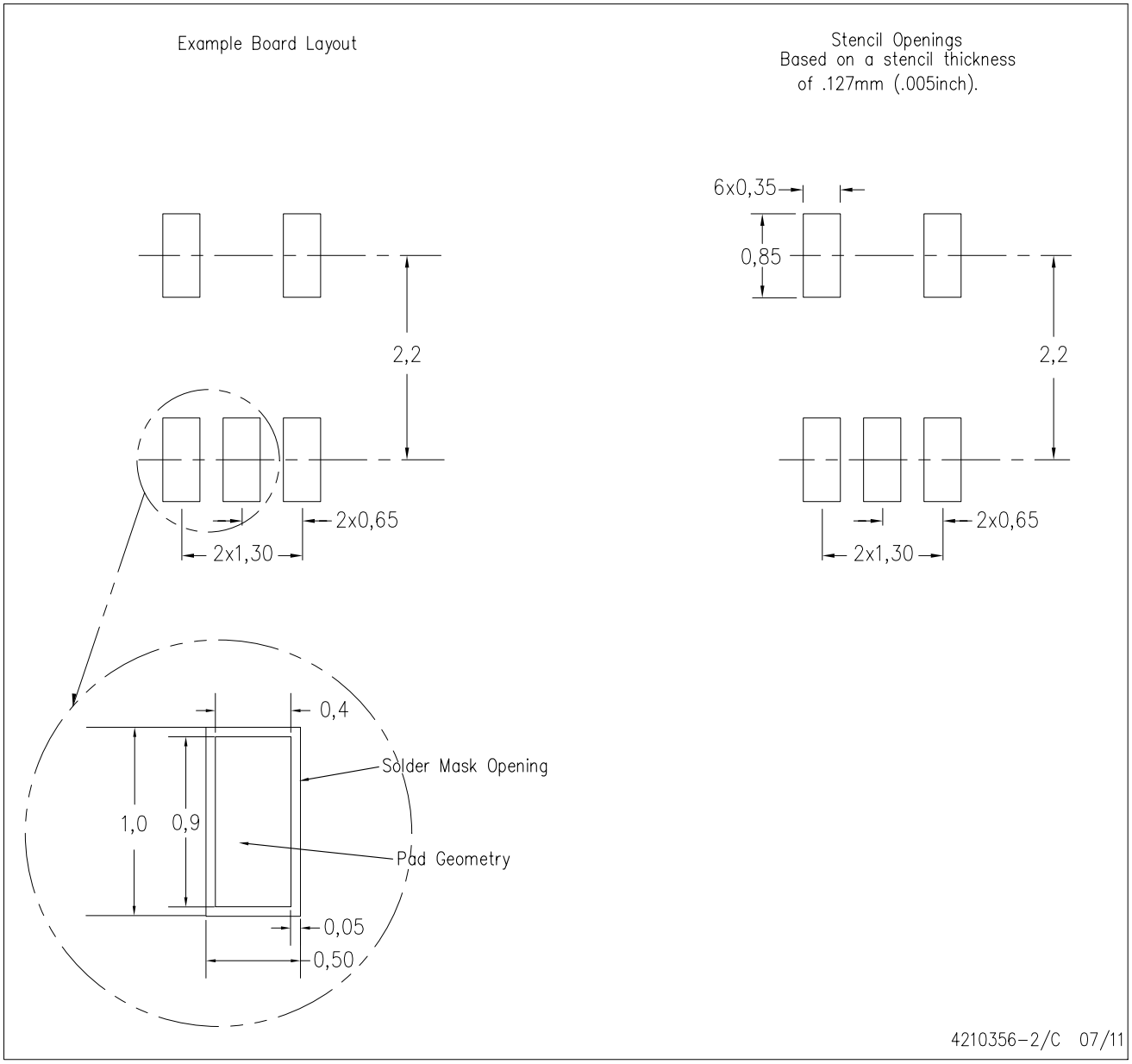
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



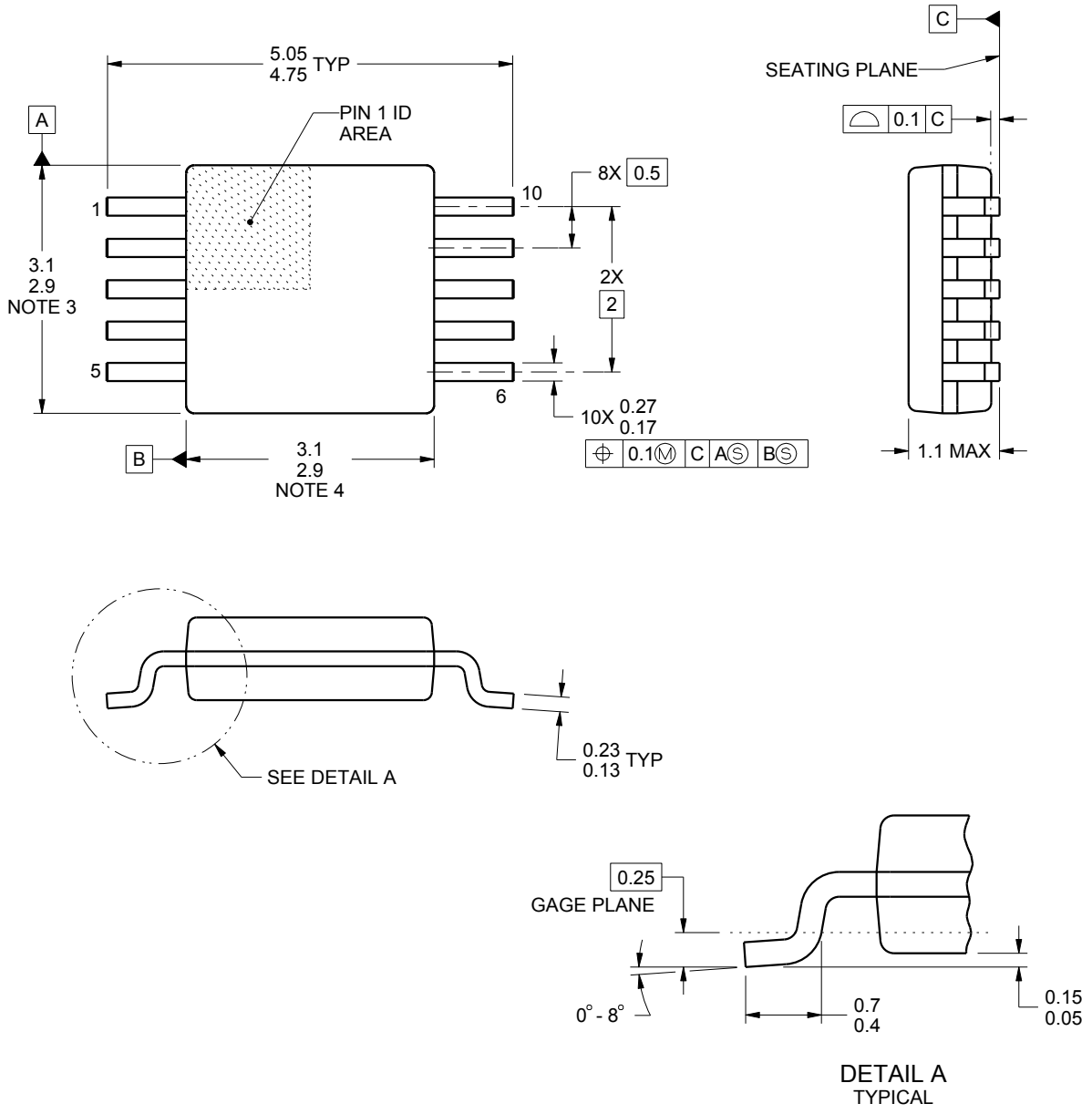
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DGS0010A

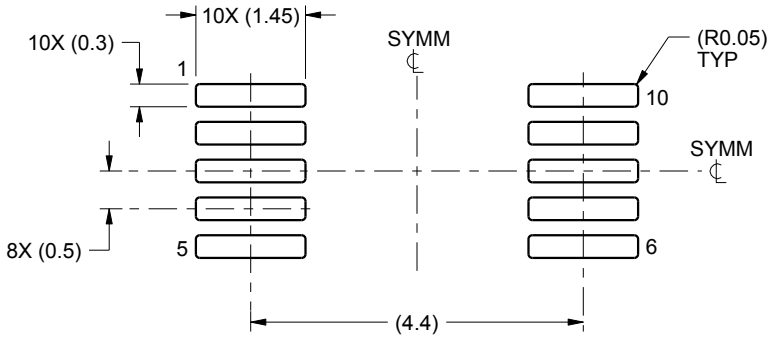
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

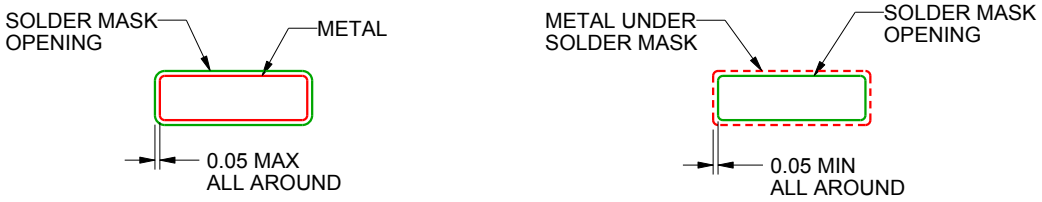


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

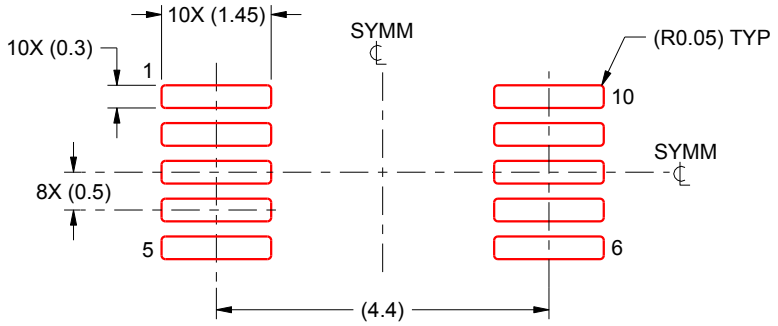


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



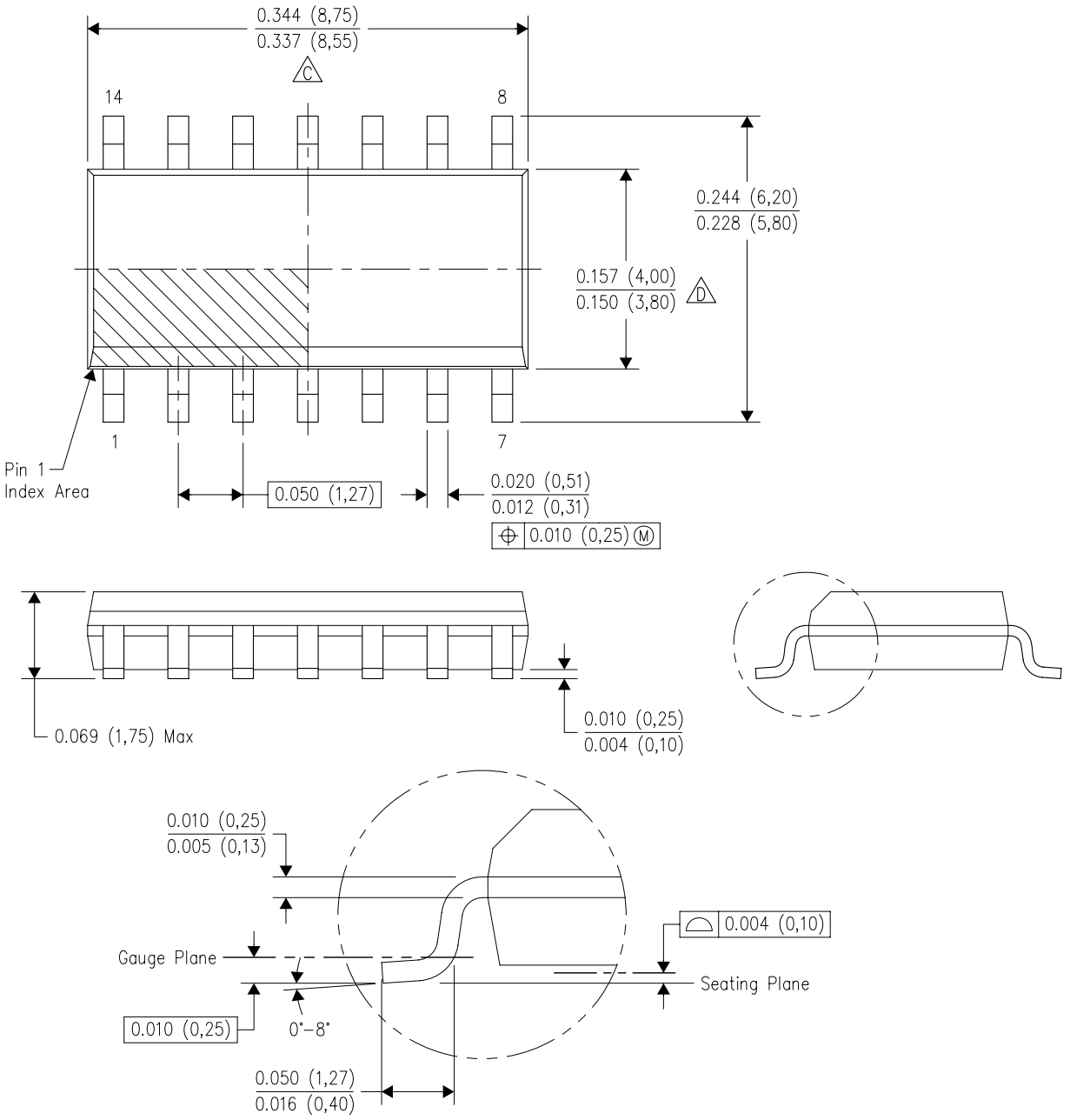
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

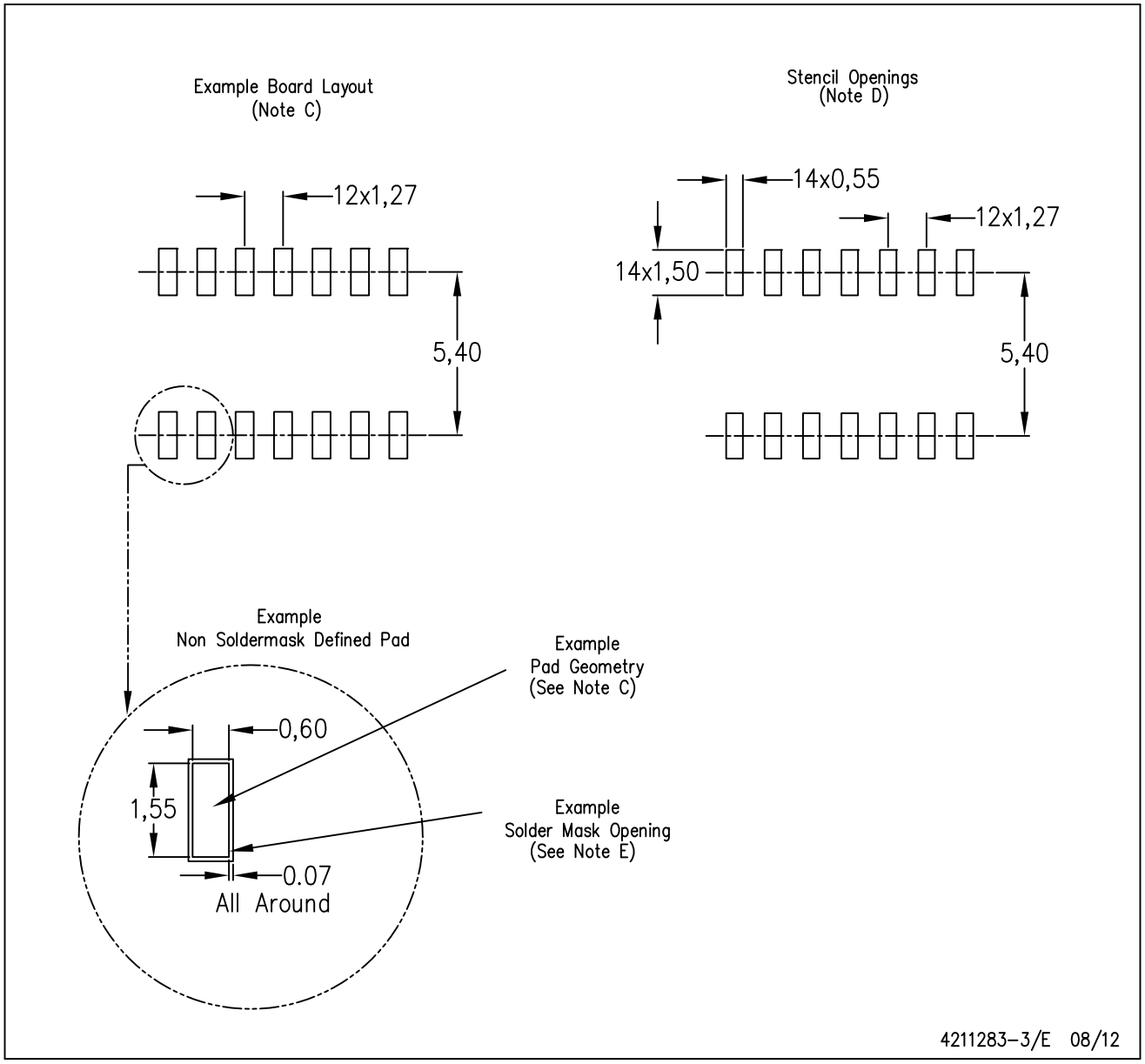
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

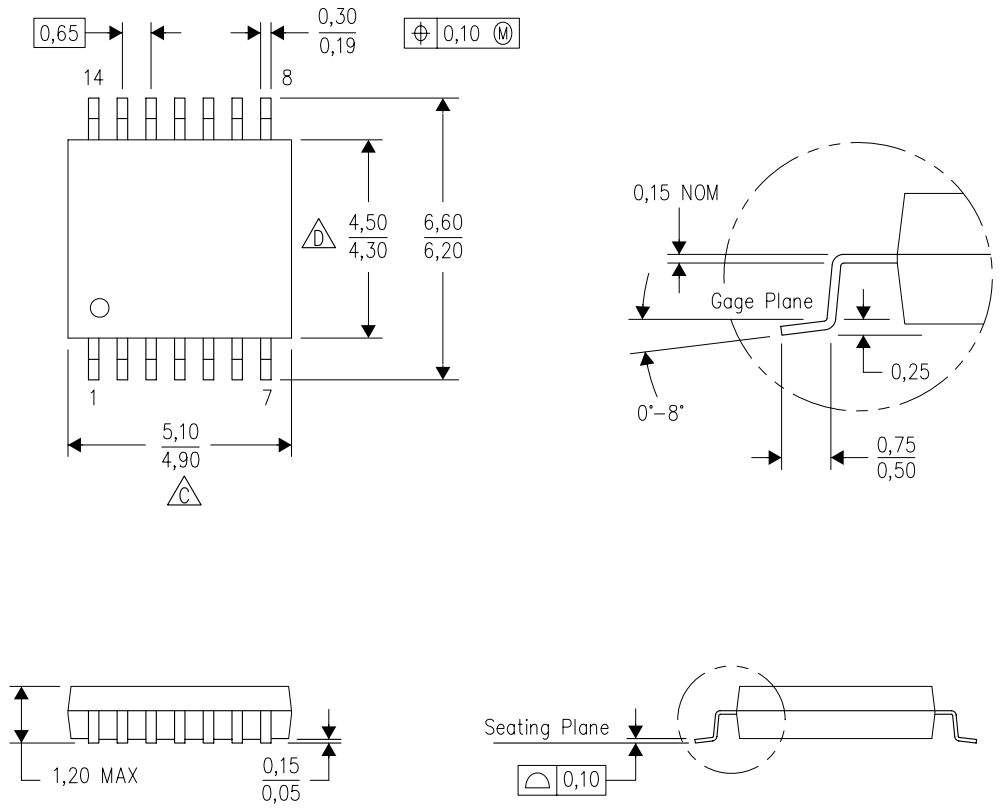
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

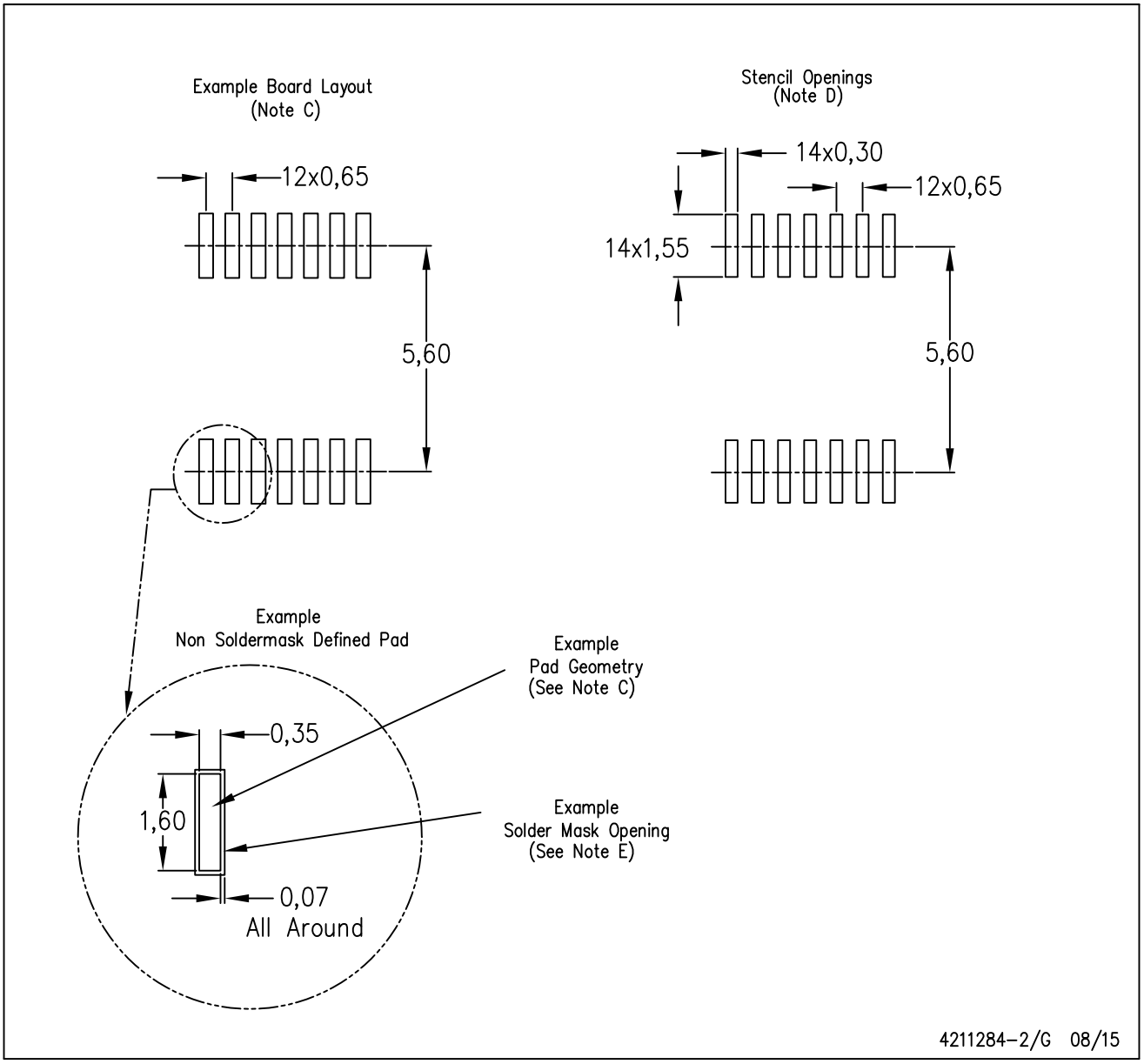
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

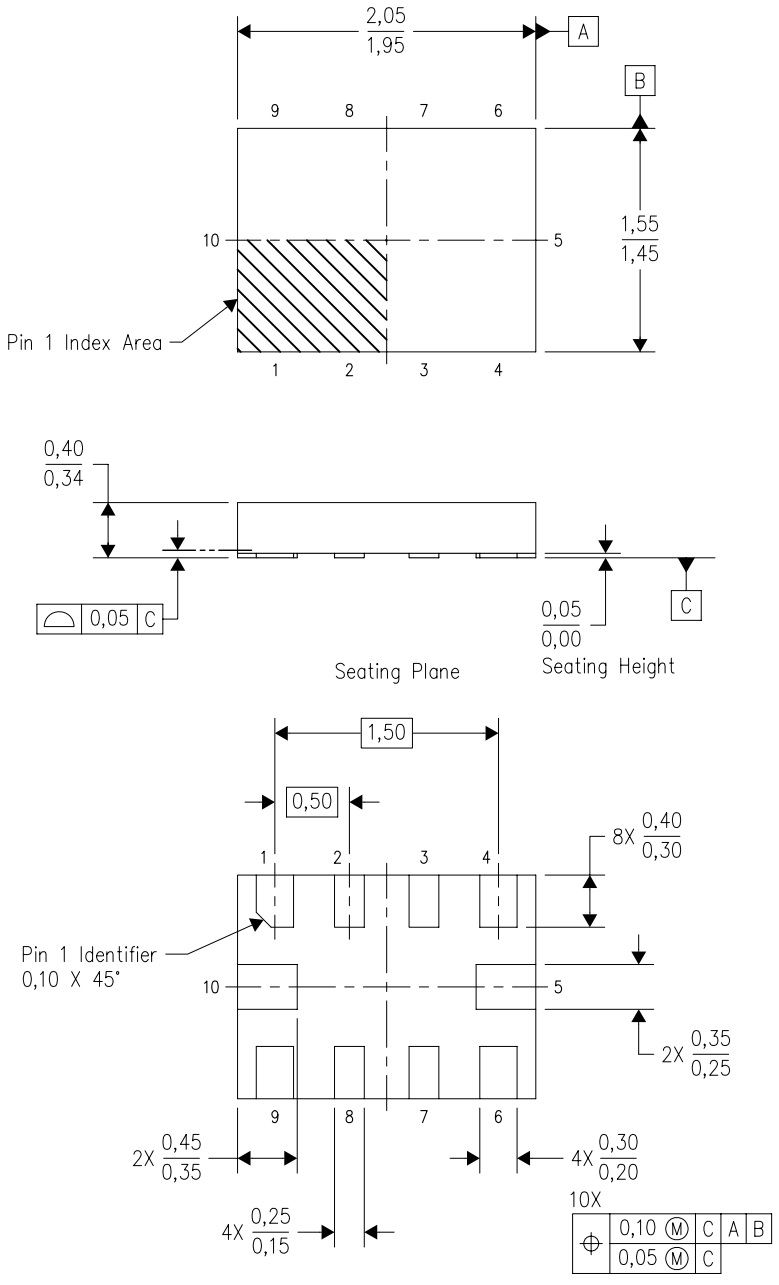
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

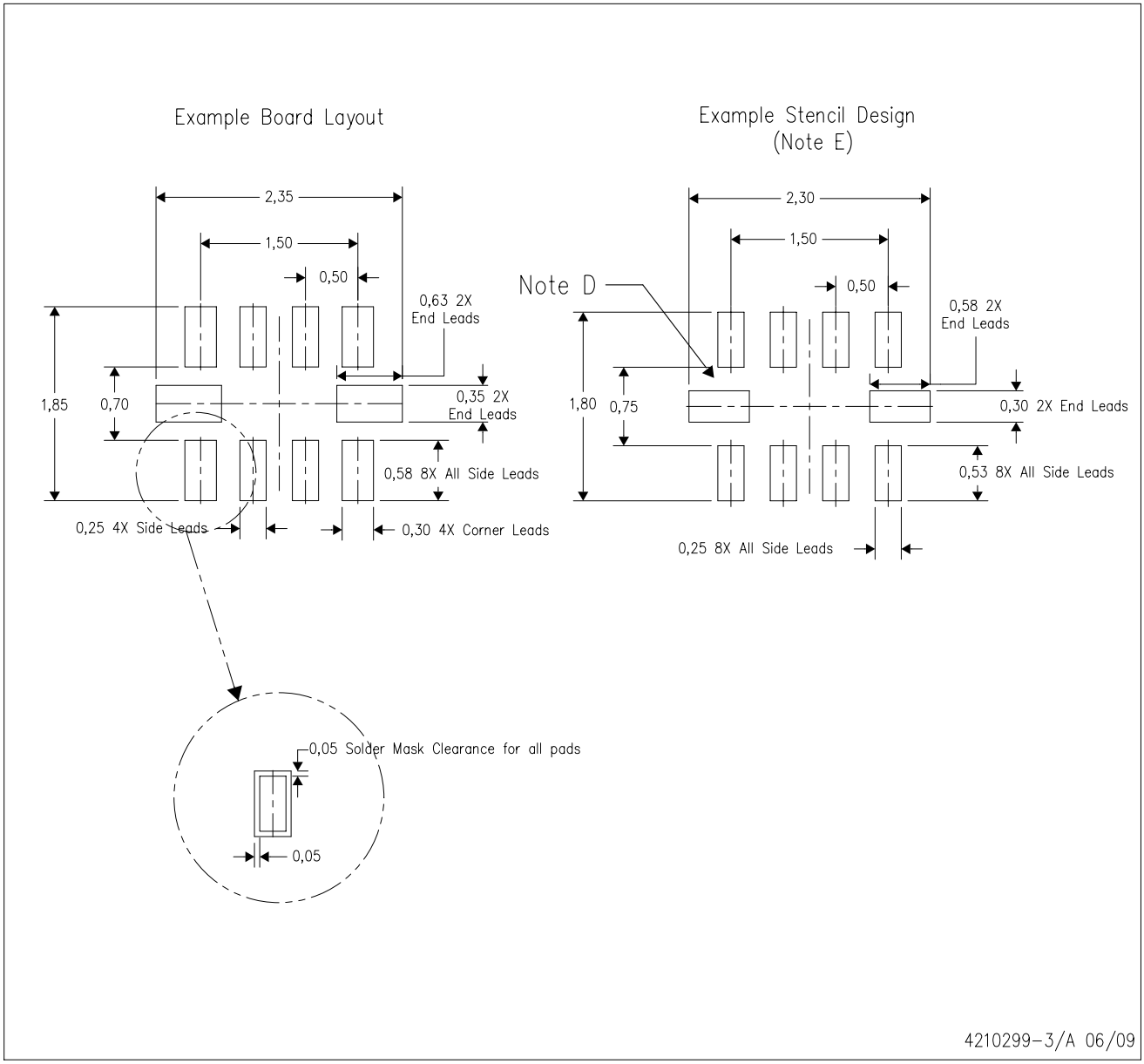
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



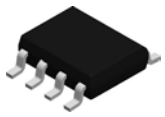
4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

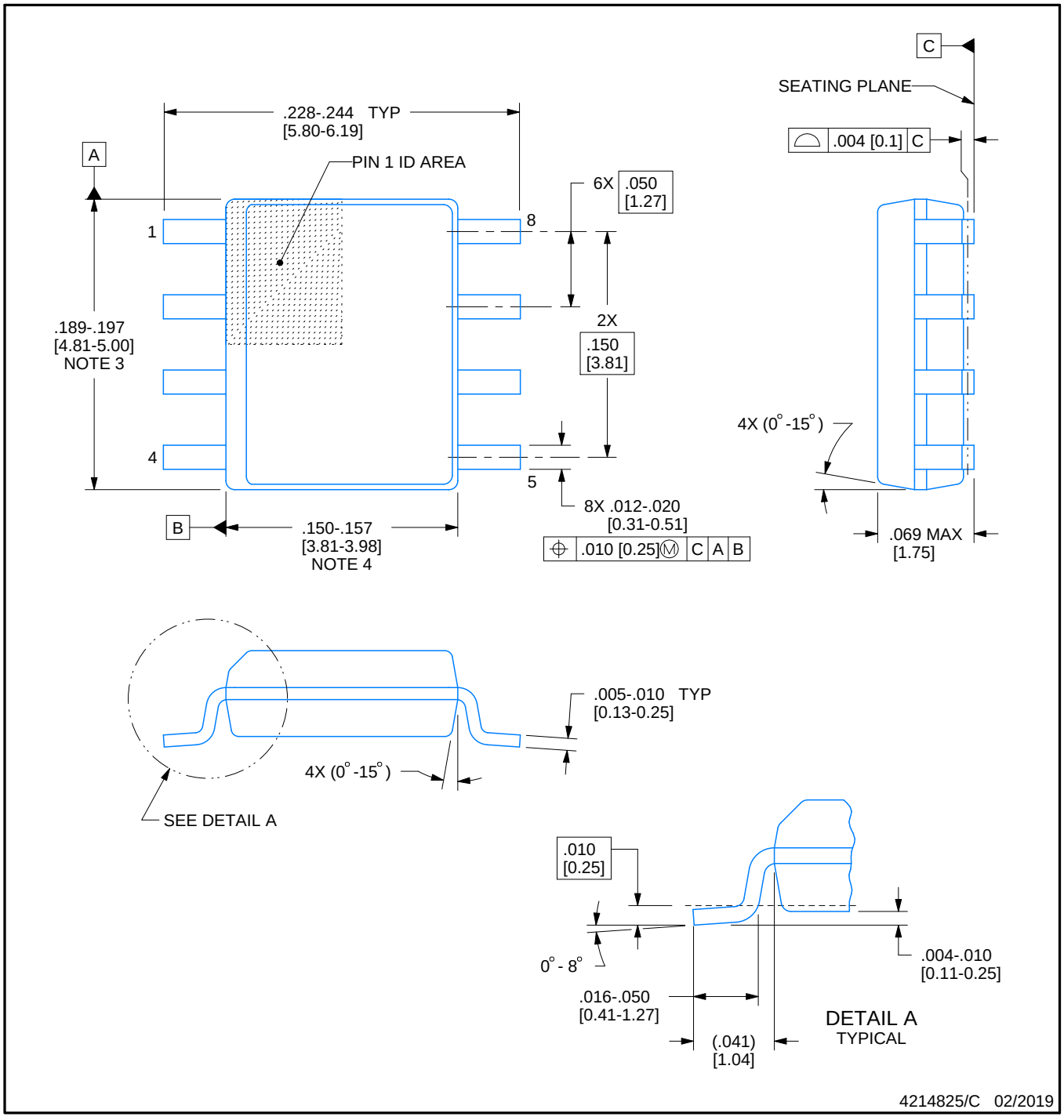


PACKAGE OUTLINE

D0008A

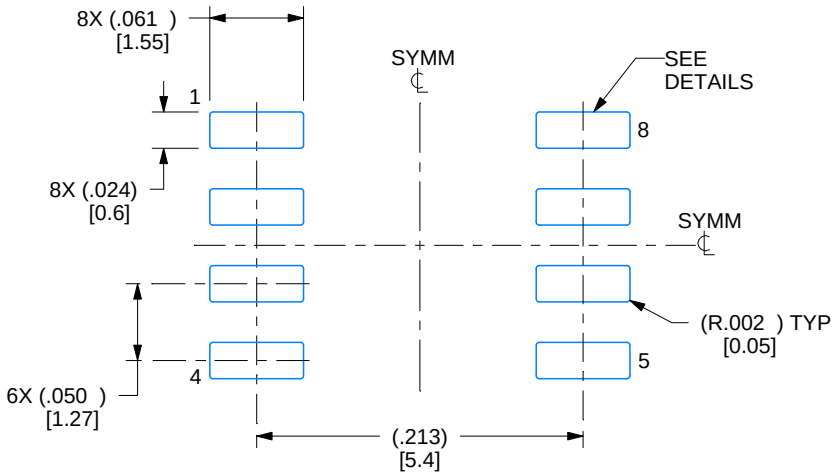
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

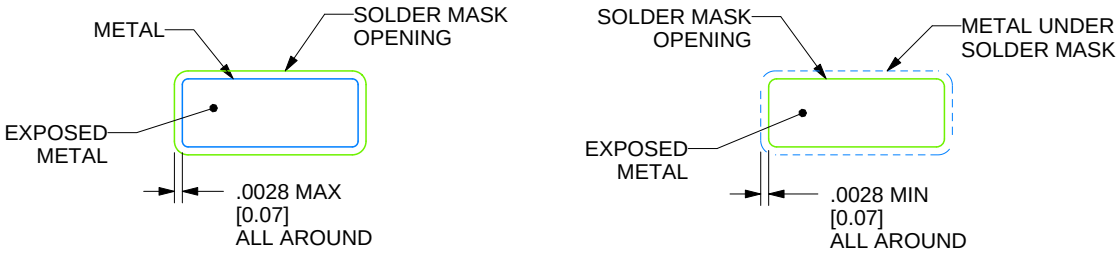


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

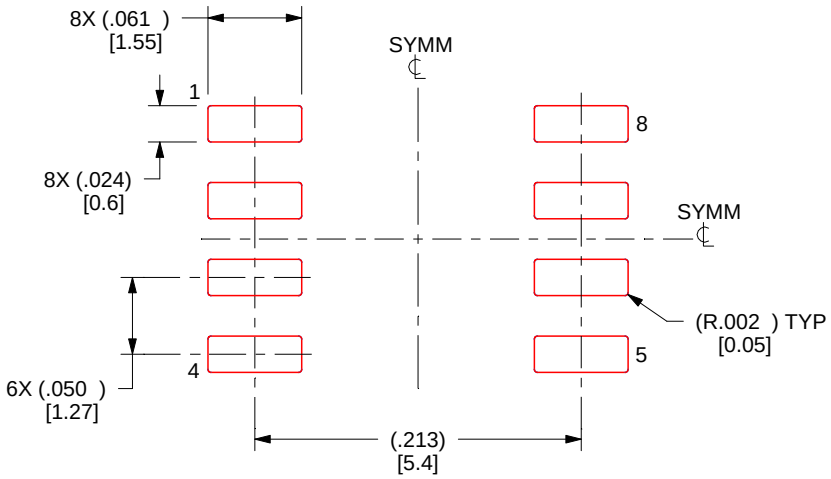
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

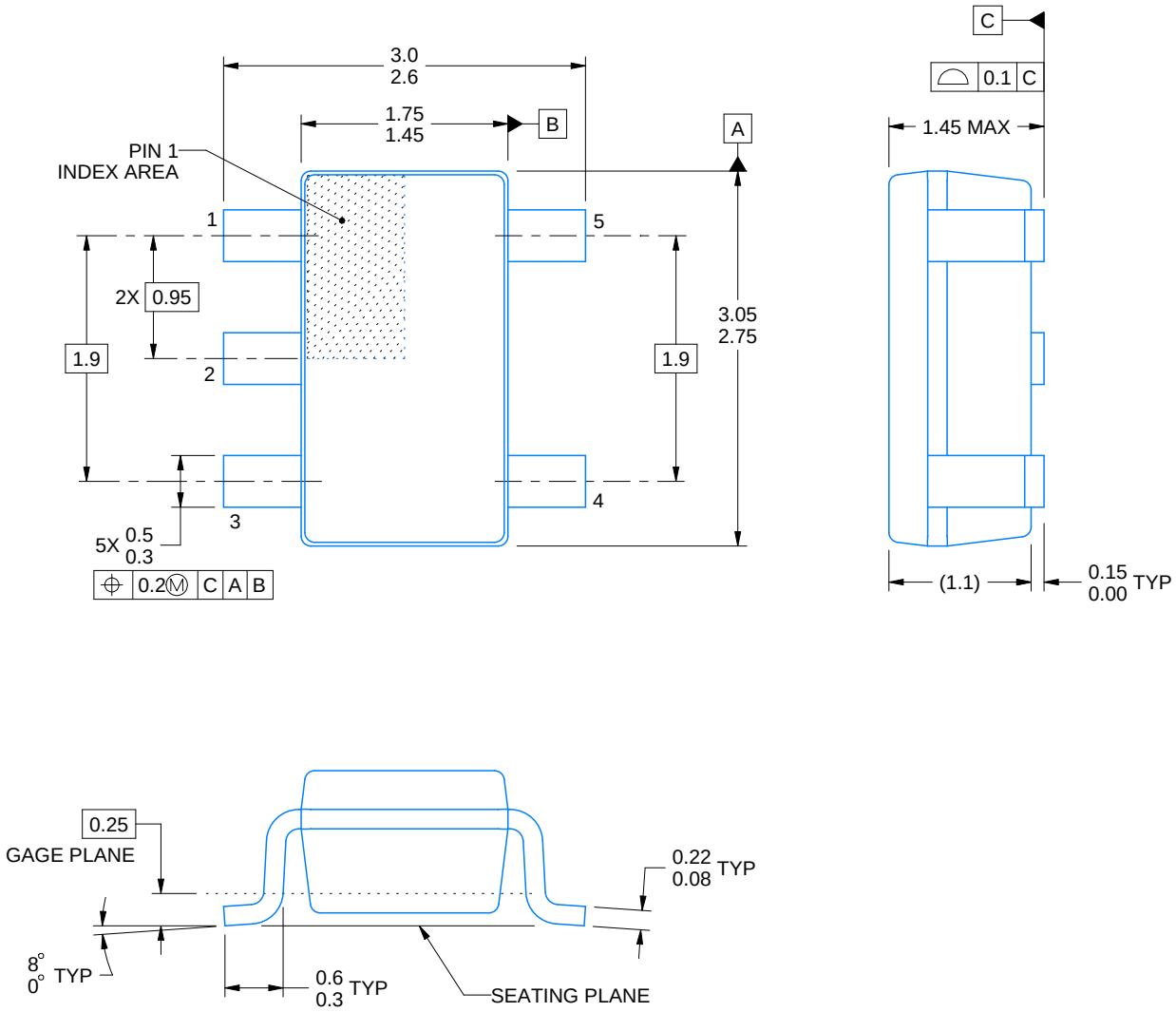
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

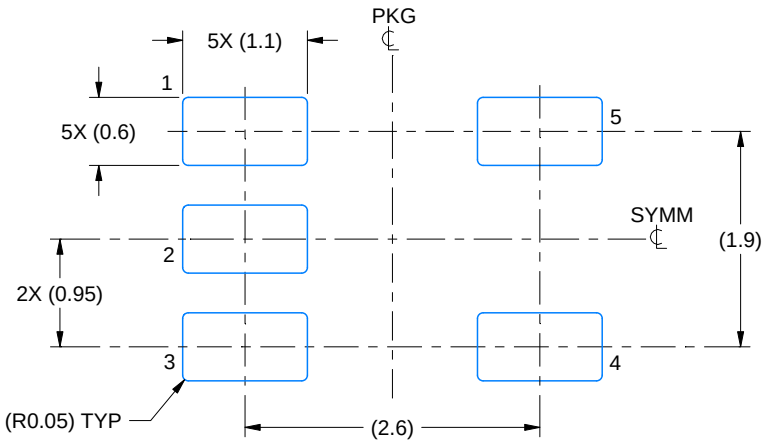
SMALL OUTLINE TRANSISTOR



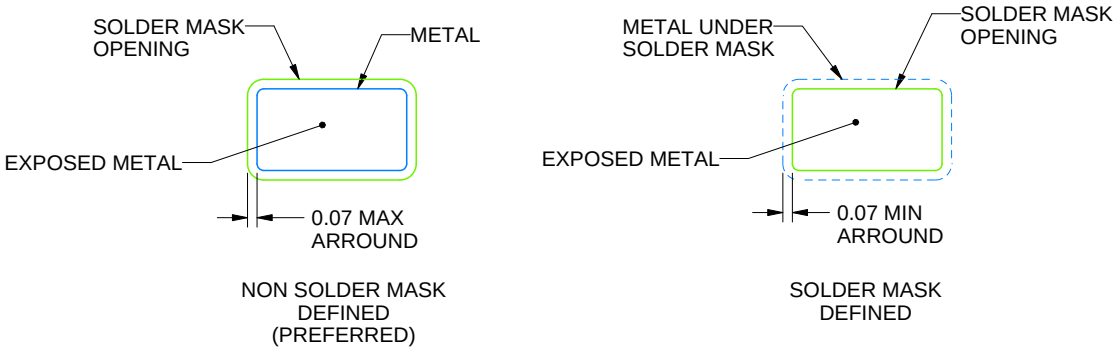
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

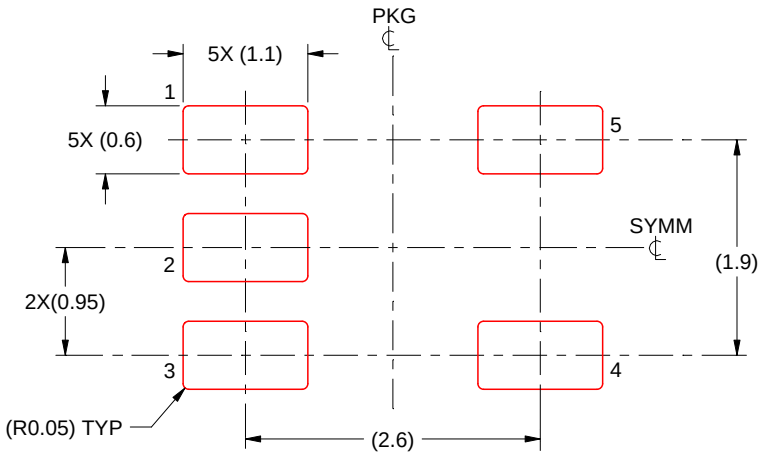


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



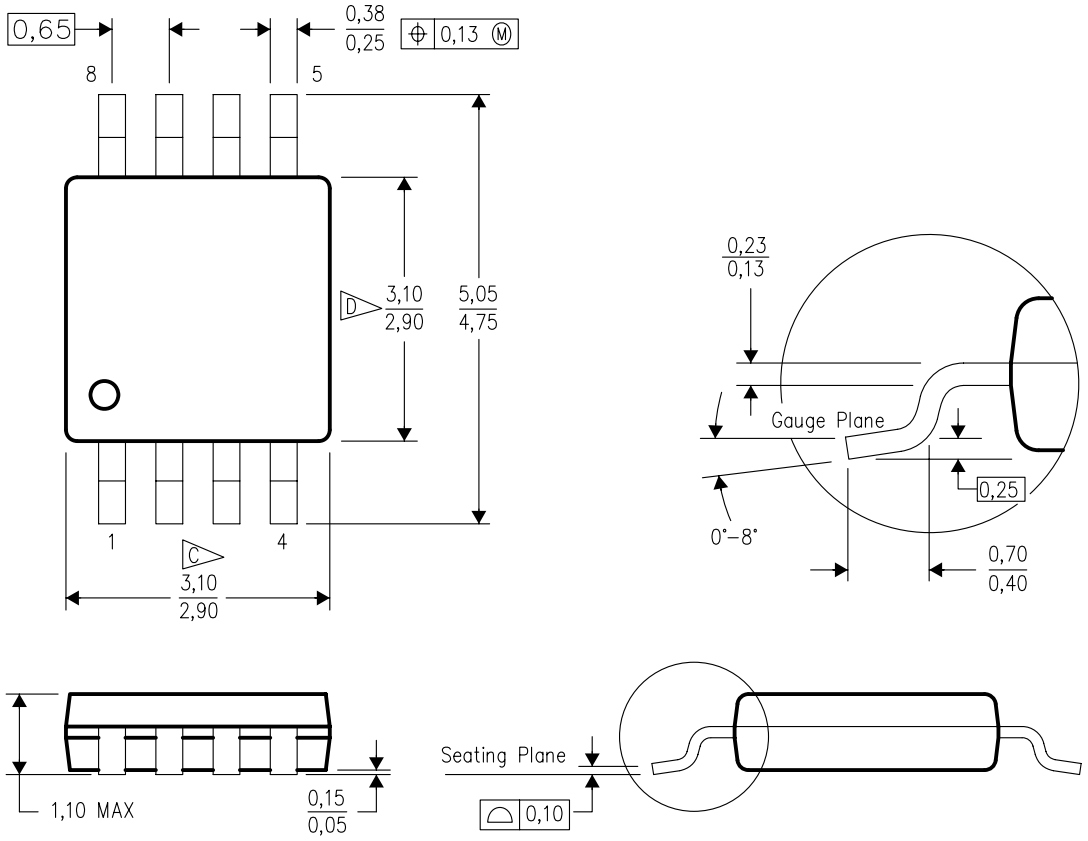
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

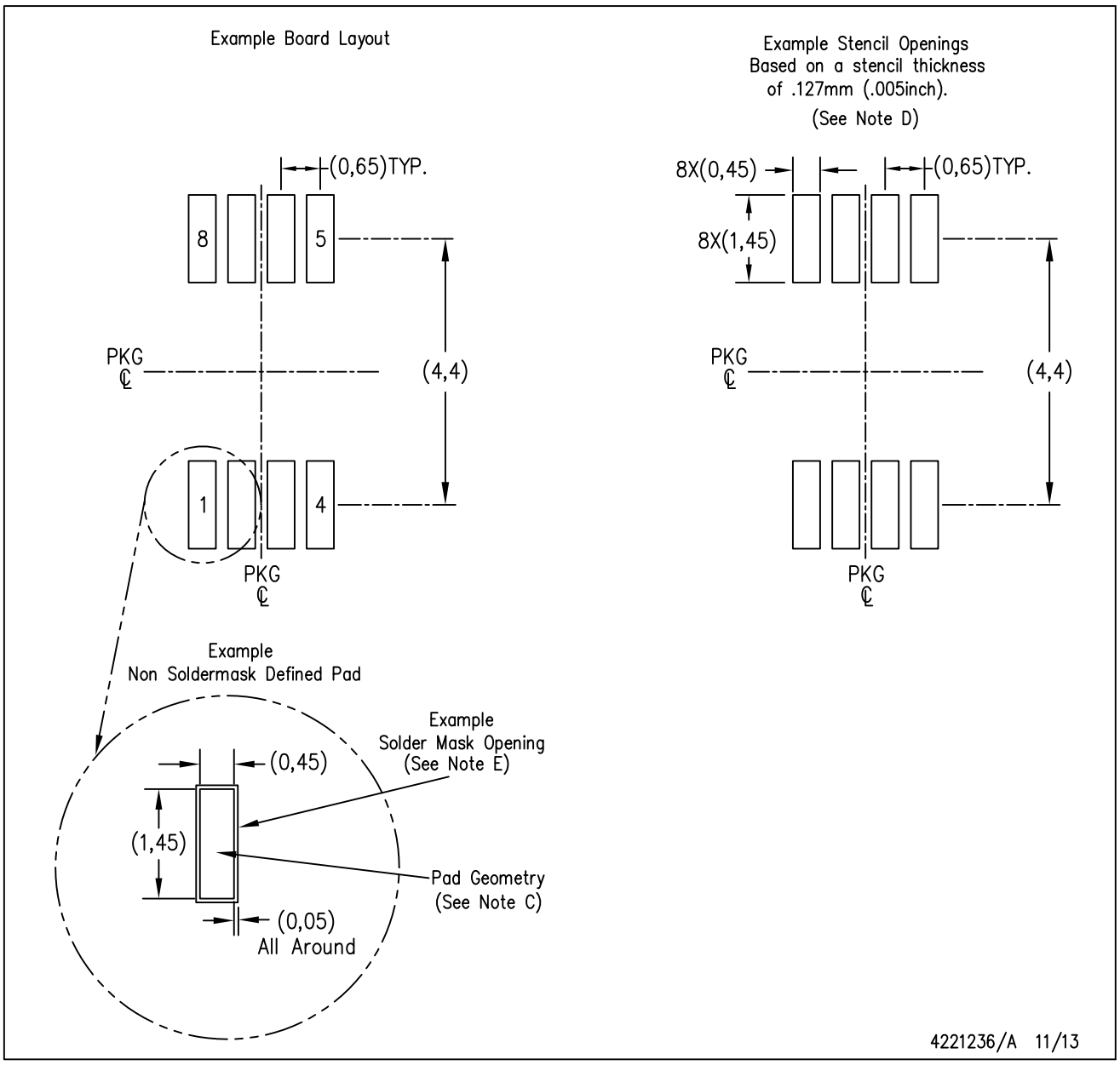
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

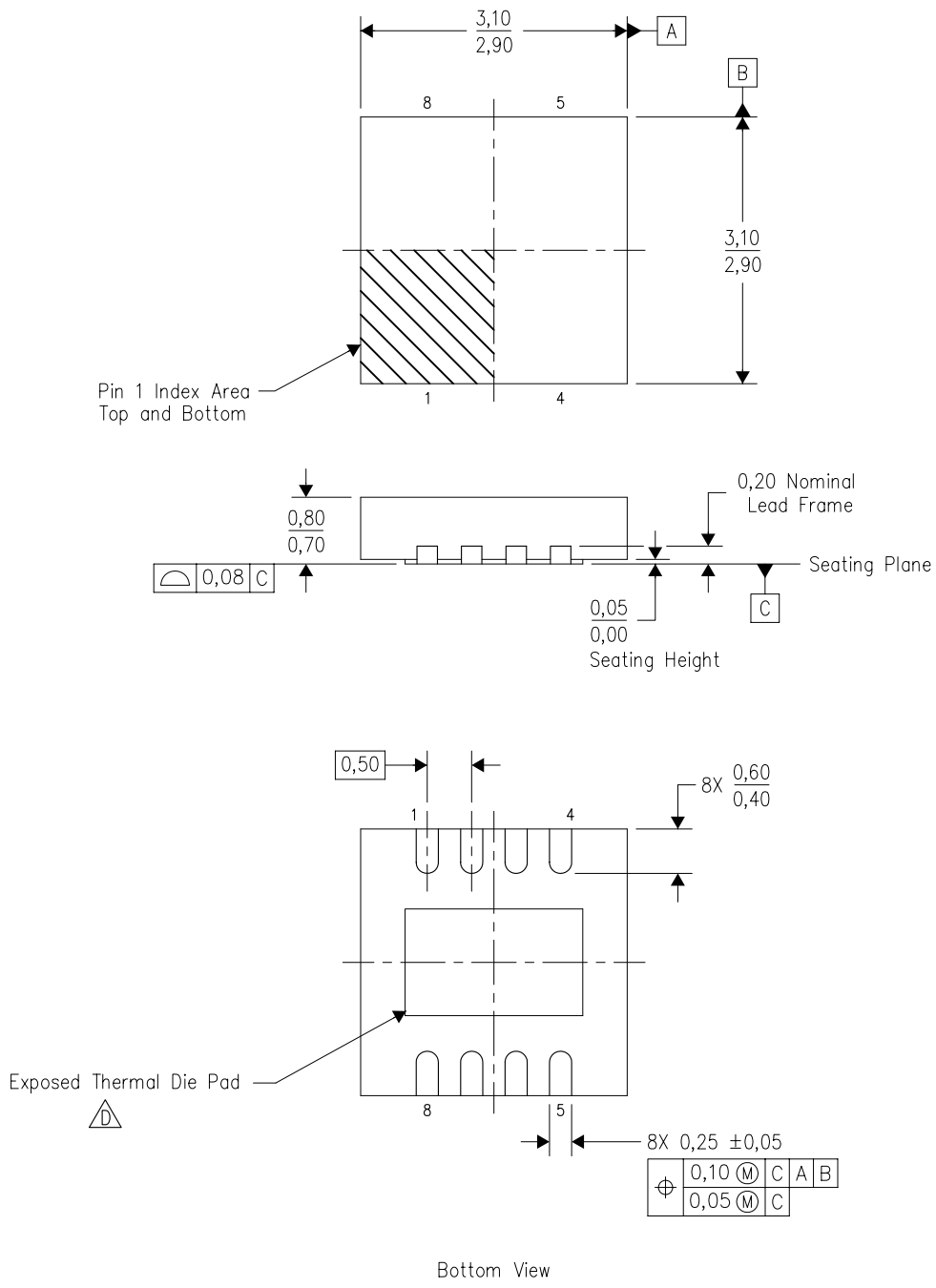
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

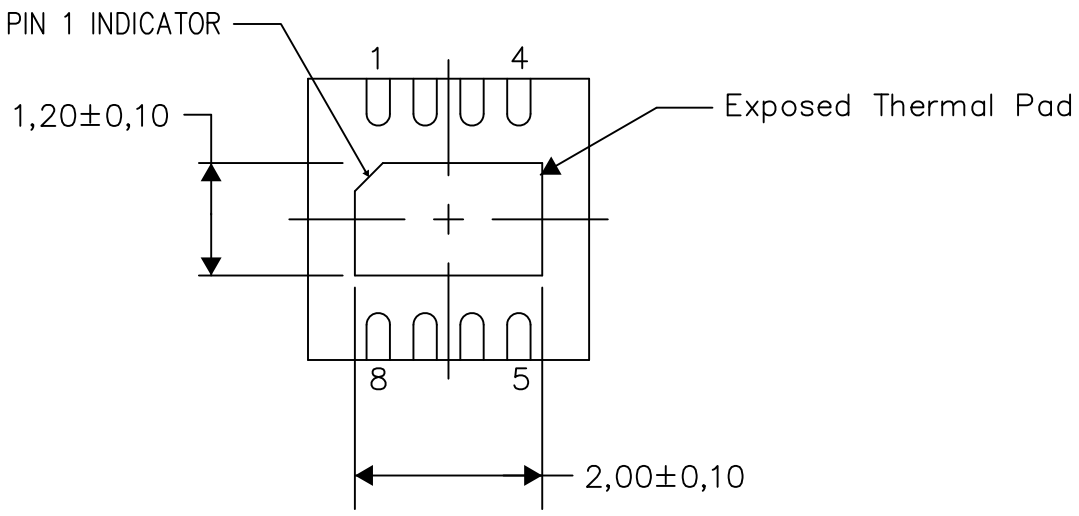
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



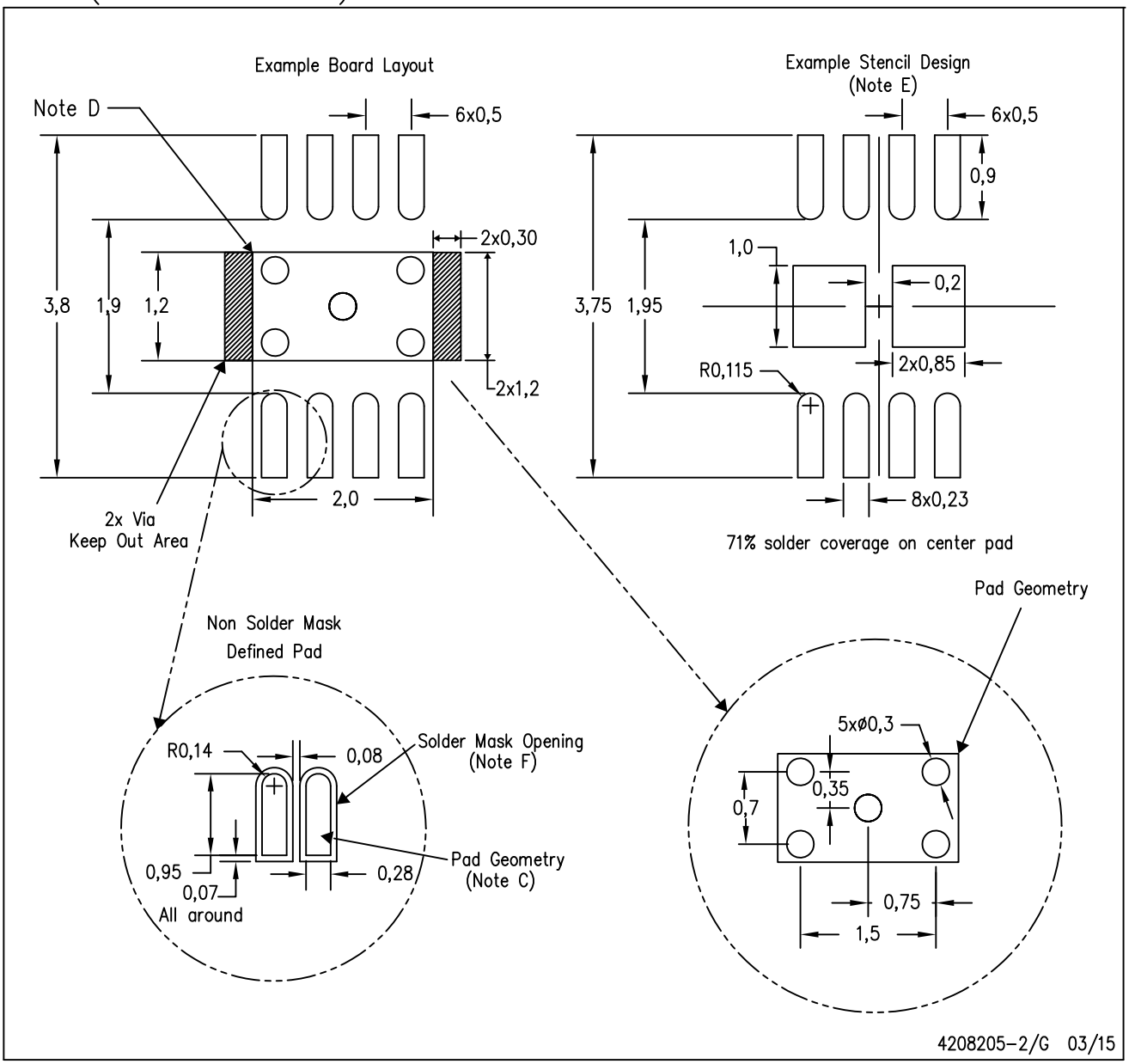
Bottom View

Exposed Thermal Pad Dimensions

4206881–2/I 03/15

NOTE: All linear dimensions are in millimeters

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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