THS56X1EVM for the THS5641A/51A/61A/71A 8-, 10-,12-, AND 14-Bit CommsDAC™ Digital-to-Analog Converters

User's Guide

Literature Number: SLAU032C
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About This Manual

This user's guide describes the characteristics, operation, and use of the THS56X1 evaluation module (EVM).

How to Use This Manual

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- Chapter 2 – Getting Started
- Chapter 3 – User Configurations
- Chapter 4 – Control Modes
- Chapter 5 – Software

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Datasheets:

LT1004	Literature No. SLVS022H
THS3001	Literature No. SLOS217A
SN74LVT245B	Literature No. SCES004C
SN74AHCT1G08DBVR	Literature No. SCLS316G
SN74ALVC08D	Literature No. SCES101D
SN74AHCTIG32	Literature No. SCLS320G
THS5671A	Literature No. SLAS201
THS5661A	Literature No. SLAS247A
THS5651A	Literature No. SLAS260
THS5641A	Literature No. SLAS277

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EVM Overview

This user's guide describes the characteristics, operation, and use of the THS56X1 evaluation module (EVM). The THS56X1 EVM can be connected to the TMS320C542/TMS320C54xx DSP and controlled by very user friendly software—TI's Code Composer Development Environment, or to a pattern generator. This gives the user possibilities to measure the performance of the CommsDAC, to evaluate different types of DAC output interface circuits, and to evaluate an external voltage reference (Vref) suitable for use with the THS56X1A family of digital-to-analog converter (CommsDAC). The CommsDAC family consists of the pin compatible 8-bit resolution THS5641A, 10-bit resolution THS5651A, 12-bit resolution THS5661A and 14-bit resolution THS5671A digital-to-analog converter (DAC).

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1.1 System Block Diagram

The THS56X1 EVM provides a practical platform for evaluating the following devices:

- THS5671A 14-bit resolution, 100 MSPS CommsDAC
- THS5661A 12-bit resolution, 100 MSPS CommsDAC
- TLV5651A 10-bit resolution, 100 MSPS CommsDAC
- THS5641A 8-bit resolution, 100 MSPS CommsDAC

The EVM supports the SOIC (DW) package style, but all devices are available in other packages (see Table 1-1).

Table 1-1. Package Styles Available

Device	DA Package [1] Supported?	DW Package [2] Supported?	PW Package [3] Supported?
THS5671A	No	Yes, 28 pins	Yes, 28 pins
THS5661A	No	Yes, 28 pins	Yes, 28 pins
THS5651A	No	Yes, 28 pins	Yes, 28 pins
THS5641A	No	Yes, 28 pins	Yes, 28 pins

(1) The DA package is a TSSOP device, with pins on a 0.65–mm pitch.
(2) The DW package is a small outline (SOIC) device, with pins on a 1.27–mm pitch.
(3) The PW package is a TSSOP device, with pins on a 0.65–mm pitch.

A block diagram for the THS56X1 EVM is drawn in Figure 1-1. The important features of each component of the block diagram are discussed at length in Section 1.2.

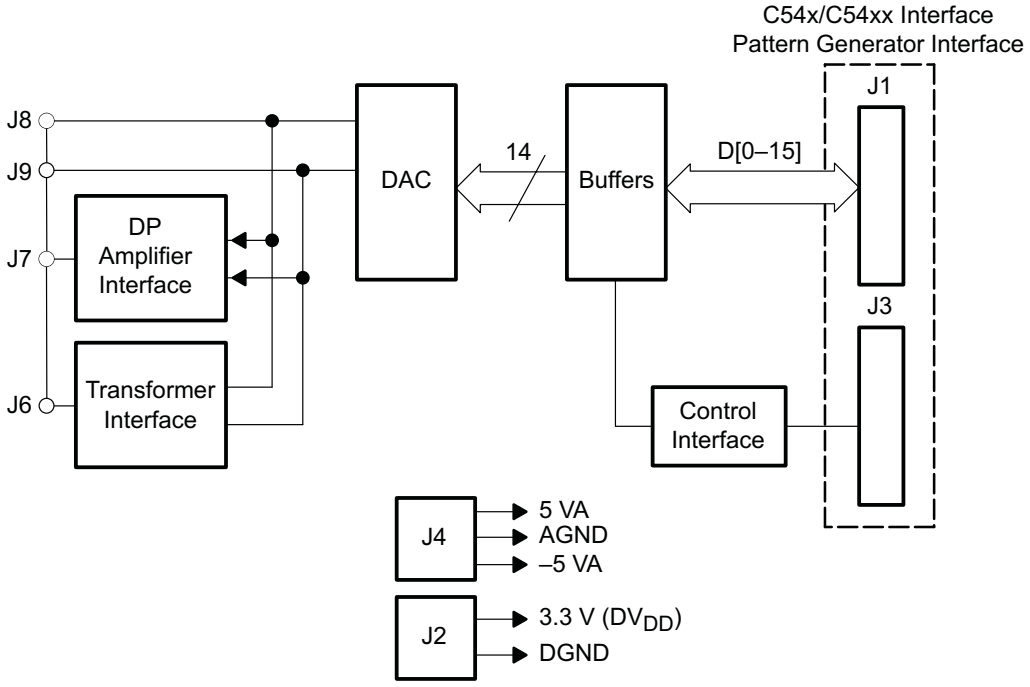

Figure 1-1. THS56X1 EVM Block Diagram

Figure 1-1 comprises two input buffers, CommsDAC control logic, a CommsDAC, an external Vref, a transformer, and an operational amplifier(op amp). This illustration provides a general overview of the EVM. It is not meant to replace the circuit diagram, but to give a brief indication of the features and functions available. It should be read in combination with the circuit diagram supplied and the device data sheet SLAS247A.

1.2 CommsDAC System Description

This printed wiring board (PWB) EVM supports four digital-to-analog converters (DACs).

- THS5641A
- THS5651A
- THS5661A
- THS5671A

The resolution is the main difference between these parts.

General features of these DACs are given in Table 1-2.

Table 1-2. General ADC Features

Device	Res.	Output Channels	Supports Vref_int/ Vref_Ext	Throughput VDD =3.3V	Throughput VDD= 5 V	Available Package	EVM Order Number
THS5571A	14-bit	2	Yes	67 MSPS	100 MSPS	DW/PW	THS5671 EVM
THS5661A	12-bit	2	Yes	67 MSPS	100 MSPS	DW/PW	THS5661 EVM
THS5651A	10–bit	2	Yes	67 MSPS	100 MSPS	DW/PW	THS5651 EVM
THS5641A	8–bit	2	Yes	67 MSPS	100 MSPS	DW/PW	THS5641 EVM

1.2.1 THS5671A/THS5661A/THS5651A/THS5641A CommsDAC

The low-power CMOS CommsDAC device integrates a 1.2-V bandgap reference, a current-source-array, a control amplifier, output current switches, and input latches/logic for controlling the differential output current switches. The device, which can directly drive a 50-Ω load, has good linearity and excellent SFDR specs, symmetrical output ON/OFF switching, and differential output. The CommsDAC family consists of pin-compatible 14-, 12-, 10-, and 8-bit DACs. All devices offer identical user interface and operate from an analog supply of 5 V and a digital supply of 3.3 V or 5 V. The THS56X1A full-scale current is adjustable from 2 mA to 20 mA. Power dissipation at 5 V is less than 175 mW and in sleep mode the standby power is about 25 mW. The THS56X1A is driven by the on-chip voltage reference or by an external voltage reference.

Any of the digital-to-analog converters (DACs) present on the EVM can be used to either process the output of a parallel output ADC or to act as an independent device driven by either a pattern generator or a DSP starter kit (DSK) board.

1.2.2 Control/Interface

The control signals can be derived from either a DSK/microprocessor or from a dedicated GND and 3-V to 5-V supply connected to J3. The signals from either source are similar. The decision regarding which host system to use is left to of the user.

1.2.3 Output Stage

Several circuits for achieving a single-ended output from the DAC's differential outputs are designed into the THS56X1 EVM. Figure 3-1 shows the arrangement of the output circuits.

1.3 EVM Operating Modes

There are two modes of operation for the EVM:

- DSK/microprocessor mode
- Pattern generator mode

Each of these modes is discussed below.

1.3.1 C542/C54xx DSK/Microprocessor Mode

The C542/C54XX starter kit (DSK)/microprocessor is used to supply the sample clock (CLKOUT), the EVM device-select control signals, and data via the 16-bit parallel data bus. The digital data sent to the DAC for conversion is usually stored in a lookup table—see the example program shown in Section 5. If the input digital data source can conveniently provide data and sample-clock, then the user must connect jumper W1 or make the following connections: J3 pin1 to J3 pin2, J2 pin 3 and pin 5 tied to either 3.3 V or 5 V in order to enable the SN74LVT245B buffers.

W5 is used to set the THS56X1A CommsDAC operating modes. Mode 0 (W5, closed) configures the device for binary input data word format. Mode 1 (W5, opened) sets a twos complement input data word format.

1.3.2 Pattern Generator Mode

A pattern generator, similar to the Tektronix HFS9009, can be used to supply the input digital data stream and sample clock. The EVM device select signal is provided via J3 or W1. The pattern generator is programmed, typically, to output a sine wave and the appropriate sample clock (either 100 MHz or 67 MHz). The clock feeds directly into SMA connector J5 and the digital data to J1 goes via a SMA-to-ribbon cable adapter (see Figure 1-2).

W5 is used to set the THS56X1A CommsDAC operating modes. Mode 0 (W5, closed) configures the device for binary input data word format. Mode 1 (W5, opened) sets a twos complement input data word format.

1.3.3 Analog Output

The techniques used in a design of this type are different from those used in lower speed DACs. Single-ended analog output is derived from the THS56X1A CommsDAC differential outputs IOUT1 and IOUT2 via a 1:1 RF transformer. A THS3001 operational amplifier (op amp) is a convenient way to derive a buffered noninverting single-ended output, a buffered inverting single-ended output, or a buffered differential to single-ended output.

1.4 Power and Cabling Requirements

The EVM dc supply voltages are analog ±5 V and digital 3 V or 5 V. These voltages should be supplied to the EVM through shielded twisted-pair wire for best performance. This type of power cabling minimizes any stray or transient pickup from the higher-frequency digital circuitry. If ribbon cables are used for interfacing to both J1 and J3, the crosstalk between adjacent conductors is minimized if shielded ribbon cables are used.

1.5 Printed Circuit Assembly as Part of a System

1.5.1 C542/C54xx DSK/Microprocessor Mode

In this mode the DSP or microprocessor supplies data, sample clock, and control signals via J1 and J3, respectively. W2 is set to positions 1-2, and W1, W3, W5, W6 – W9 are set appropriately (see the User Configuration section of this document and Figure 1-4).

1.5.2 Pattern Generator Mode

In this mode the pattern generator (Tektronix HFS9009) supplies data and sample clock signals to J1 and J5, respectively. Shown in Figure 1-2 the mating of the pattern generator adapter and the THS56X1 EVM connector J1, and control is provided via J3.

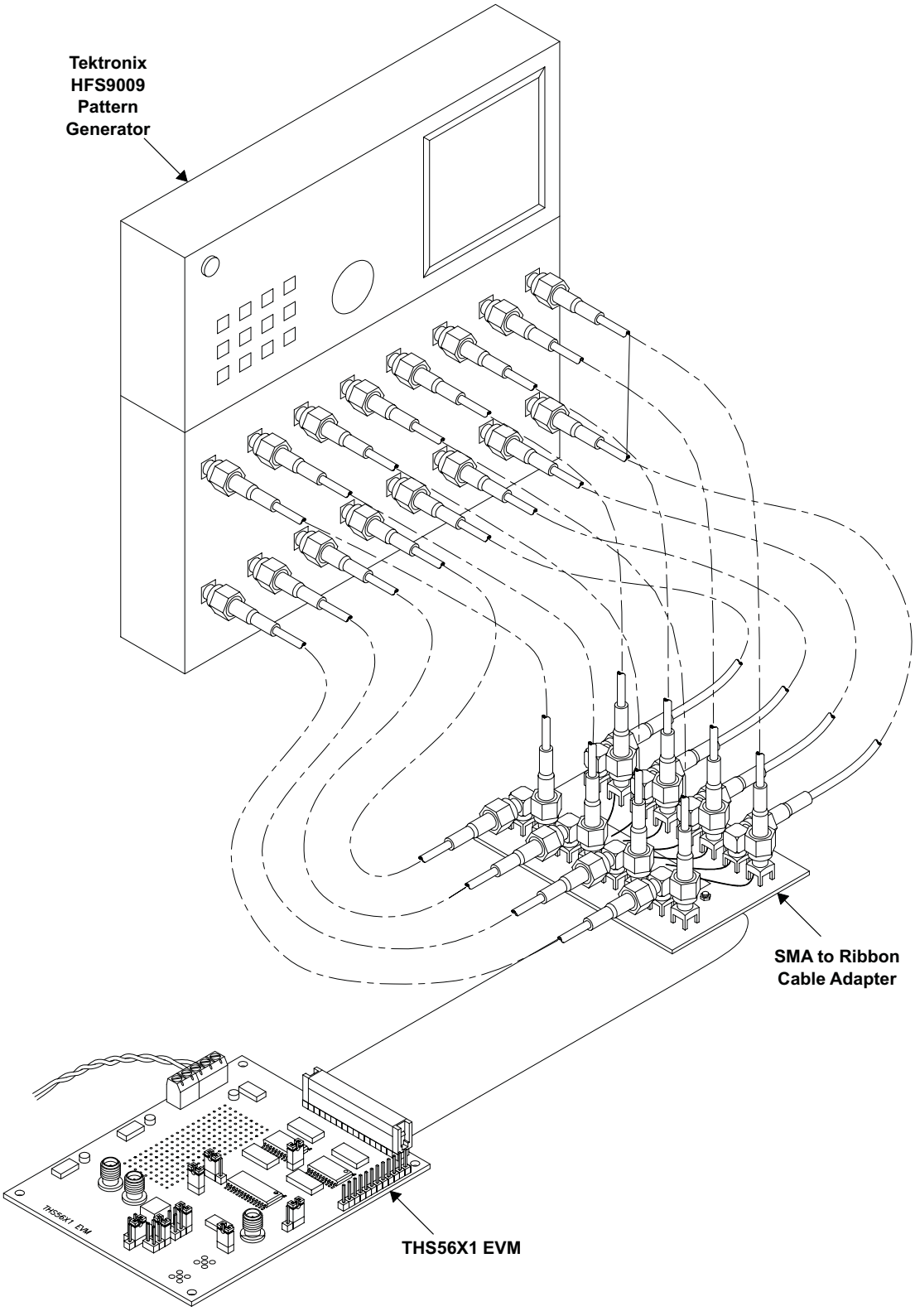

Figure 1-2. Mating of Connectors on the THS56X1 EVM to the Tektronix HFS9009 Pattern Generator

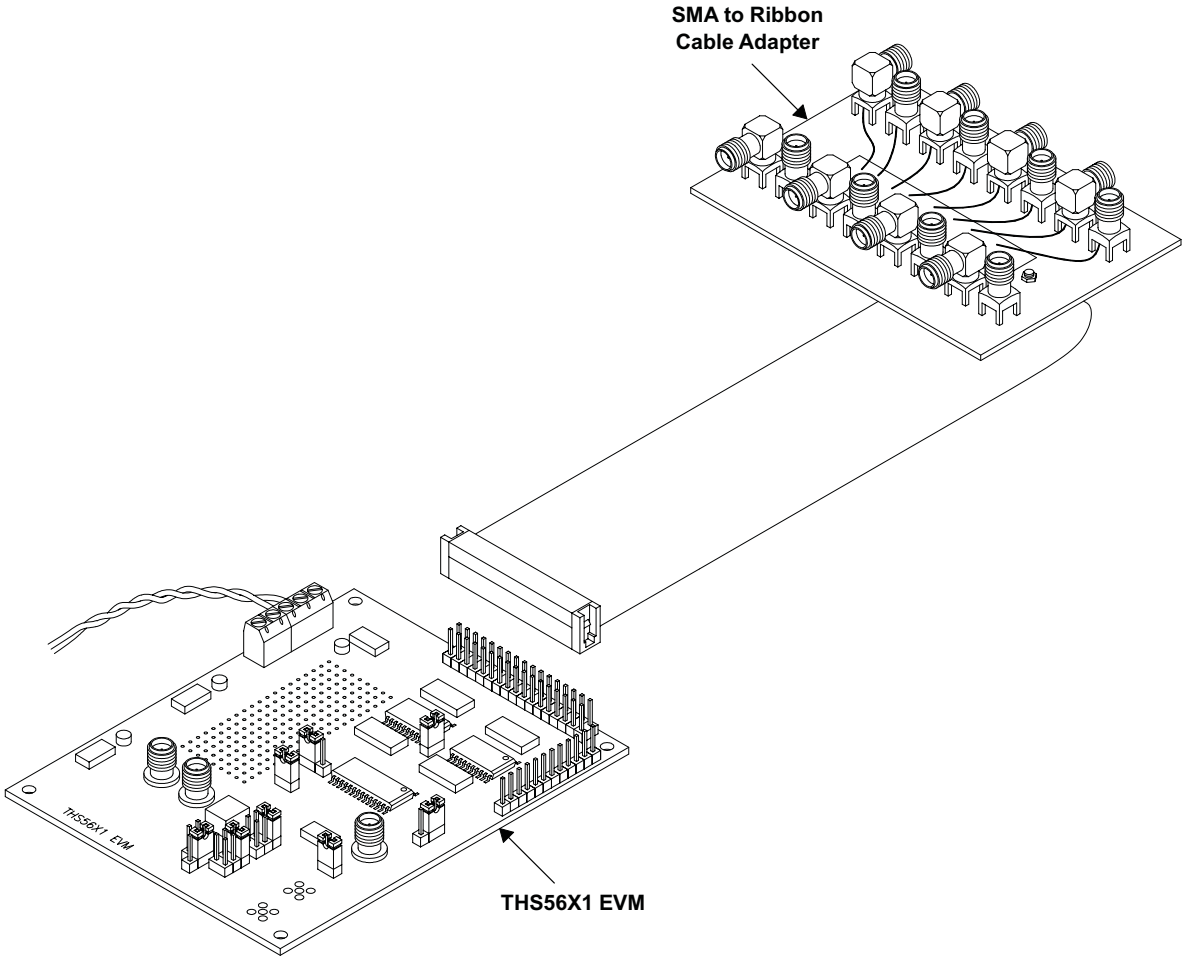

Figure 1-3. Mating of Connectors on the THS56X1 EVM to the SMA–Ribbon Cable Adapter

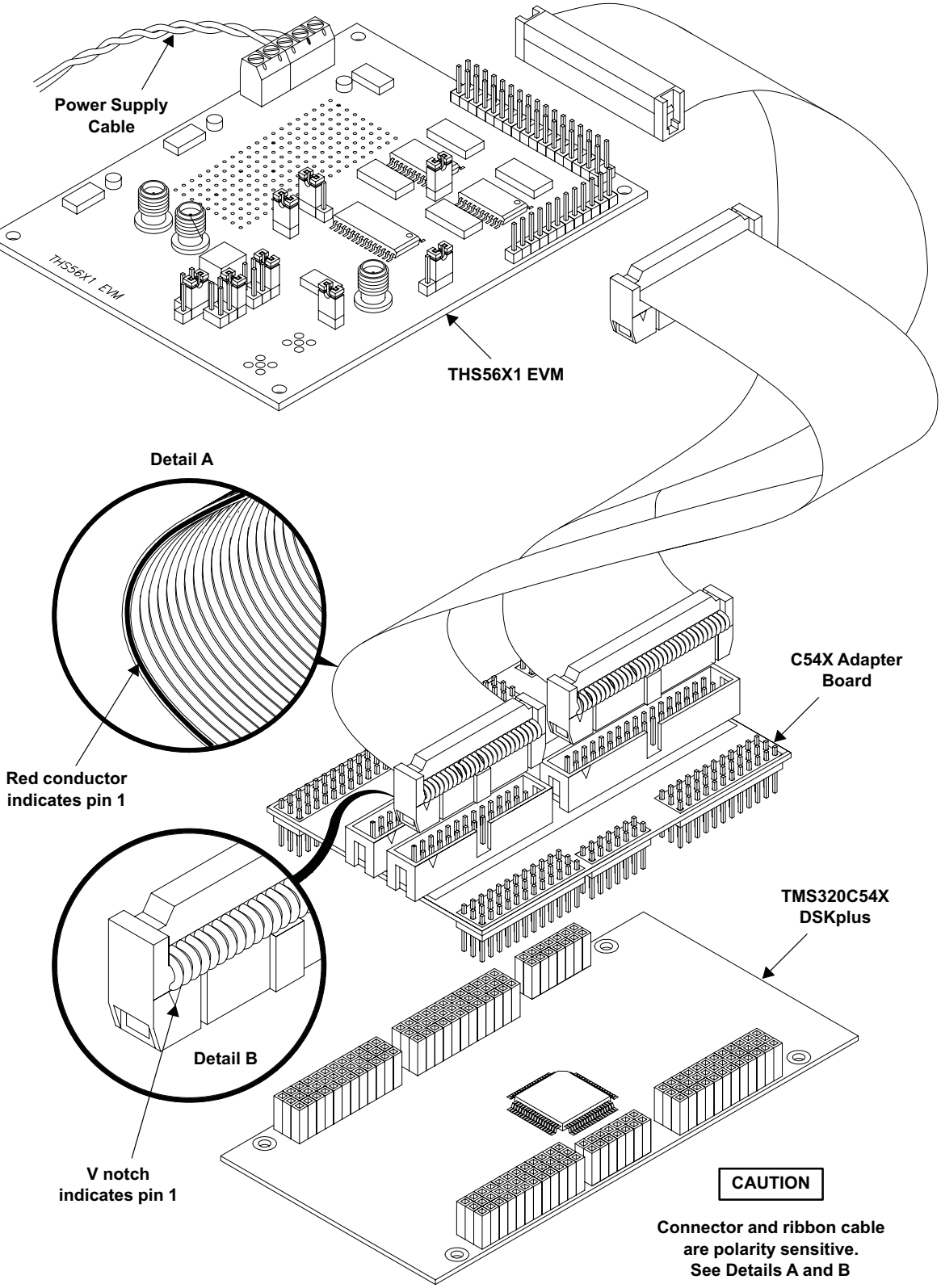

Figure 1-4. Mating of Connectors on the C542DSK to the C542 DSKplus

1.5.3 CommsDAC Output Configurations

The THS56X1A CommsDAC output can be configured as single-ended outputs or as a differential output (see also THS5661A, 12-bit, 100MSPS, CommsDAC data sheet SLAS247A). Differential output configuration requires IOUT1 and IOUT2 to feed directly into SMA connectors, J8 and J9 (see Figure 1-5).

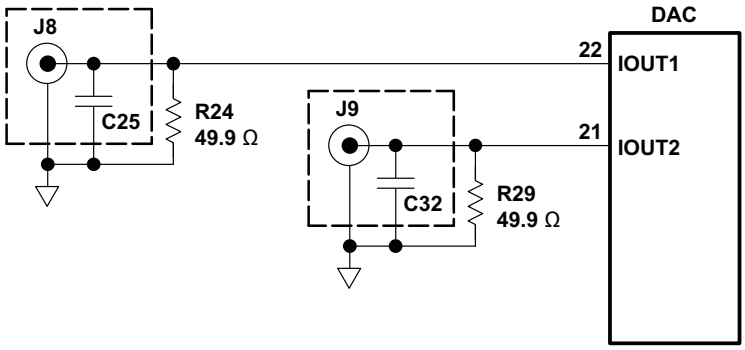

Figure 1-5. Connecting the THS56X1A Outputs to J8 and J9

1.6 Printed Circuit Assembly Options Available

To ensure the flexibility of the printed-circuit board (PCB), four possible CommsDACs featured in this series are described in Table 1-3.

Table 1-3. Possible DACs

DAC Part No.	No. of Bits	Speed EVM	Order No.
THS5671A	14	100 MSPS	THS5671 EVM
THS5661A	12	100 MSPS	THS5661 EVM
THS5651A	10	100 MSPS	THS5651 EVM
THS5641A	8	100 MSPS	THS5641 EVM

Ensure that the printed-circuit assembly (PCA) has the correct check mark on the silkscreen.

Each PCA may have additional hardware to install, if appropriate.

Getting Started

This chapter describes the physical characteristics and PCB layout of the EVM, and lists the components used on the module.

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2.1 Physical Description

The PWB is constructed in four layers as shown in the following illustrations. The dimensions of the PWB are 4.25 in × 3.375 in (107.95 mm × 85.73 mm). See Figure 2-1.

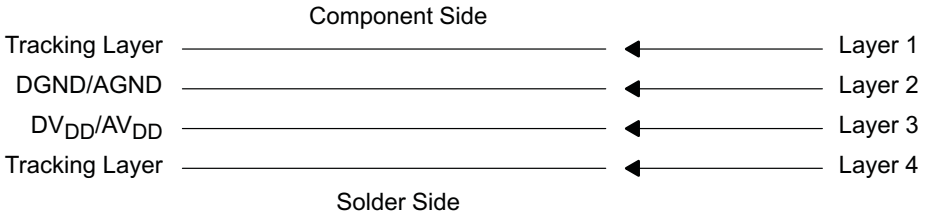

Figure 2-1. PWB Layers

Figure 2-2 through Figure 2-5 show the tracking for each layer.

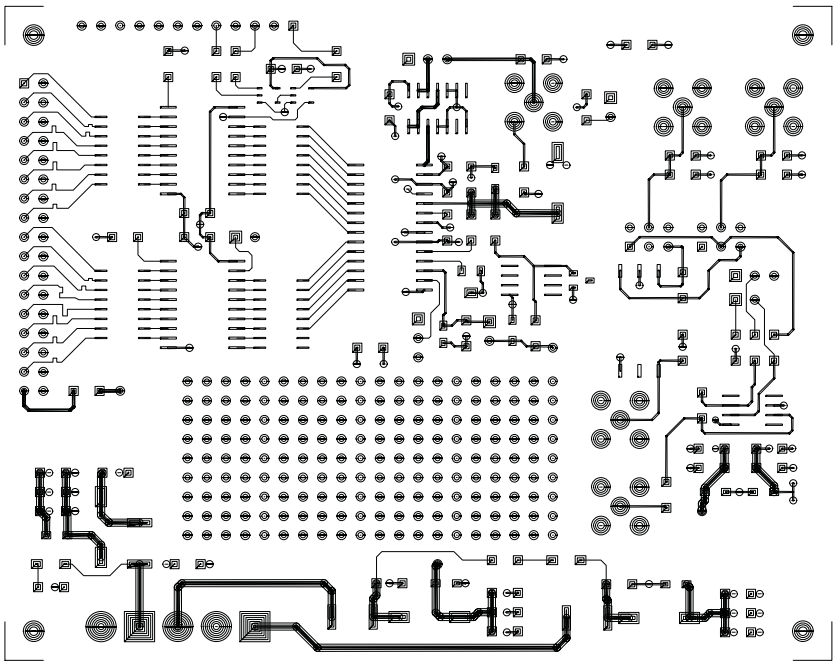

Figure 2-2. Board Layout, Layer 1

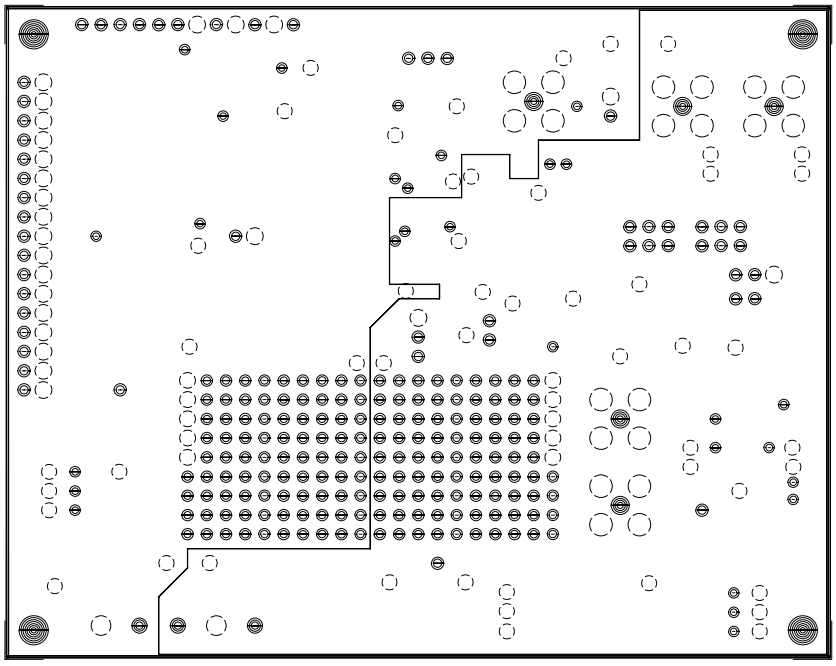

Figure 2-3. Board Layout, Layer 2

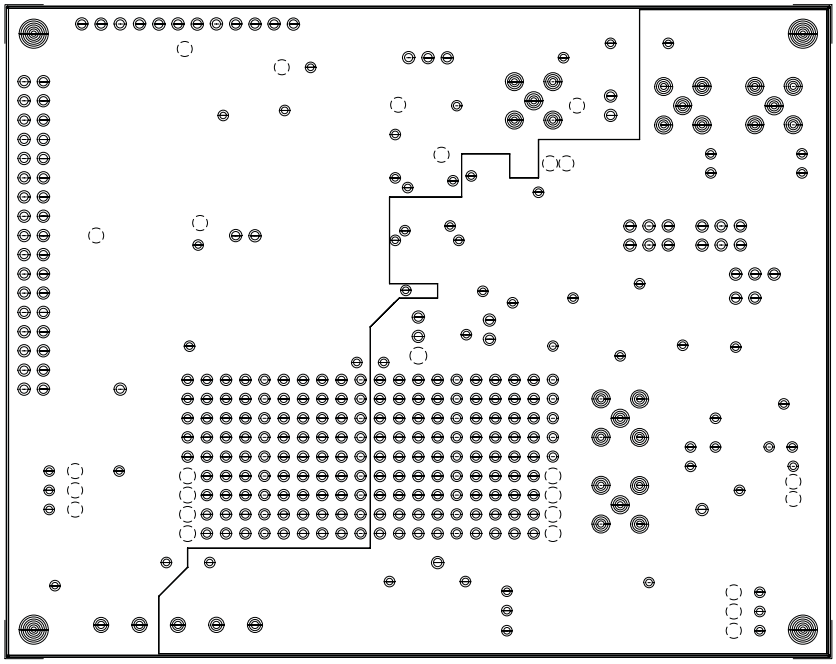

Figure 2-4. Board Layout, Layer 3

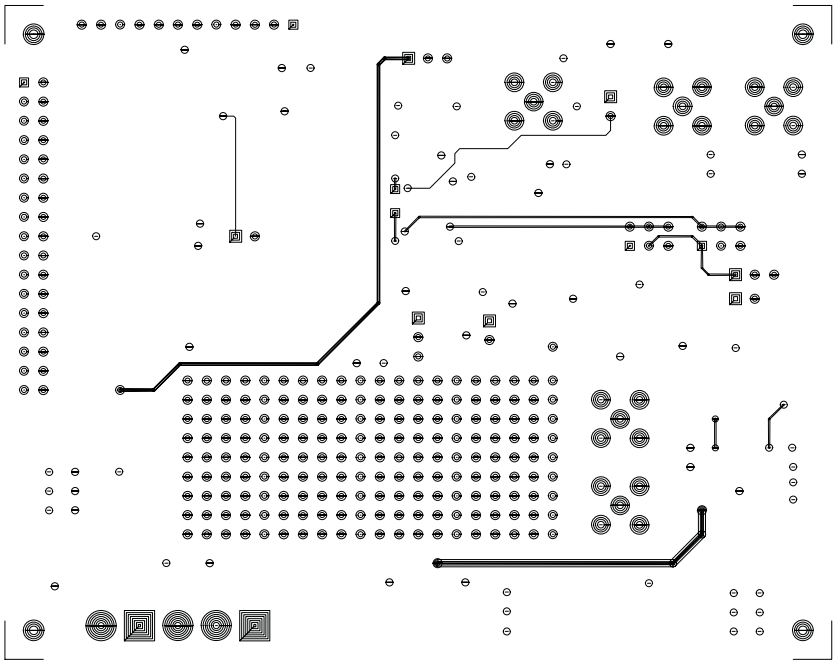

Figure 2-5. Board Layout, Layer 4

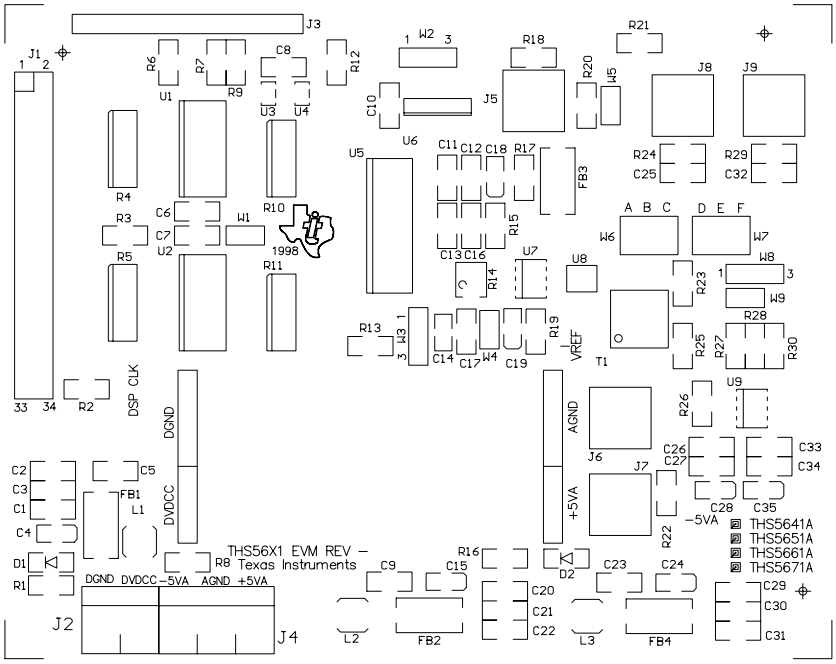

Figure 2-6. Silk Screen

2.2 Parts List

This table lists the parts required for the THS56X1 EVM assembly.

QTY	REFERENCE DESIGNATION	PART NUMBER (1)	DESCRIPTION	MANUFACTURER
3	C1, C22, C31	1206ZC105KAT2A	Ceramic 1 µF, 10 V, X7R, 10%	AVX
4	C18, C19, C28, C35	ECSTOJY475	6.3 V, 4.7 µF, tantalum	Panasonic
3	C15, C24, C4	ECSTOJY106	6.3 V, 10 µF, tantalum	Panasonic
0	C25, C32		Ceramic, not installed, 50 V, X7R, 10%	
6	C14, C2, C20, C26, C29, C33	12065C103KAT2A	Ceramic, 0.01 µF, 50 V, X7R, 10%	AVX
17	C10, C11, C12, C13, C16, C17, C21, C23, C27, C3, C30, C34, C5, C6, C7, C8, C9	12065C104KAT2A	Ceramic, 0.1 µF, 50 V, X7R, 10%	AVX
2	D1, D2	AND/AND5GA or equivalent	GREEN LED, 1206 size SM chip LED	
4	FB1, FB2, FB3, FB4	27-43-037447	Fair-Rite SM beads #27-037447	FairRite
1	J1	TSW-117-07-L-D or equivalent	34-Pin header for IDC	Samtec
1	J2	KRMZ2 or equivalent	2 Terminal screwconnector, 2TERM_CON	Lumberg
1	J3	TSW-112-07-L-S or equivalent	Single row 12-pin header	Samtec
1	J4	KRMZ3 or equivalent	3 Terminal screw connector	Lumberg
3	J5, J6, J7	142-0701-206 or equivalent	PCB Mount SMA jack, SMA_PCB_MT	Johnson Components
0	J8, J9	142-0701-206 or equivalent	PCB Mount SMA jack, not installed	Johnson Components
3	L1, L2, L3	DO1608C-472	DO1608C-series, DS1608C-472	Coil Craft
1	R1	1206	1206 Chip resistor, 1.5K, 1/4 W, 1%	
4	R10, R11, R4, R5	CTS/ CTS766-163-(R)330-G-TR	8-Element isolated resistor pack, 33 Ω	
4	R12, R19, R7, R9	1206	1206 Chip resistor, 33 Ω, 1/4 W, 1%	
5	R13, R17. R2, R21, R8	1206	1206 Chip resistor, 0 Ω, 1/4 W, 1%	
1	R14	3214W-1-502 E or equivalent	4 mm SM Pot, 5K	Bourns
1	R15	1206	1206 Chip resistor, 2.94K, 1/4 W, 1%	
1	R16	1206	1206 Chip resistor, 3K, 1/4 W, 1%	
3	R18, R24, R29	1206	1206 Chip resistor, 49.94K, 1/4 W, 1%	
3	R20, R3, R6	1206	1206 Chip resistor, 10K, 1/4 W, 1%	

(1) Manufacturer and part number data is supplied for reference only. Substitutions are permissible on all but TI parts.

QTY	REFERENCE DESIGNATION	PART NUMBER (1)	DESCRIPTION	MANUFACTURER
1	R22	1206	1206 Chip resistor, 10K, 1/4 W, 1%	
1	R23	1206	1206 Chip resistor, 100K, 1/4 W, 1%	
1	R25	1206	1206 Chip resistor, TBD, 1/4 W, 1%	
4	R26, R27, R28, R30	1206	1206 Chip resistor, 750K, 1/4 W, 1%	
1	T1	T1-1T-KK81	RF Transformer, T1-1T-KK81	MiniCircuits
2	U1, U2	SN74LVT245BDW	Octal bus transceiver, 3-state, SN74LVT245B	TI
1	U3	SN74AHCT1G00DBVR/ SN74AHC1G00DBVR	Single gate NAND, SN74AHC1G00	TI
1	U4	SN74AHCT1G32DBVR/ SN74AHCC1G32DBVR	Single 2 input positive OR gate, SN74AHC1G32	TI
1(2)	THS5641A	THS5641AIDW	DAC, 2.7–5.5 V, 8 Bit, 125 MHz	TI
1(2)	THS5651A	THS5651AIDW	DAC, 2.7–5.5 V, 10 Bit, 125 MHz	TI
1(2)	THS5661A	THS5661AIDW	DAC, 2.7–5.5 V, 12 Bit, 125 MHz	TI
1(2)	THS5671A	THS5647AIDW	DAC, 2.7–5.5 V, 14 Bit, 125 MHz	TI
1	SN74ALVC08	SN74ALVC08D	Quad AND gate	TI
1	LT1004D	LT1004CD-1-2/LT1004ID-1-2	Precision 1.2 V reference	TI
0	NOT INSTALLED	AD1580BRT	Precision voltage reference, not installed	
1	THS3001	THS3001CD/THS2001ID	THS3001 high-speed op amp	TI
4	W1, W2, W5, W9	TSW-102-07-L-S or equivalent	2 position jumper_.1’” spacing, W2	Samtec
3	W2, W3, W8	TSW-102-07-L-S or equivalent	3 position jumper_.1” spacing, W3	Samtec
2	2X3_JUMPER, W6, W7	TSW-102-07-L-S or equivalent	6-Pin header dual row, 0.025×0.1, 2X3_JUMPER	Samtec

(2) See work order for proper part installation.

User Configurations

This chapter describes the user-definable options.

Topic **Page**

3.1 Schematic Diagram

Figure 3-1 illustrates the EVM schematic.

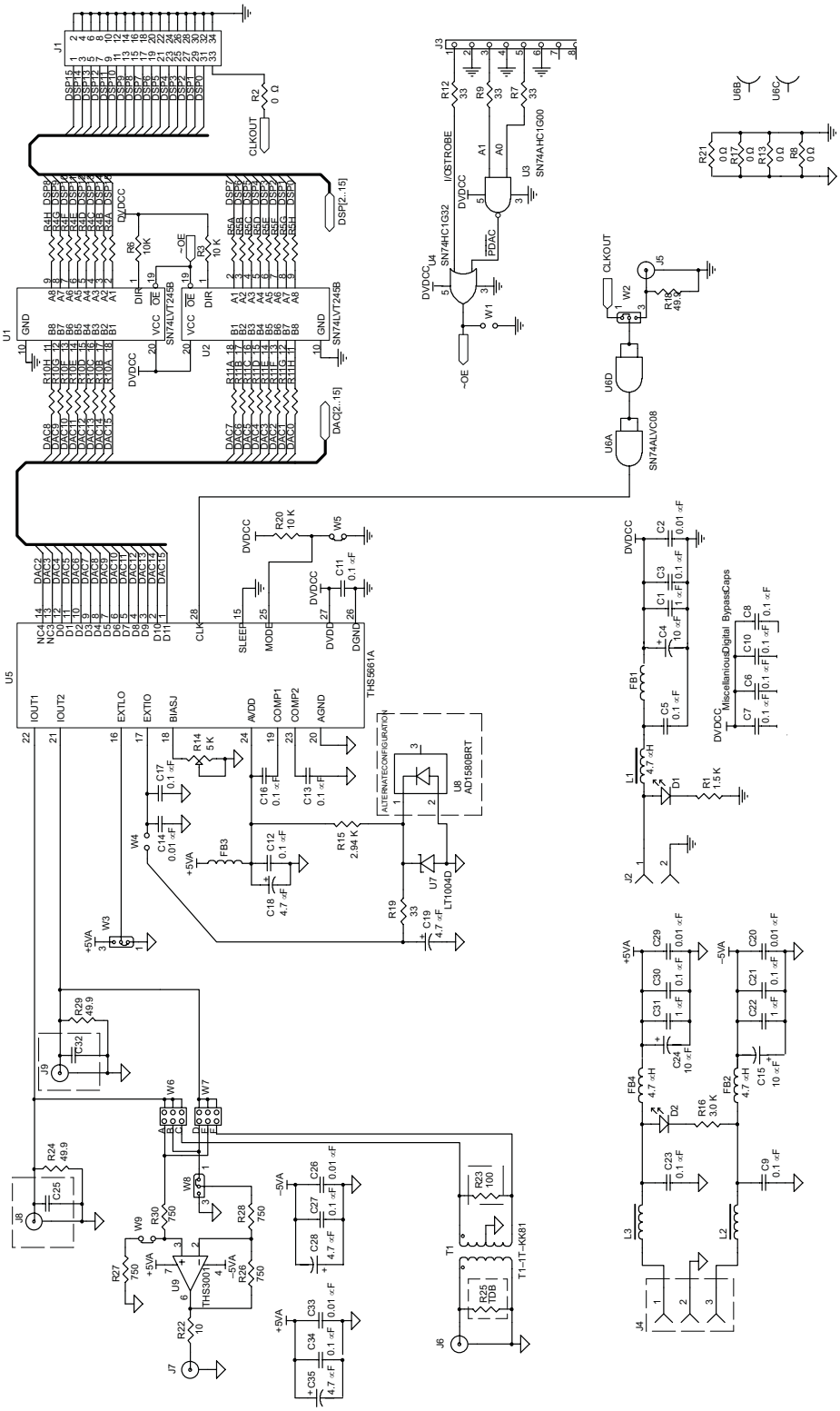

Figure 3-1. EVM Schematic Diagram

3.2 User Options

The PCA ships in a state that enables immediate evaluation of the digital-to-analog converter (DAC). However, you can reconfigure various options through hardware. This chapter discusses these options to ensure that any reconfiguration is conducted properly.

The hardware on the PCA falls into various groups:

- 18 jumpers
- 4 wire links

Table 3-1 lists jumper options, a brief description of each function, and information on where the option can be found.

Table 3-1. Jumper Functions

Jumper Reference	Function Description	Section	Comment
W1	~OE input for the SN74LVT245B buffers	3.4/3.4.2	Wire link
W2	Selects CLKOUT signal from the DSP or clock input from signal gen.	3.8/3.8.1	
W3	Selects external or internal Vref.	3.5.1/5.3.2	
W4	Supplies external Vref to the DAC	3.5.1/ 3.5.2	Wire link
W5	Selects binary input mode or 2s complement input mode to the DAC	4.2	Wire link
W6	Selects IOUT1 or IOUT2 output from DAC to amplifier or transformer	4.3	
W7	Selects IOUT1 or IOUT2 output from DAC to amplifier or transformer	4.3	
W8	Configures the op amp for either differential input, noninverting or inverting mode	3.8.3	
W9	Configures the op amp for inverting, noninverting or differential mode	3.8.3	Wire link

Figure 3-2 indicates the physical locations of this hardware.

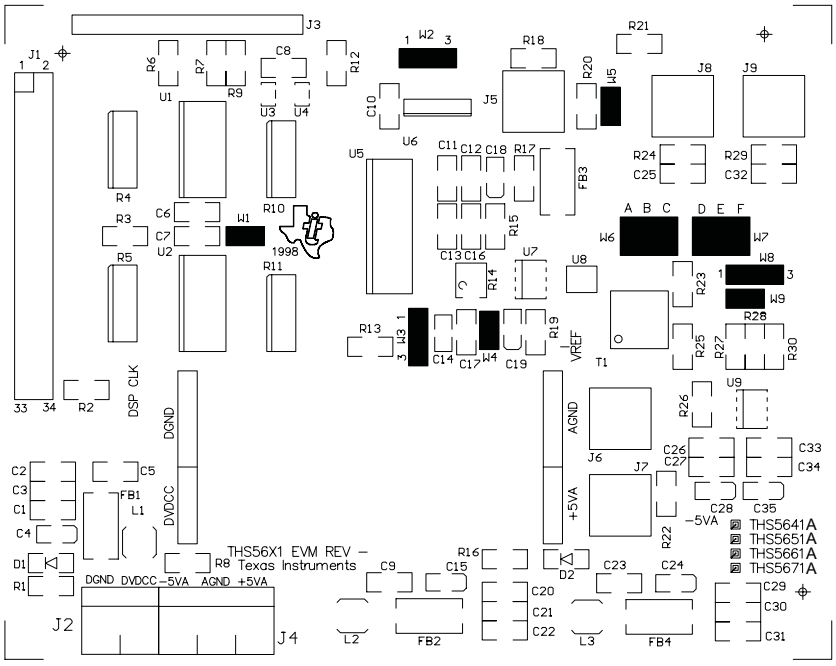

Figure 3-2. Reconfiguration Hardware Location

3.3 Analog/Digital Supply Voltages

Two options supply power to the digital section of the EVM:

- 3.3-V or 5-V digital DVDD (for 5-V operation replace U1 and U2 with SN74HC245)
- 5-V only analog AVDD

Configure the power supply voltages in accordance with the following tables.

Table 3-2. Analog Voltage Supply Configuration Options

J4	J2
J4–1 +5 V	J2–1 +3.3 V
J4–2 AGND	J2–2 DGND
J4–2 –5 V	

3.4 Digital Input Configurations

Various options are available to configure the analog inputs. This section describes these options, along with the jumper settings required.

The two alternatives for the analog inputs are given in the following table.

Table 3-3. Digital Input Options

Analog Input Option	Connector Reference and Type
	IDC
Option 1	
Apply input data/clock from DSP to J1	J1 – 2 × 17 plug
Control signals from DSP to J3	J3 – 1 × 12 plug
Option 2	
Apply input data/clock from pattern generator via an adapter board to J1	J1 – 2 × 17 plug
For control signals connect J1–1 to J1–2; connect +3.3 V to J3–3 and J2–5 (W1 open)	J3 – 1 × 12 plug

The user selects one of the above configurations based on the test equipment available. These are discussed below.

3.4.1 Apply DSP Signals to THS56X1A CommsDAC

If you intend to implement a sine wave signal, as shown in the program in List 1, you will need to store values in a look-up table in the DSP onboard memory. The DSP sequentially outputs the data from the memory via the data bus to the commsDAC, where it is converted into an analog waveform.

DSP 16-bit wide data bus lines are provided via connector J1. Section 3.9 *Connects Pin and Function Assignments*, gives the pin assignments for J1. The THS56X1 EVM to C542 DSKplus interface is shown in Figure 1-4.

3.4.2 Apply Pattern Generator Signals to THS56X1A CommsDAC

Digital inputs can also be taken directly from a pattern generator, via an adapter board, to connectors J1.

In this configuration the user should jumper J3 pin 1 to pin 2 and connect +5 V to J3 pin 3 and pin 5 or simply install W1.

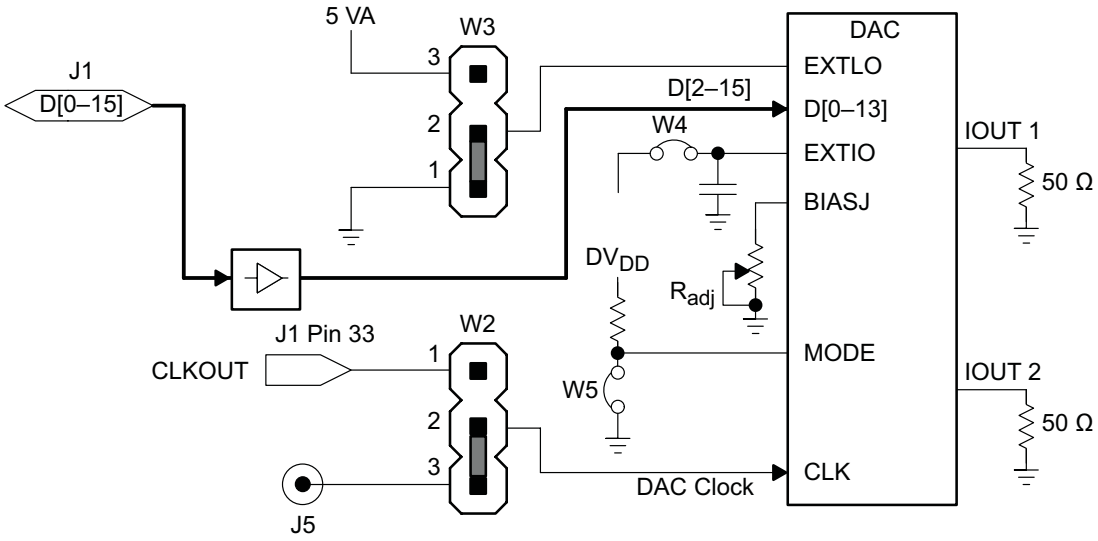

Figure 3-3. Direct Connect Jumper Configuration for THS56X1A

Table 3-4. Shipping Condition of Jumpers W1 Through W9

Jumper	Pins 1 and 2	Pins 2 and 3
W1	Jumper installed	Jumper not installed
W2	Jumper not installed	Jumper installed
W3	Jumper installed	Jumper not installed
W4	Jumper not installed	N/A
W5	Jumper installed	N/A
W6	W7 jumper positioin F to IOUT2	N/A
W7	W7 jumper position C to IOUT1	N/A
W8	Jumper not installed	Jumper installed
W9	Jumper not installed	N/A

3.5 Generating a Voltage Reference

Two options provide the voltage reference:

- Internal reference
- Onboard external reference

3.5.1 Internal Reference

To configure the THS56X1 EVM to use the internal 1.2 V on-chip Vref, set the jumper configuration as shown in Table 3-5. A drawing depicting the jumper placement is shown in Figure 3-4.

Table 3-5. Jumper Configuration for Internal Reference

Jumper	Pins 1 and 2	Pins 2 and 3
VREF setting		
W3	Jumper installed	Jumper not installed
W4	Jumper not installed	N/A

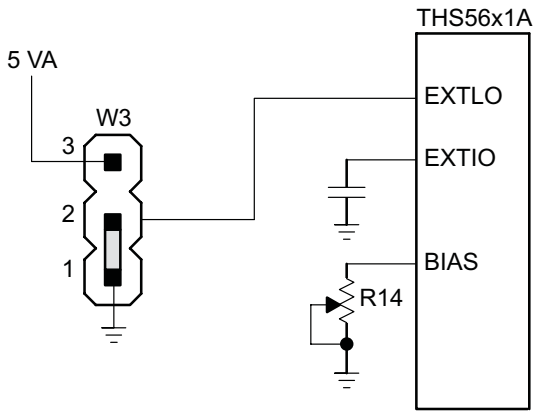

Figure 3-4. Jumper Configuration for Internal Reference Voltage

3.5.2 Onboard External Reference

To select the onboard external reference voltage, the user should follow the jumper configuration shown in Table 3-6.

Table 3-6. Jumper Configuration for External VREF

Jumper	Pins 1 and 2	Pins 2 and 3
VREF setting		
W3	Jumper not installed	N/A
W4	Jumper installed	Jumper not installed

It is important to understand that the reference voltage plays a fundamental part in the conversion process. Changes in the value of the reference voltage are reflected in the full-scale range of the device. The variation in voltage for the reference should, ideally, contribute less than 1/2 an LSB of error to the total conversion process.

External reference voltages can be supplied via W4; see Table 3-5 for details.

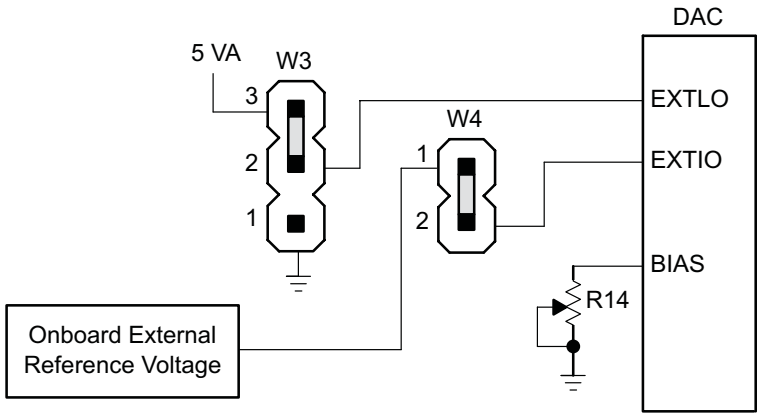

Figure 3-5. Jumper Configuration for External Reference

CAUTION

Under no circumstance should the external reference voltage exceed 1.25 V.

3.6 External Clock

The CommsDAC requires an external clock. Two possible external sources for the clock are required by the CommsDAC. To obtain optimum device performance the user should adhere to the minimum data to clock transition setup and hold times specified in the data sheet SLAS247A. Violating these timing parameters may result in increased converter output noise level. The choices are simple and are discussed in the following sections.

3.6.1 External Clock Generation

When connected to an AVDD supply of 5 V and DVDD supply of 5 V, the maximum operating speed of the CommsDAC is 100 MHz. When the DVDD supply is 3.3 V the maximum clock speed is 67 MHz. The clock signal comes from either the DSP CLKOUT signal or from the CLK output from a pattern generator via J5.

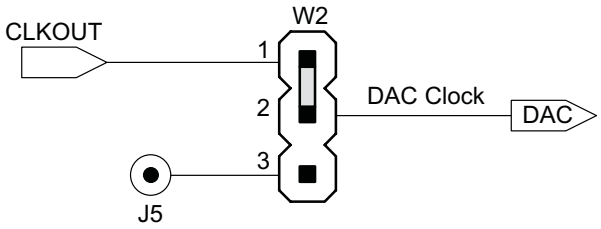

Figure 3-6. External Clock Signal

3.6.2 C542/C54xxDSK/Microprocessor Mode

A DSP subsystem such as the C54X DSPplus/C5410 DSK provides some advantage when evaluating the DAC performance with signals, such as W-CDMA data points and arbitrary generated waveform data points. The clock frequency, via the ’C54x DSK adapter board, is set at 40 MHz.

3.6.3 Analog Output Circuits

The 1:1 RF transformer is used for impedance matching, dc isolation and interfacing between the balanced differential CommsDAC outputs and an unbalanced single-ended output. The resistors R23, R24, and R29 are used to form a network that reflects 50 Ω across the primary circuit (J6).

Potentiometer R14 is used to set the CommsDAC full-scale output current. With R14 value set equal to 1.9 kΩ, the full-scale current from the DAC is 20 mA.

A spectrum analyzer with 50-Ω input impedance is normally used to measure the performance of the DAC. A 50-Ω coaxial cable is used to connect J6 output to the 50-Ω input of the spectrum analyzer. The spectrum analyzer impedance is in parallel to the transformer 50-Ω reflected impedance across J6. Therefore, the voltage at the input of the spectrum analyzer is 1/2 J6. If a larger voltage is required, use a 1:2 step up voltage ratio transformer to produce twice the voltage at J6. In addition set R23 to 200 Ω and remove R24 and R29. R14 may require some adjustments.

A 1-V output will appear at J8 and J9 when IOUT1 and IOUT2 are terminated into 50-Ω external resistor loads (output taken from J8 and J9 and W6 and W7 open). If 75-Ω external resistors are used the maximum IOUT1/IOUT2 output current is 16 mA.

The THS3001 operates as a differential amplifier when: W9 is left opened, W8 pins 1 and 2 are connected together, W6 position A is connected to IOUT1, and W7 position D is connected to IOUT2.

The THS3001 operates as an inverting amplifier under the following conditions: W9 is connected, R27 is set to 0 Ω, W8 pins 1 and 2 are connected together, and the input is from either W6 position B or W7 position D. If the input is via W6 position B, the output at J7 is –1.2 V. If the input is via W7 position D, the output will be –1.2 V.

The THS3001 operates as a noninverting amplifier when: W9 is opened, W8 pins 2 and 3 are connected together, and the input is from either W6 position A or W7 position E. If the input is via W6 position A, the output voltage is 2 V. If the input is taken via W7 position E, the output voltage at J7 is 2 V.

3.7 Connector Pin and Function Assignments

This section details the pinouts and functions for all user connectors.

Table 3-7. Connector Pin and Function Assignments

Reference Designator	Function
J1	Data bits 0 through 13 and CLKOUT input
J2, J4	Supplies power to the EVM
J3	Input control signals used to create EVM chip select
J5	Input for a clock signal source
J6,J7,J8,J9	DAC output signal

Table 3-8. J4 and J2 Power Connectors

Pin Number	Function
J2–1	Digital power 3 V – 5 V
J2–2	DGND
J4–1	Analog power +5 V
J4–2	AGND
J4–3	Analog power –5 V

Table 3-9. J6, J7, J8, and J9 Analog Output Signal Connectors

SMA	Function	SMA	Function
J6–1	Differential to single-ended DAC output via transformer	J6–2	AGND
J7–1	Differential or single-ended DAC output via op amp	J7–2	AGND
J8–1	DAC output IOUT1	J8–2	AGND
J9–1	DAC output IOUT2	J9–2	AGND

Table 3-10. C542/C54xxDSK/Microprocessor Control Connector

Pin Number	Function	Pin Number	Function
1	~ I/OSTROBE	2	Ground (digital)
3	A1	4	Ground (digital)
5	A0	6	Ground (digital)
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC

The control signals are used to generate the device select signal for the THS56X1 EVM. In general more than one device is hooked to the DSP address and data buses.

Table 3-11. J1 Parallel Data Connector

Pin Number	Function	Pin Number	Function
1	DSP_15 (MSB)	2	Ground (digital)
3	DSP_14	4	Ground (digital)
5	DSP_13	6	Ground (digital)
7	DSP_12	8	Ground (digital)
9	DSP_11	10	Ground (digital)
11	DSP_10	12	Ground (digital)
13	DSP_09	14	Ground (digital)
15	DSP_08	16	Ground (digital)
17	DSP_07	18	Ground (digital)
19	DSP_06	20	Ground (digital)
21	DSP_05	22	Ground (digital)
23	DSP_04	24	Ground (digital)
25	DSP_03	26	Ground (digital)
27	DSP_02	28	Ground (digital)
29	DSP_01	30	Ground (digital)
31	DSP_00 (LSB)	32	Ground (digital)
33	CLKOUT	34	Ground (digital)

Table 3-12. Function of Connector J5

Reference	Designator Function
J5	DAC clock input signal via SMA connector

Control Modes

The SLEEP, MODE, EXTLO, EXTIO and BIASJ pins of the THS5671A/ THS5661A/THS5651A/THS5641A control various DAC features and functions. This section describes the function of these pins.

Topic **Page**

4.1 SLEEP Input Pin

The SLEEP pin is used to power down the device. It is an active high asynchronous power-down input. The device has an internal pulldown resistor. So for normal operations of the device, it is not necessary to tie the pin to DGND. The device requires 5 µS to power down and 3 mS to power up. W5 is used to control the SLEEP input.

4.2 MODE Input Pin

MODE bit = 1

When the MODE pin is connected to DVDD, the device is configured to read 2s complement input data.

MODE bit = 0

When the MODE pin is connected to DGND, the device is configured to read binary input data.

4.3 BIASJ Input Pin

For an output current of 20 mA the potentiometer R14 value is typically set to 1.8 kΩ. Owing to the fact that the maximum full-scale current is 20 mA when IOUT1 and IOUT2 are terminated into 50 Ω load resistors, the voltage at J8 and J9 is 1 V.

4.4 EXTLO Input Pin

The internal 1.2 V Vref is selected when the EXTLO pin is grounded (W3 pins 2 and 3 shorted). When EXTLO pin is tied to 5V (W3 pins 2 and 3 shorted) and W4 jumper is in place, the external 1.2 V Vref is selected.

4.5 EXTIO Input Pin

An external reference voltage is provided via the EXTIO input pin. U7 or U8 is used to generate the external reference voltage. Jumper W4 is for selecting the external reference voltage.

Software

The code listed in this chaper runs on the 40 MHz C542 DSKplus. It allows you to output a 220 kHz sinewave from the DAC, while the DAC is being clocked at 40 MHz. Running the code on a 100 MHz C542 DSP or the C5410 DSP will give output sinewave speeds up to 2 MHz. The program is also useful for checking that the THS56X1 EVM is functioning properly.

The complete C-callable assembly code is shown in List 1.

List 1. Complete Software Listing for a Sinewave Generator

```
*************************************************************************
* TITLE           : THS5651 Interface routine                           *

* FILE            : DAC.ASM                                             *
* FUNCTION        : MAIN                                                *
* PROTOTYPE       : void MAIN ()                                        *
* CALLS           : N/A                                                 *
* PRECONDITION    : N/A                                                 *
* POSTCONDITION   : N/A                                                 *
* DESCRIPTION     : main routine is used the generated a sine wave      *
*                 : input for THS56x1 EVM using the 'C542 DSKplus board *
* AUTHOR          : AAP Application Group, L. Philipose, Dallas         *
*                 : CREATED 1999(C) BY TEXAS INSTRUMENTS INCORPORATED.  *
* REFERENCE       : TMS320C54x User's Guide, TI 1997                    *
*                 : Data Aquisation Circuits, TI 1999                   *
*************************************************************************
          .title "THS56x1 sine wave"
          .mmregs
          .width 80
          .length 55
          .version 542


       .sect ".vectors"
       .copy "vectors.asm"

       .sect ".data"
*global Variables
    .global _sinewave
*Local Varibles
AD_DP        .usect ".variabl", 0 ;
TEMP         .usect ".variabl", 1 ; temporary variable
DAC_Sample   .usect ".variabl", 1 ; last readed sample of channel 2

* Address Decoder constants:
DAC     .set 00003h           ; activate A2 when DAC1 is choosen

    .sect ".SINE"
sinevals:
    .word 07FC0h       ;sine wave table.
    .word 0A800h       ;
    .word 0C780h       ;
    .word 0E300h       ;
    .word 0F380h       ;
    .word 0FFC0h       ;
    .word 0FEC0h       ;
    .word 0EB00h       ;
    .word 0D200h       ;
    .word 0B900h       ;
    .word 09440h       ;
    .word 07380h       ;
    .word 05280h       ;
    .word 03080h       ;
    .word 01900h       ;
    .word 00900h       ;
    .word 00000h       ;
    .word 01500h       ;
    .word 02A00h       ;
    .word 04580h       ;
    .word 05E80h       ;


    .sect ".text"
_sinewave:
_MAIN:
START:
INITIALIZATION:


* copy interrupt routine, which are uncritical by the EVM to the IRQ table location:
     DP     = #1;
     AR7    =#00200h;
```

```
        repeat(#3h)
        data(0084h) = *AR7+     ; copy the NMI vector


        AR7    = #00240h
        repeat(#35)
        data(00C0h)  = *AR7+    ; copy INT0, INT1,


* initialize waitstates:
        DP         = #00000h    ; point to page zero
        IFR        = #1         ; reset any old interrupt on pin INT0
        @IMR     | = #01        ; allow INT0
        SXM=#0                  ; no sign extension


* enable global interrupt (this is even required, if no IRQ routine is used
* by this program because the debugger needs to do its backgroud interrupts)
        INTM       = #0         ; enable global IRQ


*Setup up registers
Ready: BK=#21                   ;circular addressing
        AR7=#sinevals           ;Point to sine table
        DP=#sinevals            ;point to correct Data Page


*Loop to repeatedly send Sine Wave
ReSend:
        dgoto ReSend            ;delayed goto (saves cycles)
        port(#0)=   *AR7+%
.end
```

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