

5-CHANNEL DIFFERENTIAL 10:20 MULTIPLEXER SWITCH FOR DVI/HDMI APPLICATIONS

FEATURES

- **Compatible With HDMI v1.2a (Type A) DVI 1.0 High-Speed Digital Interface**
 - Wide Bandwidth to support throughput of over 1.65 Gbps (Data rate 1.9 Gbps Typ)
 - Serial Data Stream at 10x Pixel Clock Rate
 - Supports All Video Formats up to 1080p and SXGA (1280 × 1024 at 75 Hz)
 - Total Raw Capacity 4.95 Gbps (Single Link)
 - HDCP Compatible
- **Compatible with SXGA Video Display formats up to 1080P (1280 × 1024 at 75Hz)**
- **Low Crosstalk ($X_{TALK} = -37$ dB Typ)**
- **Low Bit-to-Bit Skew ($t_{sk(o)} = 0.1$ ns Max)**
- **Low and Flat ON-State Resistance ($r_{on} = 4$ Ω Typ, $r_{on(Flat)} = 0.5$ Ω Typ)**
- **Low Input/Output Capacitance ($C_{ON} = 8$ pF Typ)**
- **Rail-to-Rail Switching on Data I/O Ports (0 to 3.6 V)**
- **V_{CC} Operating Range From 3 V to 3.6 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested**
 - 14-kV Human-Body Model Per JESD 22 (A114-B, Class II)
 - 7.5-kV Contact Discharge Per IEC 61000-4-2

APPLICATIONS

- **DVI/HDMI Signal Switching**
- **Differential DVI, HDMI Signal Multiplexing for Audio/Video Receivers and High-Definition Televisions (HDTVs)**

DESCRIPTION/ORDERING INFORMATION

The TS3DV520E is a 20-bit to 10-bit multiplexer/demultiplexer digital video switch with a single select (SEL) input. SEL controls the data path of the multiplexer/demultiplexer. The device provides five differential channels for digital video signal switching.

This device provides low and flat ON-state resistance (r_{on}) and excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various digital video applications, such as DVI and HDMI.

Voltage on the SEL pin should be less or equal to V_{CC} , even in the power-down mode ($V_{CC} = 0$ V).

ORDERING INFORMATION

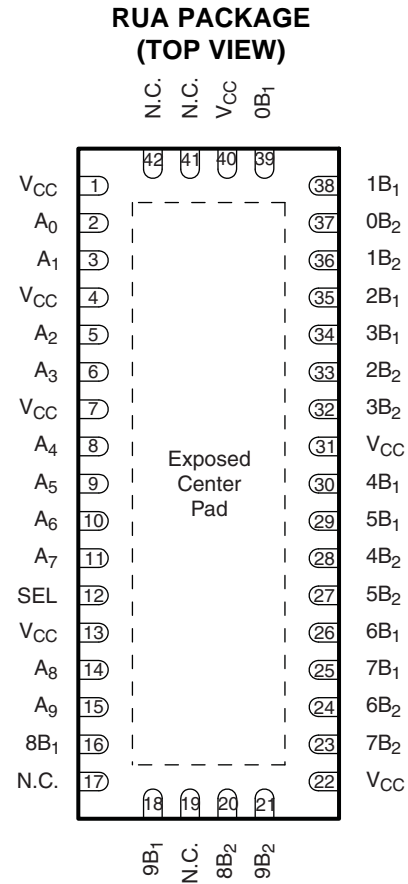
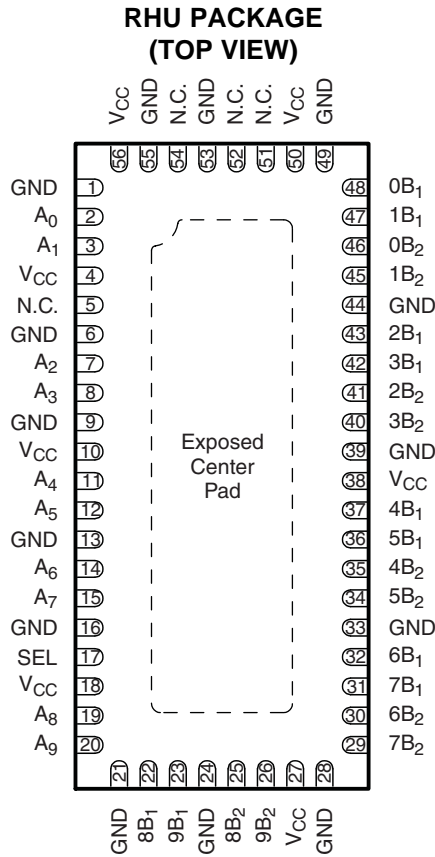
T_A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TQFN – RHU	Reel of 2000	TS3DV520ERHURG4	SD520E
	QFN – RUA	Reel of 2000	TS3DV520ERUAR	SD520E

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



The exposed center pad, if used, must be connected to GND or left electrically open.

The exposed center pad must be connected to GND for proper device operation.

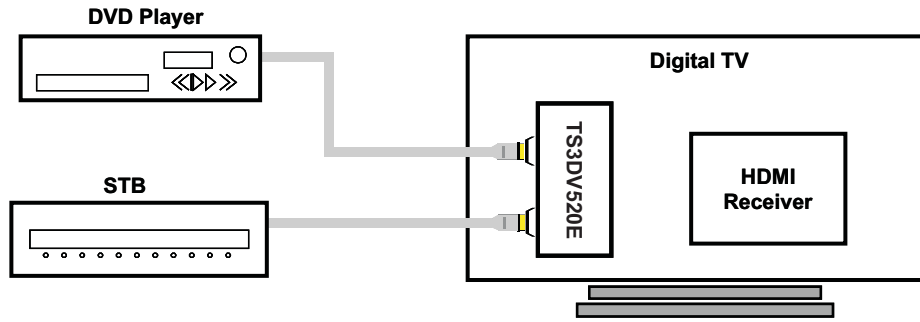
N.C. – No internal connection

FUNCTION TABLE

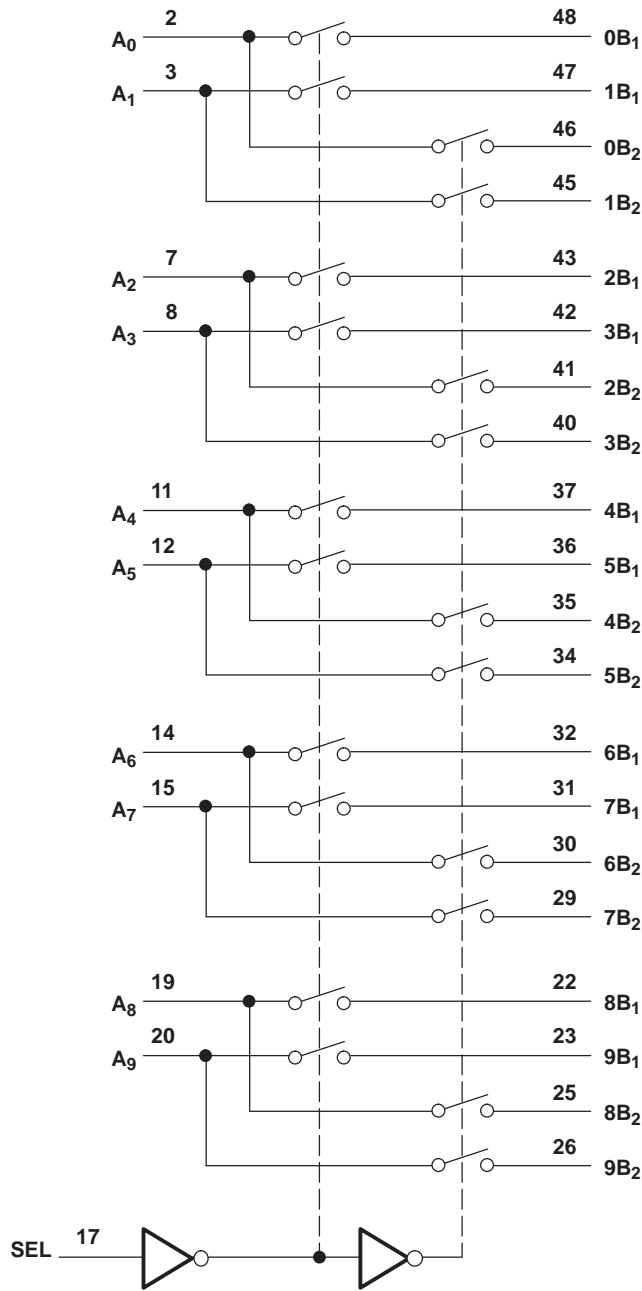
INPUT SEL	INPUT/OUTPUT A _n	FUNCTION	
L	nB ₁	A _n = nB ₁	nB ₂ high-impedance mode
H	nB ₂	A _n = nB ₂	nB ₁ high-impedance mode

PIN DESCRIPTION

NAME	DESCRIPTION
A _n	Data I/O
nB _m	Data I/O
SEL	Select input



LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	4.6	V
V_{IN}	Control input voltage range ⁽²⁾⁽³⁾	–0.5	$V_{CC} + 0.5$	V
$V_{I/O}$	Switch I/O voltage range ⁽²⁾⁽³⁾⁽⁴⁾	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Control input clamp current	$V_{IN} < 0$ or $V_{IN} > V_{CC}$		mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$		mA
$I_{I/O}$	ON-state switch current ⁽⁵⁾		±128	mA
	Continuous current through V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance ⁽⁶⁾	RHU package		°C/W
		RUA package		
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
- (5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage (SEL)	2	V_{CC}	V
V_{IL}	Low-level control input voltage (SEL)	0	0.8	V
$V_{I/O}$	Input/output voltage	0	V_{CC}	V
T_A	Operating free-air temperature	–40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS⁽¹⁾

for high-frequency switching over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
(unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT		
V_{IK}	SEL	$V_{CC} = 3.6 \text{ V}$,	$I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V		
I_{IH}	SEL	$V_{CC} = 3.6 \text{ V}$,	$V_{IN} = V_{CC}$			± 1	μA		
I_{IL}	SEL	$V_{CC} = 3.6 \text{ V}$,	$V_{IN} = \text{GND}$			± 1	μA		
I_{CC}		$V_{CC} = 3.6 \text{ V}$,	$I_{I/O} = 0$,	Switch ON or OFF		250	600	μA	
C_{IN}	SEL	$f = 1 \text{ MHz}$,	$V_{IN} = 0$		2	2.5	pF		
C_{OFF}	B port	$V_I = 0$,	$f = 1 \text{ MHz}$,	Outputs open,	Switch OFF		3	4	pF
C_{ON}		$V_I = 0$,	$f = 1 \text{ MHz}$,	Outputs open,	Switch ON		9	9.8	pF
r_{on}		$V_{CC} = 3 \text{ V}$,	$1.5 \text{ V} \leq V_I \leq V_{CC}$,	$I_O = -40 \text{ mA}$		4	8	Ω	
$r_{on(\text{flat})}$ ⁽³⁾		$V_{CC} = 3 \text{ V}$,	$V_I = 1.5 \text{ V}$ and V_{CC} ,	$I_O = -40 \text{ mA}$		0.7	Ω		
Δr_{on} ⁽⁴⁾		$V_{CC} = 3 \text{ V}$,	$1.5 \text{ V} \leq V_I \leq V_{CC}$,	$I_O = -40 \text{ mA}$		0.2	1.2	Ω	

- (1) V_I , V_O , I_I , and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at $V_{CC} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.
(3) $r_{on(\text{flat})}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} from center (A_4 , A_5) ports to any other port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $R_L = 200 \Omega$, $C_L = 10 \text{ pF}$
(unless otherwise noted) (see [Figure 5](#) and [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{pd} ⁽²⁾	A or B	B or A		0.25		ns
t_{PZH} , t_{PZL}	SEL	A or B	0.5		15	ns
t_{PHZ} , t_{PLZ}	SEL	A or B	0.5		9	ns
$t_{sk(o)}$ ⁽³⁾	A or B	B or A		0.05	0.1	ns
$t_{sk(p)}$ ⁽⁴⁾				0.05	0.1	ns

- (1) All typical values are at $V_{CC} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port (A_4 to A_5) to any other port
(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP ⁽¹⁾	UNIT
X_{TALK}	$R_L = 100 \Omega$,	$f = 250 \text{ MHz}$,	See Figure 8	-37	dB
O_{IRR}	$R_L = 100 \Omega$,	$f = 250 \text{ MHz}$,	See Figure 9	-37	dB
BW	$R_L = 100 \Omega$,	See Figure 7		950	MHz

- (1) All typical values are at $V_{CC} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

OPERATING CHARACTERISTICS

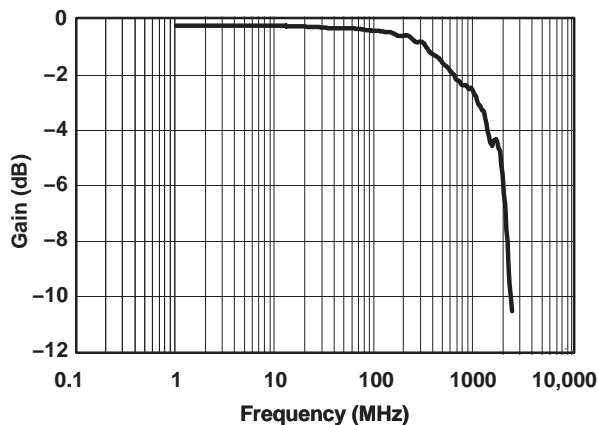


Figure 1. Gain/Phase vs Frequency

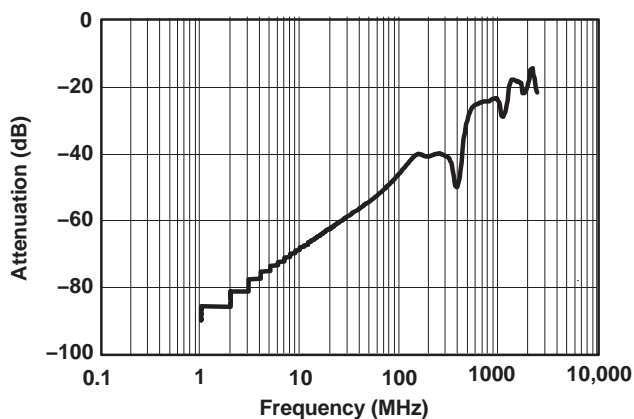


Figure 2. OFF Isolation vs Frequency

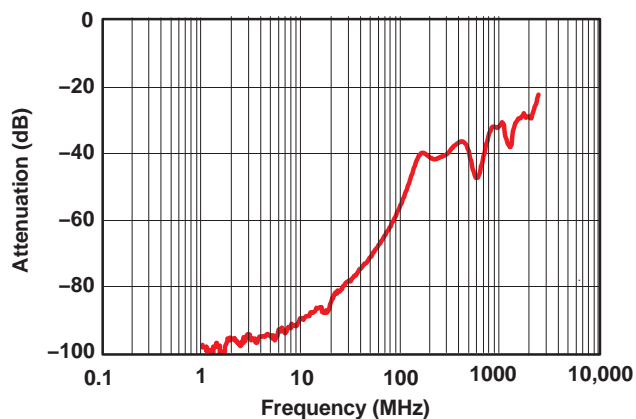


Figure 3. Crosstalk vs Frequency

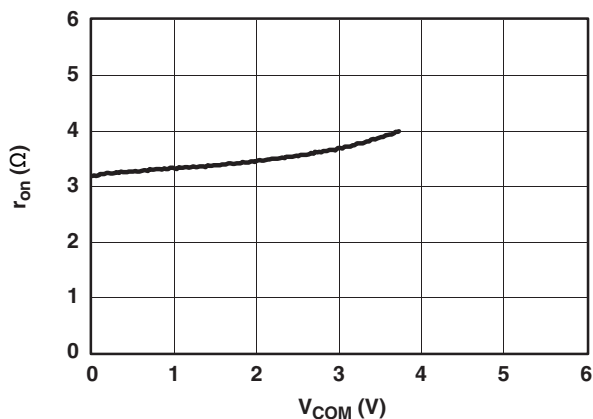
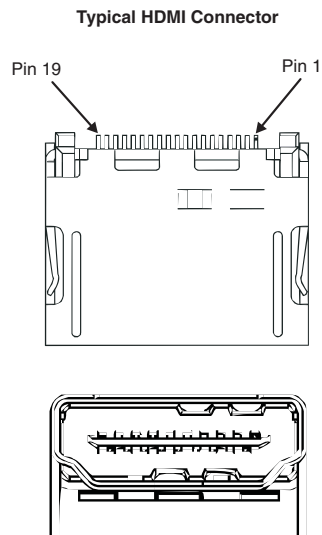
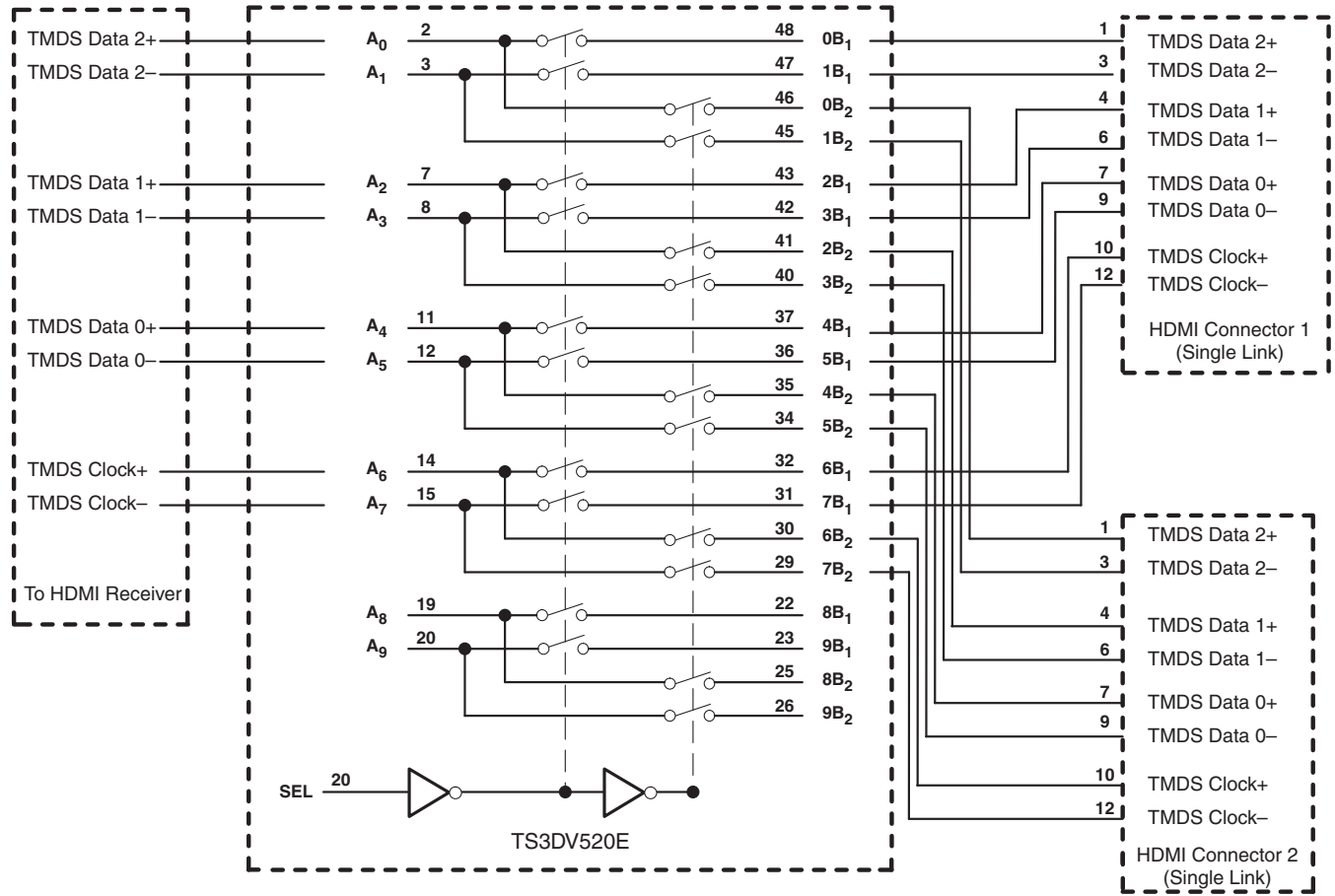


Figure 4. r_{on} vs V_{COM} ($V_{CC} = 3.6\text{ V}$)

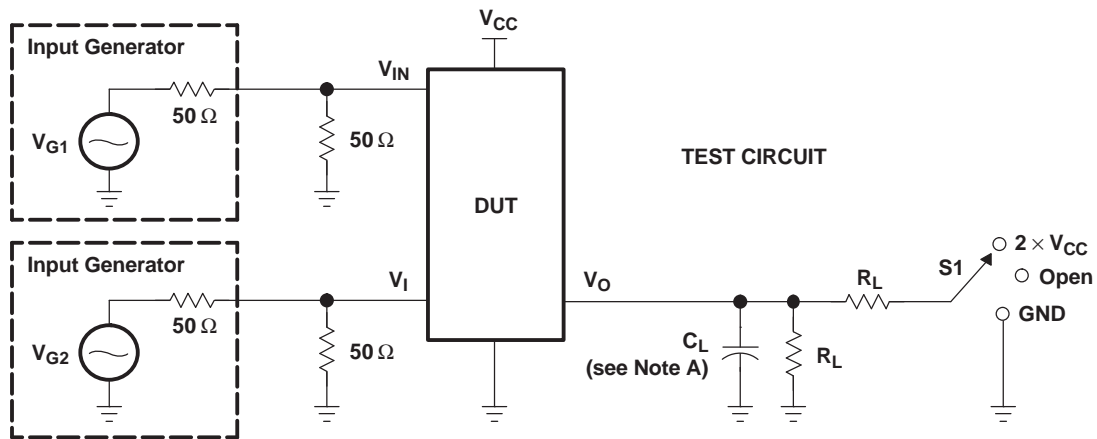
APPLICATION INFORMATION



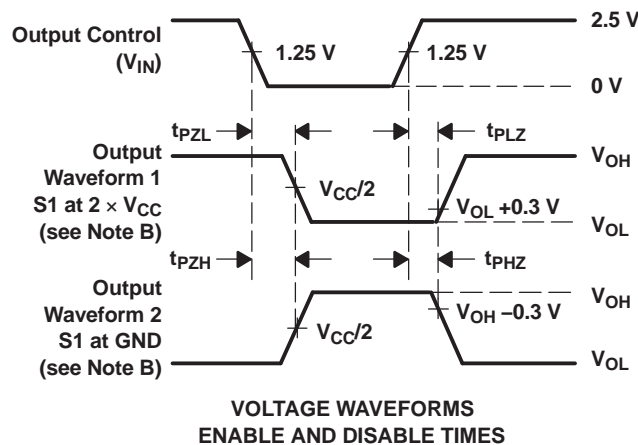
Pin	Signal Assignment
1	TMDS Data 2+
2	TMDS Data 2 Shield
3	TMDS Data 2–
4	TMDS Data 1+
5	TMDS Data 1 Shield
6	TMDS Data 1–
7	TMDS Data 0+
8	TMDS Data 0 Shield
9	TMDS Data 0–
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock–
13	CEC
14	Reserved (N.C. on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	5 V Power
19	Hot Plug Detect

The TS3DV520E can be used to switch between two digital video ports.

PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



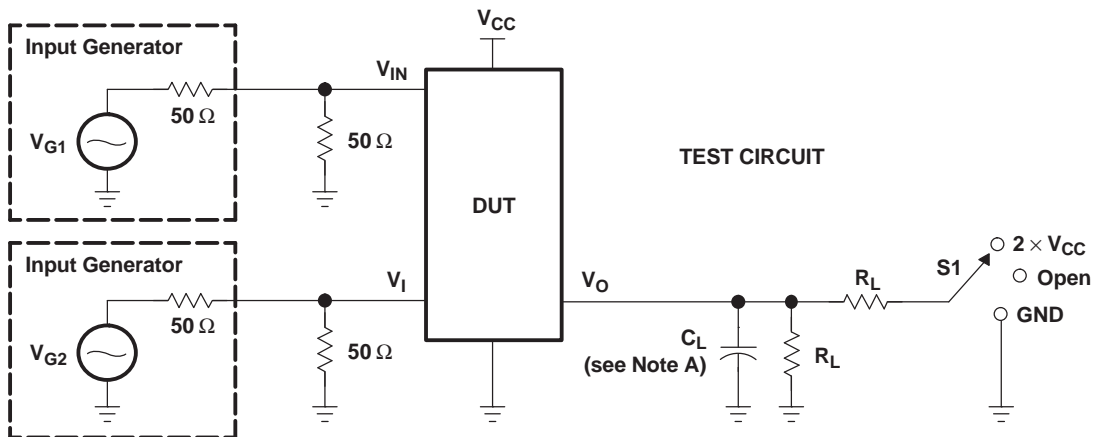
TEST	V_{CC}	S1	R_L	V_I	C_L	V_{Δ}
t_{PLZ}/t_{PZL}	$3.3\text{ V} \pm 0.3\text{ V}$	$2 \times V_{CC}$	$200\ \Omega$	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	$3.3\text{ V} \pm 0.3\text{ V}$	GND	$200\ \Omega$	V_{CC}	10 pF	0.3 V



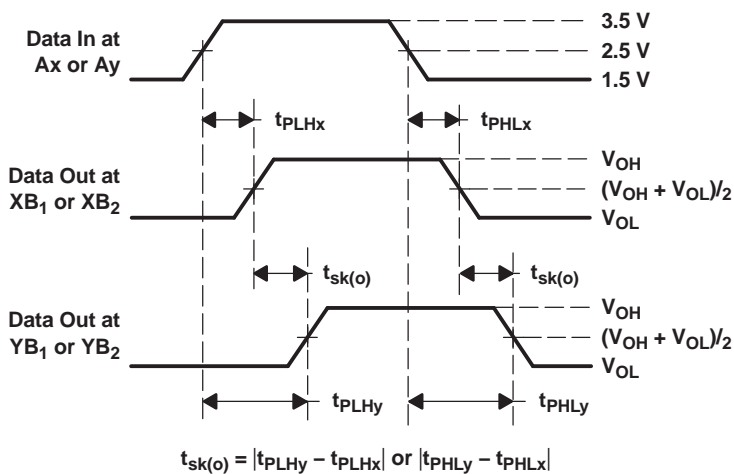
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 5. Test Circuit and Voltage Waveforms

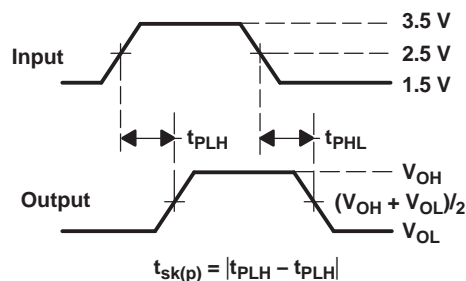
PARAMETER MEASUREMENT INFORMATION (Skew)



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{sk(o)}	3.3 V ± 0.3 V	Open	200 Ω	V _{CC} or GND	10 pF	
t _{sk(p)}	3.3 V ± 0.3 V	Open	200 Ω	V _{CC} or GND	10 pF	



**VOLTAGE WAVEFORMS
OUTPUT SKEW (t_{sk(o)})**



**VOLTAGE WAVEFORMS
PULSE SKEW (t_{sk(p)})**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 6. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

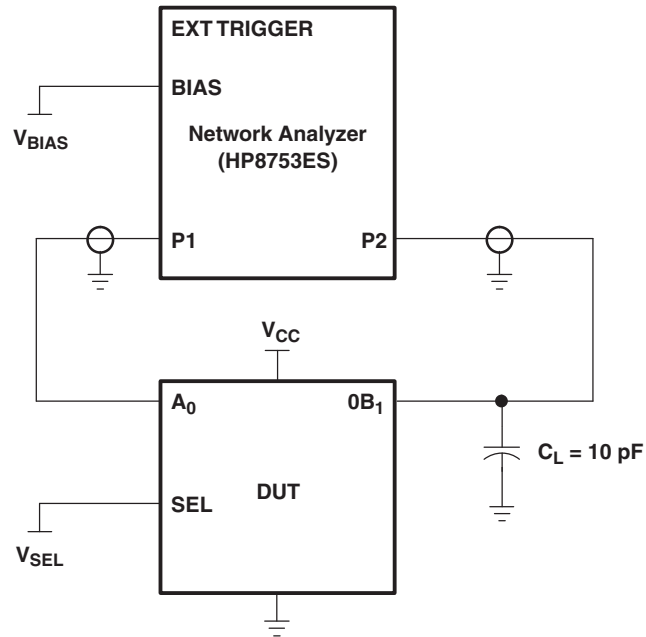


Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_{SEL} = 0$ and A₀ is the input, the output is measured at 0B₁. All unused analog I/O ports are left open.

HP8753ES setup

Average = 4

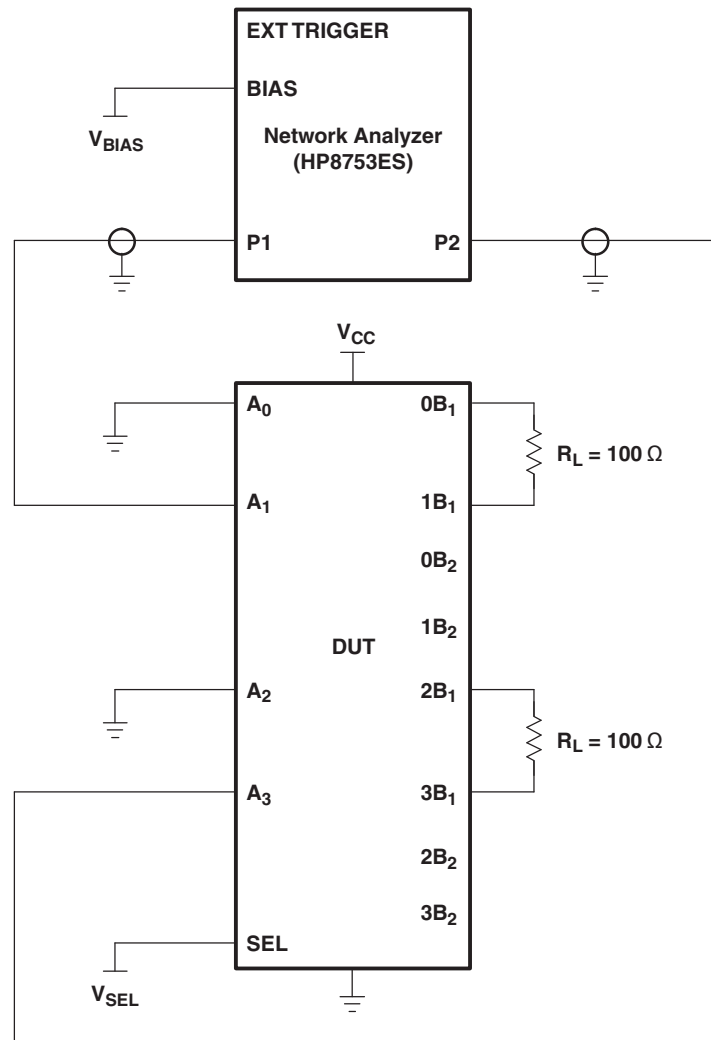
RBW = 3 kHz

$V_{BIAS} = 0.35$ V

ST = 2 s

P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION



- A. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

Figure 8. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{SEL} = 0$ and A_0 is the input, the output is measured at $1B_1$. All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through 50- Ω pull-down resistors.

HP8753ES setup

Average = 4

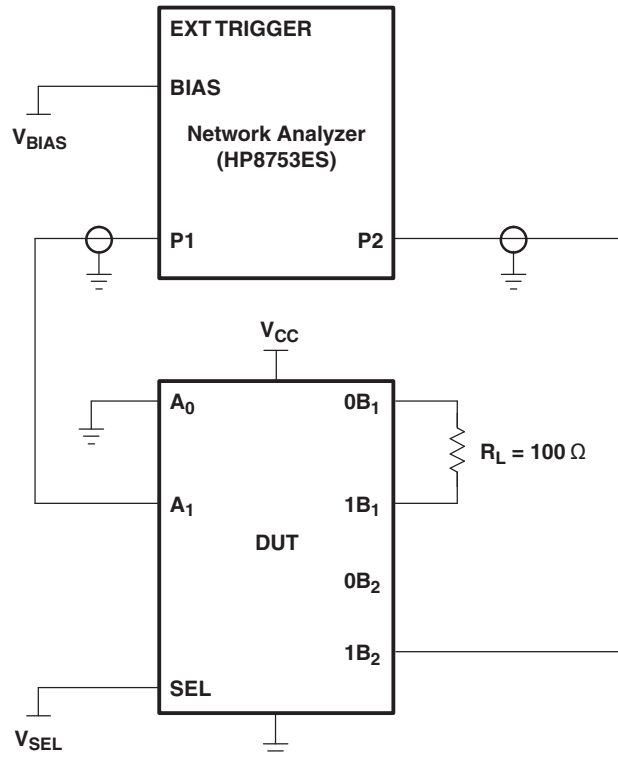
RBW = 3 kHz

$V_{BIAS} = 0.35$ V

ST = 2 s

P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION



- A. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

Figure 9. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_{SEL} = V_{CC}$ and A_0 is the input, the output is measured at $0B_2$. All unused analog input (A) ports are left open, and output (B) ports are connected to GND through 50- Ω pull-down resistors.

HP8753ES setup

Average = 4

RBW = 3 kHz

$V_{BIAS} = 0.35$ V

ST = 2

P1 = 0 dBm

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DV520ERUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	SD520E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

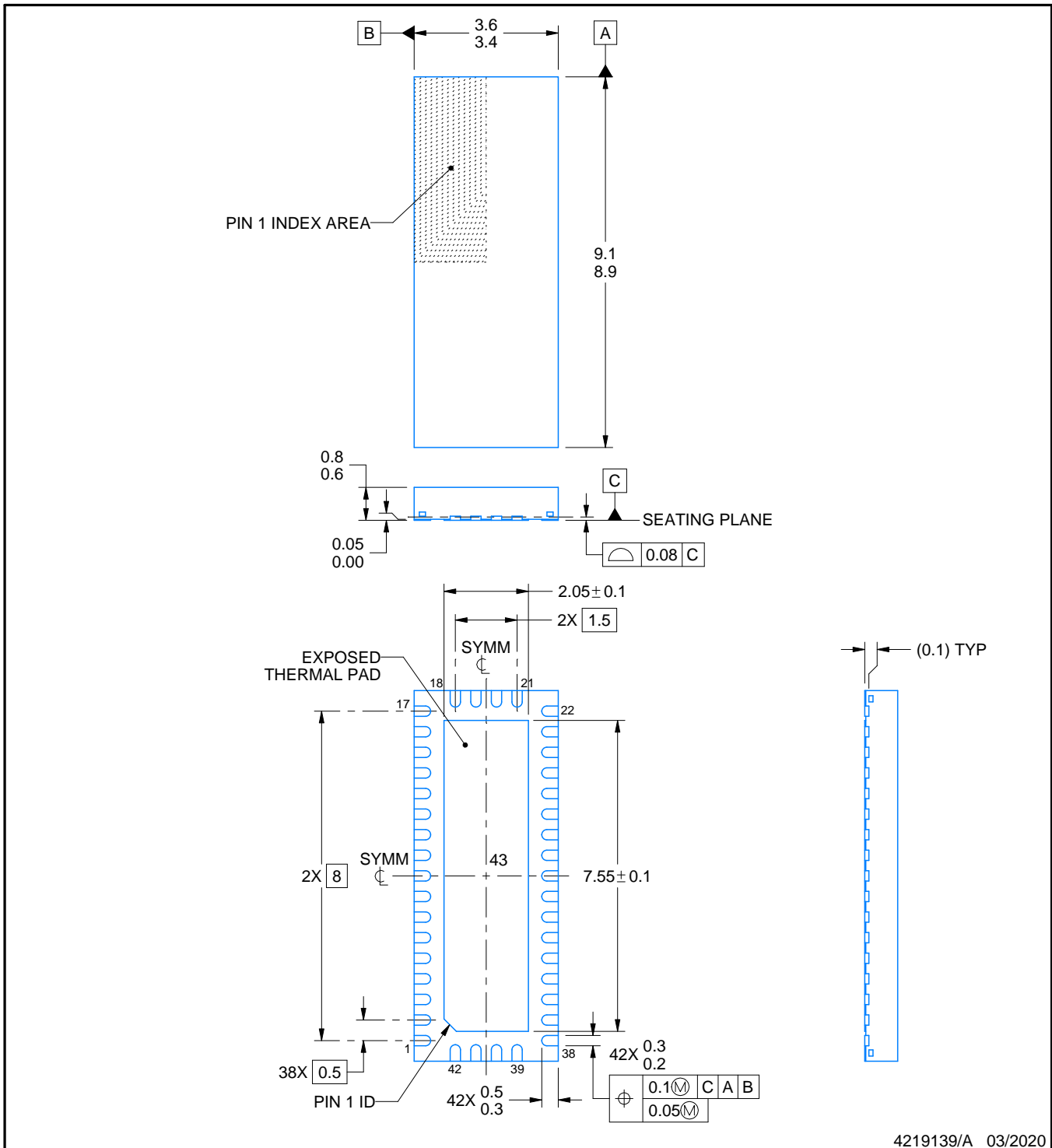
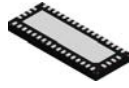
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV520ERUAR	WQFN	RUA	42	3000	330.0	24.4	3.9	9.4	1.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV520ERUAR	WQFN	RUA	42	3000	346.0	346.0	35.0



NOTES:

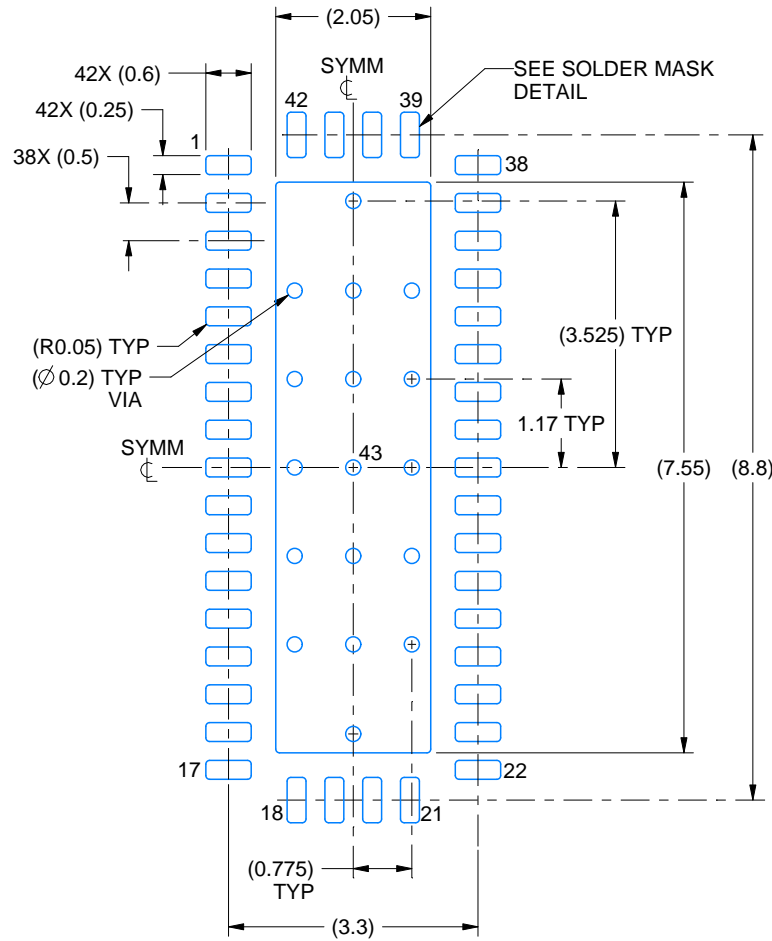
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

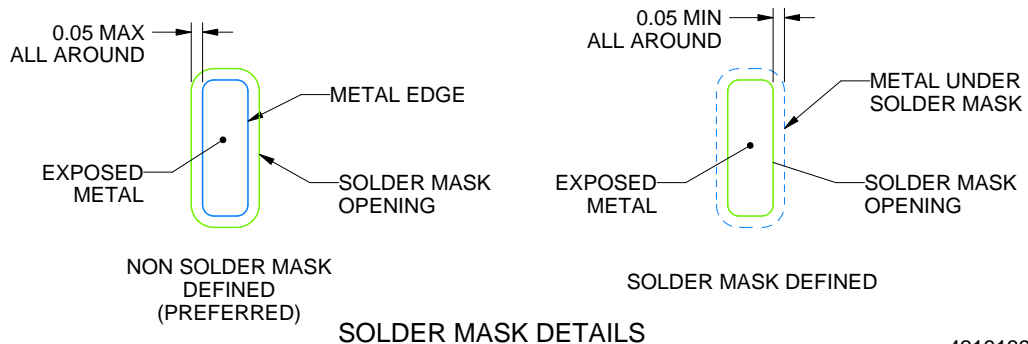
RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4219139/A 03/2020

NOTES: (continued)

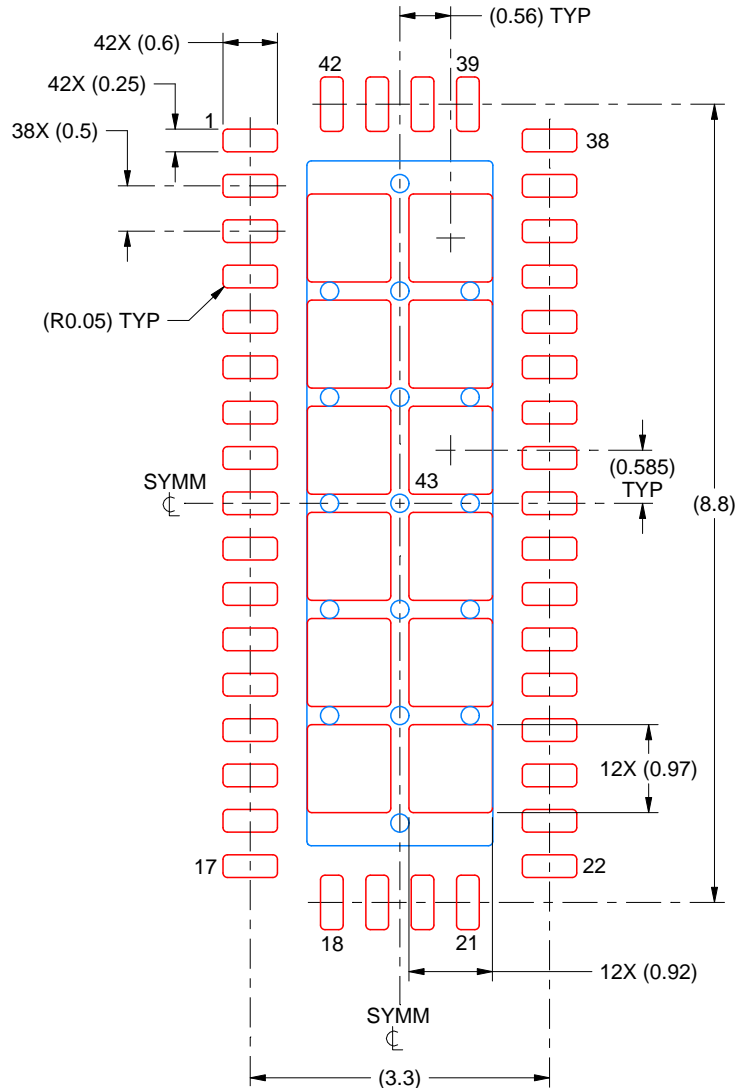
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219139/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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