MC14094B

8-Stage Shift/Store Register with Three-State Outputs

The MC14094B combines an 8−stage shift register with a data latch for each stage and a 3−state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high−speed cascaded systems. The Q_S output data is shifted on the following negative clock transition for use in low−speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by 3−state buffers which are placed in the high−impedance state by a logic Low on Output Enable.

Features

- 3−State Outputs
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial−to−Parallel Data Conversion
- Pin−for−Pin Compatible with CD4094B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Temperature Derating: "D/DW" Packages: −7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
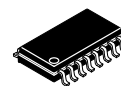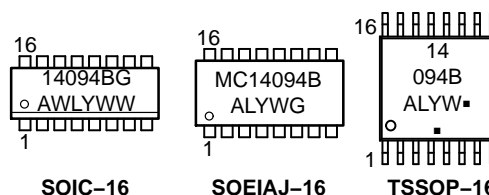
MC14094B

PIN ASSIGNMENT

```
      STROBE [ 1 •        16 ] V_DD
        DATA [ 2          15 ] OUTPUT
                               ENABLE
       CLOCK [ 3          14 ] Q5
          Q1 [ 4          13 ] Q6
          Q2 [ 5          12 ] Q7
          Q3 [ 6          11 ] Q8
          Q4 [ 7          10 ] Q'_S
        V_SS [ 8           9 ] Q_S
```
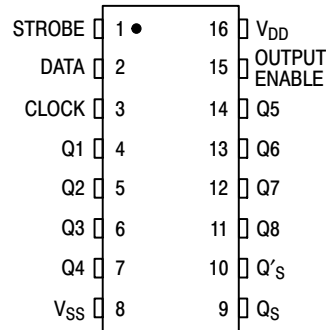
TRUTH TABLE

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S*	Q'_S
⌐⌐	0	X	X	Z	Z	Q7	No Chg.
⌐⌐	0	X	X	Z	Z	No Chg.	Q7
⌐⌐	1	0	X	No Chg.	No Chg.	Q7	No Chg.
⌐⌐	1	1	0	0	Q_N−1	Q7	No Chg.
⌐⌐	1	1	1	1	Q_N−1	Q7	No Chg.
⌐⌐	1	1	1	No Chg.	No Chg.	No Chg.	Q7

Z = High Impedance   X = Don't Care

* At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

ORDERING INFORMATION

Device	Package	Shipping†
MC14094BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14094BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14094BDR2G*	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
MC14094BDTR2G	TSSOP−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14094BDTR2G*	TSSOP−16 (Pb−Free)	2500 Units / Tape & Reel
MC14094BFELG	SOEIAJ−16 (Pb−Free)	2000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
$V_{in} = 0$ or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	− − − −	−2.4 −0.51 −1.3 −3.4	−4.2 −0.88 −2.25 −8.8	− − − −	−1.7 −0.36 −0.9 −2.4	− − − −	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	− − −	0.51 1.3 3.4	0.88 2.25 8.8	− − −	0.36 0.9 2.4	− − −	mAdc
Input Current		I_{in}	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	µAdc
Input Capacitance ($V_{in} = 0$)		C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	− − −	5.0 10 20	− − −	0.005 0.010 0.015	5.0 10 20	− − −	150 300 600	µAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15		I_T = (4.1 µA/kHz) f + I_{DD} I_T = (14 µA/kHz) f + I_{DD} I_T = (140 µA/kHz) f + I_{DD}					µAdc
3–State Output Leakage Current		I_{TL}	15	−	±0.1	−	±0.0001	±0.1	−	±3.0	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L − 50) \text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = ($V_{DD} − V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

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SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time (Figure 1)	t_{PLH}, t_{PHL}					ns
Clock to Serial out QS						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	–	350	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C L + 82 ns		15	–	95	190	
Clock to Serial out Q'S						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 350 ns		5.0	–	230	460	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 149 ns		10	–	110	220	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	–	75	150	
Clock to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 375 ns		5.0	–	420	840	
t_{PLH}, t_{PHL} = (0.35 ns/pF) C_L + 177 ns		10	–	195	390	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 122 ns		15	–	135	270	
Strobe to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 245 ns		5.0	–	290	580	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C L + 127 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	200	
Output Enable to Output	t_{PHZ}, t_{PZL}					
t_{PHZ}, t_{PZL} = (0.90 ns/pF) C_L + 95 ns		5.0	–	140	280	
t_{PHZ}, t_{PZL} = (0.36 ns/PF) C_L + 57 ns		10	–	75	150	
t_{PHZ}, t_{PZL} = (0.26 ns/pF) C_L + 42 ns		15	–	55	110	
t_{PLZ}, t_{PZH} = (0.90 ns/pF) C_L + 180 ns	t_{PLZ}, t_{PZH}	5.0	–	225	450	
t_{PLZ}, t_{PZH} = (0.36 ns/pF) C_L + 77 ns		10	–	95	190	
t_{PLZ}, t_{PZH} = (0.26 ns/pF) C_L + 57 ns		15	–	70	140	
Setup Time	t_{su}	5.0	125	60	–	ns
Data in to Clock		10	55	30	–	
		15	35	20	–	
Hold Time	t_h	5.0	0	– 40	–	ns
Clock to Data		10	20	– 10	–	
		15	20	0	–	
Clock Pulse Width, High	t_{WH}	5.0	200	100	–	ns
		10	100	50	–	
		15	83	40	–	
Clock Rise and Fall Time	$t_{r(cl)}$ $t_{f(cl)}$	5	–	–	15	μs
		10	–	–	5.0	
		15	–	–	4.0	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.25	MHz
		10	–	5.0	2.5	
		15	–	6.0	3.0	
Strobe Pulse Width	t_{WL}	5.0	200	100	–	ns
		10	80	40	–	
		15	70	35	–	

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
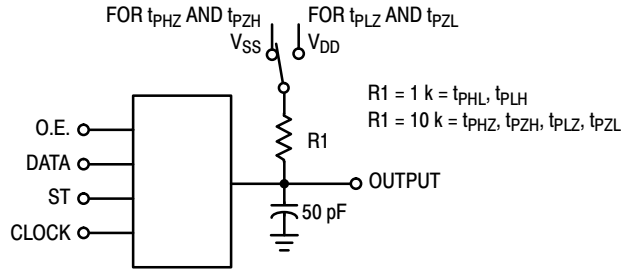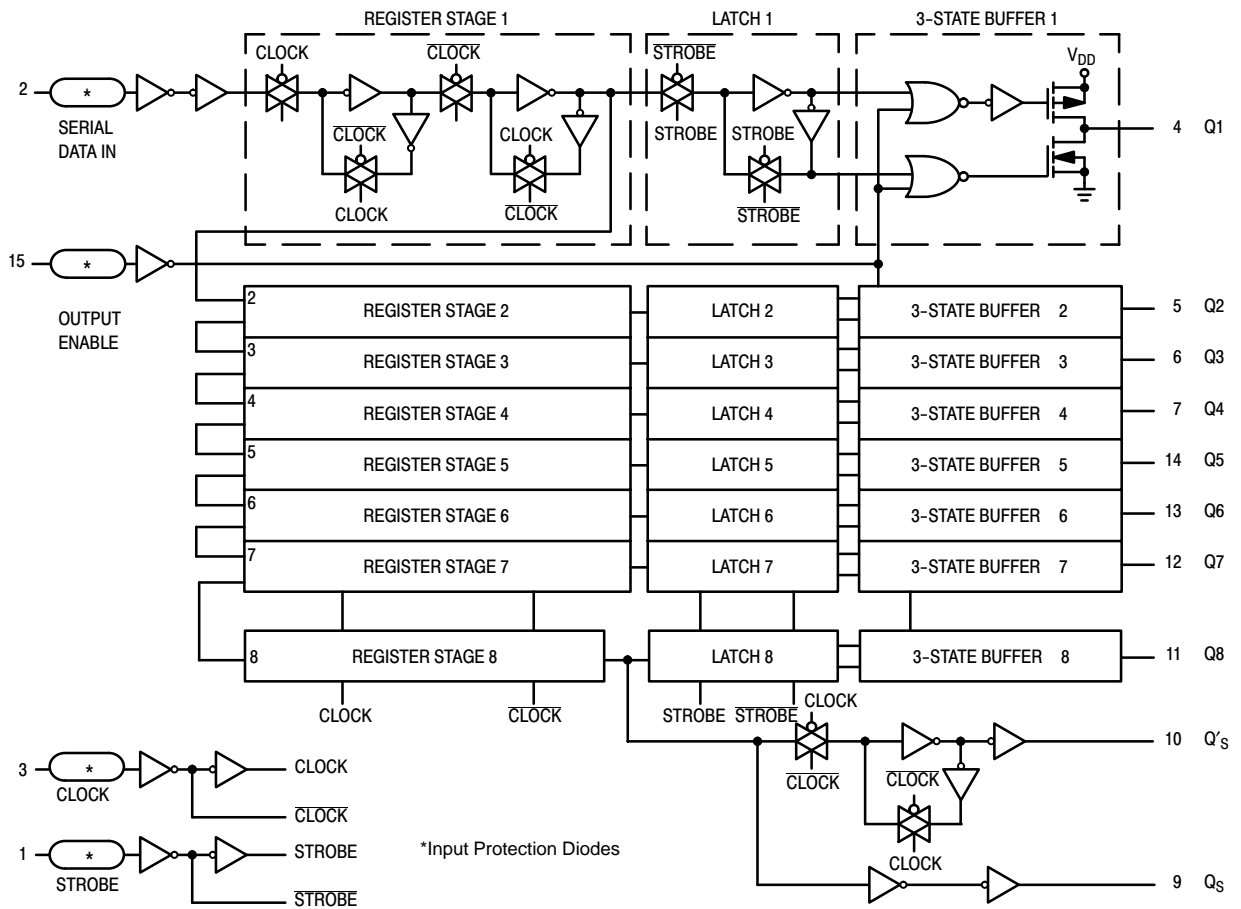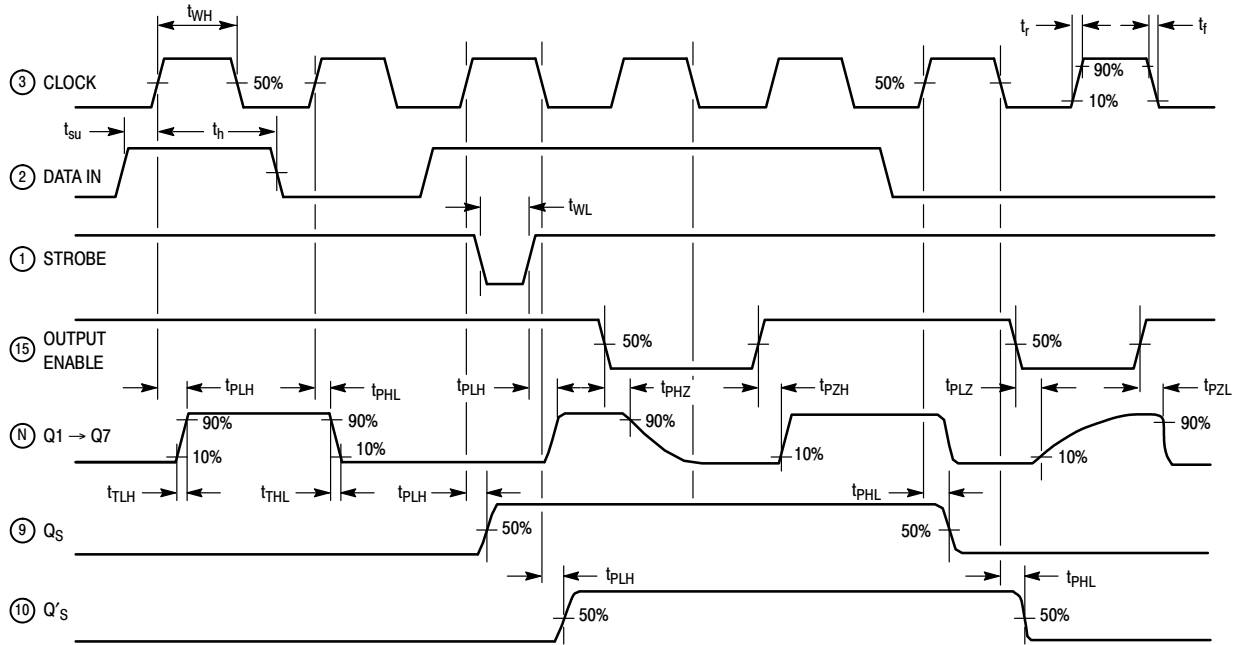
MC14094B

3−STATE TEST CIRCUIT

FOR t_{PHZ} AND t_{PZH} FOR t_{PLZ} AND t_{PZL}

V_{SS} V_{DD}

O.E.

DATA

ST

CLOCK

R1

OUTPUT

50 pF

$R1 = 1\ k = t_{PHL}, t_{PLH}$
$R1 = 10\ k = t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL}$

Figure 1.

BLOCK DIAGRAM

REGISTER STAGE 1   LATCH 1   3−STATE BUFFER 1

2   SERIAL DATA IN

CLOCK   CLOCK   STROBE V_{DD}

CLOCK   CLOCK   STROBE   STROBE

CLOCK   CLOCK   STROBE

4   Q1

15   OUTPUT ENABLE

2	REGISTER STAGE 2	LATCH 2	3−STATE BUFFER 2	5	Q2
3	REGISTER STAGE 3	LATCH 3	3−STATE BUFFER 3	6	Q3
4	REGISTER STAGE 4	LATCH 4	3−STATE BUFFER 4	7	Q4
5	REGISTER STAGE 5	LATCH 5	3−STATE BUFFER 5	14	Q5
6	REGISTER STAGE 6	LATCH 6	3−STATE BUFFER 6	13	Q6
7	REGISTER STAGE 7	LATCH 7	3−STATE BUFFER 7	12	Q7
8	REGISTER STAGE 8	LATCH 8	3−STATE BUFFER 8	11	Q8

CLOCK   CLOCK   STROBE   STROBE   CLOCK

CLOCK   CLOCK

10   Q'$_S$

3   CLOCK   CLOCK   CLOCK

CLOCK

1   STROBE   STROBE   CLOCK

STROBE

*Input Protection Diodes

9   Q$_S$

MC14094B

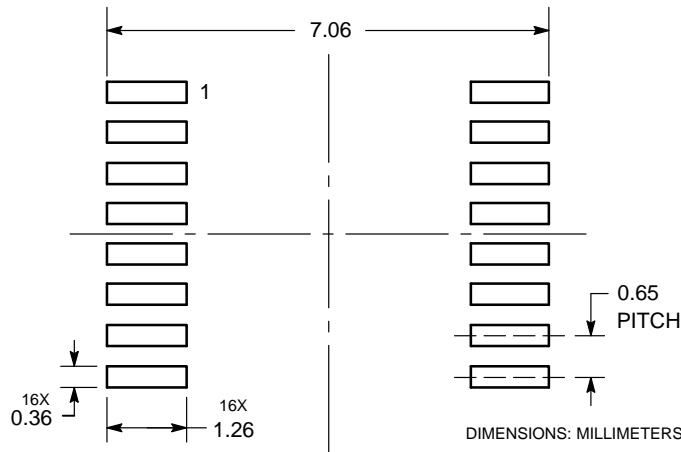## DYNAMIC TIMING DIAGRAM

MC14094B

PACKAGE DIMENSIONS

SOIC−16
D SUFFIX
CASE 751B−05
ISSUE K
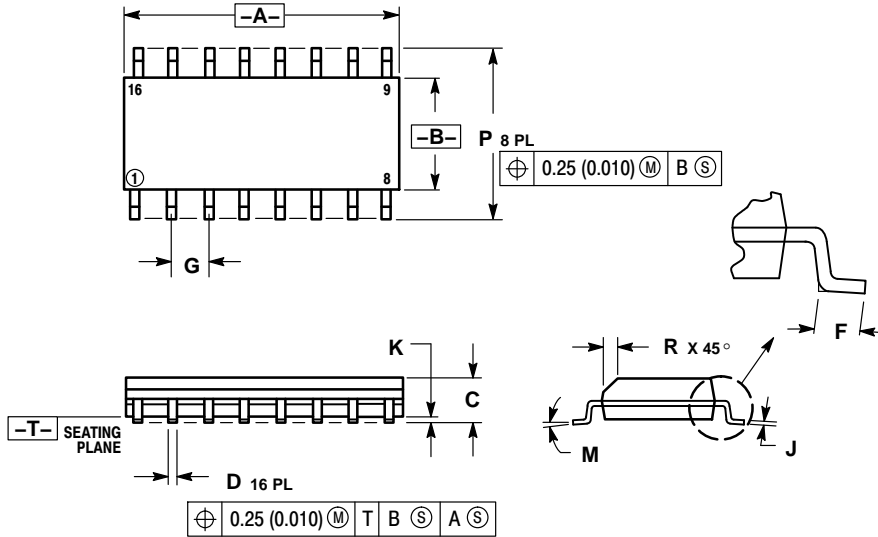
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

## SOLDERING FOOTPRINT*
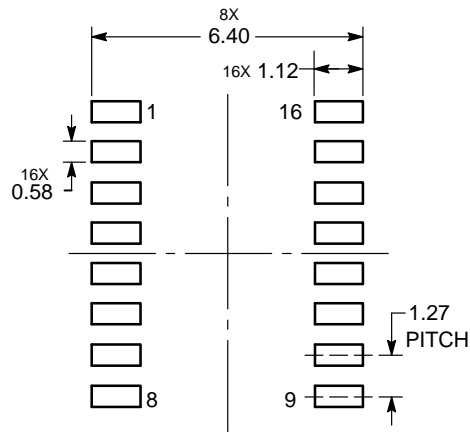
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14094B

PACKAGE DIMENSIONS

TSSOP−16
DT SUFFIX
CASE 948F
ISSUE B
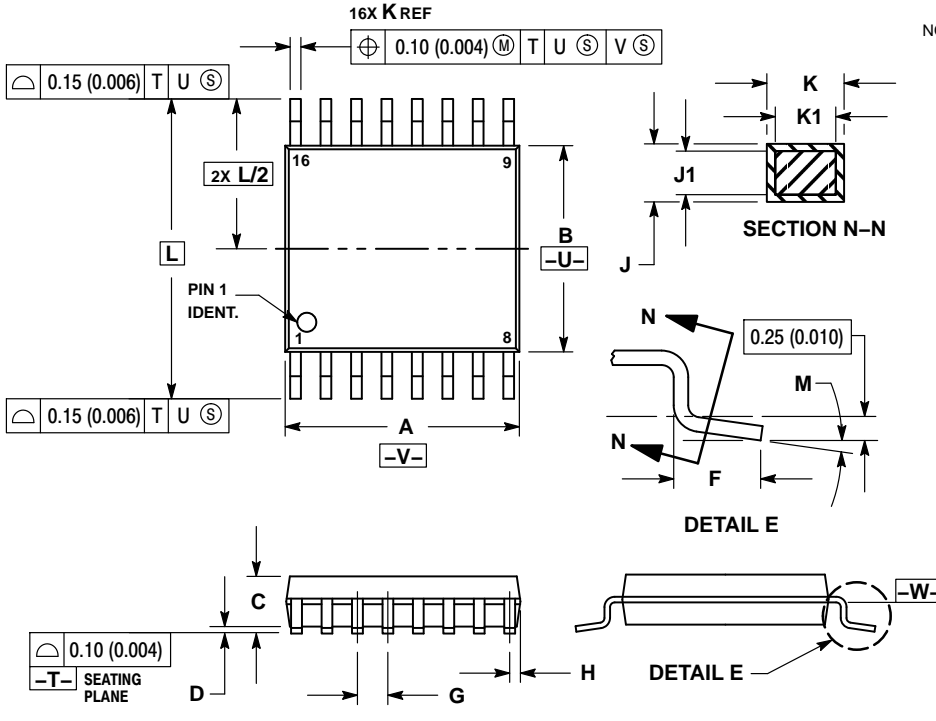
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

SECTION N−N

DETAIL E

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	–––	1.20	–––	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*

7.06

0.65 PITCH

16X 0.36

16X 1.26

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOEIAJ–16
F SUFFIX
CASE 966
ISSUE A
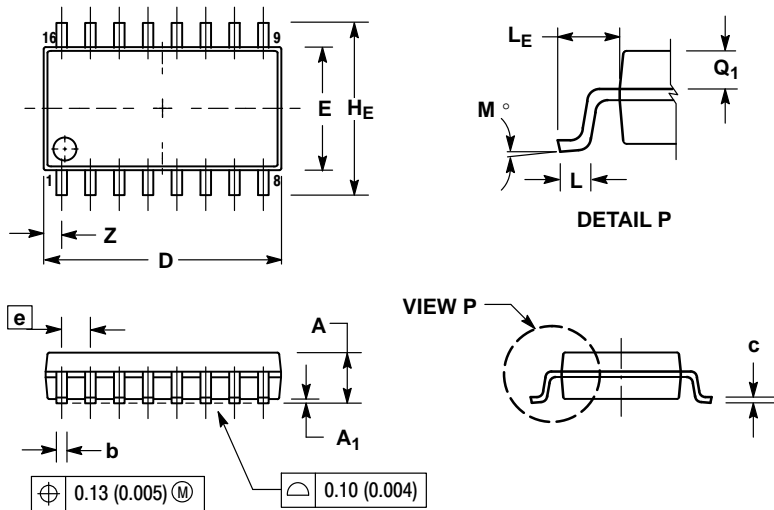
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DETAIL P

VIEW P

⊕ | 0.13 (0.005) Ⓜ

⌂ | 0.10 (0.004)

DIM	MILLIMETERS		INCHES	
	MIN	**MAX**	**MIN**	**MAX**
A	---	2.05	---	0.081
A₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

MC14094B/D

Mouser Electronics

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