LM4947 Boomer® Audio Power Amplifier Series Mono Class D and Stereo Audio Sub-System with OCL Headphone Amplifier and TI 3D

Check for Samples: LM4947, LM4947TLEVAL

FEATURES

- **I²C Control Interface**
- **I²C Programmable Texas Instruments 3D Audio**
- **I²C Controlled 32 Step Digital Volume Control (-59.5dB to +18dB)**
- **Three Independent Volume Channels (Left, Right, Mono)**
- **Eight Distinct Output Modes**
- **Small, 25–Bump DSBGA Packaging**
- **"Click and Pop" Suppression Circuitry**
- **Thermal Shutdown Protection**
- **Low Shutdown Current (0.1µA, typ)**
- **RF Suppression**
- **Differential Mono and Stereo Inputs**
- **Stereo Input Mux**

KEY SPECIFICATIONS

- **THD+N at 1kHz, 500mW into 8Ω BTL (3.3V): 1.0% (typ)**
- **THD+N at 1kHz, 37mW into 32Ω SE (3.3V): 1.0% (typ)**
- **Single Supply Operation (V_{DD}): 2.7 to 5.5 V**
- **I²C Single Supply Operation: 2.2 to 5.5 V**

APPLICATIONS

- **Mobile Phones**
- **PDAs**

DESCRIPTION

The LM4947 is an audio subsystem capable of efficiently delivering 500mW (Class D operation) of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N, 37mW (Class AB operation) power channel of continuous average power into stereo 32Ω single-ended (SE) loads with 1% THD+N, or an output capacitor-less (OCL) configuration with identical specification as the SE configuration, from a 3.3V power supply.

The LM4947 has six input channels: one pair for a two-channel stereo signal, the second pair for a secondary two-channel stereo input, and the third pair for a differential single-channel mono input. Additionally, the two sets of stereo inputs may be configured as a single stereo differential input (differential left and differential right). The LM4947 features a 32-step digital volume control and eight distinct output modes. The digital volume control, 3D enhancement, and output modes are programmed through a two-wire I²C compatible interface that allows flexibility in routing and mixing audio channels.

The RF suppression circuitry in the LM4947 makes it well-suited for GSM mobile phones and other portable applications in which strong RF signals generated by an antenna (and long output traces) may couple audibly into the amplifier.

The LM4947 is designed for cellular phones, PDAs, and other portable handheld applications. It delivers high quality output power from a surface-mount package and requires only eight external components in the OCL mode (two additional components in SE mode).

TYPICAL APPLICATION

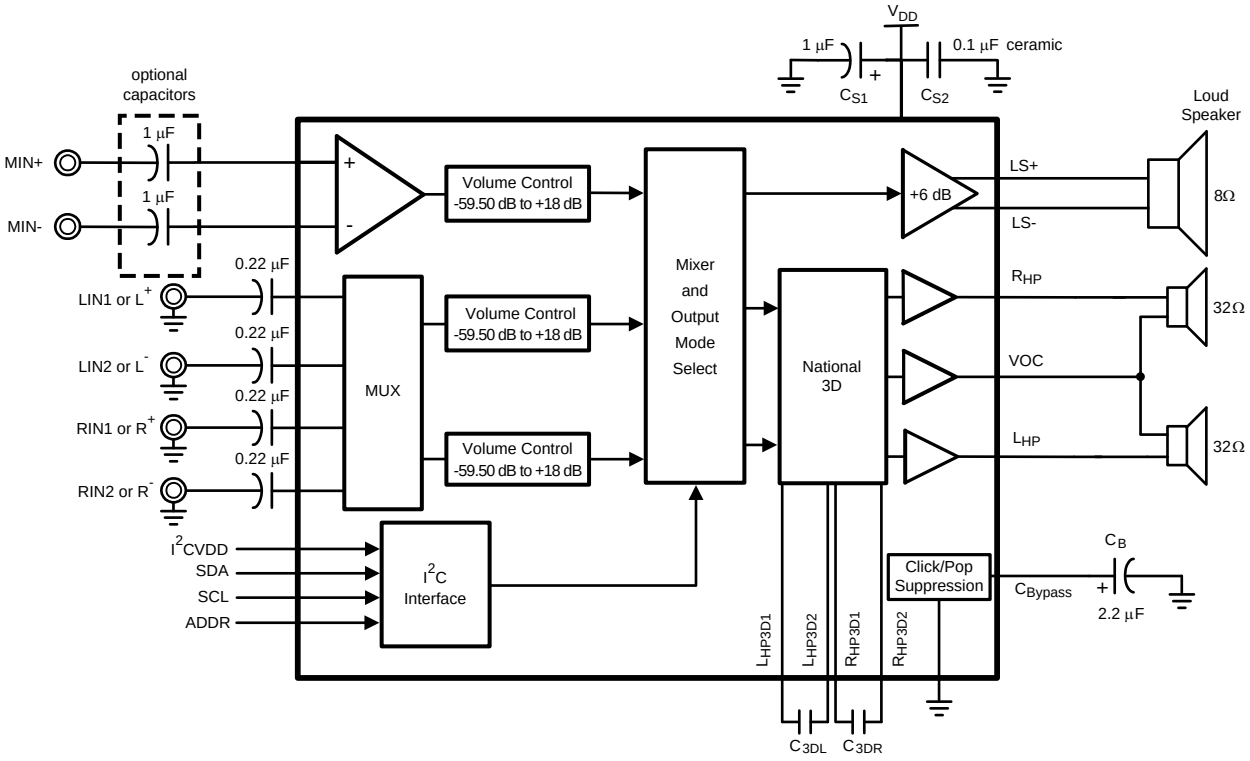


Figure 1. Typical Audio Amplifier Application Circuit-Output Capacitor-less

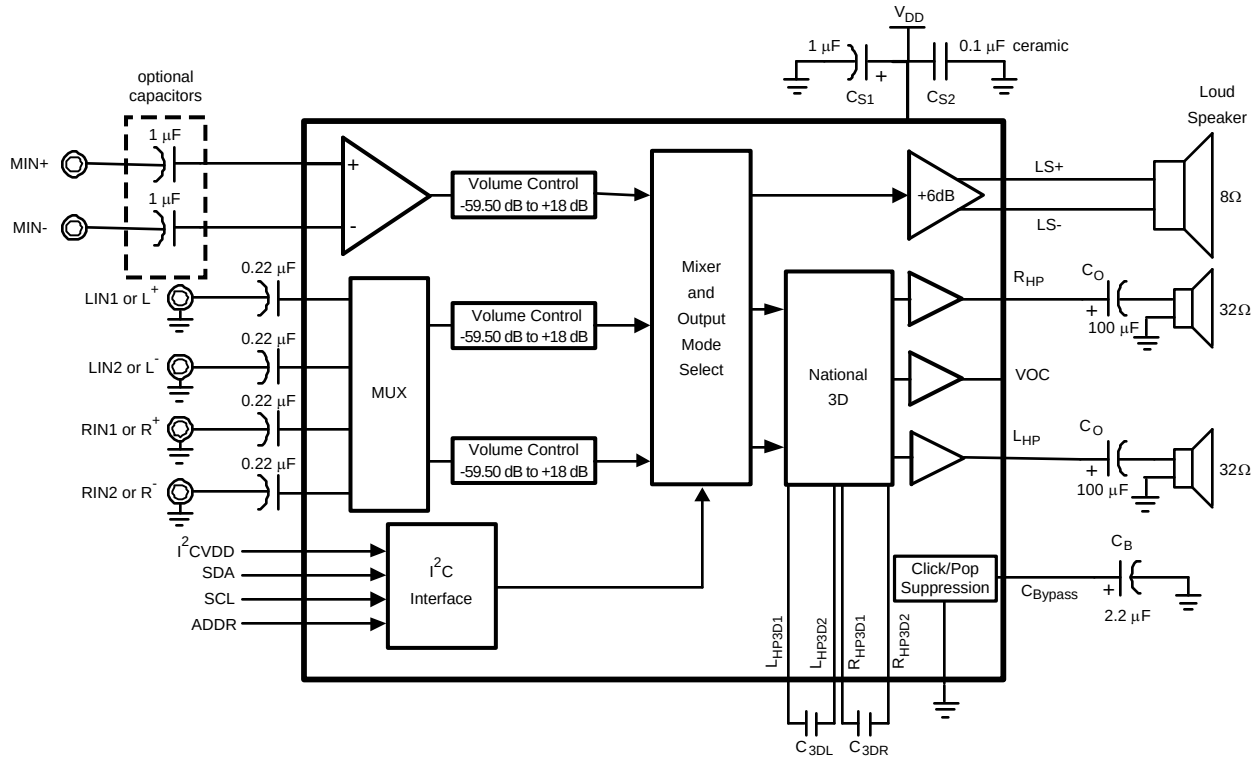


Figure 2. Typical Audio Amplifier Application Circuit-Single Ended

CONNECTION DIAGRAM

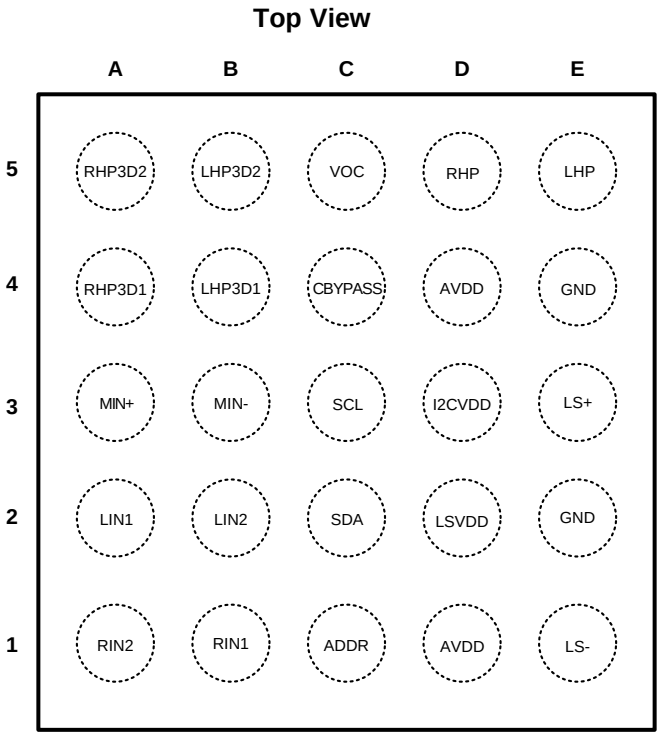


Figure 3. 25-Bump DSBGA Package
See Package Number YZR0025BBA

PIN DESCRIPTIONS

Bump	Name	Description
A1	R_{IN2}	Right Input Channel 2 or Right Differential Input –
A2	L_{IN1}	Left Input Channel 1 or Left Differential Input +
A3	MIN+	Mono Channel Non-inverting Input
A4	RHP_{3D1}	Right Headphone 3D Input 1
A5	RHP_{3D2}	Right Headphone 3D Input 2
B1	R_{IN1}	Right Input Channel 1 or Right Differential Input +
B2	L_{IN2}	Left Input Channel 2 or Left Differential Input–
B3	MIN-	Mono Channel Inverting Input
B4	L_{HP3D1}	Left Headphone 3D Input 2
B5	L_{HP3D2}	Left Headphone 3D Input 1
C1	ADDR	Address Identification
C2	SDA	Serial Data Input
C3	SCL	Serial Clock Input
C4	C_{BYPASS}	Half-Supply Bypass Capacitor
C5	VOC	Headphone return bias output
D1	AV_{DD}	Analog Power Supply
D2	LSV_{DD}	Loudspeaker Power Supply
D3	$I2CV_{DD}$	I2C Interface Power Supply
D4	AV_{DD}	Analog Power Supply
D5	R_{HP}	Right Headphone Output
E1	LS-	Loudspeaker Output Negative
E2	GND	Ground
E3	LS+	Loudspeaker Output Positive
E4	GND	Ground
E5	L_{HP}	Left Headphone Output

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3 to V_{DD} +0.3
ESD Susceptibility(3)		2.0kV
ESD Machine model(4)		200V
Junction Temperature (T_J)		150°C
Solder Information	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Thermal Resistance	θ_{JA} (typ) - YZR0025BBA	65°C/W

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 100pF discharged through a 1.5kΩ resistor.
(4) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

OPERATING RATINGS

Temperature Range	−40°C to 85°C
Supply Voltage (V_{DD})	2.7V ≤ V_{DD} ≤ 5.5V
Supply Voltage (I^2C)	2.2V ≤ V_{DD} ≤ 5.5V
Supply Voltage (Loudspeaker V_{DD})	2.7V ≤ V_{DD} ≤ 5.5V

ELECTRICAL CHARACTERISTICS 3.3V(1)(2)

The following specifications apply for V_{DD} = 3.3V, T_A = 25°C, and all gains are set for 0dB unless otherwise specified.

Symbol	Parameter	Conditions	LM4947		Units (Limits)
			Typical(3)	Limits(4)	
I_{DDQ}	Quiescent Supply Current	Output Modes 2, 4, 6 V_{IN} = 0V; No load, OCL = 0 (Table 2)	4.5	6.5	mA (max)
		Output Modes 1, 3, 5, 7 V_{IN} = 0V; No load, BTL, OCL = 0 (Table 2)	6.5	8	mA (max)
I_{SD}	Shutdown Current	Output Mode 0	0.1	1	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Mode 7, Mono	2	15	mV (max)
		V_{IN} = 0V, Mode 7, Headphones	2	15	mV (max)
P_O	Output Power	MONO $_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz, BTL, Mode 1	500	400	mW (min)
		R_{OUT} and L_{OUT}; R_L = 32Ω THD+N = 1%; f = 1kHz, SE, Mode 4	37	33	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	$MONO_{OUT}$ f = 1kHz, P_{OUT} = 250mW; R_L = 8Ω, BTL, Mode 1	0.03		%
		R_{OUT} and L_{OUT} f = 1kHz, P_{OUT} = 12mW; R_L = 32Ω, SE, Mode 4	0.02		%

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are specified to AOQL (Average Outgoing Quality Level).

ELECTRICAL CHARACTERISTICS 3.3V[1][2] (continued)

The following specifications apply for V_{DD} = 3.3V, T_A = 25°C, and all gains are set for 0dB unless otherwise specified.

Symbol	Parameter	Conditions	LM4947		Units (Limits)
			Typical[3]	Limits[4]	
N_{OUT}	Output Noise	A-weighted, 0dB inputs terminated, output referred			
		Speaker; Mode 1	39		µV
		Speaker; Mode 3	39		µV
		Speaker; Mode 5	42		µV
		Speaker; Mode 7	38		µV
		Headphone; SE, Mode 2	15		µV
		Headphone; SE, Mode 4	15		µV
		Headphone; SE, Mode 6	17		µV
		Headphone; OCL, Mode 2	12		µV
		Headphone; OCL, Mode 4	15		µV
		Headphone; OCL, Mode 6	17		µV
PSRR	Power Supply Rejection Ratio Loudspeaker out	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, R_L = 8Ω, C_B = 2.2µF, BTL All audio inputs terminated to GND; output referred			
		BTL, Output Mode 1	79		dB
		BTL, Output Mode 3	78		dB
		BTL, Output Mode 5	79		dB
		BTL, Output Mode 7	80		dB
	Power Supply Rejection Ratio R_{OUT} and L_{OUT}	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, R_L = 32Ω, C_B = 2.2µF, BTL All audio inputs terminated to GND; output referred			
		SE, Output Mode 2	78		dB
		SE, Output Mode 4	71		dB
		SE, Output Mode 6	71		dB
		OCL, Output Mode 2	83		dB
		OCL, Output Mode 4	74		dB
		OCL, Output Mode 6	74		dB
η	Class D Efficiency	Output Mode 1, 3, 5	86		%
CMRR	Common-Mode-Rejection Ratio	f = 217Hz, V_{CM} = 1Vpp, Mode 1, BTL, R_L = 8Ω	–49		dB
XTALK	Crosstalk	Headphone, P_O = 12mW, f = 1kHz, OCL, Mode 4, R_L = 32Ω	–58		dB
		Headphone, P_O = 12mW, f = 1kHz, SE, Mode 4, R_L = 32Ω	–73		dB
T_{WU}	Wake-Up Time from Shutdown	C_B = 2.2µF, OCL, R_L = 32Ω	90		ms
		C_B = 2.2µF, SE, R_L = 32Ω	115		ms
	Volume Control Step Size Error		±0.2		dB
	Digital Volume Range	Input referred maximum attenuation	-59.5	–60.25 –58.75	dB (min) dB (max)
		Input referred maximum gain	+18	17.25 18.75	dB (min) dB (max)
	Mute Attenuation	Output Mode 1, 3, 5	87		dB (min)
	MONO_IN Input Impedance R_{IN} and L_{IN} Input Impedance	Maximum gain setting	12	8 14	kΩ (min) kΩ (max)
		Maximum attenuation setting	100	75 125	kΩ (min) kΩ (max)

ELECTRICAL CHARACTERISTICS 5V[1][2]

The following specifications apply for V_{DD} = 5V, T_A = 25°C and all gains are set for 0dB unless otherwise specified.

Symbol	Parameter	Conditions	LM4947		Units (Limits)
			Typical[3]	Limits[4]	
I_{DDQ}	Quiescent Supply Current	Output Modes 2, 4, 6 V_{IN} = 0V; No load, OCL = 0 (Table 2)	5.4	7.5	mA
		Output Modes 1, 3, 5, 7 V_{IN} = 0V; No load, BTL, OCL = 0 (Table 2)	7.6	12	mA
I_{SD}	Shutdown Current	Output Mode 0	0.1	1	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Mode 7, Mono	2	15	mV (max)
		V_{IN} = 0V, Mode 7, Headphones	2	15	mV (max)
P_O	Output Power	$MONO_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz, BTL, Mode 1	1.19		W
		R_{OUT} and L_{OUT}; R_L = 32Ω THD+N = 1%; f = 1kHz, SE, Mode 4	87		mW
THD+N	Total Harmonic Distortion + Noise	$MONO_{OUT}$ f = 1kHz, P_{OUT} = 500mW; R_L = 8Ω, BTL, Mode 1	0.04		%
		R_{OUT} and L_{OUT} f = 1kHz, P_{OUT} = 30mW; R_L = 32Ω, SE, Mode 4	0.01		%
N_{OUT}	Output Noise	A-weighted, 0dB inputs terminated, output referred			
		Speaker; Mode 1	38		µV
		Speaker; Mode 3	38		µV
		Speaker; Mode 5	39		µV
		Speaker; Mode 7	36		µV
		Headphone; SE, Mode 2	21		µV
		Headphone; SE, Mode 4	21		µV
		Headphone; SE, Mode 6	24		µV
		Headphone; OCL, Mode 2	16		µV
		Headphone; OCL, Mode 4	16		µV
		Headphone; OCL, Mode 6	19		µV

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are specified to AOQL (Average Outgoing Quality Level).

ELECTRICAL CHARACTERISTICS 5V[1][2] (continued)

The following specifications apply for V_{DD} = 5V, T_A = 25°C and all gains are set for 0dB unless otherwise specified.

Symbol	Parameter	Conditions	LM4947		Units (Limits)
			Typical[3]	Limits[4]	
PSRR	Power Supply Rejection Ratio Loudspeaker out	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, R_L = 8Ω, C_B = 2.2µF, BTL All audio inputs terminated to GND; output referred			
		BTL, Output Mode 1	70		dB
		BTL, Output Mode 3	61		dB
		BTL, Output Mode 5	64		dB
		BTL, Output Mode 7	61		dB
	Power Supply Rejection Ratio R_{OUT} and L_{OUT}	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, R_L = 32Ω, C_B = 2.2µF, BTL All audio inputs terminated to GND; output referred			
		SE, Output Mode 2	72		dB
		SE, Output Mode 4	70		dB
		SE, Output Mode 6	65		dB
		OCL, Output Mode 2	76		dB
		OCL, Output Mode 4	72		dB
		OCL, Output Mode 6	70		dB
η	Class D Efficiency	Output Mode 1, 3, 5	86		%
CMRR	Common-Mode Rejection Ratio	f = 1kHz, V_{CM} = 1Vpp, 0dB gain, Mode 1, BTL, R_L = 8Ω	–49		dB
XTALK	Crosstalk	Headphone, P_O = 30mW, f = 1kHz, OCL, Mode 4	–55		dB
		Headphone, P_O = 30mW, f = 1kHz, SE, Mode 4	–72		dB
T_{WU}	Wake-Up Time from Shutdown	C_B = 2.2µF, OCL, R_L = 32Ω	116		ms
		C_B = 2.2µF, SE, R_L = 32Ω	150		ms
	Volume Control Step Size Error		±0.2		dB
	Digital Volume Range	Input referred maximum attenuation	-59.5		dB
		Input referred maximum gain	+18		dB
	Mute Attenuation	Output Mode 1, 3, 5	90		dB (min)
	MONO_IN Input Impedance R_{IN} and L_{IN} Input Impedance	Maximum gain setting	11		kΩ (min) kΩ (max)
		Maximum attenuation setting	100		kΩ (min) kΩ (max)

I^2C (1)(2)

The following specifications apply for V_{DD} = 5V and 3.3V, T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4947		Units (Limits)
			Typical (3)	Limits (4)	
t_1	Clock Period			2.5	µs (max)
t_2	Clock Setup Time			100	ns (min)
t_3	Data Hold Time			100	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
V_{IH}	SPI Input Voltage High			0.7xI^2C V_{DD}	V (min)
V_{IL}	SPI Input Voltage Low			0.3xI^2C V_{DD}	V (max)

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are specified to AOQL (Average Outgoing Quality Level).

I^2C Protocol Information

The I^2C address for the LM4947 is determined using the ID_ENB pin. The LM4947's two possible I^2C chip addresses are of the form 111110$X_1$0 (binary), where X_1 = 0, if ID_ADDR is logic LOW; and X_1 = 1, if ID_ENB is logic HIGH. If the I^2C interface is used to address a number of chips in a system, the LM4947's chip address can be changed to avoid any possible address conflicts.

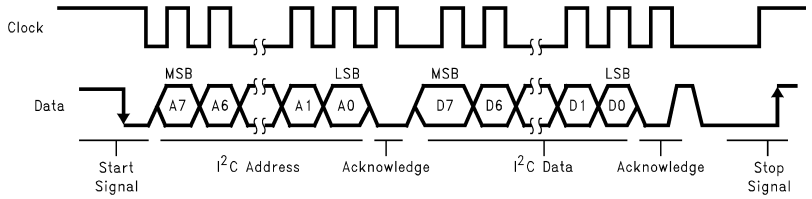


Figure 4. I^2C Bus Format

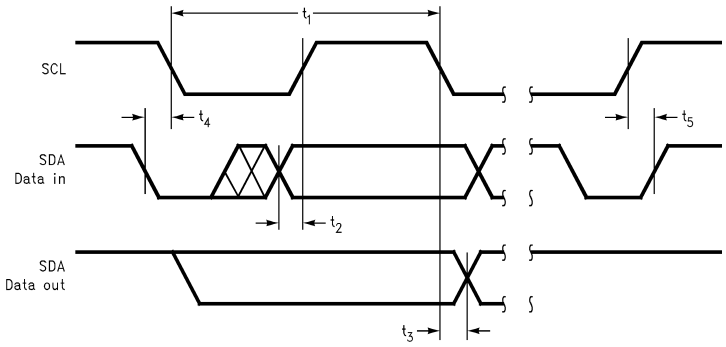


Figure 5. I^2C Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Mode 1, MONO

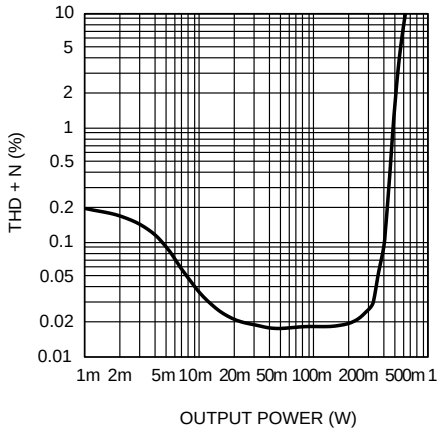


Figure 6.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Mode 3, MONO

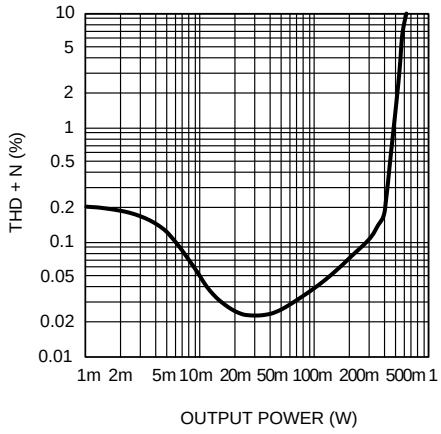


Figure 7.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Mode 5, MONO

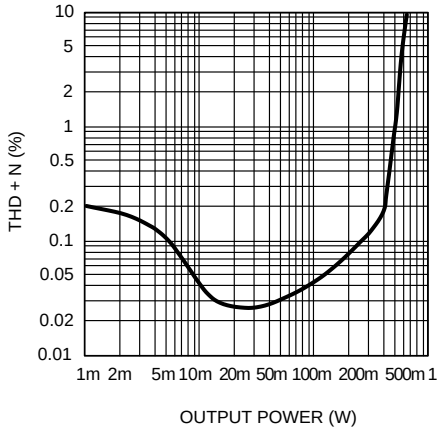


Figure 8.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 2, OCL

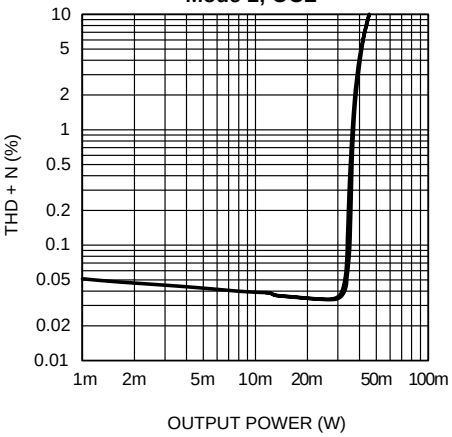


Figure 9.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 2, SE

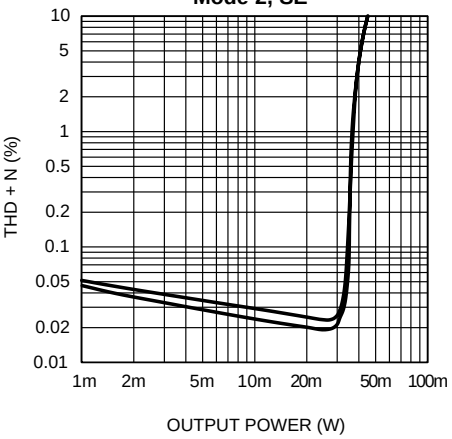


Figure 10.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 4, OCL

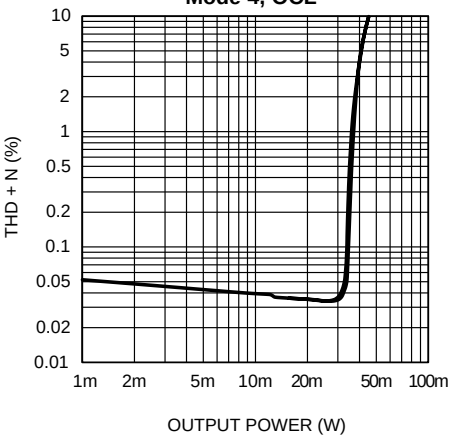


Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 4, SE

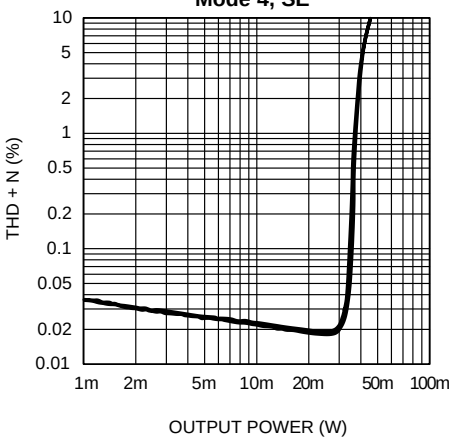


Figure 12.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 6, OCL

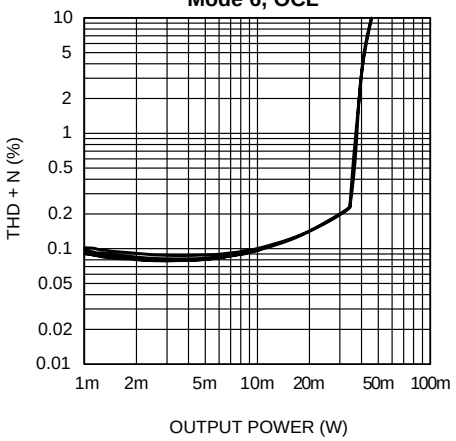


Figure 13.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 6, SE

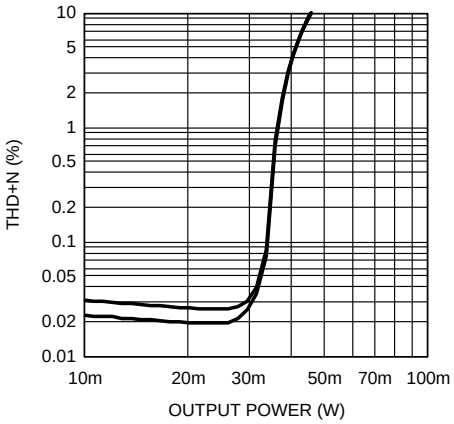


Figure 14.

THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Mode 1, MONO

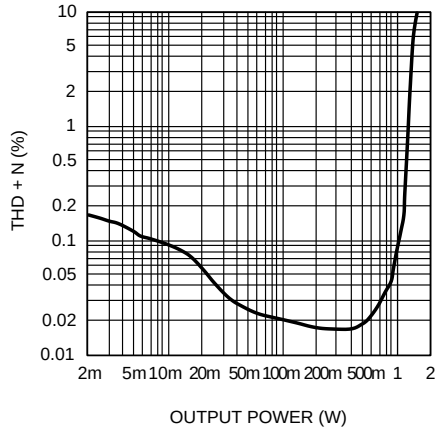


Figure 15.

THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Mode 3, MONO

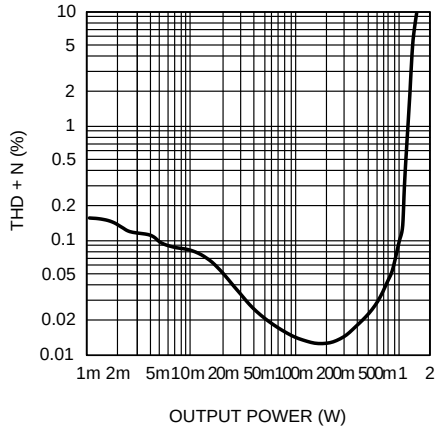


Figure 16.

THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Mode 5, MONO

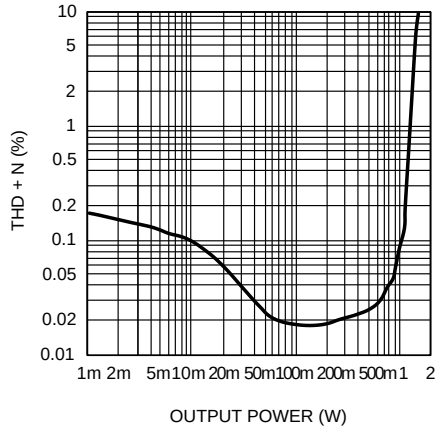


Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 2, OCL

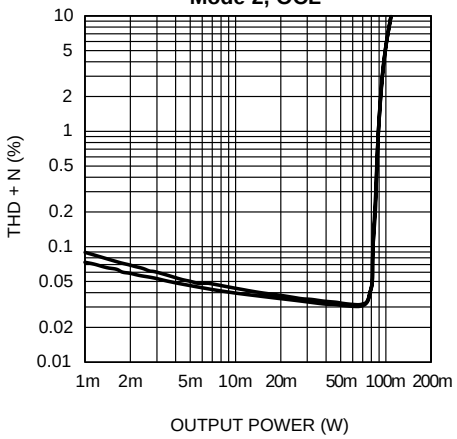


Figure 18.

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 2, SE

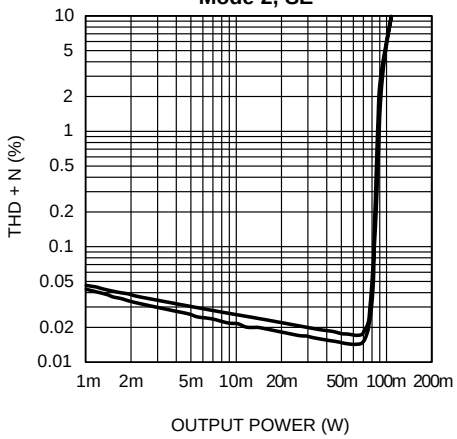


Figure 19.

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 4, OCL

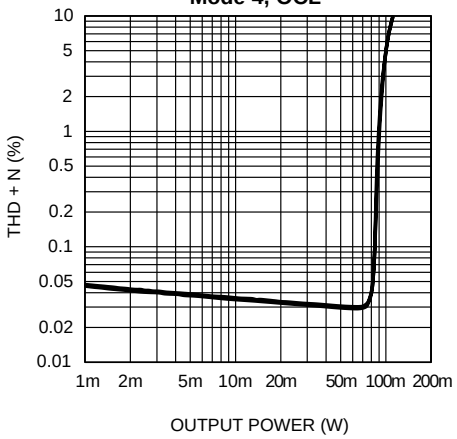


Figure 20.

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 4, SE

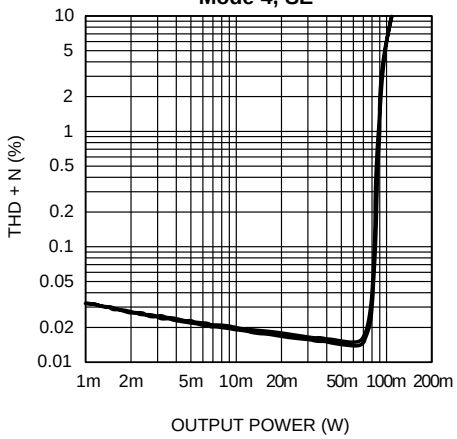


Figure 21.

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 6, OCL

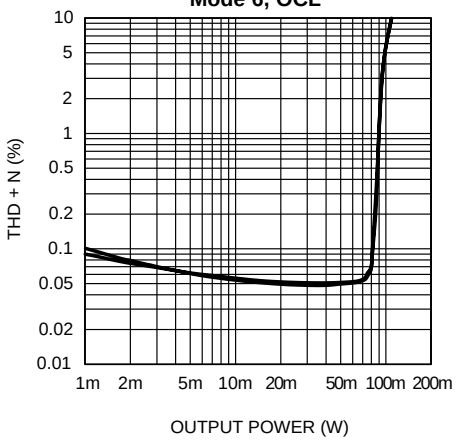


Figure 22.

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 6, SE

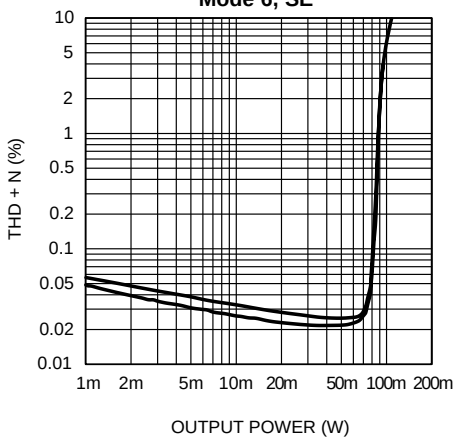


Figure 23.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW
Diff In, Mode 1

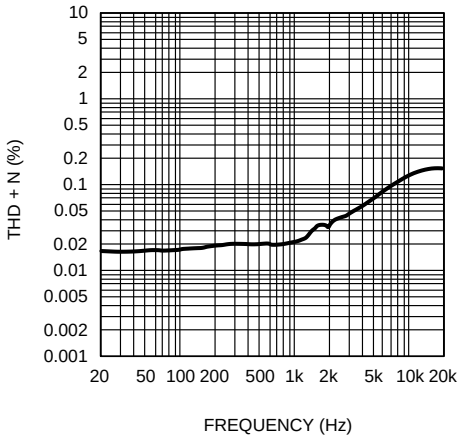


Figure 24.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW
Diff In, Mode 5

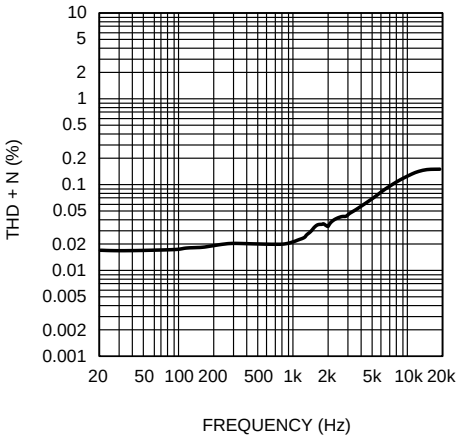


Figure 25.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW
Diff In, Mode 3

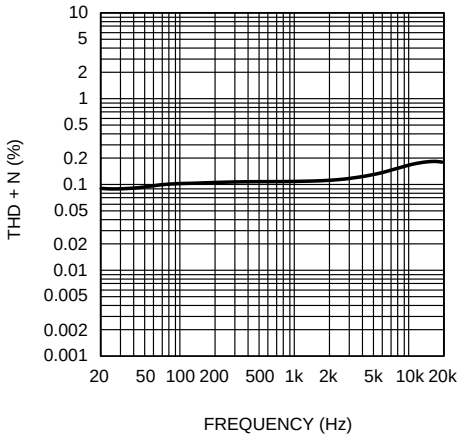


Figure 26.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 2, OCL

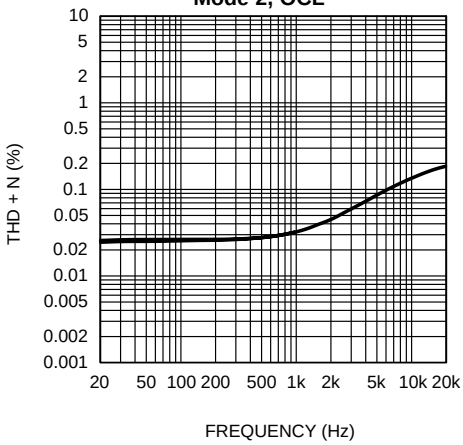


Figure 27.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 2, SE

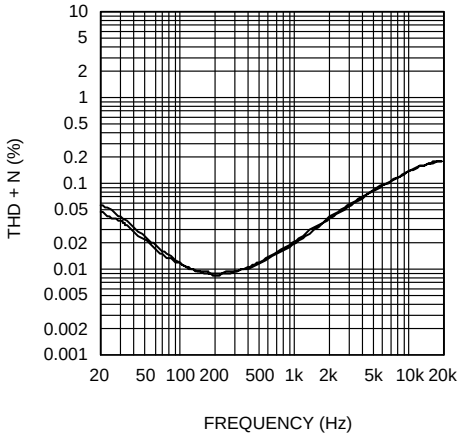


Figure 28.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 4,7, OCL

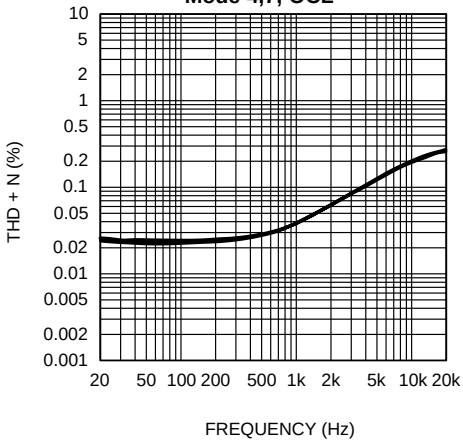


Figure 29.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 4,7, SE

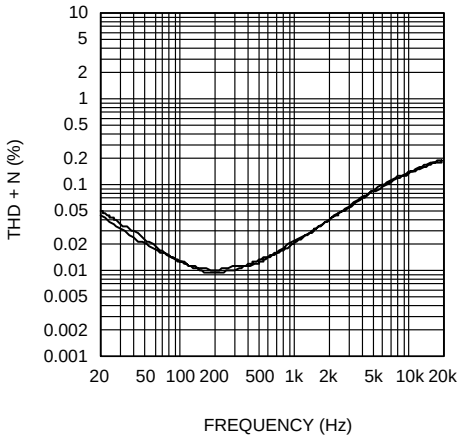


Figure 30.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 6, OCL

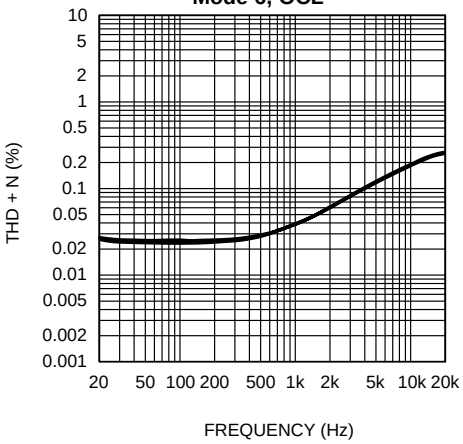


Figure 31.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 6, SE

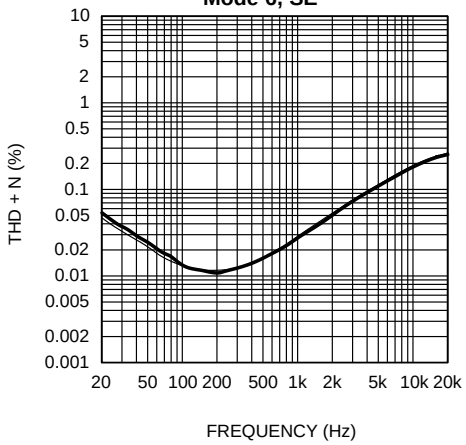


Figure 32.

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 500mW
Diff In, Mode 1

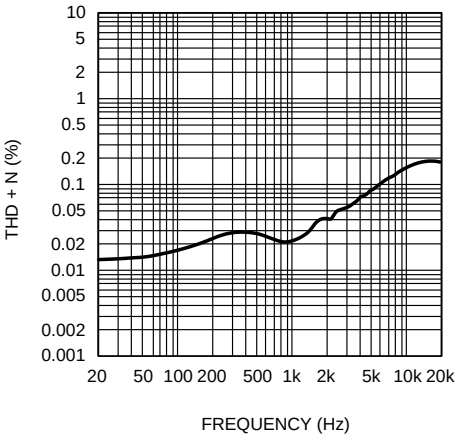


Figure 33.

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 500mW
Diff In, Mode 3

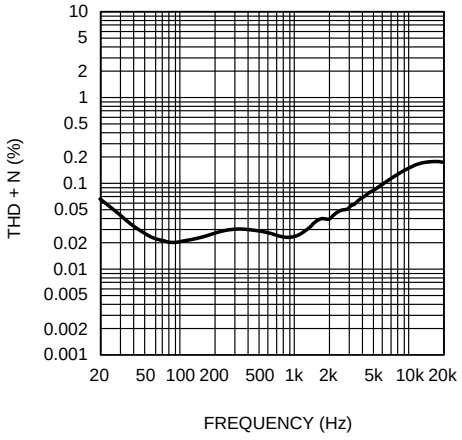


Figure 34.

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 500mW
Diff In, Mode 5

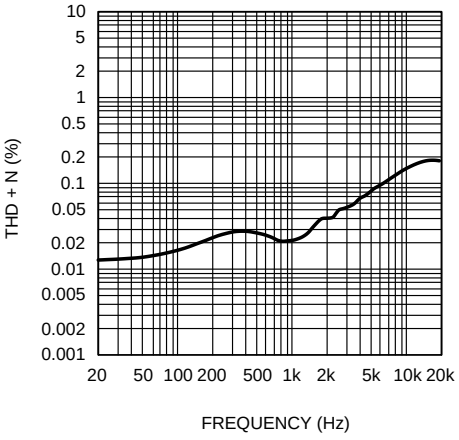


Figure 35.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

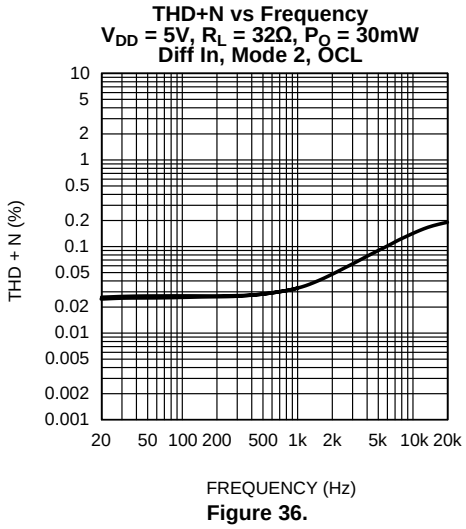


Figure 36.

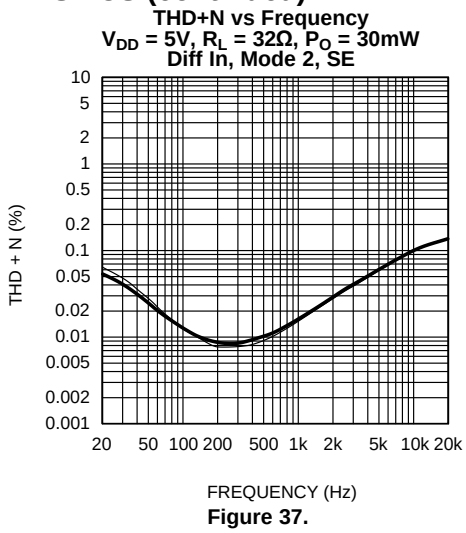


Figure 37.

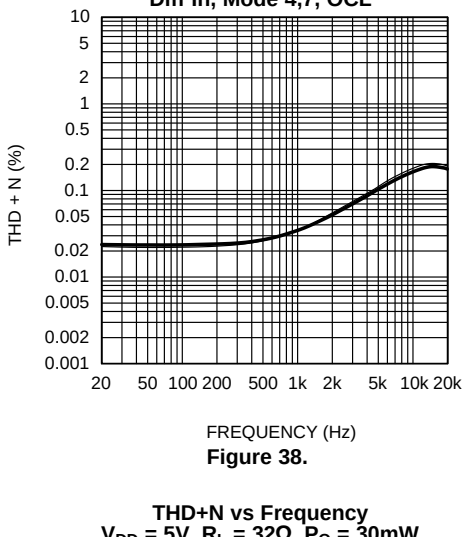


Figure 38.

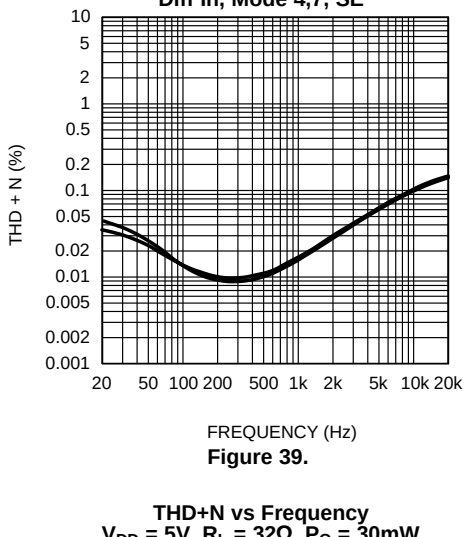


Figure 39.

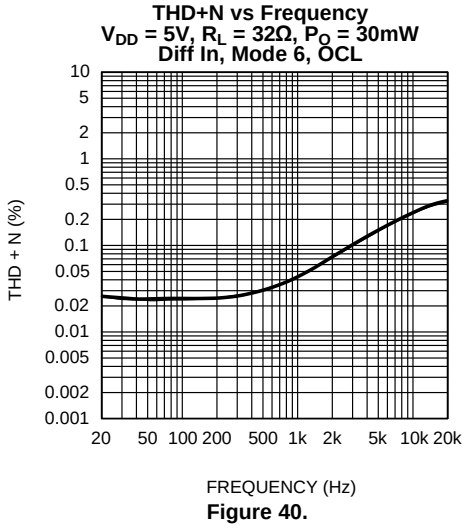


Figure 40.

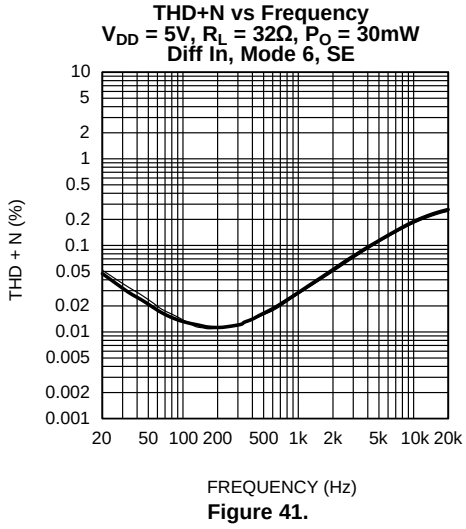


Figure 41.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 1, MONO

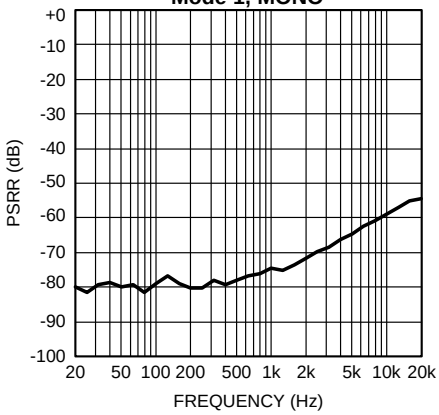


Figure 42.

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 2, OCL

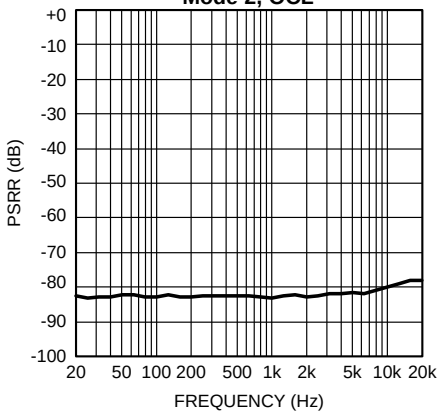


Figure 43.

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 2, SE

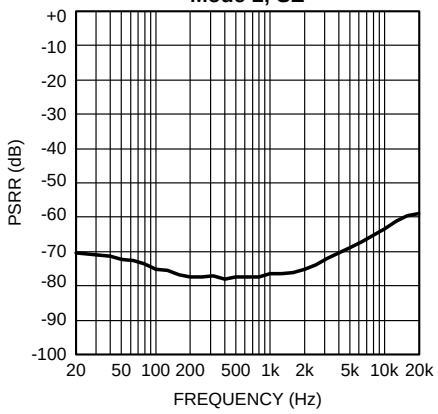


Figure 44.

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 3, MONO

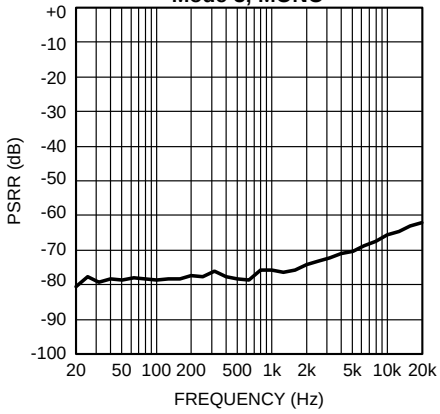


Figure 45.

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 4, OCL

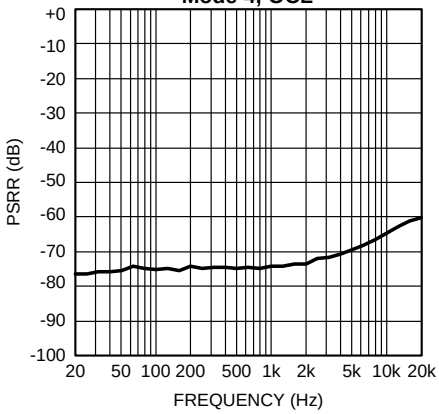


Figure 46.

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 4, SE

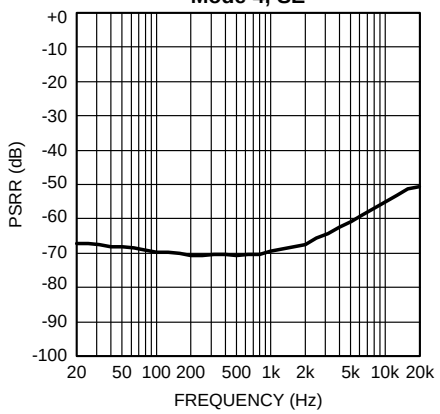


Figure 47.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 5, MONO

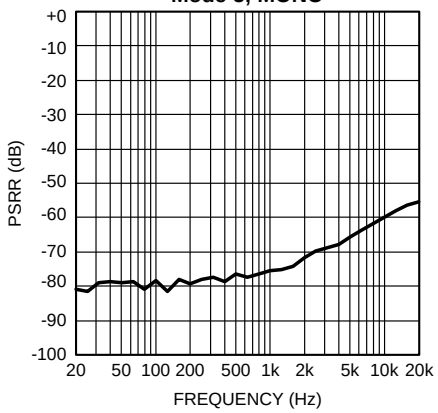


Figure 48.

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 6, OCL

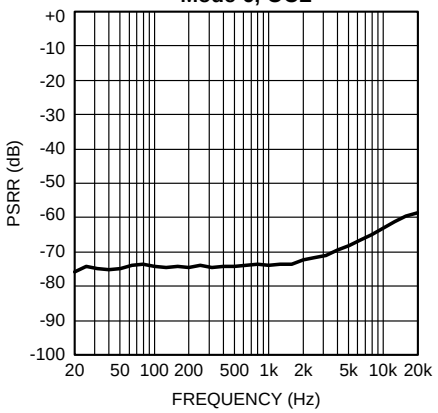


Figure 49.

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 6, SE

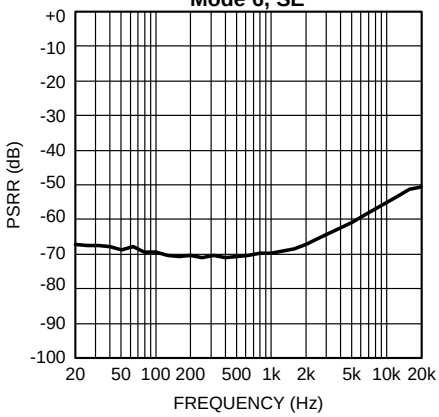


Figure 50.

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 7, MONO

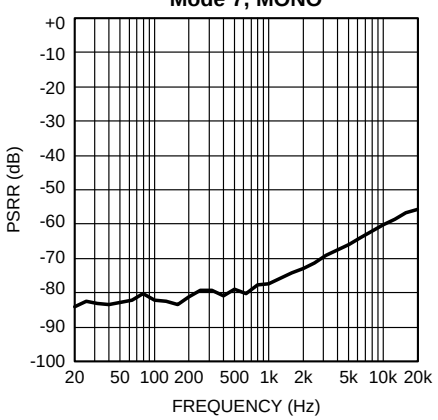


Figure 51.

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 1, MONO

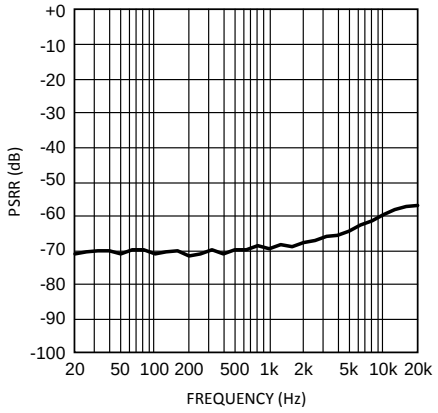


Figure 52.

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 2, OCL

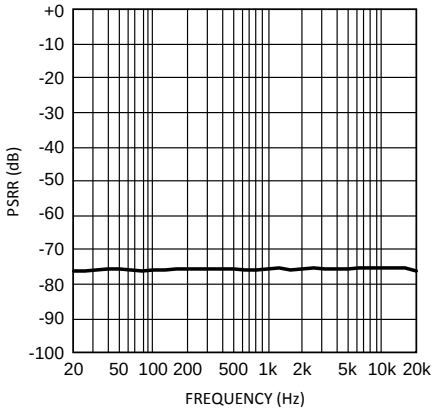


Figure 53.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 2, SE

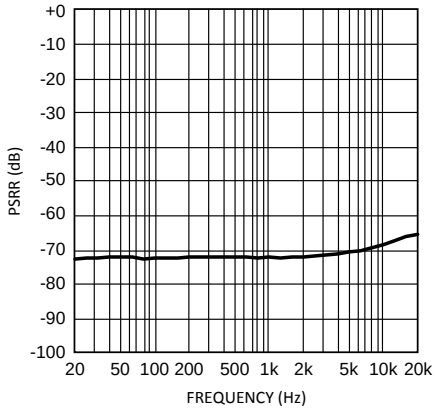


Figure 54.

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 3, MONO

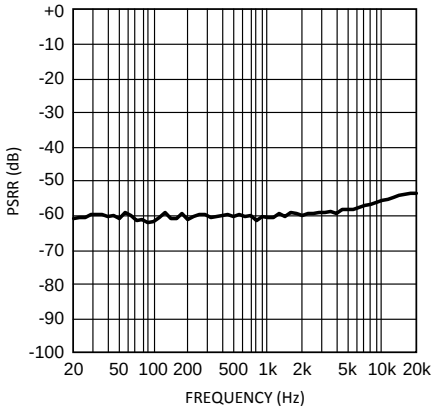


Figure 55.

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 4, OCL

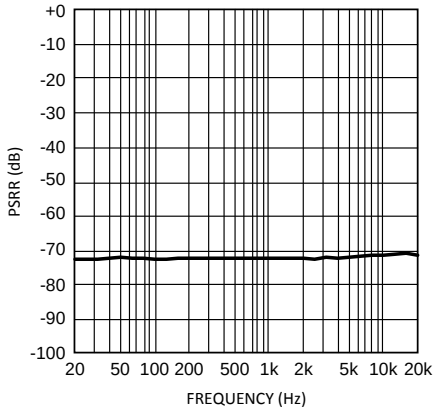


Figure 56.

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 4, SE

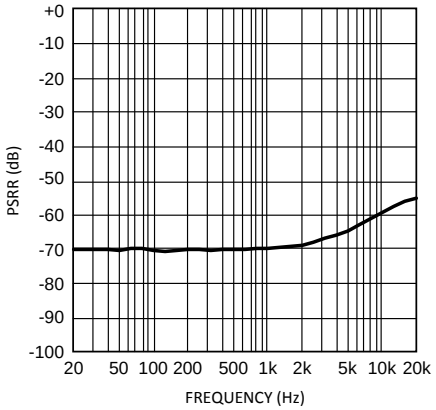


Figure 57.

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 5, MONO

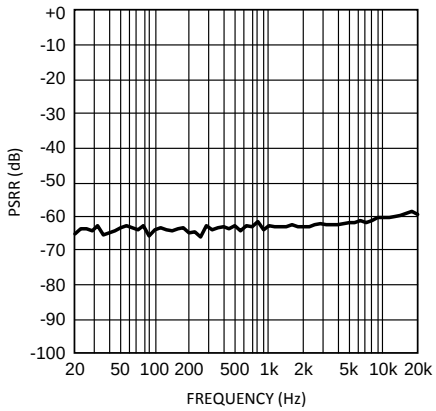


Figure 58.

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 6, OCL

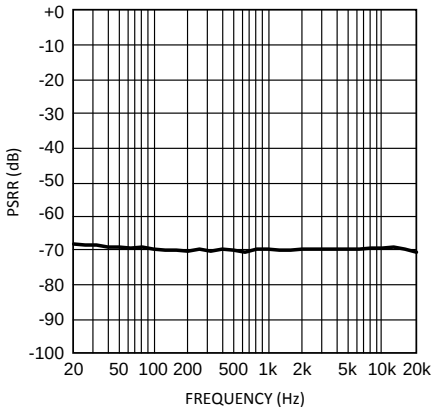


Figure 59.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 6, SE

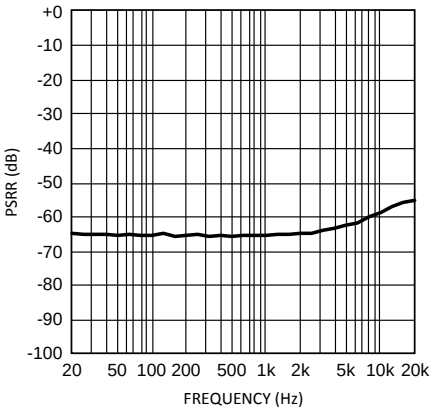


Figure 60.

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 7, MONO

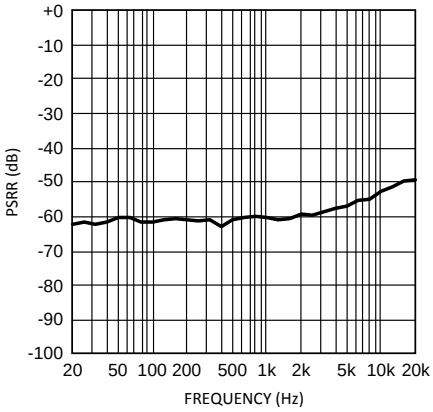


Figure 61.

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 7, OCL

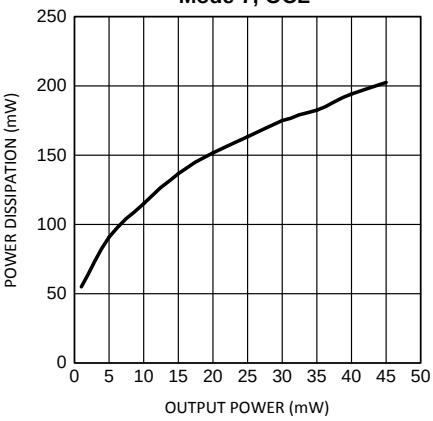


Figure 62.

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 7, SE

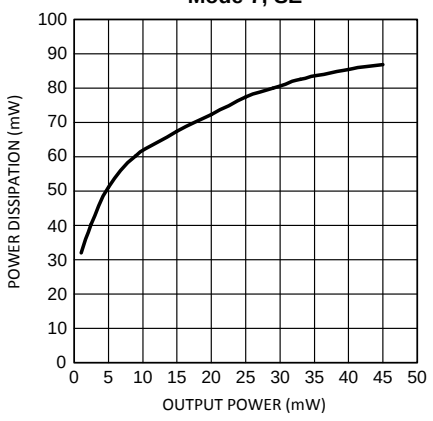


Figure 63.

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Mode 1, 3, 5, MONO

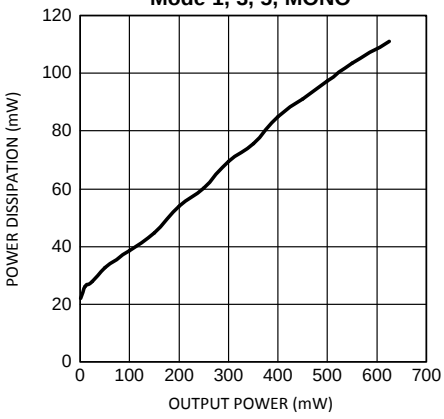


Figure 64.

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 2, 4, 6, OCL

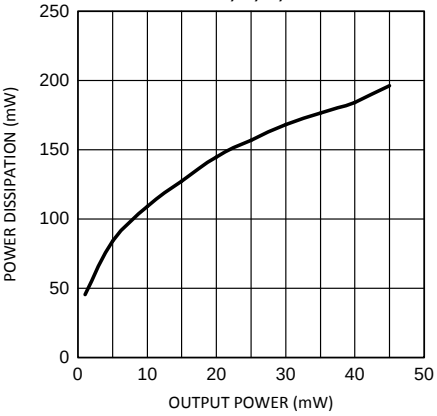


Figure 65.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 2, 4, 6, SE

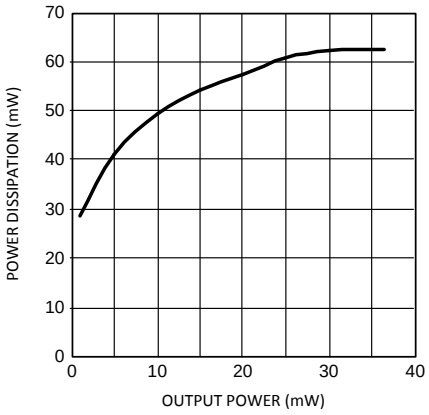


Figure 66.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 7, OCL

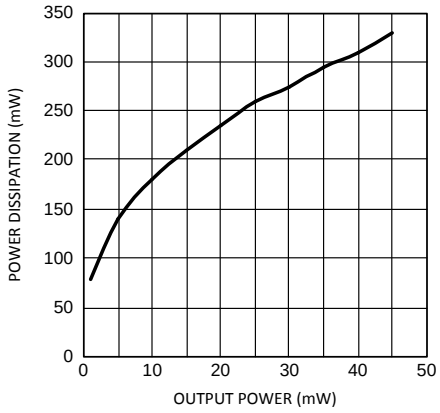


Figure 67.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 7, SE

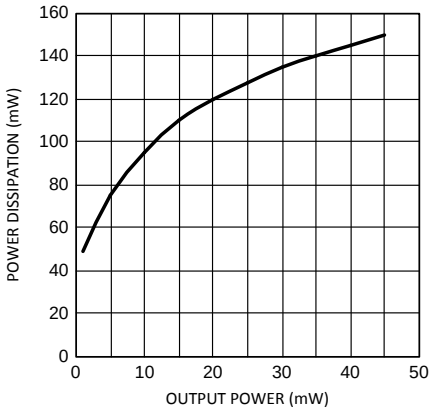


Figure 68.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Mode 1, 3, 5, MONO

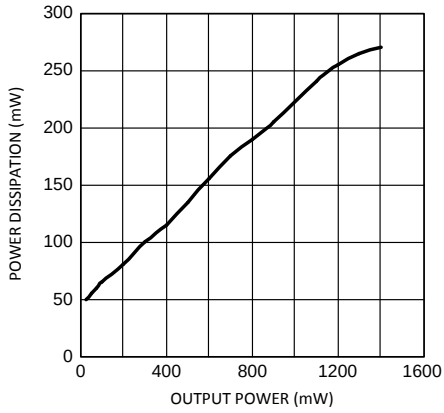


Figure 69.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 2, 4, 6, OCL

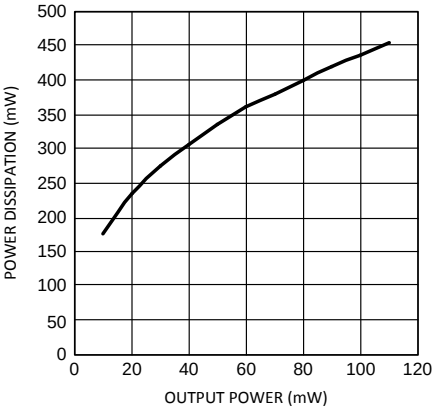


Figure 70.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 2, 4, 6, SE

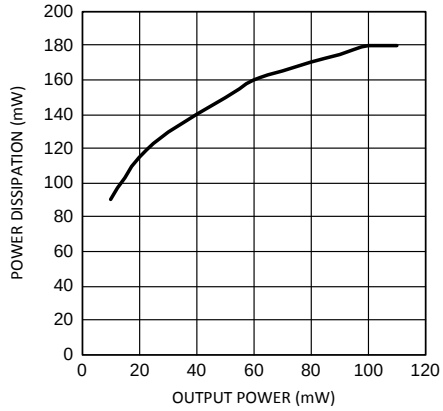


Figure 71.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Crosstalk vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 4, OCL

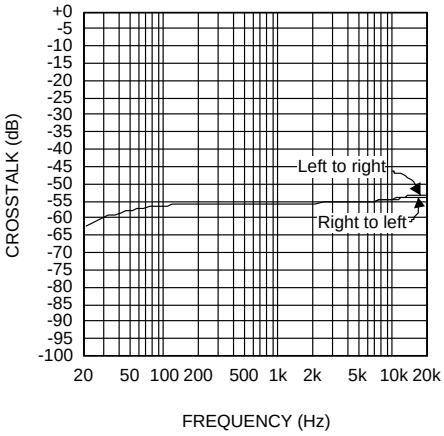


Figure 72.

Crosstalk vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 4, SE

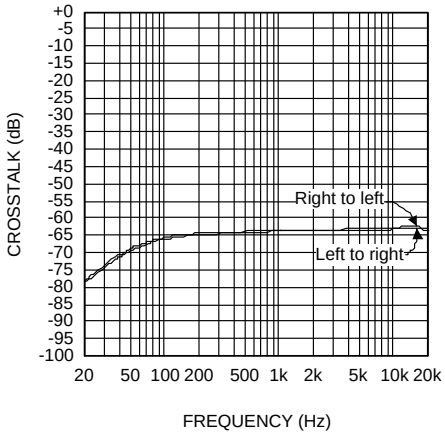


Figure 73.

Crosstalk vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Mode 4, OCL

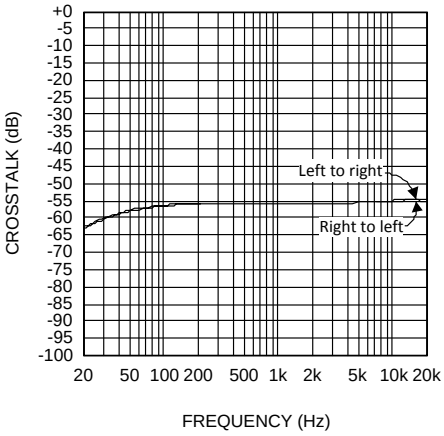


Figure 74.

Crosstalk vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Mode 4, SE

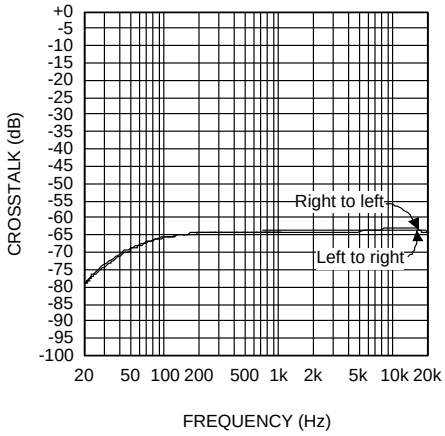


Figure 75.

Supply Current vs Supply Voltage
No Load, Mode 7, OCL

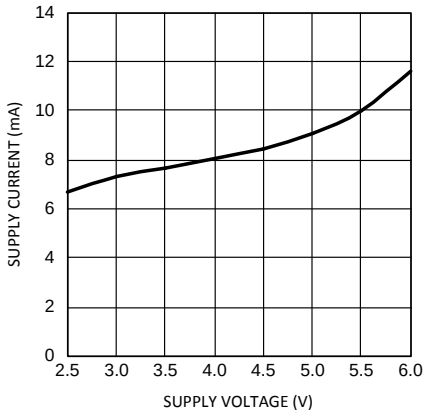


Figure 76.

Supply Current vs Supply Voltage
No Load, Mode 7, SE

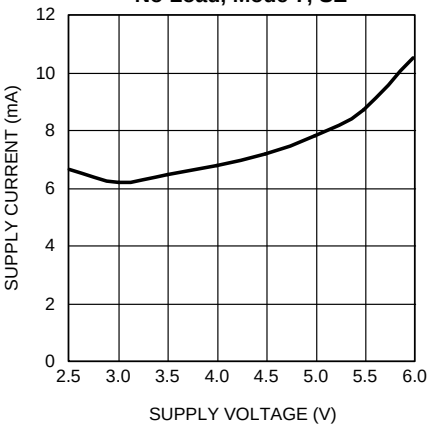


Figure 77.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Supply Current vs Supply Voltage
No Load, Mode 1, 3, 5, MONO

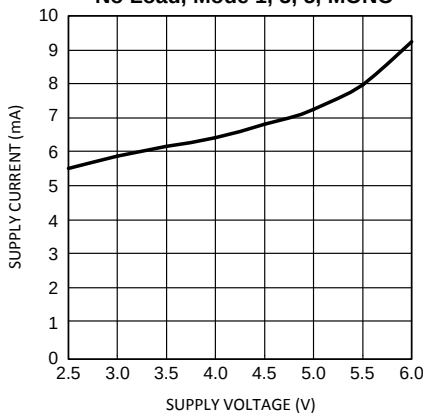


Figure 78.

Supply Current vs Supply Voltage
No Load, Mode 2, 4, 6, OCL

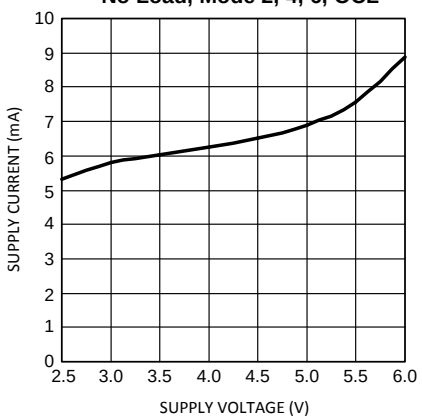


Figure 79.

Supply Current vs Supply Voltage
No Load, Mode 2, 4, 6, Headphone SE

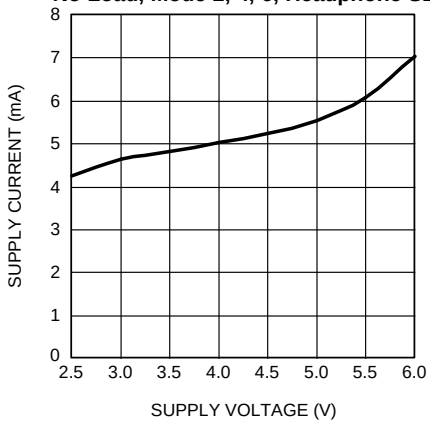


Figure 80.

Output Power vs Supply Voltage
R_L = 8Ω, Mode 1, 3, 5, MONO

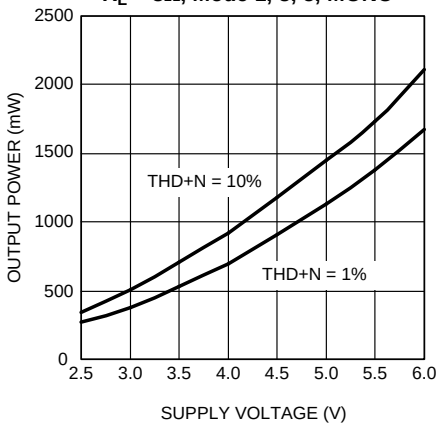


Figure 81.

Output Power vs Supply Voltage
R_L = 32Ω, Mode 2, 4, 6, OCL

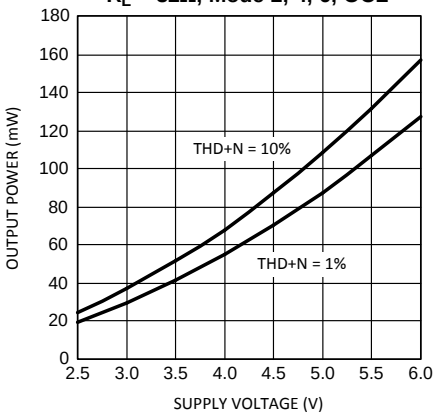


Figure 82.

Output Power vs Supply Voltage
R_L = 32Ω, Mode 2, 4, 6, SE

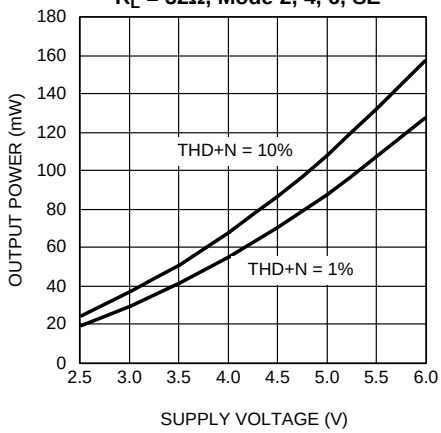


Figure 83.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Power vs Supply Voltage
R_L = 32Ω, Mode 7, OCL

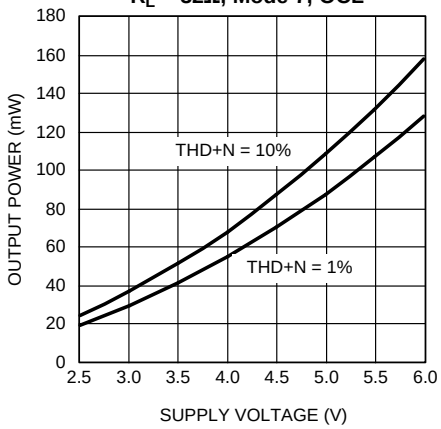


Figure 84.

Output Power vs Supply Voltage
R_L = 32Ω, Mode 7, SE

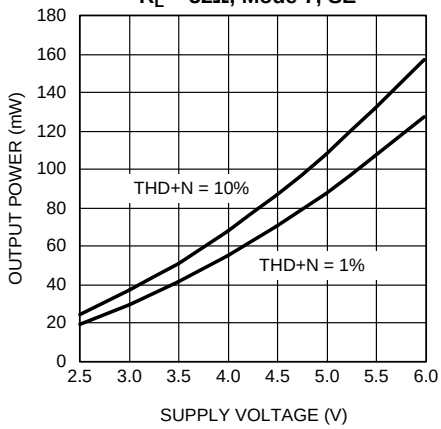


Figure 85.

Efficiency vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, Mode 1, 3, 5, BTL

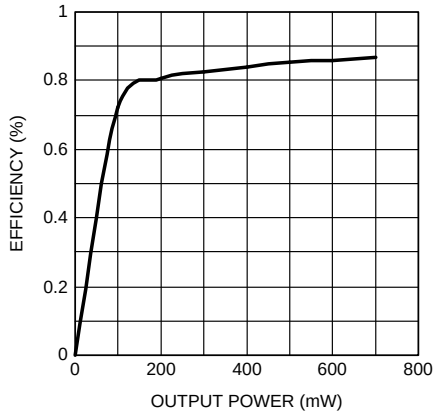


Figure 86.

Efficiency vs Output Power
V_{DD} = 5V, R_L = 8Ω, Mode 1, 3, 5, BTL

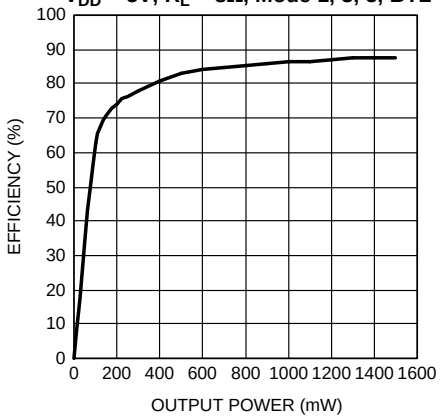


Figure 87.

APPLICATION INFORMATION

I²C PIN DESCRIPTION

SDA: This is the serial data input pin.

SCL: This is the clock input pin.

ID_ENB: This is the address select input pin.

I²C COMPATIBLE INTERFACE

The LM4947 uses a serial bus which conforms to the I²C protocol to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I²C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4947.

The I²C address for the LM4947 is determined using the ID_ENB pin. The LM4947's two possible I²C chip addresses are of the form 111110$X_1$0 (binary), where X_1 = 0, if ID_ADDR is logic LOW; and X_1 = 1, if ID_ENB is logic HIGH. If the I²C interface is used to address a number of chips in a system, the LM4947's chip address can be changed to avoid any possible address conflicts.

The bus format for the I²C interface is shown in Figure 4. The bus format diagram is broken up into six major sections:

1. The "start" signal is generated by lowering the data signal while the clock signal is HIGH. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own address.
2. The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is HIGH.
3. After the last bit of the address bit is sent, the master releases the data line HIGH (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM4947 has received the address correctly, then it holds the data line LOW during the clock pulse. If the data line is not held LOW during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM4947.
4. The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable HIGH.
5. After the data byte is sent, the master must check for another acknowledge to see if the LM4947 received the data.
6. The "stop" signal ends the transfer. To signal "stop", the data signal goes HIGH while the clock signal is HIGH. The data line should be held HIGH when not in use.

I²C INTERFACE POWER SUPPLY PIN (I²CV_{DD})

The LM4947's I²C interface is powered up through the I²CV_{DD} pin. The LM4947's I²C interface operates at a voltage level set by the I²CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I²C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

Table 1. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	1	0	EC	0
ID_ADDR = 0	1	1	1	1	1	0	0	0
ID_ADDR = 1	1	1	1	1	1	0	1	0

Table 2. Control Registers

	D7	D6	D5	D4	D3	D2	D1	D0
Mode Control	0	0	SE/Diff (select)	0	OCL (select)	MC2	MC1	MC0
Programmable 3D	0	1	L2R2 (select)	L1R1 (select)	N3D3	N3D2	N3D1	N3D0
Mono Volume Control	1	0	0	MVC4	MVC3	MVC2	MVC1	MVC0
Left Volume Control	1	1	0	LVC4	LVC3	LVC2	LVC1	LVC0
Right Volume Control	1	1	1	RVC4	RVC3	RVC2	RVC1	RVC0

Table 3. Programmable Texas Instruments 3D Audio

	N3D3	N3D2
Low	0	0
Medium	0	1
High	1	0
Maximum	1	1

Table 4. Input/Output Control

	L2R2	L1R1	SE/DIFF
Select L_{IN1} and R_{IN1} Stereo Pair	0	1	0
Select L_{IN2} and R_{IN2} Stereo Pair	1	0	0
Select L_{IN1}+L_{IN2} and R_{IN1}+R_{IN2} Stereo Pair	1	1	0
Sets Stereo Inputs to Differential	x	x	1

Table 5. Output Volume Control Table

Volume Step	xVC4	xVC3	xVC2	xVC1	xVC0	Gain, dB
1	0	0	0	0	0	–59.50
2	0	0	0	0	1	–48.00
3	0	0	0	1	0	–40.50
4	0	0	0	1	1	–34.50
5	0	0	1	0	0	–30.00
6	0	0	1	0	1	–27.00
7	0	0	1	1	0	–24.00
8	0	0	1	1	1	–21.00
9	0	1	0	0	0	–18.00
10	0	1	0	0	1	–15.00
11	0	1	0	1	0	–13.50
12	0	1	0	1	1	–12.00
13	0	1	1	0	0	–10.50
14	0	1	1	0	1	–9.00
15	0	1	1	1	0	–7.50
16	0	1	1	1	1	–6.00
17	1	0	0	0	0	–4.50
18	1	0	0	0	1	–3.00
19	1	0	0	1	0	–1.50
20	1	0	0	1	1	0.00
21	1	0	1	0	0	1.50
22	1	0	1	0	1	3.00
23	1	0	1	1	0	4.50
24	1	0	1	1	1	6.00

Table 5. Output Volume Control Table (continued)

Volume Step	xVC4	xVC3	xVC2	xVC1	xVC0	Gain, dB
25	1	1	0	0	0	7.50
26	1	1	0	0	1	9.00
27	1	1	0	1	0	10.50
28	1	1	0	1	1	12.00
29	1	1	1	0	0	13.50
30	1	1	1	0	1	15.00
31	1	1	1	1	0	16.50
32	1	1	1	1	1	18.00

Table 6. Output Mode Selection

Output Mode Number	MC2	MC1	MC0	Handsfree Mono Output	Right HP Output	Left HP Output
0	0	0	0	SD	SD	SD
1	0	0	1	2 x G_M x M	MUTE	MUTE
2	0	1	0	SD	G_M x M	G_M x M
3	0	1	1	G_L x L + G_R x R	MUTE	MUTE
4	1	0	0	SD	G_R x R	G_L x L
5	1	0	1	G_L x L + G_R x R + 2(G_M x M)	MUTE	MUTE
6	1	1	0	SD	G_R x R + G_M x M	G_L x L + G_M x M
7	1	1	1	G_R x R + G_L x L	G_R x R	G_L x L

TI 3D ENHANCEMENT

The LM4947 features a stereo headphone, 3D audio enhancement effect that widens the perceived soundstage from a stereo audio signal. The 3D audio enhancement creates a perceived spatial effect optimized for stereo headphone listening. The LM4947 can be programmed for a “narrow” or “wide” soundstage perception. The narrow soundstage has a more focused approaching sound direction, while the wide soundstage has a spatial, theater-like effect. Within each of these two modes, four discrete levels of 3D effect that can be programmed: low, medium, high, and maximum (Table 2), each level with an ever increasing aural effect, respectively. The difference between each level is 3dB.

The external capacitors, shown in Figure 88, are required to enable the 3D effect. The value of the capacitors set the cutoff frequency of the 3D effect, as shown by Equation 1 and Equation 2. Note that the internal 20kΩ resistor is nominal (±25%).

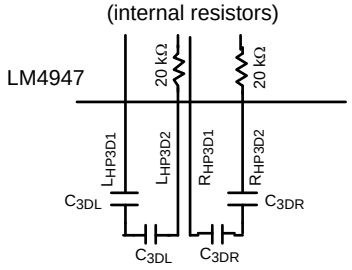


Figure 88. External 3D Effect Capacitors

$$f_{3DL(-3dB)} = 1 / 2\pi * 20k\Omega * C_{3DL} \quad (1)$$

$$f_{3DR(-3dB)} = 1 / 2\pi * 20k\Omega * C_{3DR} \quad (2)$$

Optional resistors R_{3DL} and R_{3DR} can also be added (Figure 89) to affect the -3dB frequency and 3D magnitude.

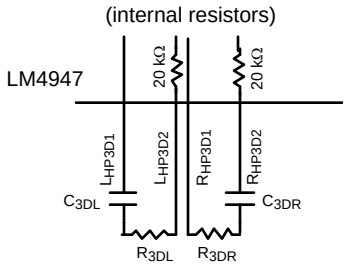


Figure 89. External RC Network with Optional R_{3DL} and R_{3DR} Resistors

$$f_{3DL(-3dB)} = 1 / 2\pi * (20k\Omega + R_{3DL}) * C_{3DL} \quad (3)$$

$$f_{3DR(-3dB)} = 1 / 2\pi * 20k\Omega + R_{3DR}) * C_{3DR} \quad (4)$$

ΔAV (change in AC gain) = 1 / 1 + M, where M represents some ratio of the nominal internal resistor, 20kΩ (see example below).

$$f_{3dB} (3D) = 1 / 2\pi (1 + M)(20k\Omega * C_{3D}) \quad (5)$$

$$C_{Equivalent} (new) = C_{3D} / 1 + M \quad (6)$$

Table 7. Pole Locations

R_{3D} (kΩ) (optional)	C_{3D} (nF)	M	ΔAV (dB)	f-3dB (3D) (Hz)	Value of C_{3D} to keep same pole location (nF)	new Pole Location (Hz)
0	68	0	0	117		
1	68	0.05	–0.4	111	64.8	117
5	68	0.25	–1.9	94	54.4	117
10	68	0.50	–3.5	78	45.3	117
20	68	1.00	–6.0	59	34.0	117

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 8Ω LOAD

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by an 8Ω load from 158.3mW to 156.4mW. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

POWER DISSIPATION AND EFFICIENCY

In general terms, efficiency is considered to be the ratio of useful work output divided by the total energy required to produce it with the difference being the power dissipated, typically, in the IC. The key here is “useful” work. For audio systems, the energy delivered in the audible bands is considered useful including the distortion products of the input signal. Sub-sonic (DC) and super-sonic components (>22kHz) are not useful. The difference between the power flowing from the power supply and the audio band power being transduced is dissipated in the

LM4947 and in the transducer load. The amount of power dissipation in the LM4947 is very low. This is because the ON resistance of the switches used to form the output waveforms is typically less than 0.25Ω. This leaves only the transducer load as a potential "sink" for the small excess of input power over audio band output power. The LM4947 dissipates only a fraction of the excess power requiring no additional PCB area or copper plane to act as a heat sink.

The LM4947 also has a pair of single-ended amplifiers driving stereo headphones, R_{HP} and L_{HP}. The maximum internal power dissipation for R_{HP} and L_{HP} is given by Equation 7 and Equation 8. From Equation 7 and Equation 8, assuming a 5V power supply and a 32Ω load, the maximum power dissipation for L_{HP} and R_{HP} is 40mW, or 80mW total.

$$P_{DMAX-LHP} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (7)$$

$$P_{DMAX-RHP} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (8)$$

The maximum internal power dissipation of the LM4947 occurs when all 3 amplifiers pairs are simultaneously on; and is given by Equation 9.

$$P_{DMAX-TOTAL} = P_{DMAX-SPKROUT} + P_{DMAX-LHP} + P_{DMAX-RHP} \quad (9)$$

The maximum power dissipation point given by Equation 9 must not exceed the power dissipation given by Equation 10:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (10)$$

The LM4947's T_{JMAX} = 150°C. In the ITL package, the LM4947's θ_{JA} is 65°C/W. At any given ambient temperature T_A, use Equation 10 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 10 and substituting $P_{DMAX-TOTAL}$ for P_{DMAX}' results in Equation 11. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4947's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX-TOTAL}\,\theta_{JA} \quad (11)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 104°C for the ITL package.

$$T_{JMAX} = P_{DMAX-TOTAL}\,\theta_{JA} + T_A \quad (12)$$

Equation 12 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4947's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation 9 is greater than that of Equation 10, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance). Refer to the TYPICAL PERFORMANCE CHARACTERISTICS curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 1µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.1µF tantalum bypass capacitance connected between the LM4947's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4947's power supply pin and ground as short as possible. Connecting a 2.2µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, SELECTING EXTERNAL COMPONENTS), system cost, and size constraints.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figure 1 and Figure 2). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

The internal input resistor (R_i), nominal 20kΩ, and the input capacitor (C_i) produce a high pass filter cutoff frequency that is found using Equation 13.

$$f_c = 1 / (2\pi R_i C_i) \quad (13)$$

As an example when using a speaker with a low frequency limit of 150Hz, C_i, using Equation 13 is 0.053µF. The 0.22µF C_i shown in Figure 1 allows the LM4947 to drive high efficiency, full range speaker whose response extends below 40Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS bump. Since C_B determines how fast the LM4947 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4947's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops. C_B's value should be in the range of 5 times to 7 times the value of C_i. This ensures that output transients are eliminated when power is first applied or the LM4947 resumes operation after shutdown.

DEMO BOARD SCHEMATIC

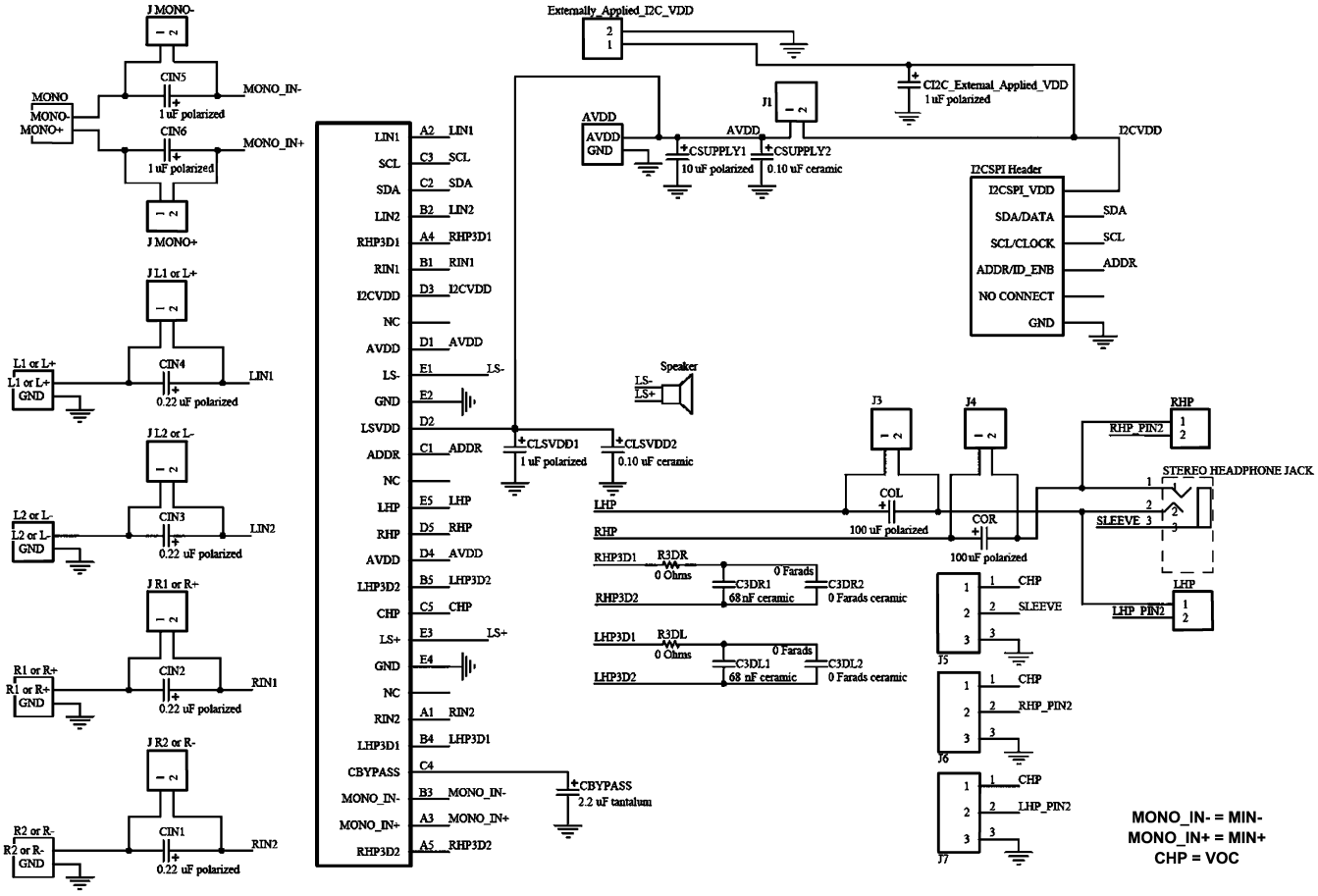


Figure 90.

REVISION HISTORY

Rev	Date	Description
1.0	06/16/06	Initial release.
1.1	06/19/06	Changed the Class D Efficiency (n) on Typical limit (from 79 to 86) on the 5V specification table.
1.2	06/22/06	Added more Typ Perf curves.
1.3	07/18/06	Replaced some of the curves.
1.4	08/29/06	Text edits.
1.5	10/18/06	Edited DSBGA pkg drawing, Figure 1 and Figure 2. Changed I_{DDQ} typical and limit values on the 3.3V and 5.0V specification table. Removed CMRR SE condition and changed typical values for CMRR BTL on 3.3V and 5.0V specification table. Changed Mute Attenuation typical value on 5.0V specification table.
1.6	03/02/07	Edited the 3.3V and 5V EC tables.
1.7	03/02/07	Composed (CONFIDENTIAL) D/S for customer (SAMSUNG).
1.8	09/06/07	Edited Table 4.
1.9	11/09/07	Text edits.
D	05/03/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4947TL/NOPB	ACTIVE	DSBGA	YZR	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GH1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

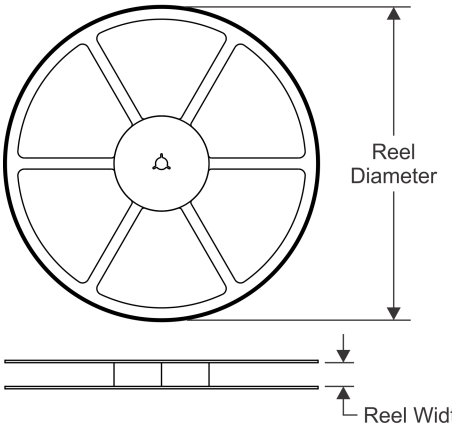
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

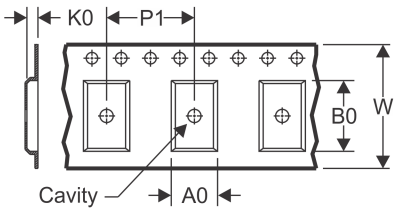
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

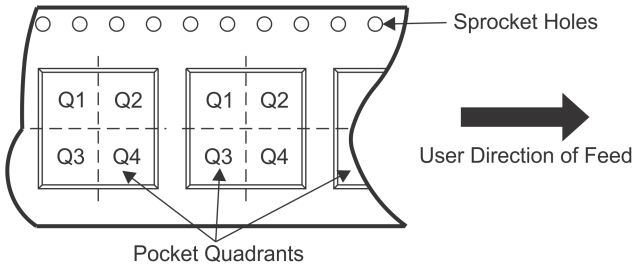


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

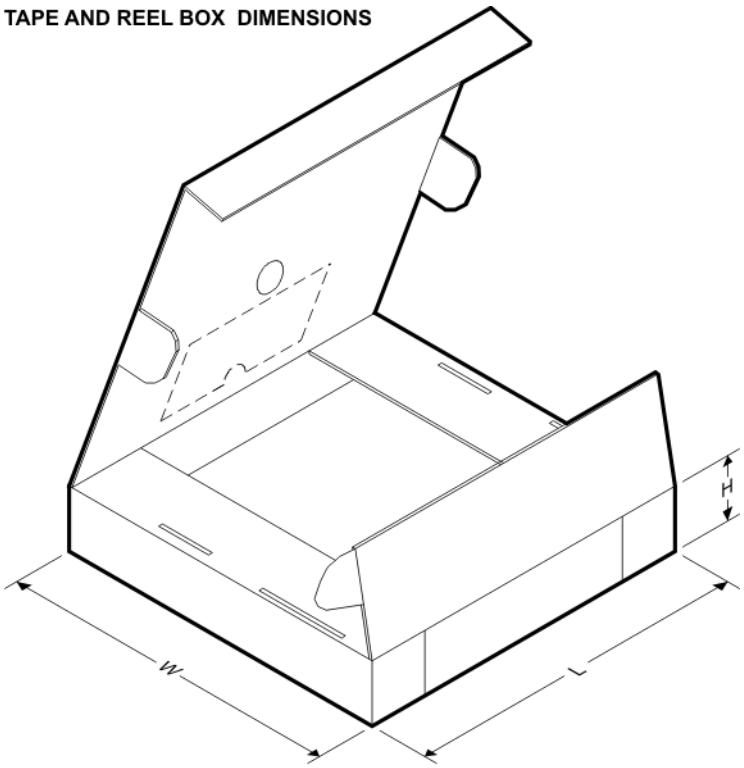
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4947TL/NOPB	DSBGA	YZR	25	250	178.0	8.4	2.69	2.69	0.76	4.0	8.0	Q1

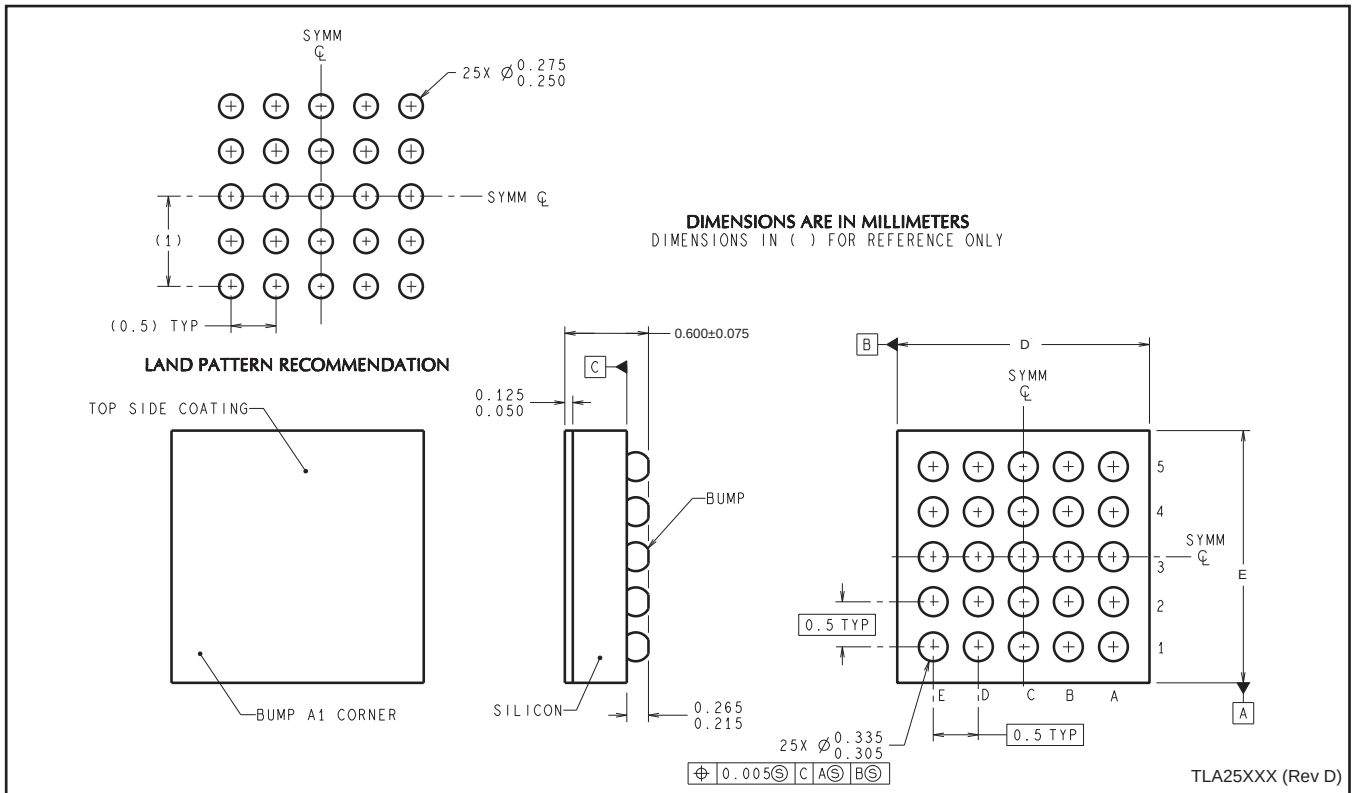
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4947TL/NOPB	DSBGA	YZR	25	250	210.0	185.0	35.0

YZR0025



D: Max = 2.532 mm, Min =2.472 mm

E: Max = 2.532 mm, Min =2.472 mm

4215055/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265