MCP795WXX/MCP795BXX Family Silicon Errata and Data Sheet Clarification

The MCP795WXX/MCP795BXX family devices that you have received conform functionally to the current Device Data Sheet (DS22280**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for all current production devices. The silicon issues are summarized in Table 1.

The errata described in this document will be addressed in a future revision of the MCP795WXX/MCP795BXX silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 1 apply to the current silicon revision (**A3**).
Note:	Operation below 3.6V is not affected.

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

TABLE 1: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A3
Time Registers	Fast Counter Operation	1.1	Time runs fast at VCC > 3.6V.	X
Clock Out	Incorrect Frequency for 1Hz and 4.096/8.192 kHz	1.2	Incorrect frequency when VCC > 3.6V.	X
Event Detect – Low Speed	Debounce Timing	1.3	Incorrect timing when VCC> 3.6V.	X
Watchdog Timer	Time-out Period and Reset Pulse Width	1.4	Incorrect time-out and pulse width when VCC > 3.6V.	X
Alarms	Incorrect Pulse Width when using $\overline{WDO}$ Pin	1.5	Incorrect pulse width when using the $\overline{WDO}$ pin and VCC > 3.6V.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1.1 Time Registers

When VCC is greater than 3.6V the internal time keeping registers do not count correctly, resulting in fast operation.

Work around

Operate the device at or below 3.6V.

1.2 Clock Out

When VCC is greater than 3.6V, setting a frequency on the clock out pin other than 32.768 kHz will result in the incorrect frequency.

Work around

Operate the device at or below 3.6V or select 32.768 kHz output. For the MCP795BXX the boot clock will be correct at 32.768 kHz.

1.3 Event Detect – Low Speed

When VCC is greater than 3.6V, the debounce timing will be incorrect from the value set by the EVLDB bit in register 0x0B.

Work around

Operate the device at or below 3.6V.

1.4 Watchdog Timer

When VCC is greater than 3.6V, both the Watchdog Time-out period, as set by WD<3:0> bits, and also the Watchdog Reset pulse period set by the WDTPLS bit in register 0x0A, will be incorrect.

Work around

Operate the device at or below 3.6V.

1.5 Alarms

If the $\overline{\text{WDO}}$ pin is selected as the alarm output pin, the alarm pulse generated will be incorrect.

Work around

Operate the device at or below 3.6V.

Affected Silicon Revisions

A3							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS22280**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (03/2012)

Initial release of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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