

2N5457, 2N5458

JFETs - General Purpose

N-Channel – Depletion

N-Channel Junction Field Effect Transistors, depletion mode (Type A) designed for audio and switching applications.

Features

- N-Channel for Higher Gain
- Drain and Source Interchangeable
- High AC Input Impedance
- High DC Input Resistance
- Low Transfer and Input Capacitance
- Low Cross-Modulation and Intermodulation Distortion
- Plastic Encapsulated Package
- Pb-Free Packages are Available*

MAXIMUM RATINGS

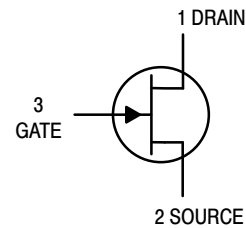
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	-25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	310 2.82	mW mW/ $^\circ\text{C}$
Operating Junction Temperature	T_J	135	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

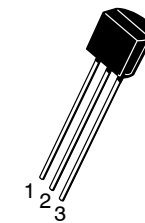


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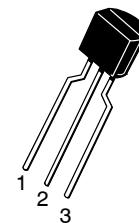
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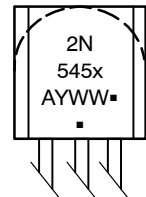
MARKING DIAGRAM



STRAIGHT LEAD
BULK PACK



BENT LEAD
TAPE & REEL
AMMO PACK



**TO-92
CASE 29
STYLE 5**

2N545x = Device Code

x = 7 or 8

A = Assembly Location

Y = Year

WW = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
2N5457	TO-92	1000 Units/Box
2N5457G	TO-92 (Pb-Free)	1000 Units/Box
2N5458	TO-92	1000 Units/Box
2N5458G	TO-92 (Pb-Free)	1000 Units/Box

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

2N5457, 2N5458

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage ($I_G = -10 \mu\text{Adc}$, $V_{DS} = 0$)		$V_{(BR)GSS}$	-25	-	-	Vdc
Gate Reverse Current ($V_{GS} = -15 \text{Vdc}$, $V_{DS} = 0$) ($V_{GS} = -15 \text{Vdc}$, $V_{DS} = 0$, $T_A = 100^\circ\text{C}$)		I_{GSS}	-	-	-1.0 -200	nAdc
Gate-Source Cutoff Voltage ($V_{DS} = 15 \text{Vdc}$, $i_D = 10 \text{nAdc}$)	2N5457 2N5458	$V_{GS(off)}$	-0.5 -1.0	-	-6.0 -7.0	Vdc
Gate-Source Voltage ($V_{DS} = 15 \text{Vdc}$, $i_D = 100 \mu\text{Adc}$) ($V_{DS} = 15 \text{Vdc}$, $i_D = 200 \mu\text{Adc}$)	2N5457 2N5458	V_{GS}	-	-2.5 -3.5	-	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (Note 1) ($V_{DS} = 15 \text{Vdc}$, $V_{GS} = 0$)	2N5457 2N5458	I_{DSS}	1.0 2.0	3.0 6.0	5.0 9.0	mAdc
DYNAMIC CHARACTERISTICS						
Forward Transfer Admittance (Note 1) ($V_{DS} = 15 \text{Vdc}$, $V_{GS} = 0$, $f = 1 \text{kHz}$)	2N5457 2N5458	$ Y_{fs} $	1000 1500	3000 4000	5000 5500	μhos
Output Admittance Common Source (Note 1) ($V_{DS} = 15 \text{Vdc}$, $V_{GS} = 0$, $f = 1 \text{kHz}$)		$ Y_{os} $	-	10	50	μhos
Input Capacitance ($V_{DS} = 15 \text{Vdc}$, $V_{GS} = 0$, $f = 1 \text{kHz}$)		C_{iss}	-	4.5	7.0	pF
Reverse Transfer Capacitance ($V_{DS} = 15 \text{Vdc}$, $V_{GS} = 0$, $f = 1 \text{kHz}$)		C_{rss}	-	1.5	3.0	pF

1. Pulse Width $\leq 630 \text{ms}$, Duty Cycle $\leq 10\%$.

2N5457, 2N5458

TYPICAL CHARACTERISTICS For 2N5457 Only

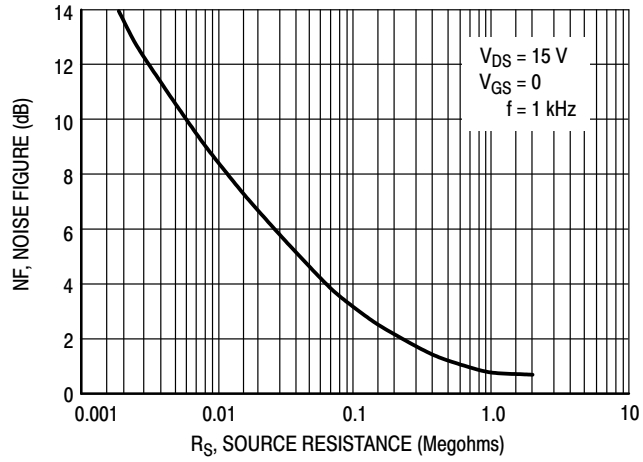


Figure 1. Noise Figure versus Source Resistance

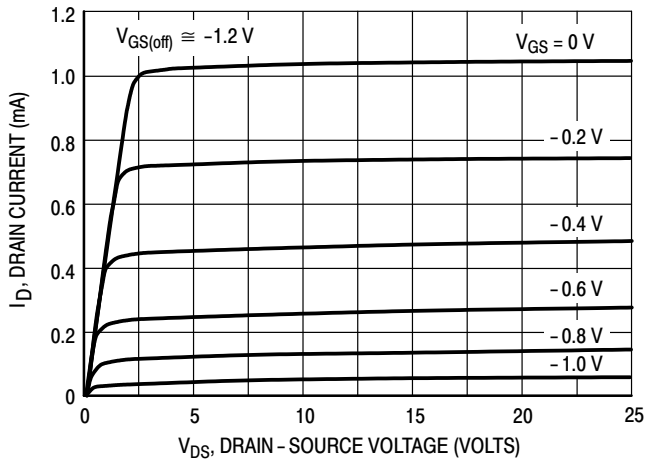


Figure 2. Typical Drain Characteristics

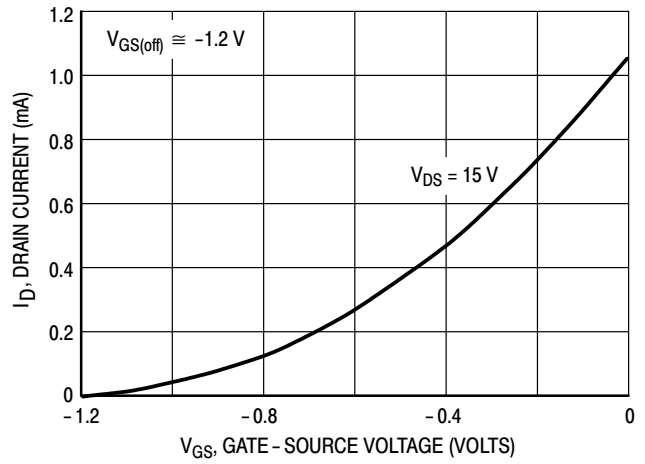


Figure 3. Common Source Transfer Characteristics

2N5457, 2N5458

TYPICAL CHARACTERISTICS For 2N5457 Only

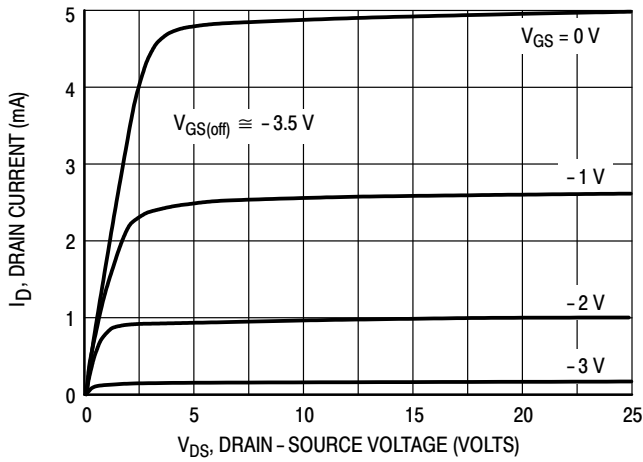


Figure 4. Typical Drain Characteristics

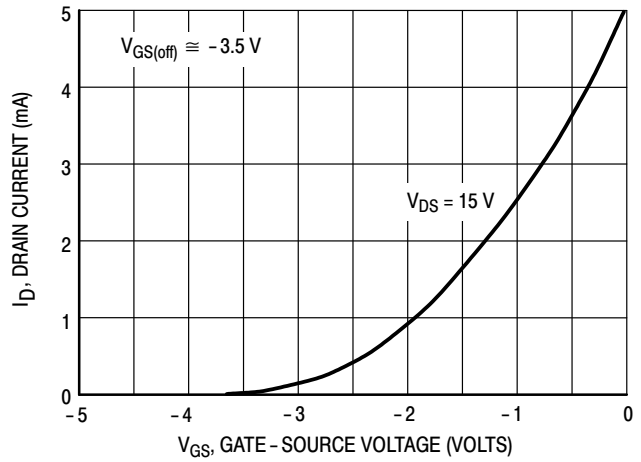


Figure 5. Common Source Transfer Characteristics

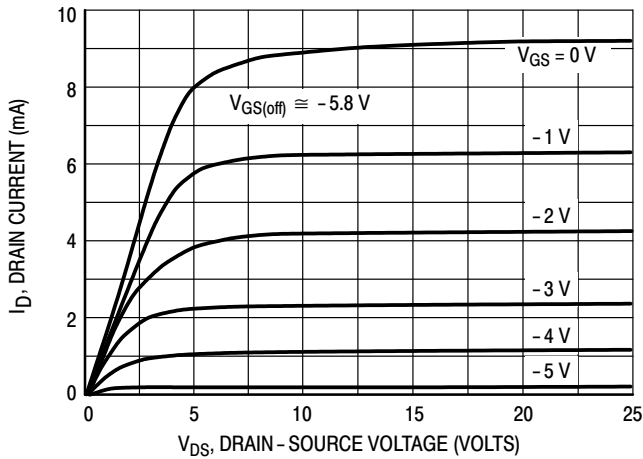


Figure 6. Typical Drain Characteristics

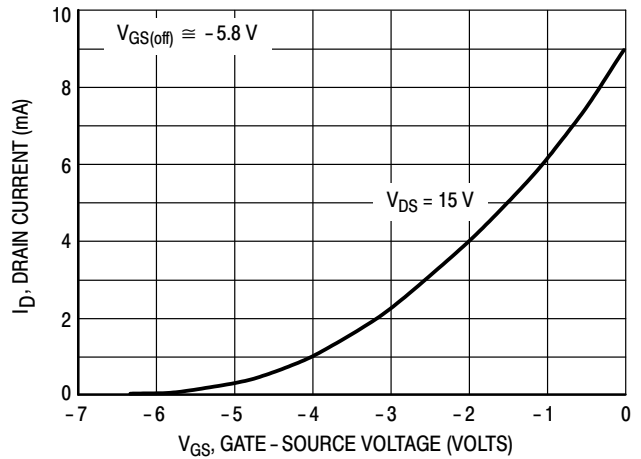


Figure 7. Common Source Transfer Characteristics

NOTE: Note: Graphical data is presented for dc conditions. Tabular data is given for pulsed conditions (Pulse Width = 630 ms, Duty Cycle = 10%). Under dc conditions, self heating in higher I_{DSS} units reduces I_{DSS} .

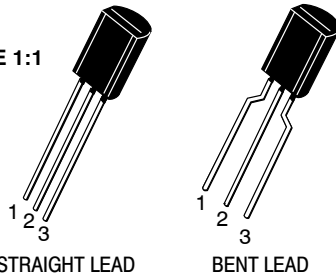
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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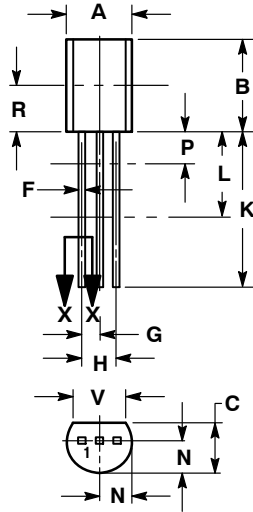


SCALE 1:1



TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE A

DATE 08 MAY 2012

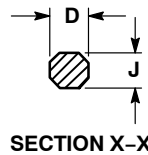


STRAIGHT LEAD

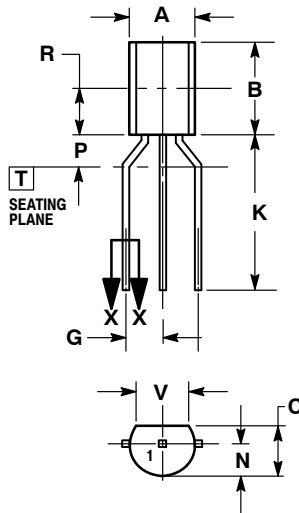
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---



SECTION X-X

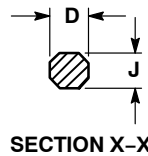


BENT LEAD

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

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C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
G	0.094	0.102	2.40	2.80
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---



SECTION X-X

STYLES ON PAGE 2

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**TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE A**

DATE 08 MAY 2012

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE


STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

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