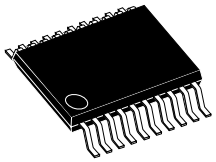
# STPM10

## Programmable single-phase energy metering IC with tamper detection

Datasheet - production data



TSSOP20

## Features

- Measures active, reactive, and apparent energies
- Current, voltage RMS and instantaneous measurement
- Frequency measurement
- Ripple-free active energy pulsed output
- Live and neutral monitoring for tamper detection
- Fast and simple one-point digital calibration over the whole current range
- Integrated linear voltage regulators for digital and analog supply
- Selectable RC or crystal oscillator
- Supports 50 - 60 Hz - IEC62052-11, IEC62053- 2x specifications
- Less than 0.1% error in the 1000:1 range
- Precision voltage reference: 1.23 V with 30 ppm/°C max.

## Description

The STPM10 is designed for effective measurement of active, reactive and apparent energy in a power line system using current transformer and shunt sensors. The device can be implemented for peripheral measurement in a microcontroller-based single-phase or poly-phase energy meter. The STPM10 consists of two main sections: analog and digital. The analog part is composed of preamplifier and first-order sigma-delta A/D converter blocks, a band-gap voltage reference and low-drop voltage regulator. The digital part is composed of system control, oscillator, hard-wired DSP and SPI interface. There is also an internal volatile memory, which is controlled through the SPI by means of a dedicated command set. The configured bits are used for configuration and calibration purposes. From a pair of sigma-delta output signals produced by the analog section, the DSP unit computes the amount of active, reactive and apparent energy consumed, as well as the RMS and instantaneous voltage and current values. The results of the computation are available as pulse frequencies and states on the digital outputs of the device, or as data bits in a data stream, which can be read from the device by means of the SPI interface. The system bus interface is also used for temporary programming of bits of internal volatile memory. The STPM10 generates an output signal with a pulse frequency proportional to the energy, and this signal is used in the calibration phase of the energy metering application.

**Table 1: Device summary**

| Oder code | Temperature range | Package | Packing |
|---|---|---|---|
| STPM10BTR | - 40 to 85 °C | TSSOP20 ( tape and reel) | 2500 pieces per reel |

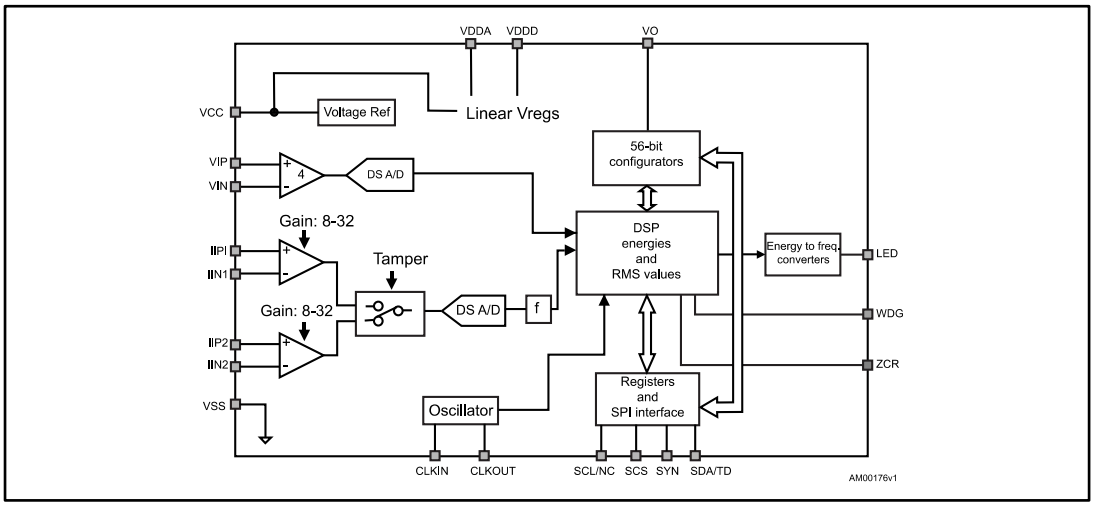
# Contents

# List of tables

# List of figures

# 1 Schematic diagram

**Figure 1: Block diagram**



# 2 Pin configuration

**Figure 2: Pin connections (top view)**

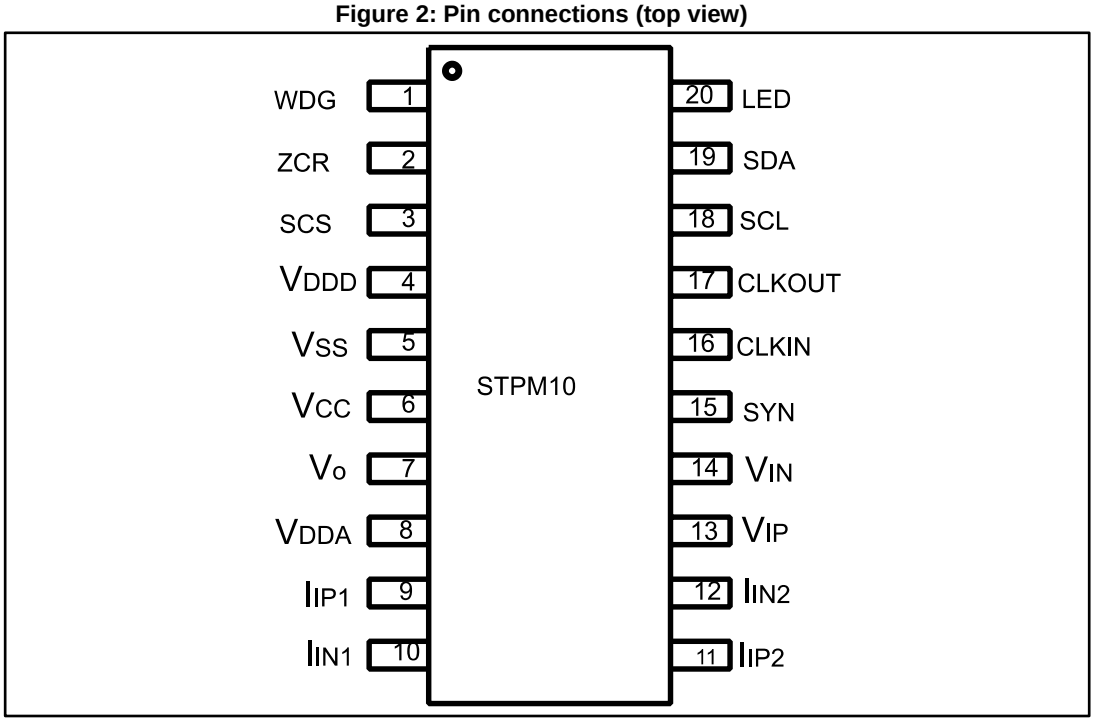



**Table 2: Pin description**

| Pin | Symbol | Type[(1)] | Description |
|---|---|---|---|
| 1 | WDG | D O | Watchdog |
| 2 | ZCR | D O | Zero-crossing signal |
| 3 | SCS | D IN | SPI interface enable pin |
| 4 | $V_{DDD}$ | A OUT | 1.8 V output of internal low drop regulator which supplies the digital core |
| 5 | $V_{SS}$ | GND | Ground |
| 6 | $V_{CC}$ | P IN | Supply voltage |
| 7 | $V_O$ | P OUT | Output of internal low drop regulator |
| 8 | $V_{DDA}$ | A OUT | 3 V output of internal low drop regulator which supplies the analog part |
| 9 | $I_{IP1}$ | A IN | Positive input of primary current channel |
| 10 | $I_{IN1}$ | A IN | Negative input of primary current channel |
| 11 | $I_{IP2}$ | A IN | Positive input of secondary current channel |
| 12 | $I_{IN2}$ | A IN | Negative input of secondary current channel |
| 13 | $V_{IP}$ | A IN | Positive input of voltage channel |
| 14 | $V_{IN}$ | A IN | Negative input of voltage channel |
| 15 | SYN | D I/O | SPI interface pin |
| 16 | CLKIN | A IN | Crystal oscillator input |
| 17 | CKOUT | A OUT | Crystal oscillator output |

| Pin | Symbol | Type(1) | Description |
|---|---|---|---|
| 18 | SCL | D I/O | SPI interface clock pin |
| 19 | SDA | D I/O | SPI interface data pin |
| 20 | LED | D O | Active energy pulsed output |

**Notes:**

(1)A: analog, D: digital, P: power.

# 3 Electrical ratings

**Table 3: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC input voltage | -0.3 to 6 | V |
| $I_{PIN}$ | Current on any pin (sink/source) | ± 150 | mA |
| $V_{ID}$ | Input voltage at digital pins (SCS, ZCR, WDG, SYN, SDA, SCL, LED) | -0.3 to $V_{CC}$ + 0.3 | V |
| $V_{IA}$ | Input voltage at analog pins ($I_{IP1}$, $I_{IN1}$, $I_{IP2}$, $I_{IN2}$, $V_{IP}$, $V_{IN}$) | -0.7 to 0.7 | V |
| ESD | Human body model (all pins) | ±3.5 | kV |
| $T_{OP}$ | Operating ambient temperature | -40 to 85 | C |
| $T_J$ | Junction temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage temperature range | -55 to 150 | °C |

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**Table 4: Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJA}$ | Thermal resistance junction-to-ambient | 114.5(1) | °C/W |

**Notes:**

(1)This value is based on a single-layer PCB, JEDEC standard test board.

# 4 Electrical characteristics

$V_{CC}$ = 5 V, $T_A$ = 25 °C, 100 nF to 1 µF between $V_{DDA}$ and $V_{SS}$, 100 nF to 1 µF between $V_{DDD}$ and $V_{SS}$, 100 nF to 1 µF between $V_{CC}$ and $V_{SS}$ unless otherwise specified.

**Table 5: Absolute maximum ratings**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Energy measurement accuracy** | | | | | | |
| $f_{BW}$ | Effective bandwidth | Limited by digital filtering (-3 dB) | 4 | | 800 | Hz |
| $e_{AW}$ | Accuracy of active power | Over 1 to 1000 of dynamic range | | 0.1 | | % |
| $e_{RW}$ | Accuracy of reactive power | Over 1 to 1000 of dynamic range | | 0.1 | | % |
| $e_{SW}$ | Accuracy of apparent power | Over 1 to 500 of dynamic range | | 0.1 | | % |
| SNR | Signal-to-noise ratio | Over the entire bandwidth | | 52 | | db |
| $PSRR_{DC}$ | Power supply DC rejection | Voltage signal: 200 $mV_{rms}$/50 Hz<br>Current signal: 10 mVrms/50 Hz<br>$f_{CLK}$= 4.194 MHz<br>$V_{CC}$=3.3 V ±10%, 5 V±10% | | | 0.2 | % |
| $PSRR_{AC}$ | Power supply AC rejection | Voltage signal: 200 $mV_{rms}$/50 Hz<br>Current signal: 10 mVrms/50 Hz<br>$f_{CLK}$= 4.194 MHz<br>$V_{CC}$ = 3.3 V+0.2 $V_{rms}$1@100 Hz<br>$V_{CC}$ = 5.0 V+0.2 $V_{rms}$1@100 Hz | | | 0.1 | % |
| **General section** | | | | | | |
| $V_{CC}$ | Operating supply voltage | | 3.165 | | 5.5 | V |
| $I_{CC}$ | Supply current Configuration registers cleared | 4 MHz, $V_{CC}$ = 5 V | | 3 | 4 | mA |
| | | 8 MHz, $V_{CC}$ = 5 V | | 5 | 6 | |
| POR | Power-on-reset on $V_{CC}$ | | | 2.5 | | V |
| $V_{DDA}$ | Analog supply voltage | | 2.85 | 3.00 | 3.15 | V |
| $V_{DDD}$ | Digital supply voltage | | 1.725 | 1.80 | 1.875 | V |
| $f_{CLK}$ | Oscillator clock frequency | MDIV bit = 0 | 4.000 | | 4.194 | MHz |
| | | MDIV bit = 1 | 8.000 | | 8.192 | |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{LINE}$ | Nominal line frequency | | 45 | | 65 | Hz |
| $I_{LATCH}$ | Current injection latch-up immunity | | | | 300 | mA |
| **Analog inputs ($I_{IP1}$, $I_{IN1}$, $I_{IP2}$, $I_{IN2}$, $V_{IP}$, $V_{IN}$)** | | | | | | |
| $V_{MAX.}$ | Maximum input signal levels | Voltage channel | -0.3 | | +0.3 | V |
| | | Current channel, gain 8X | -0.15 | | +0.15 | V |
| | | Current channel, gain 32X | -0.035 | | +0.035 | V |
| $f_{ADC}$ | A/D converter bandwidth | | | 10 | | kHz |
| $f_{SPL}$ | A/D sampling frequency | | | FCLK/4 | | Hz |
| $V_{OFF}$ | Amplifier offset | | | | ±20 | mV |
| $Z_{IP}$ | $V_{IP}$, $V_{IN}$ impedance | Over the total operating voltage range | 100 | | 400 | kΩ |
| $Z_{IN}$ | $I_{IP1}$, $I_{IN1}$, $I_{IP2}$, $I_{IN2}$ impedance | Over the total operating voltage range | | 100 | | kΩ |
| $G_{ERR}$ | Current channels gain error | | | ±10 | | % |
| $I_{VL}$ | Voltage channel leakage current | | -1 | | 1 | µA |
| $I_{IL}$ | Current channel leakage current | Channel disabled (PST=0 to 1 CH2 disabled if CSEL=0, CH1 disabled if CSEL=1) or device off | -1 | | 1 | µA |
| | | Input enabled | -15 | | 15 | µA |
| **Digital I/O characteristics (SDA, CLKIN, CLKOUT, SCS, SYN, LED)** | | | | | | |
| $V_{IH}$ | Input high voltage | SDA, SCS, SYN, LED | 0.75 $V_{CC}$ | | | V |
| | | CLKIN | 1.5 | | | |
| $V_{IL}$ | Input low voltage | SDA, SCL, SYN, LED | | | 0.75 $V_{CC}$ | V |
| | | CLKIN | | | 0.8 | |
| $V_{OH}$ | Output high voltage | $I_O$ = -2 mA | $V_{CC}$-0.4 | | | V |
| $V_{OL}$ | Output low voltage | $I_O$ = +2 mA | | | 0.4 | V |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{UP}$ | Pull-up current | | | 15 | | µA |
| $t_{TR}$ | Transition time | $C_{LOAD}$ = 50 pF | | 10 | | ns |
| **Crystal oscillator** | | | | | | |
| $I_I$ | Input current on CLKIN | | | | 1 | µA |
| $R_P$ | External resistor | 1 | | | 4 | MΩ |
| Cp | External capacitors | | | 22 | | pF |
| $f_{CLK}$ | Nominal output frequency | | 4.00 | 4.194 | | MHz |
| | | | 8.00 | 8.192 | | |
| $I_{CLKIN}$ | Settling current | $f_{CLK}$ = 4 MHz | 40 | | 60 | µA |
| $R_{SET}$ | Settling resistor | | | 12 | | kΩ |
| $t_{JIT}$ | Frequency jitter | | | 1 | | ns |
| **On-chip reference voltage** | | | | | | |
| $V_{REF}$ | Reference voltage | | | 1.23 | | V |
| | Reference accuracy | | | ±1 | | % |
| $T_C$ | Temperature coefficient | After calibration | | 30 | 50 | ppm/°C |
| **SPI interface timing** | | | | | | |
| $F_{SCLKr}$ | Data read speed | After calibration | | | 32 | MHz |
| $F_{SCLKw}$ | Data write speed | | | | 100 | MHz |
| $t_{DS}$ | Data set-up time | | 20 | | | ns |
| $t_{DH}$ | Data hold time | | 0 | | | ns |
| $t_{ON}$ | Data driver on time | | | | 20 | |
| $t_{OFF}$ | Data driver off time | | | | 20 | |
| $t_{SYN}$ | SYN active width | | $2/f_{CLK}$ | | | s |

# 5 Terminology

## 5.1 Measurement error

The error associated with the energy measurement made by the STPM10 is defined as: percentage error = [STPM10 (reading) - true energy] / true energy.

## 5.2 ADC offset error

This is the error due to the DC component associated with the analog inputs of the A/D converters. Due to the internal automatic DC offset cancellation, the STPM10 measurement is not affected by DC components in the voltage and current channel. The DC offset cancellation is implemented in the DSP.

## 5.3 Gain error

The power section is implemented with an avalanche ruggedness N-channel MOSFET, which guarantees safe operation within the specified energy rating as well as high dv/dt capability. The power section has a $BV_{DSS}$ of 800 V min. and a typical $R_{DS(on)}$ of 20 Ω at 25 °C.

The integrated SenseFET structure allows a virtually loss-less current sensing.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the Power section cannot be turned on accidentally.

## 5.4 Power supply DC and AC rejection

This parameter quantifies the STPM10 measurement error as a percentage of the reading when the power supplies are varied. With reference to the PSRRAC measurement, a reading at two nominal supply voltages (3.3 and 5 V) is taken. A second reading is obtained with the same input signal levels when an AC (200 $mV_{RMS}$/100 Hz) signal is introduced on the supplies. Any error introduced by this AC signal is expressed as a percentage of the reading. Concerning the PSRRDC measurement, a reading at two nominal supply voltages (3.3 and 5 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ± 10%. Any error introduced is again expressed as a percentage of the reading.

## 5.5 Conventions

The lowest analog and digital power supply voltage is called VSS, which represents system ground (GND). All voltage specifications for digital input/output pins are referred to GND. Positive currents flow into a pin. Sinking current refers to the current flowing into the pin, and thus it is positive. Sourcing current means that the current is flowing out of the pin, so it is negative. Timing specifications of signals treated by the digital control part are relative to CLKOUT. This signal is provided by the 4.194 MHz nominal-frequency crystal oscillator or from the internal RC oscillator. An external source of 4.194 MHz or 8.192 MHz can also be used. Timing specifications of signals from the SPI interface are relative to the SCL, and there is no direct relationship between the clock (SCL) of the SPI interface and the clock of the DSP block. A positive logic convention is used in all equations.

# 6 Typical performance characteristics

**Figure 3: Supply current vs. supply voltage, TA = 25 °C (f = 4.194 MHz, 8.192 MHz)**

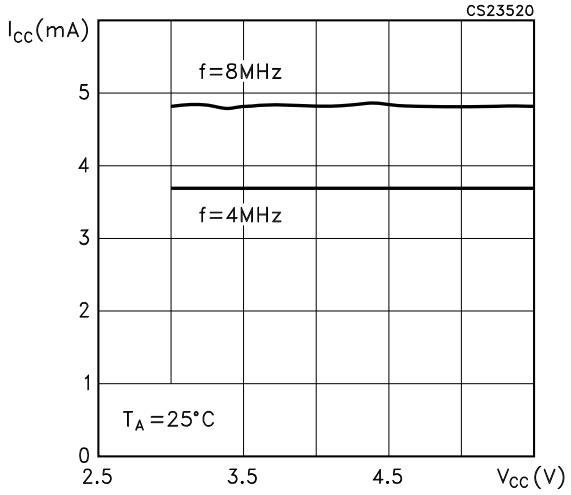



**Figure 4: RC oscillator frequency vs. VCC, R = 12 kΩ, TA = 25 °C**

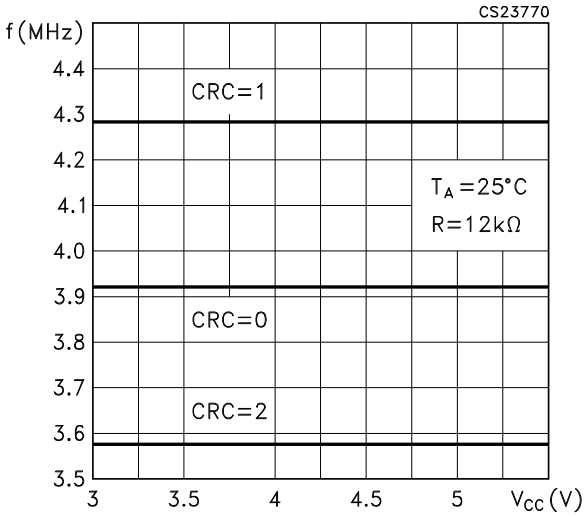



**Figure 5: RC oscillator: frequency jitter vs. temperature**

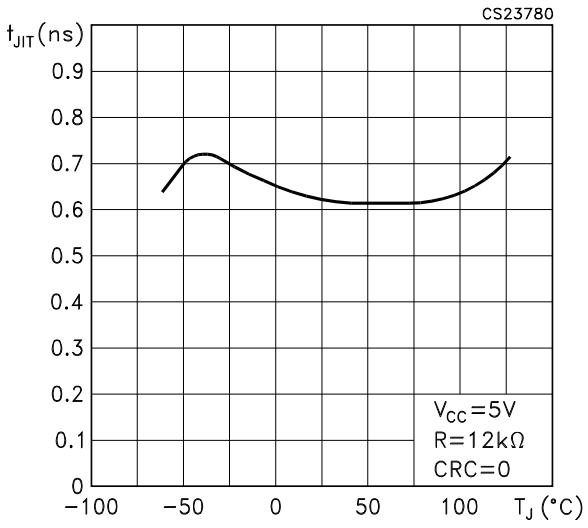



**Figure 6: Analog voltage regulator: line - load regulation**

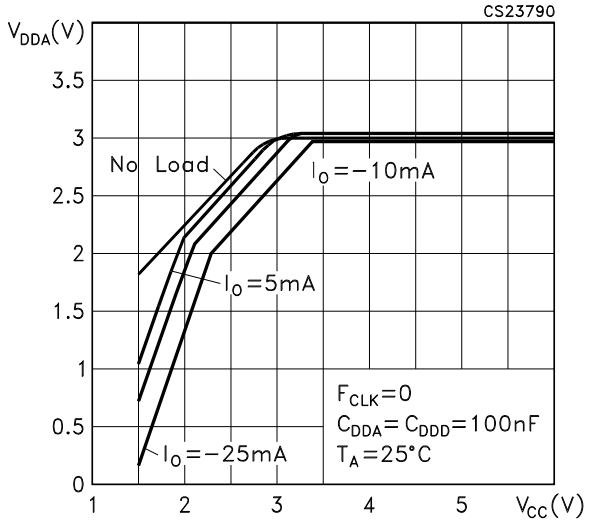


**Figure 7: Digital voltage regulator: line - load regulation**

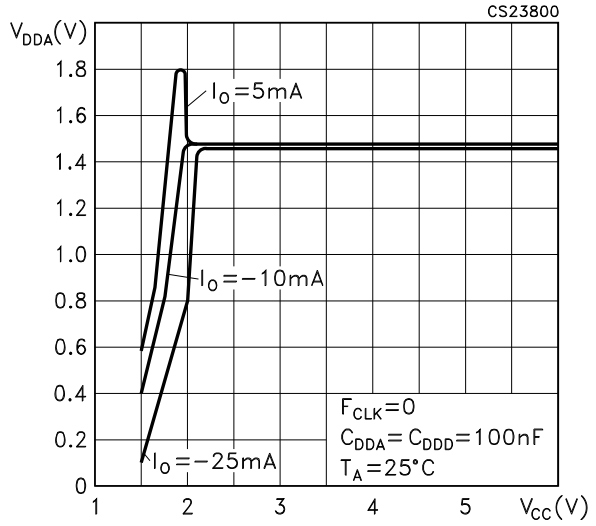



**Figure 8: Voltage channel linearity at different VCC voltages**

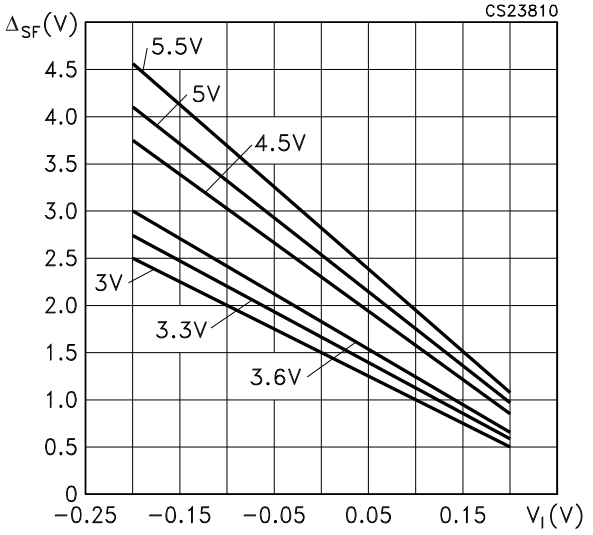



**Figure 9: Power supply AC rejection vs. VCC**

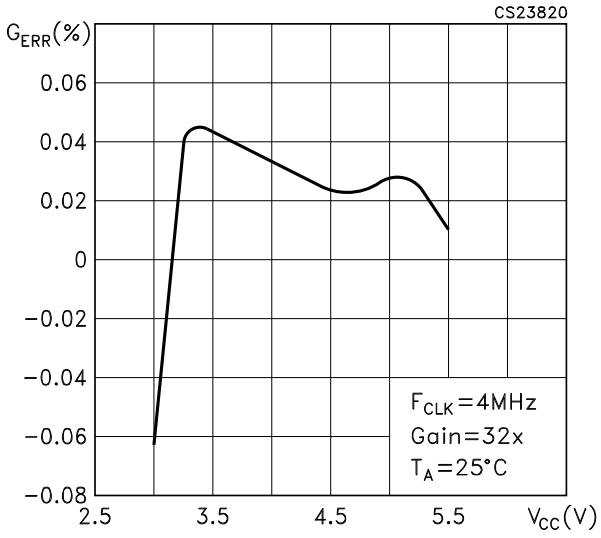



**Figure 10: Power supply DC rejection vs. VCC**

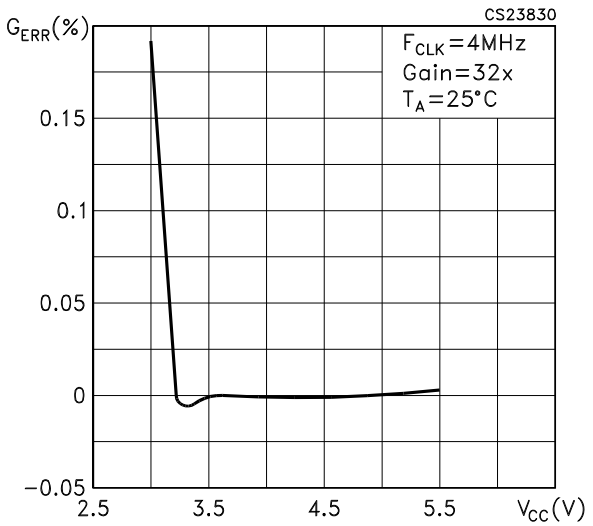


**Figure 11: Error over dynamic range gain dependence**

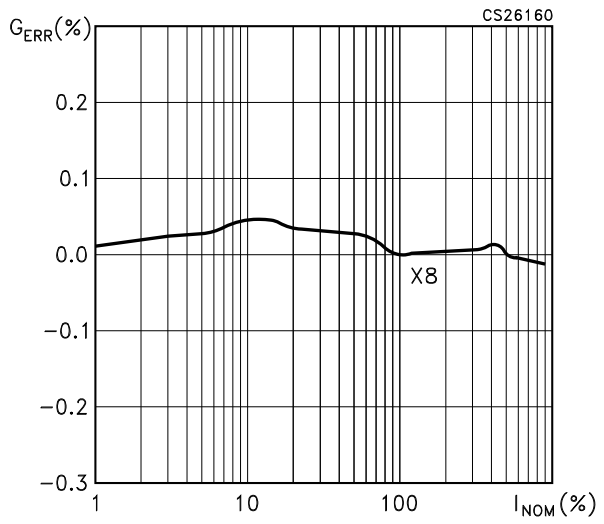



**Figure 12: Primary current channel linearity at different VCC**

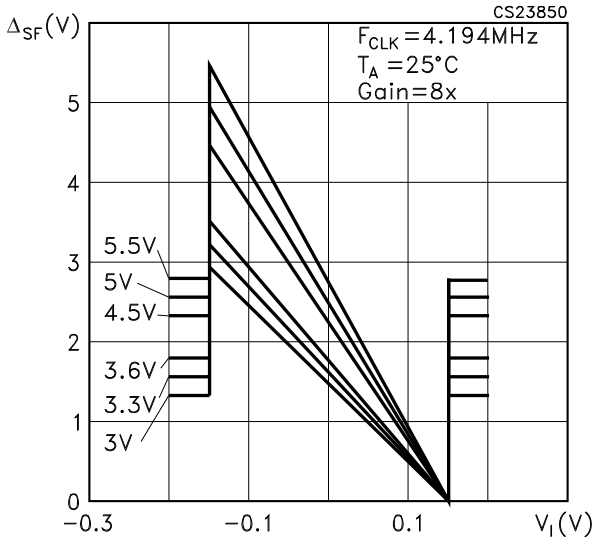
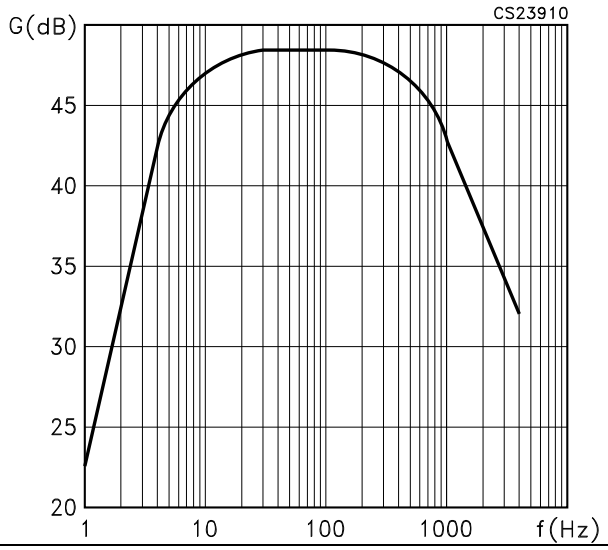



**Figure 13: Gain response of ΔΣ A/D converters**



# 7 Theory of operation

## 7.1 General operation description

The STPM10 is capable of performing measurements of active, reactive and apparent energy, RMS and instantaneous voltage and current values, and line frequency information. Most of the functions are fully programmable using internal configuration bits accessible through the SPI interface. The STPM10 works as a peripheral in microcontroller-based metering systems. The ZCR and WDG pins are used to provide zero-crossing and watchdog information, and the SPI pins are used to communicate with the microcontroller. The STPM10 includes volatile internal registers that hold the useful information about the metering system. Two kinds of active energy are available: wide-band active energy (AW) which includes all harmonic content (also called type 0) and fundamental active energy (AF), limited to the 1$^{st}$ harmonic (also called type 1). This latter energy value is obtained by filtering type 0 active energy. Both of the two active energies are stored in up-down counting accumulator registers with a 20-bit length. Reactive and apparent energies are also available with a 20-bit accumulation. The STPM10 also provides the RMS values for voltage and current. Due to the modest dynamic variation of the voltage, the RMS value is stored with a resolution of 11 bits, while the RMS current value has a resolution of 16 bits. The instantaneous (momentary) sampled value of voltage and current are also available with a resolution of 11 and 16 bits, respectively. The line frequency value is stored with a resolution of 14 bits. Due to the proprietary energy computation algorithm, the STPM10 calibration is quick and simple, allowing calibration at only one point over the entire current range. The configuration and calibration parameters must be downloaded in the internal non-volatile memory of the STPM10 at power-up.

## 7.2 Analog inputs

The STPM10 has one fully differential voltage input channel and two fully differential current input channels. The voltage channel consists of a differential amplifier with a gain of 4. The maximum differential input voltage for the voltage channel is ± 0.3 V. The two current channels are multiplexed (see *Section 7.9: "Tamper detection module"* for details) to provide a single input to a preamplifier with a gain of 4. The output of this preamplifier is connected to the input of a programmable gain amplifier (PGA) with possible gain selections of 2 and 8. The total gain of the current channels are then 8 and 32. The gain selections are made by writing to the gain register, and they can be different for the two current channels. If the tamper function is not used, the secondary current can be disabled. The maximum differential input voltage is dependent on the selected gain, in accordance with the table below.

**Table 6: Gain of voltage and current channels**

| Voltage channels | | Current channels | |
|---|---|---|---|
| **Gain** | **Max. input voltage (V)** | **Gain** | **Max. input voltage (V)** |
| 4 | ±0.30 | 8X | ±0.15 |
| | | 32X | ±0.35 |

The gain register is included in the device configuration register with the address name PST. The table below shows the gain configuration according to the register values:

**Table 7: Configuration of current sensors**

| Primary | | Secondary | | Configuration bits | |
|---|---|---|---|---|---|
| **Gain** | **Sensor** | **Gain** | **Sensor** | **PST** | **TMP** |
| 8 | CT | Disabled | Disabled | 0 | 0 |
| 32 | Shunt | Disabled | Disabled | 1 | 0 |
| 8 | CT | 8 | CT | 0 | 1 |
| 8 | | 32 | Shunt | 1 | 1 |

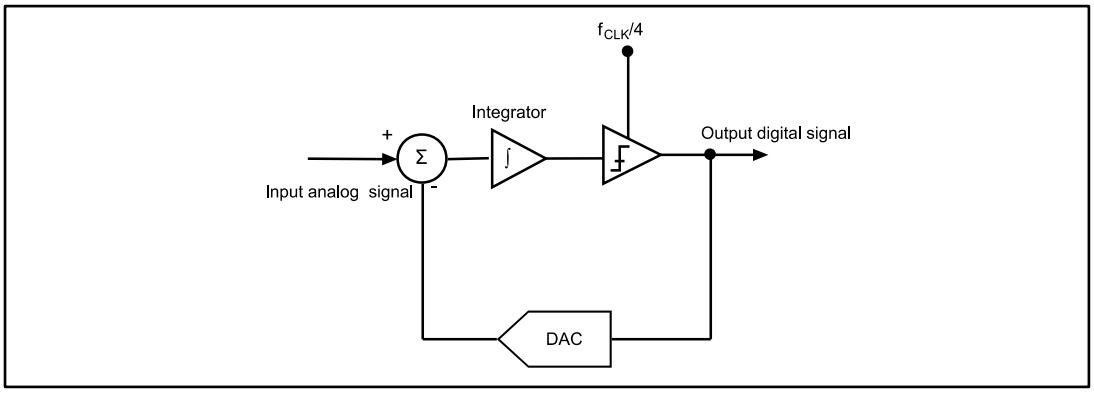
If the device is used in configuration PST = 1, TMP = 1 (primary channel with CT, secondary channel with Shunt), the shunt $K_s$ must always be equal to one fourth of the current transformer $K_s$.

Both the voltage and current channels implement an active offset correction architecture which provides the benefit of avoiding any offset compensation. The analog voltage and current signals are processed by the ΣΔ analog-to-digital converters, which feed the hardwired DSP. The DSP implements an automatic digital offset cancellation that makes it possible to avoid any manual offset calibration on the analog inputs.

## 7.3 ΣΔ A/D converters

Analog-to-digital conversion in the STPM10 is carried out using two first-order ΣΔ converters. The device performs A/D conversions of analog signals on two independent channels in parallel. The current channel is multiplexed as a primary or secondary current channel in order to perform the tamper function, if enabled. The converted ΣΔ signals are supplied to the internal hard-wired DSP unit, which filters and integrates these signals in order to boost the resolution and to yield all the necessary signals for the computations. A ΣΔ modulator converts the input signal into a continuous serial stream of 1's and 0's at a rate determined by the sampling clock. In the STPM10, the sampling clock is equal to $f_{CLK}/4$. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) can approach that of the input signal level. When a large number of samples are averaged, a very precise value for the analog signal is obtained. This averaging is carried out in the DSP section, which implements decimation, integration and DC offset cancellation of the supplied ΣΔ signals. The gain of the decimation filters is 1.004 for the voltage channel and 0.502 for the current channel. The resulting signal has a resolution of 11 bits per voltage channel and 16 bits per current channel.

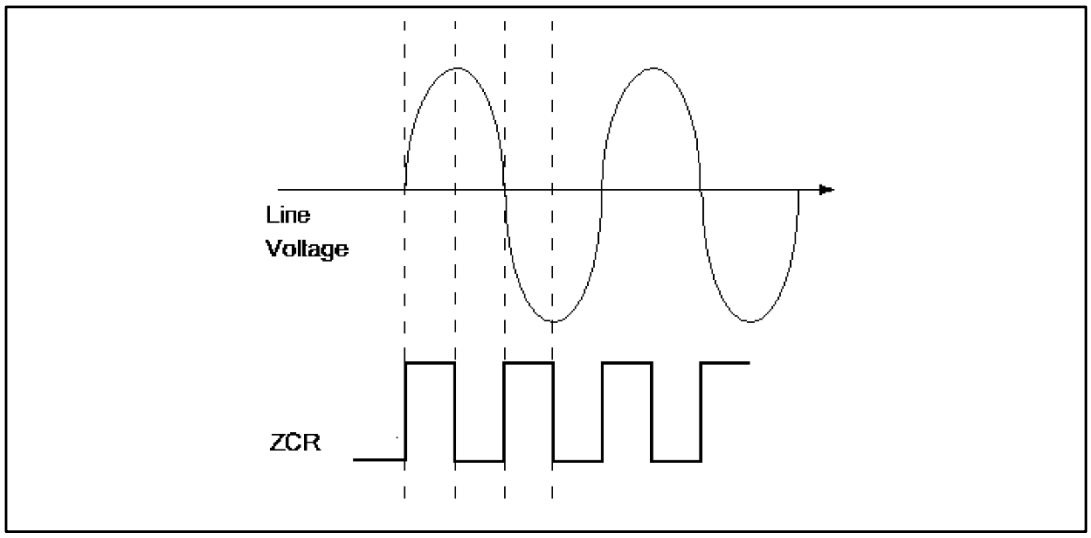
**Figure 14: First-order ΣΔ A/D converter**




## 7.4 Zero-crossing detection

The STPM10 has a zero-crossing detector circuit on the voltage channel which can be used by application for synchronization of some utility equipment in the event of zero-crossing of the line voltage. This circuit produces the internal signal ZCR which has a rising edge every time the line voltage crosses zero, and a negative edge every time the voltage reaches its positive or negative peak. The ZCR signal is then at twice the line voltage frequency. The ZCR signal is available on the ZCR pin.

**Figure 15: ZCR signal**

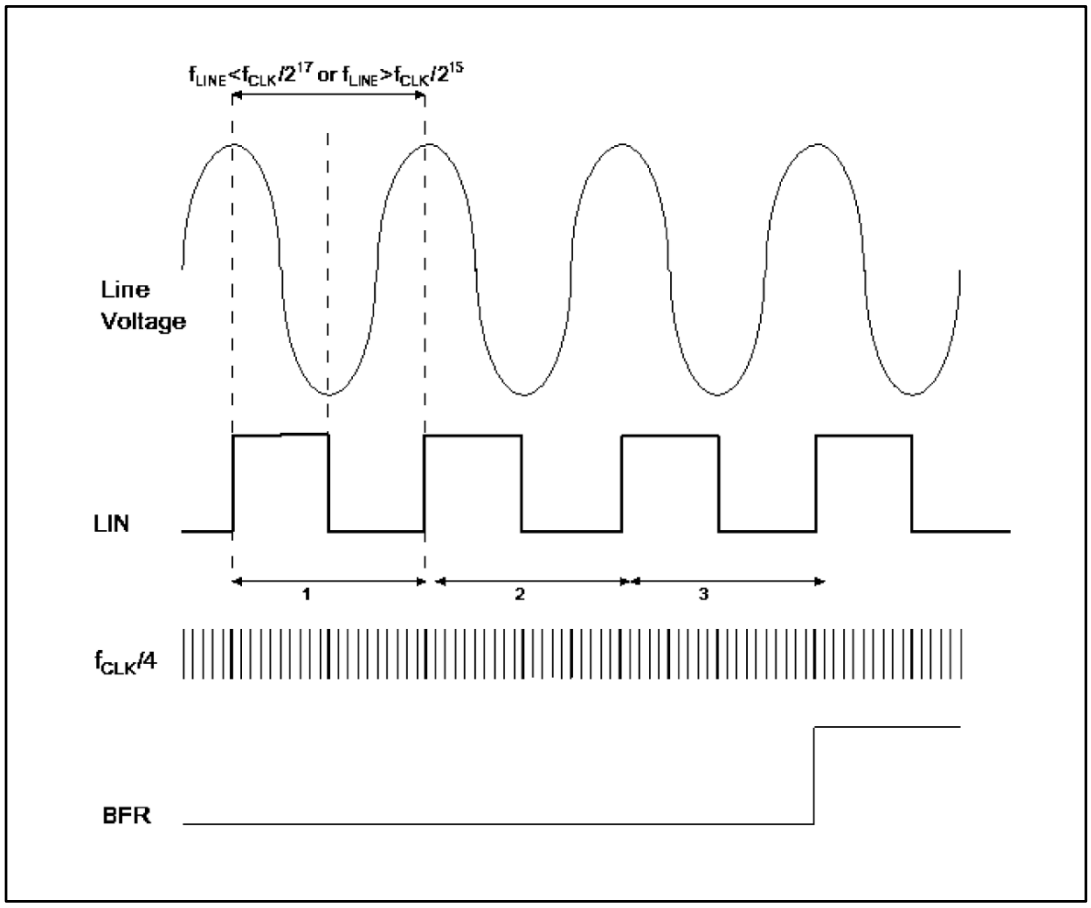



## 7.5 Period and line voltage measurement

The period module measures the period of the base frequency of the voltage channel and checks if the voltage signal frequency is within the $f_{CLK}/217$ to $f_{CLK}/215$ band. To do this, the LIN signal is produced, which is low when the line voltage rises, and high when the line voltage falls. This means that the LIN signal is the sign of dv/dt. With further elaboration, the ZCR signal is also produced. On the trailing edge of LIN (line frequency) the period counter starts counting up pulses of the $f_{CLK}/4$ reference signal. The LIN signal is available on the status bit register (see *Table 10: "Status bit description"* ). If the counted number of pulses between two trailing edges of LIN is higher than 215, or if the counting is never

stopped (no LIN trailing edge) this means that the base frequency is lower than $f_{CLK}/217$ Hz and a BFR (base frequency range) error flag is set.

**Figure 16: LIN and BFR signals**




If the number of pulses counted between two trailing edges of LIN is lower than 213, the base frequency exceeds the limit (this means it is higher than $f_{CLK}/215$). In this case, the error must be repeated three consecutive times in order to set the BFR error flag. For example, with a 4.194304 MHz oscillator frequency and MDIV bit clear (or 8.192 MHz with MDIV set), $f_{CLK}/4$ is 1.048576 MHz. If the line frequency is 30 Hz, the counted $f_{CLK}/4$ pulses between two LIN trailing edges are 34952, more than 215 (32768 pulses). The BFR low frequency limit is as follows:

$f_{CLK}/217 = 4194304/131072 = 32$ Hz

With the same clock frequency, if the line frequency is 130 Hz, the $f_{CLK}/4$ pulses between two LIN trailing edges are 8066, less than 213 (8192). The BFR high frequency limit is then:

$f_{CLK}/215 = 4194304/32768 = 128$ Hz

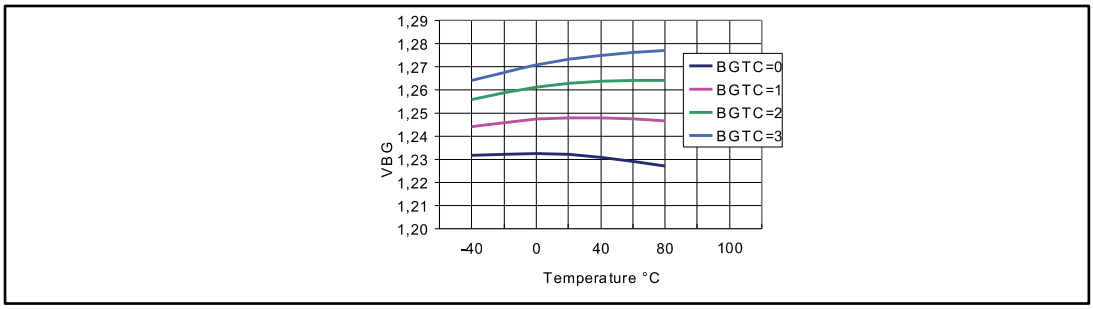
The BFR flag is also set if the register value of the RMS voltage drops below 64. BFR is cleared when the register value goes above 128. The BFR, then, also gives information about the presence of the line voltage within the meter. When the BFR error is set, the computation of power is zero unless the FRS bit is set. In fact, the effect of the BFR bit can be overridden by setting FRS configuration bit.

It means that if FRS is set and BFR is also set, all the energy computation is carried on as BFR was cleared. In this case then p=u*i, where u could be zero or not (if BFR was set because voltage RMS register value is below 64). When the line frequency re-enters the nominal band, the BFR flag is automatically reset. This BFR error flag is also assembled as part of the 8-bit status register (see *Table 10: "Status bit description"*).

## 7.6 Power supply

The main STPM10 supply pin is the VCC pin. From the VCC pin two linear regulators provide the necessary voltage for the analog part VDDA (3 V) and for the digital part VDDD (1.8 V). The VSS pin represents the reference point for all the internal signals. A 100 nF low ESR capacitor should be connected between VCC and VSS, VDDA and VSS, VDDD and VSS. All these capacitors must be located very close to the device. The STPM10 contains a power on reset (POR) detection circuit. If the VCC supply is less than 2.5 V, then the STPM10 goes into an inactive state, all the functions are blocked and a reset condition is asserted. This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering, which give a high degree of immunity from false triggering due to noisy supplies. A band-gap voltage reference (VBG) of 1.23 V ±1% is used as the reference voltage level source for the two linear regulators and for the A/D converters. Also, this module produces several bias currents and voltages for all other analog modules. The band-gap voltage can be compensated regardless of the temperature variations with the BGTC bits.

**Figure 17: Band-gap temperature variation**




## 7.7 Load monitoring

The STPM10 includes a no-load condition detection circuit with adjustable threshold. This circuit monitors the voltage and the current channels and, when the measured voltage is below the set threshold, the internal signal BIL becomes high. Information about this signal is also available in the status bit BIL.

The no-load condition occurs when the product of the VRMS and IRMS register values is below a given value. This value can be set with the LTCH configuration bits. Four different no-load threshold values can be chosen according to the two configuration bits LTCH (see table below). When a no-load condition occurs (BIL=1) the integration of power is suspended and the tamper module is disabled. The BIL signal can be accessed only through the SPI interface.

**Table 8: No-load detection thresholds**

| LTCH | $K_{LTCH}$ |
|---|---|
| 0 | 800 |
| 1 | 1600 |
| 2 | 3200 |
| 3 | 6400 |

## 7.8 Error detection

In addition to the no-load condition and the line frequency band, the integration of power can also be suspended due to an error detected on the source signals. There are two kinds of error-detection circuits involved. The first checks all the ΣΔ signals from the analog part if any is stacked at 1 or 0 within the 1/128 of $f_{CLK}$ period of observation. In case of a detected error, the corresponding ΣΔ signal is replaced with an idle ΣΔ signal, which represents a constant value of 0. All error and other resolved flags are treated as bits of a device status and can be read out by means of the SPI interface. Another error condition occurs if LED pin output signals are different from the internal signals that drive them. This can occur if some of these pins are forced to GND or to some other imposed voltage value. In this case, the internal status bit PIN is activated, providing the information that some hardware problem has been detected.

## 7.9 Tamper detection module

The STPM10 measures the current in both live and neutral wire with a time domain multiplexing approach on a unique sigma delta modulator. This mechanism is adopted to implement anti-tamper function. If this function is selected (see *Table 7: "Configuration of current sensors"*), the live and neutral wire currents are monitored; when the difference between the two measurements exceeds a rated threshold, the STPM10 enters the "tamper state", while in "normal state" the two measurements are below the threshold. In particular, both channels are not observed all the time, rather a time multiplex mechanism is used. During the observation time of each channel, its active energy is calculated. A tamper condition occurs when the absolute value of the difference between the two active energy values is greater than a certain percentage of the averaged energy during the activated tamper module (see equation below). This percentage value can be selected between two different values (12.5% and 6.25%) according to the value of the configuration bit CRIT. The tamper condition is detected when the following formula is satisfied:

**Equation 1:**

EnergyCH1 - EnergyCH2 > KCRIT (EnergyCH1 + EnergyCH2)/2

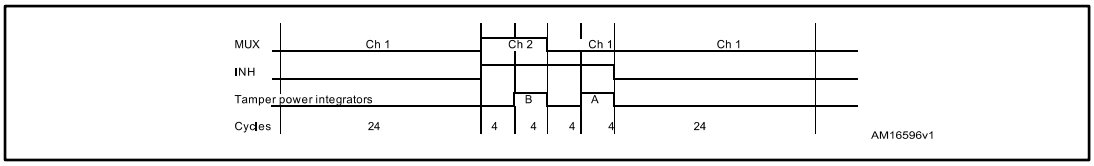
where $K_{CRIT}$ can be 12.5% or 6.25%.

The detection threshold is much higher than the accuracy difference of the current channels, which should be less than 0.2 %, but, some headrooms should be left for possible transition effect, due to accidental synchronism of actual load current change with the rhythm of taking the energy samples. The tamper circuit works if the energies associated with the two current channels are both positive or negative, if the two energies have different sign, the tamper is on all the time however, the channel with the associated higher power is selected for the final computation of energy. When internal signals are not good enough to perform the calculations, i.e. line period is out or range or ΔΣ signals from analog section are stacked at high or low logic level, or no-load condition is activated, the tamper module is disabled and its state is preset to normal.

### 7.9.1 Detail operational description

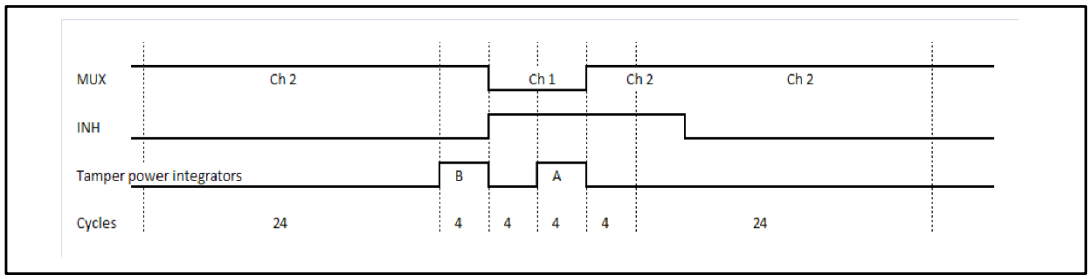
The meter is initially set to normal state, i.e. tamper not detected. In this condition the primary channel is selected for final integration of energy. In such state the values of both load currents should not differ more than the accuracy difference of the channels does. Sixty-four periods of line voltage is used as a tamper checking period. After 24 periods of line voltage two internal signals MUX and INH are changed in order to enable secondary current channel and to freeze the last power and RMS values of primary current channel. The following 16 periods of line frequency are used for tamper detection integration. During this gap, the final energy calculation does not use the signal from selected channel but the frozen values. Four line periods after the INH switch, the integration of power from secondary current channel is started and lasts four periods. Additional four line periods later MUX signal is switched back to primary current channel and the integration for tamper detection is started. The timings of MUX and INH signals are shown in the figure below.

**Figure 18: Timings of tamper module - primary channel selected**




When the secondary channel is selected to be integrated by the final energy integrator, the MUX and INH signals change according to the figure below.

**Figure 19: Timings of tamper module - secondary channel selected**




This means that energy of four periods from secondary channel followed by energy of four periods from primary channel is sampled within the tamper module. From these two samples, called B and A respectively, the criteria of tamper is calculated and the channel with higher current is selected, resulting in a new tamper state. If four consecutive new results of criteria happen, i.e. after elapsed 5.12 s at 50 Hz, the meter enters into tamper state. Thus, the channel with the higher current is selected for the energy calculation. If samples of power A and B had different signs, the tamper would be on all the time but, the channel with bigger power would be still selected for the final integration of energy. If a tamper status has been detected, the multiplex ratio is 56:8 if the primary channel energy is greater than the secondary one, otherwise it is 8:56. The detected tamper condition is stored in the BIT status bit. If BIT = 0 tamper is not detected, if BIT = 1 a tamper condition has been detected. In standalone mode the BIT flag is also available in the SDATD pin.

## 7.10 Phase compensation

The STPM10 does not introduce any phase shift between the voltage and current channel. However, the voltage and current signals come from transducers, which could have inherent phase errors. For example, a phase error of 0.1 ° to 0.3 ° is not uncommon for a

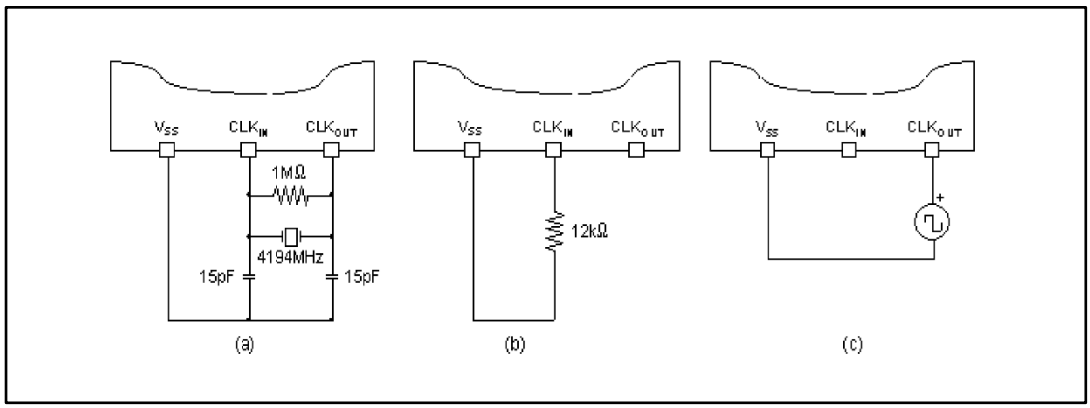
current transformer (CT). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The STPM10 can calibrate these small phase errors by introducing delays on the voltage or current signal. The amount of phase compensation can be set using the 4 bits of the phase calibration register (CPH). The default value of this register is at a value of 0, which gives 0 ° phase compensation. When the 4 bits give a CPH of 15 (1111) the compensation introduced is +0.576 °. This compensates the phase shift usually introduced by the current sensor, while the voltage sensor, normally a resistor divider, does not introduce any delay. The resolution step of the phase compensation is 0.038 °.

## 7.11 Clock generator

All the internal timing of the STPM10 is based on the CLKOUT signal. This signal can be generated in three different ways:

1. RC: this oscillator mode can be selected using the RC configuration bit. If RC = 1, the STPM10 runs using the RC oscillator. A resistor connected between CLKIN and ground sets the RC current. For 4 MHz operation, the recommended settling resistor is 12 kΩ. The oscillator frequency can be compensated using the CRC configuration bit.
2. Quartz: If RC = 0, the oscillator works with an external crystal. The recommended circuit is depicted in the figure below (b).
3. External clock: by keeping RC=0, it is also possible to feed the CLKOUT pin with an external oscillator signal.

**Figure 20: Different oscillator circuits with (a) quartz, (b) internal oscillator, (c) external source**




The clock generator is powered from an analog supply and is responsible for two tasks. The first is to retard the turn-on of some function blocks after POR in order to help smooth the start of the external power supply circuitry by keeping off all major loads. The second task of the clock generator is to provide all necessary clocks for the analog and digital parts. During this task, the MDIV configuration bit is used to inform the device about the nominal frequency value of CLKOUT. Two nominal frequency ranges are expected to be from 4.000 MHz to 4.194 MHz (MDIV = 0) or from 8.000 MHz to 8.192 MHz (MDIV = 1).

### 7.11.1 RC start-up procedure

To use the device with RC oscillator the configuration bit RC (see *Table 11: "Configuration bit map"*) must be set. Since the default configuration is for a crystal oscillator, when an RC oscillator is used instead and the device is supplied for the very first time it is not internally clocked and consequently the DSP is inactive. In this condition it is not possible to set RC

or any other configuration bit. The following SPI procedure can be run in order to set the RC bit and provide the clock to the device:

- Set the mode signal BANK
- Perform a software reset
- Read the registers: BANK mode signal should be checked and the records should show something (not 000000F0)
- Clear the mode signal BANK
- Do not perform a reading, and write configuration bit RC

In this way the RC oscillator is started. If the registers are read again, it can be seen that RC bit is set and BANK is cleared. Once the RC start-up procedure is complete, the device is clocked and active. For details on mode signals refer to *Section 7.18: "Mode signals"*, for SPI operations refer to *Section 7.19: "SPI interface"*.

## 7.12 Resetting the STPM10

The STPM10 has no reset pin. The device is automatically reset by the POR circuit when the VCC crosses the 2.5 V value, but it can also be reset through the SPI interface by providing a dedicated command (see *Section 7.19: "SPI interface"* for remote reset command details). In case of reset caused by the POR circuit, all clocks and both of DC buffers in the analog part are kept off for about 30 ms, as well as all blocks of the digital part, except for the SPI interface, which is held in a reset state for about 125 ms after a reset condition. When a reset is performed through SPI, no delayed turn-on is generated. Resetting the STPM10 causes all the functional modules of the STPM10 to be cleared, including the volatile memory. The reset through SPI (remote reset request) normally takes place during production testing.

## 7.13 Using the STPM10 in microcontroller-based meters

The STPM10 can be used in microcontroller-based energy meters. The SPI pins (SCS, SCL, SDA, SYN) are used for communication purposes, allowing the microcontroller to write and read the internal STPM10 registers. The zero-crossing signal is available at the ZCR pin (see *Section 7.4: "Zero-crossing detection"* for details about the ZCR signal). The WDG pin provides the watchdog signal (DOG). The DOG signal generates a 16 ms long positive pulse every 1.6 seconds. Generation of these pulses can be suspended if data are read in intervals shorter than 1.6 s. The DOG signal is actually a watchdog reset signal which can be used to control operation of an on-board microcontroller. It is set to high whenever the VDDA voltage is below 2.5 V, but after VDDA goes above 2.5 V this signal starts running. It is expected that an application microcontroller should access the data in the metering device on a regular basis at least 1/s (recommended is 32/s). Every latching of results in the metering device requested from the microcontroller also resets the watchdog. If latching requests are not 1.6 seconds from one another, an active high pulse on WDG is produced, because the device assumes that the microcontroller is not operating properly. An application can use this signal either to control the reset pin of its microcontroller, or it can be tied to an interrupt pin. The latter option is recommended for a battery-backup application which can enter a sleep mode due to power-down conditions, and should not be reset by a metering device as it would exit from sleep mode.

## 7.14 Energy-to-frequency conversion

The STPM10 provides energy-to-frequency conversion both for calibration and energy readout purposes. In fact, one convenient way to verify the meter calibration is to provide a pulse train signal with 50% duty cycle whose frequency signal is proportional to the active energy under steady load conditions. In this case, the user chooses a certain number of pulses on the LED pin that correspond to 1 kWh. This value is called P. Let us consider the

case in which the LED pin is configured to be driven from internal signal AW (active energy) whose frequency is proportional to the active energy. The signal AW is taken from the 11th bit of the active energy register, and consequently a relationship between the LSB value of the active energy register and the number of pulses provided per each kWh (P) can be defined as:

**Equation 2:**

$$K_W = \frac{1000}{2^{11} \cdot P}[Wh]$$

Due to the innovative and proprietary power calculation algorithm, the frequency signal is not affected by any ripple at twice the line frequency. This feature strongly reduces the calibration time of the meter. In a practical example where the desired P is 64000 pulses/kWh (=17.7 Hz*kW), we have:

**Equation 3:**

$k_{AW}$ = 7.63*10-6 Wh

This means that the reading of 0x00001 in the active energy register represents 7.63 µWh, while 0xFFFFF represents 8 Wh. The LED pin can be driven from AW (active energy wide band), AF (active energy limited at fundamental), RW (reactive energy) or SW (apparent energy) according to the value of the KMOT bit. In this case, since the LED pin is driven by different signals from that of AW, some other relationship between the LSB of the register and the number of pulses per kWh provided by the meter (P) must be defined as follows:

**Equation 4:**

$k_{AF} = 4*k_{AW}$ [Wh]

$k_{RW} = 2*k_{AW}$ [VARh]

$k_{SW} = k_{AW}$ [VAh]

**Table 9: LED pin configuration**

| KMOT (2 bits) | Signal available on LED pin | Number of pulses |
|---|---|---|
| 0 | AW Type0* | P [kWh] |
| 1 | AF Type1* | P [kWh] |
| 2 | RW | P [kVARh] |
| 3 | SW | P [kVAh] |

## 7.15 Status bit

The STPM10 includes 8 status bits, which provide information about the current status of the meter. The status bits are the following:

**Table 10: Status bit description**

| Bit # | Name | Description | Conditions |
|---|---|---|---|
| 0 | BIL | No-load condition | BIL = 0: no-load condition not detected |
| | | | BIL = 1: no-load condition detected |
| 1 | BCF | ΣΔ signals status | BCF = 0: ΣΔ signals active |
| | | | BCF = 1: one or both ΣΔ signals are stacked |
| 2 | BFR | Line frequency | BFR = 0: line frequency within the 45 Hz - 65 Hz range |

| Bit # | Name | Description | Conditions |
|---|---|---|---|
| | | range | BFR = 1: line frequency out of range |
| 3 | BIT | Tamper condition | BIT = 0: tamper not detected |
| | | | BIT = 1: tamper detected |
| 4 | MUX | Current channel selection | MUX = 0: primary current channels selected by the tamper module |
| | | | MUX = 1: secondary current channels selected by the tamper module |
| 5 | LIN | Trend of the line voltage | LIN = 0: line voltage going from the minimum to the maximum value. (dv/dt > 0) |
| | | | LIN = 0: line voltage going from the minimum to the maximum value. (dv/dt > 0) |
| 6 | PIN | Output pin check | PIN = 0: output pins are consistent with the data |
| | | | PIN = 1: output pins are different from the data, this means an output pin is forced to 1 or 0 |
| 7 | HLT | Data validity | HLT = 0: data records reading are valid |
| | | | HLT = 1: data records are not valid. A reset occurred and a restart is in progress |

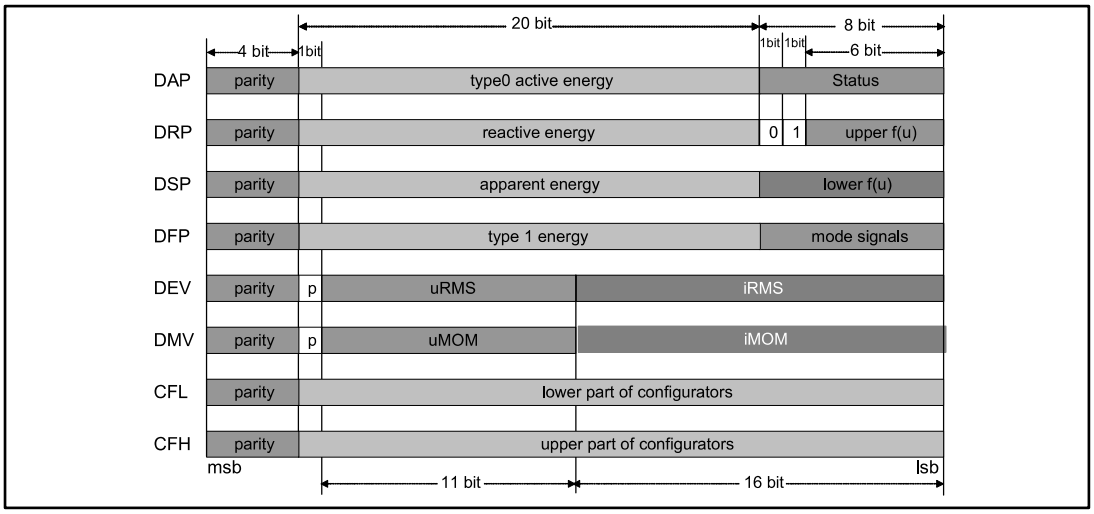
All these signal can be read through the SPI interface.

## 7.16 Programming the STPM10

### 7.16.1 Data records

The STPM10 has 8 internal data record registers. Every data record consists of a 4-bit parity code and 28-bit data value where the parity code is computed from the data value, which makes a total of 32 bits, or 4 bytes. Figure below shows the data record structure with the name of the contained information. Each bit of parity nibble is defined as odd parity of all seven corresponding bits of data nibbles. The first 6 registers are read-only, except for the 8-bit mode signals in the DFP register (the mode signals are described later in this paragraph). The last two registers are CFL and CFH.

**Figure 21: STPM10 data record map**




## 7.17 Configuration bits

All the configuration bits that control the operation of the device (CFL and CFH data records) can be written in a temporary way. The configuration bit values are written in the so-called volatile memory, which are simple latches that hold the configuration data until the power is on or until a reset condition occurs (both POR and remote reset). As indicated in the data records table, the configuration bits are 56. Each configuration bit can be written by sending a byte command to the STPM10 through its SPI interface. The procedure to write the configuration bits is described in *Section 7.19: "SPI interface"*.

**Table 11: Configuration bit map**

| Address | | Name | Number of bits | Description[(1)] |
|---|---|---|---|---|
| 6-bit binary | DEC | | | |
| 000000 | 0 | | 1 | Reserved |
| 000001 | 1 | MDIV | 1 | Measurement frequency range selection:<br>MDIV=0: 4.000 MHz to 4.194 MHz<br>MDIV=1: 8.000 MHz to 8.192 MHz |
| 000010 | 2 | RC | 1 | Type of internal oscillator selection:<br>RC = 0:crystal oscillator<br>RC = 1:RC oscillator |
| 000011 | 3 | | 1 | Reserved |
| 000100 | 4 | | 1 | Reserved |
| 000101 | 5 | PST | 1 | Current channel sensor type and gain:<br>if TMP=0<br>PST=0: primary is CT X8, secondary is not used, no tamper<br>PST=1: primary is shunt X32, secondary is not used, no tamper |
| | | | | if TMP=1<br>PST=0: primary is CT X8, secondary is CT X8, tamper<br>PST=1: primary is CT X8, secondary is shunt X32, tamper |

| Address | | Name | Number of bits | Description[1] |
|---|---|---|---|---|
| 6-bit binary | DEC | | | |
| 000110 | 6 | | 1 | Reserved |
| 000111 | 7 | TMP | 1 | Tamper enable |
| 001000 | 8 | FRS | 1 | Power calculation when BFR=1<br>FRS=0: energy accumulation is frozen, power is set to zero<br>FRS=1: normal energy accumulation and power computation (p=u*i) |
| 001001 | 9 | MSBF | 1 | Bit sequence output during record data reading selection:<br>MSBF=0: MSB first<br>MSBF=1: LSB first |
| 001010 | 10 | FUND | 1 | This bit swaps the information stored in the type0 (first 20 bits of DAP register) and type1 (first 20 bits of DFP register) active energy.<br>FUND = 0: type 0 contains wide-band active energy, type1 contains fundamental active energy<br>FUND = 1: type 0 contains fundamental active energy, type1 contains wideband active energy |
| 001100 | 12 | LTCH | 2 | No-load condition threshold as product between $V_{RMS}$ and $I_{RMS}$:<br>LTCH=0 800<br>LTCH=1 1600<br>LTCH=2 3200<br>LTCH=3 6400 |
| 001101 | 13 | | | |
| 001110 | 14 | KMOT | 2 | Selection of pulses for LED:<br>KMOT=0 type 0 active Energy<br>KMOT=1 type 1 active Energy<br>KMOT=2 reactive energy<br>KMOT=3 apparent energy |
| 001111 | 15 | | | |
| 010000 | 16 | | 1 | Reserved |
| 010001 | 17 | | 1 | Reserved |
| 010010 | 18 | BGTC | 2 | Band-gap temperature compensation bits. See *Figure 17: "Band-gap temperature variation"* |
| 010011 | 19 | | | |
| 010100 | 20 | CPH | 4 | 4-bit unsigned data for compensation of phase error, 0 °+0.576 °. 16 values are possible with a compensation step of 0.0384 °. When CPH=0 the compensation is 0 °, when CPH=15 the compensation is 0.576 ° |
| 010101 | 21 | | | |
| 010110 | 22 | | | |
| 010111 | 23 | | | |
| 011000 | 24 | CHV | 8 | 8-bit unsigned data for voltage channel calibration. 256 values are possible. When CHV is 0 the calibrator is at -12.5% of the nominal value. When CHV is 255 the calibrator is at +12.5%. The calibration step is then 0.098% |
| 011001 | 25 | | | |
| 011010 | 26 | | | |
| 011011 | 27 | | | |
| 011100 | 28 | | | |
| 011101 | 29 | | | |

| Address | | Name | Number of bits | Description[(1)] |
|---|---|---|---|---|
| 6-bit binary | DEC | | | |
| 011110 | 30 | | | |
| 011111 | 31 | | | |
| 100000 | 32 | CHP | 8 | 8-bit unsigned data for secondary current channel calibration. 256 values are possible. When CHS is 0 the calibrator is at -12.5% of the nominal value. When CHS is 255 the calibrator is at +12.5%. The calibration step is then 0.098% |
| 100001 | 33 | | | |
| 100010 | 34 | | | |
| 100011 | 35 | | | |
| 100100 | 36 | | | |
| 100101 | 37 | | | |
| 100110 | 38 | | | |
| 100111 | 39 | | | |
| 101000 | 40 | | | |
| 101001 | 41 | | | |
| 101010 | 42 | | | |
| 101011 | 43 | | | |
| 101100 | 44 | | | |
| 101101 | 45 | | | |
| 101110 | 46 | | | |
| 101111 | 47 | | | |
| 110000 | 48 | CRC | 2 | 2-bit unsigned data for calibration of RC oscillator (see *Table 5: "Absolute maximum ratings"*)<br>CRC=0, or CRC=3 cal=0%<br>CRC=1, cal = +10%<br>CRC=2, cal = -10% |
| 110001 | 49 | | | |
| 110010 | 50 | | 1 | Reserved |
| 110011 | 51 | | 1 | Reserved |
| 110100 | 52 | | 1 | Reserved |
| 110101 | 53 | CRIT | 1 | Selection of tamper threshold: CRIT=0: 12,5% / CRIT=1: 6,25% |
| 110110 | 54 | | 1 | Reserved |
| 110111 | 55 | | 1 | Reserved |

**Notes:**

(1)These bits represent the MSB of the decimal value indicated in the description column

As indicated above, the STPM10 includes 56 CFG bits. The CFG bits are not retained when the STPM10 supply is not available and they are cleared when a POR occurs, but they are not cleared when a remote reset command (RRR) is sent through SPI. Normally, some of these bits must be loaded during power-up of the application. From the microcontroller, it could also reload the configuration and calibration values after power-on restart.

## 7.18 Mode signals

The STPM10 includes 8 mode signals located in the DFP data record. 3 out of these are used for internal testing purposes only while 5 are useful to change some operations of the STPM10. The mode signals are not retained when the STPM10 supply is not available and they are cleared when a POR occurs, but they are not cleared when a remote reset command (RRR) is sent through SPI. The mode signals bit can be written using the normal writing procedure of the SPI interface, in the following section.

**Table 12: Mode signal description**

| Bit | Signal name | Bit value | Status | Binary command | Hex command |
|---|---|---|---|---|---|
| 0 | Bank | 0 | Used for RC start-up procedure | 0111000x | 70 or 71 |
| | | 1 | | 1111000x | F0 or F1 |
| 1 | Reserved | | | | |
| 2 | Reserved | | | | |
| 3 | Reserved | | | | |
| 4 | CSEL | 0 | Current channel 1 selected when tamper is disabled | 0111 100x | 78 or 79 |
| | | 1 | Current channel 2 selected when tamper is disabled | 1111 100x | F8 or F9 |
| 5 | Reserved | | | | |
| 6 | Reserved | | | | |
| 7 | Pre-charge | 1 | Swap the 32-bit data record readings. From 1,2,3,4,5,6,7,8, to 5,6,7,8,1,2,3,4 and vice-versa | 1111111x | FF |

**CSEL:** in normal operation, if the anti-tamper module is not activated, the STPM10 selects channel 1 as the source of current information. For debug or calibration purposes it is possible to select channel 2 as the source of the current channel signal when the tamper module is disabled. This is done by setting the CSEL mode bit.

**Pre-charge:** this command swaps the sequence of data records read, allowing the reading of the last four data records first, and the first four second. The reading sequence is 5, 6, 7, 8, 1, 2, 3, 4. Unlike the other mode signals, the pre-charge command is not retained inside the STPM10, but should be sent each time before the reading of the data records.

**BANK:** it is used to activate RC oscillator (as indicated in *Section 7.11.1: "RC start-up procedure"*).

## 7.19 SPI interface

The SPI interface supports a simple serial protocol, which is implemented to enable communication of some master system (microcontroller or PC) and the device. Three tasks can be performed with this interface:

- Remote resetting of the device
- Reading data records
- Writing the mode bits and the configuration bits

Four pins of the device are dedicated to this purpose: SCS, SYN, SCL and SDA. SCS, SYN and SCL are all input pins, while SDA can be input or output according to whether the SPI is in write or read mode. A high level signal for these pins means a voltage level higher than 0.75 x VCC, while a low level signal means a voltage value lower than 0.25 x VCC.

The internal registers are not directly accessible. Instead, 32 bits of transmission latches are used to pre-load the data before being read or written to the internal registers. The condition in which SCS, SYN and SCL inputs are set to high level determines the idle state of the SPI interface, and no data transfer occurs.

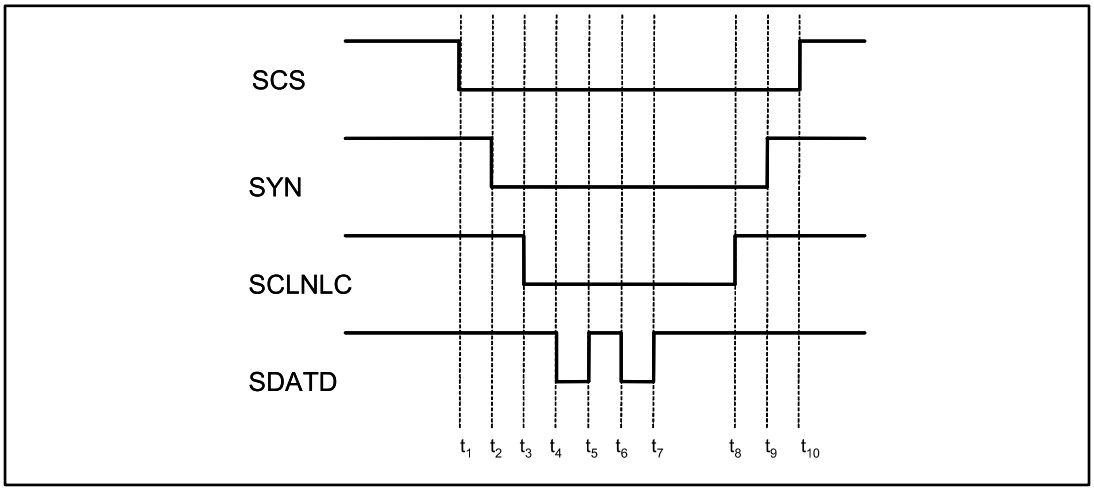
- SCS: enables SPI operation when low
- SYN: operates different functions according to the status of the SCS pin. When SCS is low, the SYN pin status selects if the SPI is in read (SYN = 1) or write mode (SYN = 0). When the SCS is high and SYN is also high, the results of the input or output data are transferred to the transmission latches
- SCL: basically the clock pin of the SPI interface. This pin function is also controlled by the SCS status. If SCS is low, SCL is the input of the serial bit synchronization clock signal. When SCS is high, SCL is also high, causing the idle state of the SPI
- SDA: the data pin. If SCS is low, the operation of SDA is dependent on the status of the SYN pin. If SYN is high, SDA is the output of the serial bit data (read mode). If SYN is low, SDA is the input of the serial bit data signal (write mode). If SCS is high, SDA is the input of the idle signal. Any pin above has an internal weak pull-up mechanism of nominal 15 µA. This means that when a pin is not forced by external signals, the state of the pin is logic high. A high state of any input pin described above is considered an idle (not active) state. To let SPI operate correctly, the STPM10 must be correctly supplied as described in *Section 7.6: "Power supply"*

An idle state of the SPI module is recognized when the signals of pins SYN, SCS, SCL and SDA are in a logic high state. Any SPI operation should start from this idle state. When SCS is active (low), signal SDATD should change its state at trailing edge of signal SCLNLC and the signal SDATD should be stable at next leading edge of signal SCLNLC. The first valid bit of SDATD always starts together with activation of signal SCLNLC.

## 7.20 Remote reset

The timing diagram of this operation is shown in the figure below. The time step can be as short as 30 ns. The internal reset signal is called RRR. Unlike the POR, the RRR signal does not cause the 30 ms delayed restart of the analog module, and the 120 ms delay in the restart of the digital module. This signal does not clear the mode signals.

**Figure 22: Timing to provide remote reset request**



All time intervals must be longer than 30 ns. t7 → t8 is the reset time; this interval must be longer than 30 ns as well.

## 7.21 Reading data records

A microcontroller is able to read all measurement results and all system signals (configuration, calibration, status, mode). As already written above, the time step can be as short as 30 ns. There are two phases of reading, called latching and shifting. Latching is used to sample results into transmission latches. The transmission latches are the flip-flops that hold the data in the SPI interface. This happens with the active pulse on SYN when SCS is idle. The length of the pulse on SYN must be longer than 2 periods of the measurement clock, i.e. more than 500 ns at 4 MHz. The shifting starts when SCS becomes active. At the beginning of this phase, another pulse, much shorter, (30 ns), should be applied on SYN so to ensure that an internal transmission serial clock counter is reset to zero. An alternative way is to extend the pulse on SYN into the second phase of reading. After this reset, a 32 serial clock-per-data record should be applied. It is possible to read up to 8 data records in this way. This procedure can be aborted at any time through deactivation of SCS (see *Figure 24: "Timing for data record reading"* ). The first read-out byte of the data record is the least significant byte (LSB) of the data value and, of course, the fourth byte is the most significant byte (MSB) of the data value. Each byte can be further divided into a pair of 4-bit nibbles, referred to the most and the least significant nibble ( MSN, LSN). This division makes sense with the MSB of the data value because its MSN holds the parity code rather than useful data. The sequence of the data record during the read operation is fixed. Normally, an application reads the 1st through the 6th data record; the 7th and 8th data record are read only when it needs to fetch the configuration data. However, an application may apply a pre-charge command (see *Table 12: "Mode signal description"*) prior to the reading phase. This command forces the device to respond with the sequence 5th - 8th, 1st - 4th. Such a change of sequence can be used to skip the first four data records. The timing diagram of the reading operation is shown in *Figure 24: "Timing for data record reading"*. User can see the latching and beginning of the shifting phase of the first byte (0x5F) of the first data record, and the end of reading. Also, both of alternatives to reset the internal transmission serial clock counter are shown in signal SYN.

**Figure 23: Data record reconstruction**

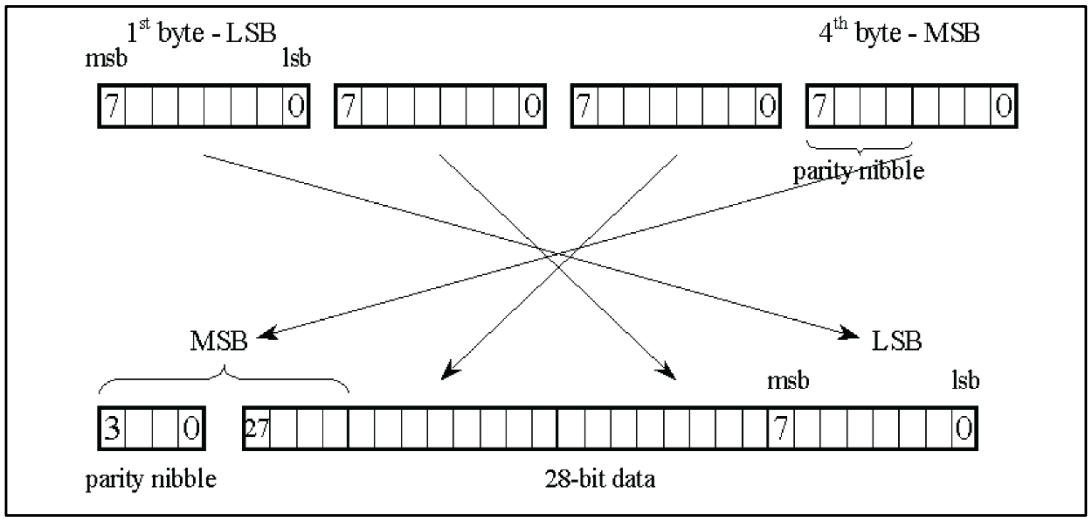
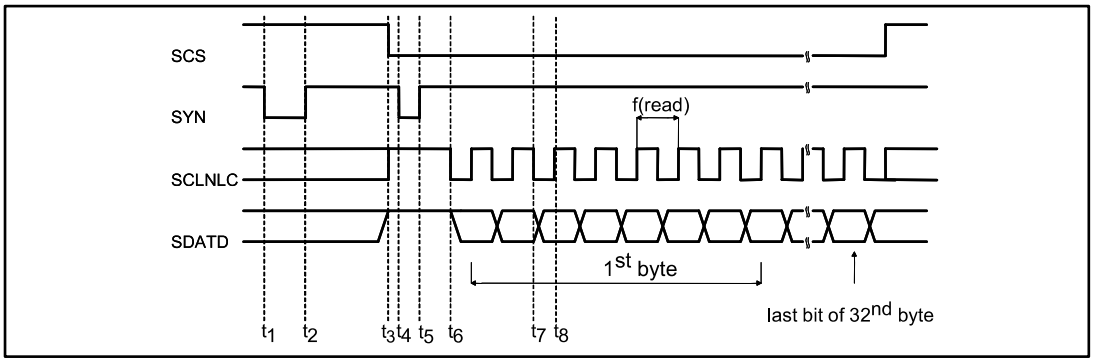


**Figure 24: Timing for data record reading**




t1 → t2: Latching phase. Interval value > $2/f_{CLK}$

t2 → t3: Data latched, SPI idle. Interval value > 30 ns

t3 → t4: Enable SPI for read operation. Interval value > 30 ns

t4 → t5: Serial clock counter is reset. Interval value > 30 ns

t5 → t6: SPI reset and enabled for read operation. Interval value > 30 ns

t7: Internal data transferred to SDA

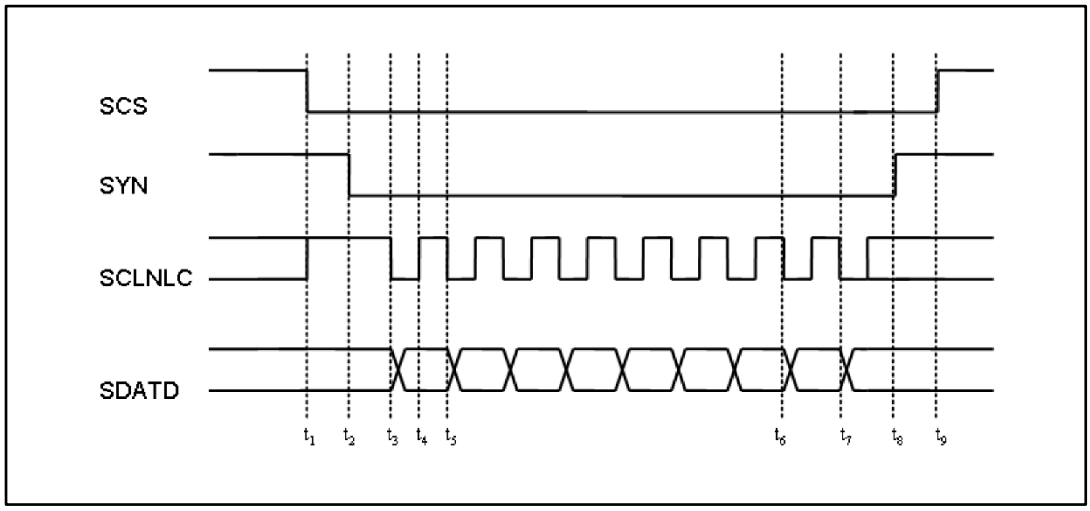
t8: SDA data is stable and can be read

The system that reads the data record from the STPM10 should check the integrity of each data record. If the check fails, the reading should be repeated, but the shifting should be applied this time only. Otherwise, new data are latched into transmission latches and the one incorrectly read is lost. Normally, each byte is read out as the most significant bit (MSB) first. But this can be changed by setting the MSBF configuration bit in the STPM10 CFL data record. In this manner each byte is read out as the least significant bit (LSB) first.

## 7.22 Writing procedure

Each writable bit (configuration and mode bits) has its own 6-bit absolute address. Concerning the configuration bits, the 6-bit address value corresponds to its decimal value, while for mode bits, see *Section 7.18: "Mode signals"*. In order to change the state of a latch, a byte of data must be sent to the STPM10, which is the normal way to send data via SPI. This byte consists of 1-bit data to be latched (MSB), followed by the 6-bit address of the destination latch, followed by 1-bit; do not care LSB data, which makes a total of 8 bits of command byte. For example, if we want to set configuration bit 47 (part of the secondary current channel calibrator) to 0, we must convert the decimal 47 to its 6-bit binary value: 101111. The byte command is then composed of the following: 1-bit data value+6-bits address+1-bit (0 or 1) as depicted in the figure below. In this case the binary command is 01011111 (0x5F), which is the one depicted, or 01011110 (0x5E):

**Figure 25: Timing for writing configuration and mode bits**




t1 → t2 (> 30 ns): SPI out of idle state

t2 → t3 (> 30 ns): SPI enabled for writing operation

t3: data value is placed in SDA

t4: SDA value is stable and shifted into the device

t3 → t5 (> 10 µs): writing clock period

t3 → t5: 1 bit data value

t5 → t6: 6 bit address of the destination latch

t6 → t7: 1 bit EXE command

t8: end of SPI writing

t9: SPI enters idle state

The same procedure should be applied for the mode signals, but in this case the 6-bit address must be taken from *Table 12: "Mode signal description"*. The LSB of the command is also called the EXE bit because instead of the data bit value, the corresponding serial clock pulse is used to generate the necessary latching signal. In this manner the writing mechanism does not need the measurement clock to operate and the operation of SPI module of STPM10 is completely independent from the rest of the device logic except for the signal POR. Commands to change system signals should be sent during active signals SCS and SYN, as shown in the figure above. The SYN must be put low in order to disable the SDA output driver of the STPM10 and make the SDA an input pin. A string of commands can be sent within one period of active SCS and SYN signals, or a command can be followed by reading the data record. However, in this case, the SYN should be deactivated in order to enable the SDA output driver, and SYN pulse should be applied before activation of the SCS in order to latch the data.

### 7.22.1 Interfacing the standard 3-wire SPI with the STPM10 SPI

Due to the fact that a 2-wire SPI is implemented in the STPM10, it is clear that sending any command from a standard 3-wire SPI requires a 3-wire to 2-wire interface, which should produce a proper signal on SDA from host signals SDI, SDO and SYN. The need for a single-gate 3-state buffer could be avoided through an emulation of SPI just to send some commands. On a microcontroller this can happen by performing the following steps:

1. Disable the SPI module
2. Set the SDI pin, which is connected to SDA as an output
3. Activate SYN first, and then SCS
4. Apply a new bit value to SDI, and activate SCL
5. Deactivate SCL
6. Repeat the previous two steps seven times to complete a one byte transfer
7. Repeat the previous three steps for any remaining byte transfers
8. Set the SDI pin as an input
9. Deactivate SCS and SYN
10. Enable the SPI module

In case of a pre-charge command (0xFF), the emulation above is not necessary. Due to the pull-up device on the SDA pin of the STPM10, the processor needs to perform the following steps:

1. Activate SYN first in order to latch the results
2. After at least 1 µs, activate SCS
3. Write one byte to the transmitter of SPI (this produces 8 pulses on SCL with SDI=1)
4. Deactivate SYN
5. Optionally read the data records (the sequence of reading is altered)
6. Deactivate SCS

## 7.23 Energy calculation algorithm

Within the STPM10, the computing section of the measured active power uses a completely new patented signal processing approach. This approach allows the device to reach high level of performance in terms of accuracy. The signals, coming from the sensors, for the instantaneous voltage are calculated as follows:

**Equation 5:**

$v(t) = V \cdot \sin \omega t$

where V is the peak voltage and ω is related to the line frequency.

The instantaneous current is calculated using:

**Equation 6:**

$i(t) = I \cdot \sin(\omega t + \phi)$ where I is the peak current, ω is related to the line frequency and ϕ is the phase difference between voltage and current.

### 7.23.1 Active power

In the STPM10, after the pre-conditioning and the A/D conversion, the digital voltage signal (which is dynamically more stable with respect to the current signal) is processed by a differentiator stage which transforms:

**Equation 7:**

$v(t) \rightarrow v'(t) = dv/dt = V \cdot \omega \cdot \cos \omega t$

See *Figure 26: "Active energy computation diagram"* (5)

the resulting signal, together with the pre-processed and digitalized current signal

**Equation 8:**

$i(t) = I \cdot \sin(\omega t + \phi)$

See *Figure 26: "Active energy computation diagram"* (6)

are then available for the calculation process. These digital signals are also provided to two additional stages, which then integrate of themselves, obtaining:

**Equation 9:**

$dv/dt \rightarrow v(t) = V \cdot \sin \omega t$

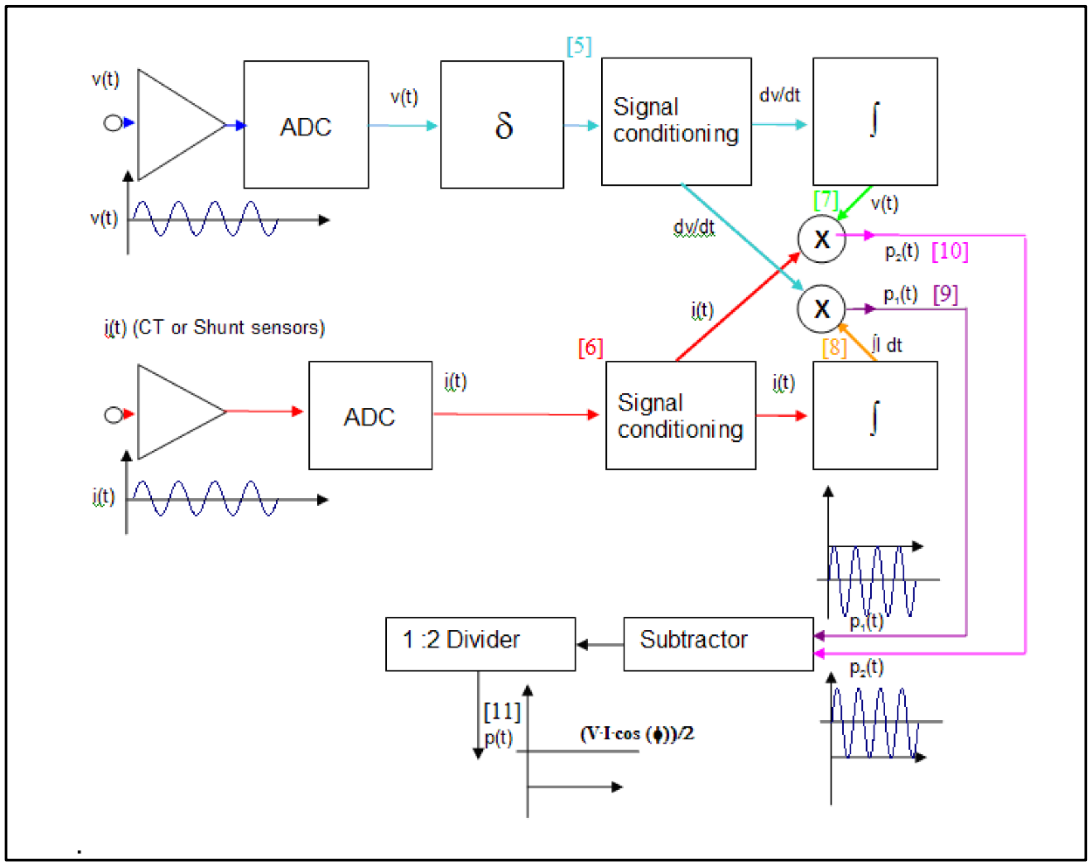
see below figure (7)]

**Equation 10:**

$i(t) \rightarrow I(t) \int i(t) \cdot dt = = -I/\omega \cdot \cos(wt + \phi)$

See figure below (8)

**Figure 26: Active energy computation diagram**




At this point four signals are available. By combining (pairing) them by means of two multiplying stages, two results are obtained

**Equation 11:**

$$p_1(t) = \frac{d_v}{d_t} \cdot \int \mathrm{i(t)} \cdot \mathrm{dt} \quad = -\frac{\mathrm{V \cdot I \cdot cos\phi}}{2} - \frac{\mathrm{V \cdot I \cdot cos(2wt + \phi)}}{2}$$

See figure above (9)

**Equation 12:**

$$p_2(t) = v(t) \cdot \mathrm{i(t)} = -\frac{\mathrm{V \cdot I \cdot cos\phi}}{2} - \frac{\mathrm{V \cdot I \cdot cos(2wt + \phi)}}{2}$$

See *Figure 26: "Active energy computation diagram"* (10)

After these two operations, another stage performs the subtraction between the results p2 and p1 and a division by 2, obtaining the active power:

**Equation 13:**

$$\mathrm{p}(t) = \frac{(p_2(\mathrm{t}) - p_1(\mathrm{t}))}{2} = \frac{\mathrm{V \cdot I \cdot cos\varphi}}{2}$$

See *Figure 26: "Active energy computation diagram"* (11)

In this way, the AC part V· I· cos(2ωt + ϕ)/2 has been removed from the instantaneous power.

The absence of any AC component allows a very fast calibration procedure. It only requires the setting of (using the internal device programming registers) the voltage and current sensor conversion constants, using the effective voltage and current ($V_{rms}$, $I_{rms}$) readings provided by the device built-in communication port, avoiding the time-averaged readings of the active power or the need for line synchronization.

### 7.23.2 Reactive power

The reactive power is produced using the previously-computed signals. In case of shunt sensor the voltage signal is derived while the current signal is not. A first computation is to multiply the DS value of the integrated voltage channel with the value of the integrated current channel, which yields:

**Eqaution 14:**

$$Q_1(t) = \int v(t)dt \cdot \mathrm{l(t)} = v(t) \cdot \mathrm{I(t)} = (\mathrm{V sin\omega t}) \cdot \left(-\frac{1}{\omega}\cos(\omega t + \varphi)\right) = \frac{\mathrm{VI}}{2\omega} \cdot (sin\varphi - \sin(2\omega t + \varphi))$$

The second is to multiply the filtered DS value of the voltage channel with the value of the filtered current channel:

**Equation 15:**

$$Q_2(t) = v(t) \cdot \mathrm{I(t)} = \mathrm{V\omega cos\omega t \cdot I sin(\omega t + \varphi)} = \frac{VI}{2} \cdot \omega \cdot ((sin\varphi + \sin(2\omega t + \varphi))$$

From the above results, Q1(t) is proportional to 1/ω, while Q2(t) is proportional to ω. The correct reactive power would result from the following formula:

**Equation 16:**

$$Q = \frac{1}{2} \cdot Q_1(t) \cdot \omega + Q_2(\mathrm{t}) \cdot \frac{1}{\omega} = \frac{VI}{2} sin\varphi$$

Since the above computation needs a significant additional circuitry, the reactive power in the STPM10 is calculated using only the Q1(t) multiplied by ω, which means:

**Equation 17:**

$$Q_3(t) = \frac{1}{2} \cdot Q_1(t) \cdot \omega = \frac{VI}{2} \cdot (sin\varphi - \sin(2\omega t + \varphi))$$

The reactive power, then, presents a ripple at twice the line frequency. Since the average value of a sinusoid is 0, this ripple does not contribute to the reactive energy calculation over time. Moreover, in the STPM10 the reactive power is not used for meter calibration or to generate the stepper pulses, so this ripple does not affect the overall system performance.

### 7.23.3 Apparent power and RMS values

The RMS values are calculated starting from the following formulas:

**Equation 18:**

$$\sqrt{\frac{1}{T}\int_0^T I^2(t)dt} = \frac{I}{\omega\cdot\sqrt{2}}$$

Multiplying the equation above by ω, the $I_{RMS}$ value is obtained:

**Equation 19:**

$$I_{RMS} = \frac{I}{\sqrt{2}}$$

The RMS voltage value is obtained by:

**Equation 20:**

$$V_{RMS} = \sqrt{\frac{1}{T}\int_0^T V^2(t)dt} = \frac{I}{\sqrt{2}}$$

For the apparent power, another value is produced:

**Equation 21:**

$$\sqrt{\frac{1}{T}\int_0^T v^2(t)dt} = \frac{V\cdot\omega}{\sqrt{2}}$$

Multiplying equation 18 and equation 21, the apparent power is produced:

**Equation 22:**

$$S = \frac{I}{\omega\cdot\sqrt{2}}\cdot\frac{V\cdot\omega}{\sqrt{2}} = \frac{VI}{2}$$

The DSP performs the integration of the computed powers into energies. These integrators are implemented as up/down counters and they can roll over. 20-bit output buses of the counters are assigned as the most significant part of the energy data records. An application reads the counters at least every second, to avoid missing any rollover.

## 7.24 STPM10 calibration

Energy meters based on the STPM10 device can be calibrated in a fast and simple way. The calibration is essentially based on the single calibration of the voltage and current channel considering their RMS values rather than on the frequency of the output pulse signal. When two channels are calibrated, all other measurements are calibrated too. This allows the calibration to be performed in only one point, thereby shortening the production time of the meter. This procedure is possible due to the following key factors:

- The device comprises two independent meter channels for line voltage and current, respectively. Each channel includes its own digital calibrator, to adjust the RMS in the range of ±12.5% in 256 steps, and a digital filter, to remove any signal DC component. None of the final results are subject to the calibration procedure because they are achieved from such corrected signals by mathematical modules implemented by hardwired DSP

- The device computes different kinds of energies: active, reactive and apparent. The active energy is produced without the 2nd harmonic of the line frequency. It also computes RMS values of measured voltage and current
- The device produces an energy output pulse signal, but information can also be read through the serial port interface (SPI) and communication channel
- The device has an embedded memory of 56 bits, used for configuration and calibration purposes. The values of these bits can be read, or they can be changed temporarily through the SPI communication channel

Let's consider the basic information needed to start the calibration procedure:

**Table 13: Working point settings**

| Parameter | | Value |
|---|---|---|
| Line RMS voltage | $V_n$ | 230 V |
| Line RMS current | $I_n$ | 5 A |
| Power sensitivity | P | LED: P=128000 pulses/kWh |
| Shunt sensor | $K_S$ | 0.42 mv/A |

The typical STPM10 parameters and constants are also known (see table below).

**Table 14: Device constants**

| Parameter | | Value | Tolerance |
|---|---|---|---|
| Internal reference voltage | $V_{BG}$ | 1.23 V | ± 2% |
| Internal calculation frequency | $f_M$ | $2^{23}$ Hz | ± 50 ppm |
| Amplification of voltage ADC | $A_V$ | 4 | ± 1% |
| Amplification of current ADC | $A_I$ | 8, 16, 24, 32 | ± 2% |
| Gain of differentiator | $G_{DIF}$ | 0.6135 | |
| Gain of integrator | $G_{INT}$ | 0.815 | |
| Gain of decimation filter | $G_{DF}$ | 1.004 | |
| RMS voltage record length | $B_V$ | $2^{11}$ | |
| RMS current record length | $B_I$ | $2^{16}$ | |
| Constant | $D_{UD}$ | $2^{17}$ | |

As shown in the table above, analog parameters only are the object of calibration because they introduce a certain error. Voltage ADC amplification $A_V$ is constant, while $A_I$ is chosen according to the sensors used. The calibration algorithm first calculates the voltage divider ratio and, as a final result, the correction parameters, called $K_V$ and $K_I$, which applied to the STPM10 voltage and current measures compensate the small tolerances of the analog components that affect energy calculation. Since $K_V$ and $K_I$ calibration parameters are the decimal representation of the corresponding configuration bytes CHV and CHP or CHS (respectively, the voltage channel, primary current channel and secondary current channel calibration bytes), at the end of calibration, CHV and CHP or CHS (according to the current channel under calibration, primary or secondary, respectively) the bit values are obtained. In the following procedure CHV, CHP and CHS are indicated as $C_V$ and $C_I$. Through hard-wired formulas, $K_V$ and $K_I$ tune measured values varying from 0.75 to 1, in 256 steps, according to the value of $C_V$ and $C_I$ (from 0 to 255).

To obtain the greatest correction dynamic, initially calibrators are set in the middle of the range, thus obtaining a calibration range of 12.5% per voltage or current channel:

Calibrator value

$K_V = K_I = 0.875$

$C_I = C_V = 128$

In this way, $K_V$ and $K_I$ are tuned to obtain a precise measurement: for example $C_V = 0$ generates a correction factor of -12.5% ($K_V = 0.75$) and $C_V = 255$ determines a correction factor of +12.5% ($K_V = 1$), and so on.

Based on the above, the following formulas relating to $K_{V,I}$ and $C_{V,I}$ are obtained:

$K_{V,I} = (C_{V,I} / 128) \cdot 0.125 + 0.75$

$C_{V,I} = 1024 \cdot K_{V,I} - 768$

The calibration procedure outputs $C_V$ and $C_I$ values, which allow the above power sensitivity of the meter. This sensitivity is used to calculate target frequency at the LED pin for nominal voltage and current values:

$XF = f \cdot 64$

with:

$f = PM \cdot I_n \cdot V_n / 3600000$

From the values above and for both chosen amplification factor AI = 32 and initial calibration data, the following target values can be calculated:

Target RMS reading for a given $I_n$:

$X_I = I_n \cdot K_S \cdot A_I \cdot K_I \cdot G_{INT} \cdot G_{DF} \cdot G_{DIF} \cdot B_I / (V_{BG} \cdot 1000) = 1573$

Target RMS reading for a given $V_n$:

$X_V = f \cdot B_V \cdot B_I \cdot D_{UD} / (f_M \cdot X_I) = 852$

The output of the voltage divider is then:

$V_{DIV} = (X_V \cdot V_{BG}) / (2 \cdot G_{DIF} \cdot A_V \cdot K_V \cdot G_{DF} \cdot G_{INT} \cdot B_V) = 145.6$ mV

Choosing $R_2 = 500\ \Omega$ (connected between $V_I$ and $V_{SS}$), the $R_1$ resistor (connected between $V_{LINE}$ and $V_{IP}$) value is obtained:

$R1 = R2 \cdot (V_n - V_{DIV}) / V_{DIV} = 789.3\ \Omega$

Indicating, with $I_A$ and $V_A$, the real readings on the STPM10 RMS voltage and current registers, and with $X_I$ and $X_V$ ideal values of RMS current and voltage readings already calculated, the final values for calibrators can be calculated as:

$X_V = (K_v \cdot V_A) / 0.875$

$X_I = (K_i \cdot I_A) / 0.875$

If the computed final calibration data falls out of the calibration data range, the energy meter should be recognized as bad, or the given presumptions and calculations above should be checked. Otherwise, if the final data of the calibrators is written into the energy meter, the RMS readings should be very close to the target values I and V, and the frequency of the LED output should be very close to the target value f.

# 8 Application design

The choice of the external components in the transduction section of the application is a crucial point in the application design, affecting the precision and the resolution of the whole system. Among the several considerations, a compromise has to be found between the following needs:

1. Maximize the signal to noise ratio in the voltage channel

2. Choose the current-to-voltage conversion ratio $K_S$ and the voltage divider ratio in a way that calibration can be achieved (please refer to AN2299)

3. Choose $K_S$ to take advantage of the whole current dynamic range according to desired maximum current and resolution. To maximize the signal to noise ratio of the current channel the voltage divider resistors ratio should be as close as possible to those shown in the table below

**Table 15: Resistor divider ratio**

| Function | Component | Parameter | Value | Unit |
|---|---|---|---|---|
| Line voltage interface | Resistor divider | R to R ratio $V_{RMS}$ = 230 V | 1650 | V/V |
| | | R to R ratio $V_{RMS}$ = 110 V | 830 | |

Next figure below shows a reference schematic for an application with the following properties:

Typical values for the current sensors sensitivity, also used in the reference schematic below, are shown in the table below.

- P = 64000 imp/kWh
- $I_{NOM}$ = 5 A
- $I_{MAX.}$ = 60 A

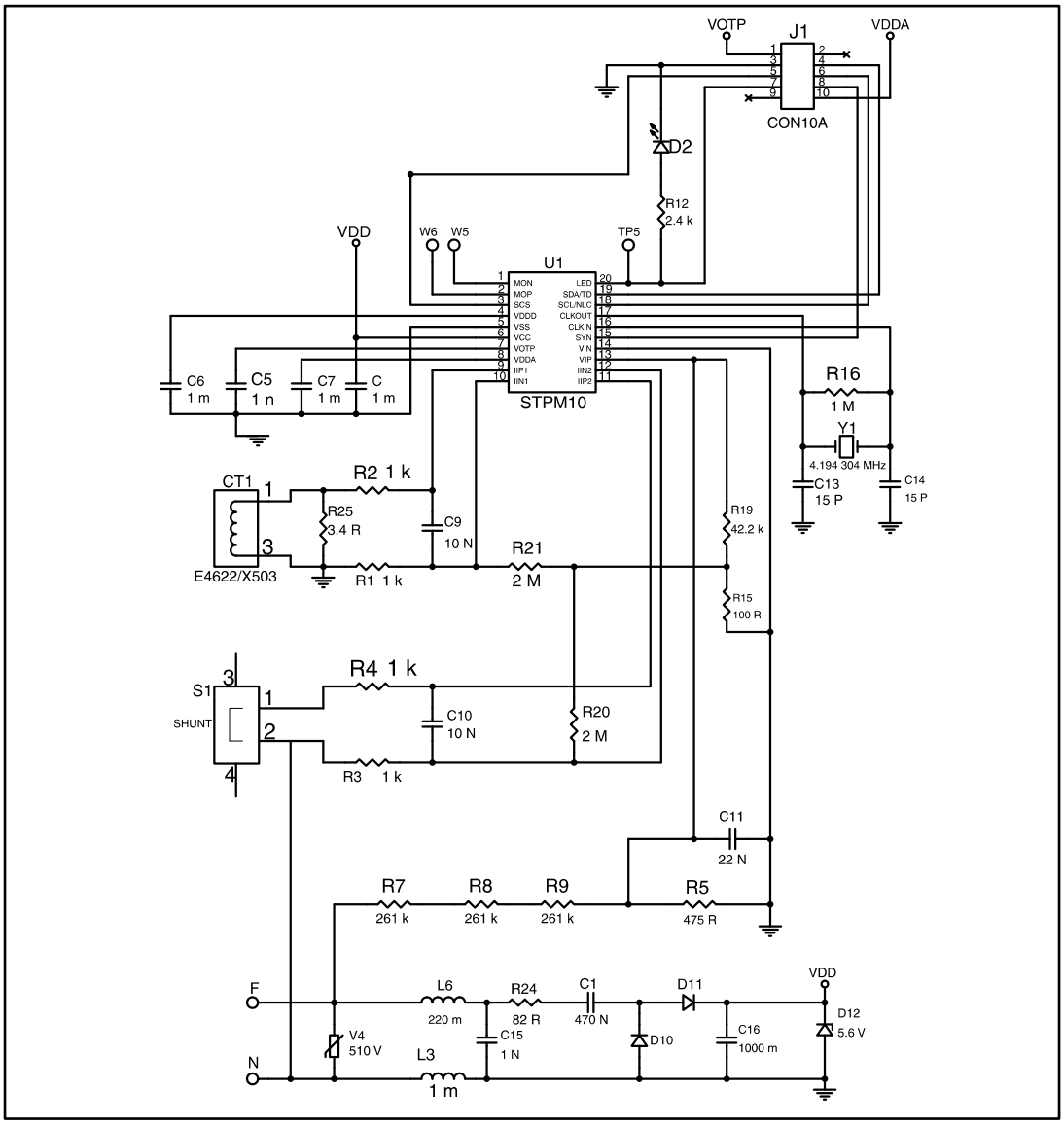
**Table 16: Current channel typical components**

| Function | Component | Parameter | Value | Unit |
|---|---|---|---|---|
| Line current interface | Current shunt | Current-to-voltage conversion ratio $K_S$ | 0.425 | mV/A |
| | Current transformer | | 1.7 | |
| | Rogowsky coil | | 0.13 | |

If the device is used in configuration PST = 1, TMP = 1 (primary channel with CT, secondary channel with shunt), the shunt $K_S$ must always be equal to one fourth of the current transformer $K_S$.

Additional considerations on the application design, suggestions for noise and crosstalk reduction can be found in the AN2317.

**Figure 27: STPM10 reference schematic with one current transformer and one shunt**



# 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 9.1 TSSOP20 package information

**Figure 28: TSSOP20 package outline**

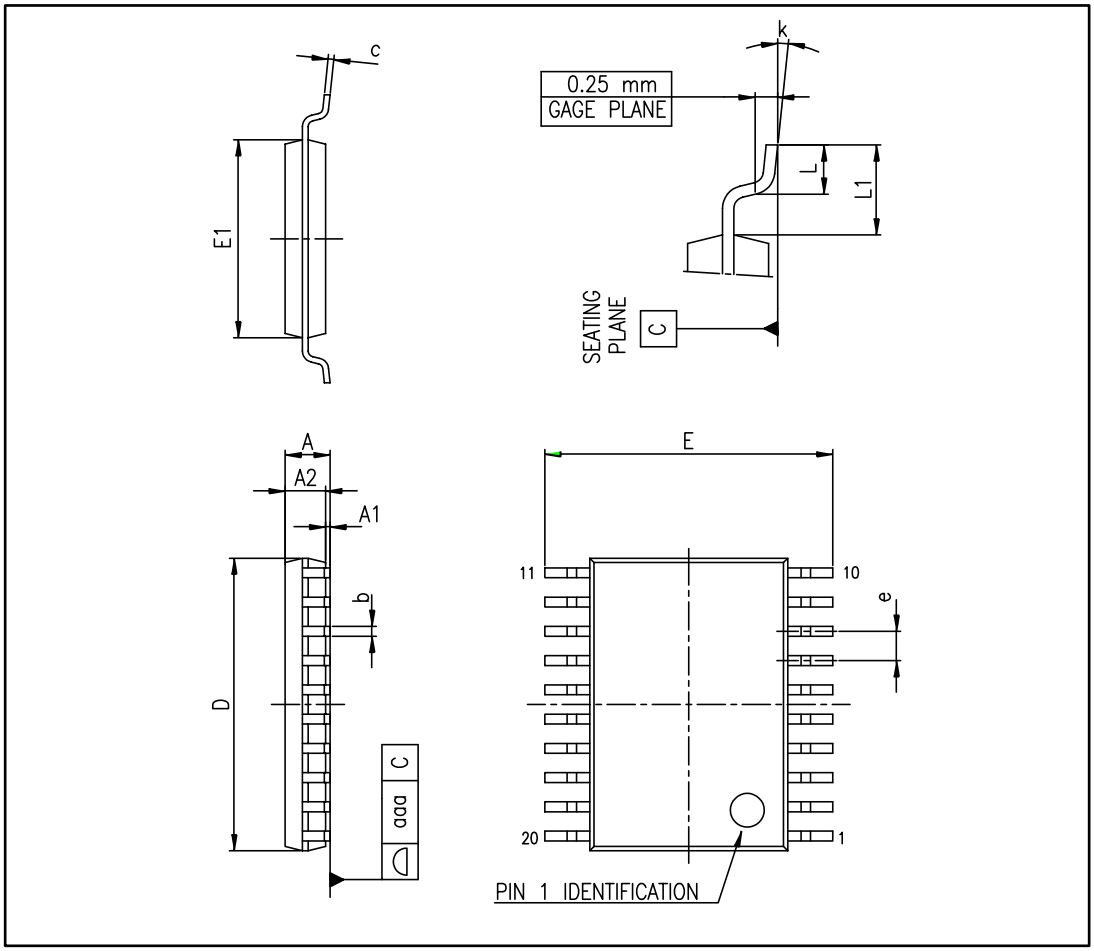


**Table 17: TSSOP20 package mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 6.40 | 6.50 | 6.60 |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | | 0.65 | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 | |
| k | 0 | | 8 |
| aaa | | | 0.10 |

# 10 Revision history

**Table 18: Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 31-Aug-2010 | 1 | Initial release. |
| 25-Nov-2010 | 2 | Modified: *Table 5 on page 9, 7.9: Tamper detection module on page 22*.<br>Added: 7.*11.1: RC startup procedure on page 25* and *8: Application design on page 46.* |
| 09-Jun-2011 | 3 | Updated *Table 5*. |
| 29-Jan-2013 | 4 | Updated *Table 9*. |
| 08-Feb-2017 | 5 | Updated $I_L$ parameter in *Table 5: "Absolute maximum ratings"*. |

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