

## LP38842 1.5A Ultra Low Dropout Linear Regulators Stable with Ceramic Output Capacitors

Check for Samples: [LP38842](#)

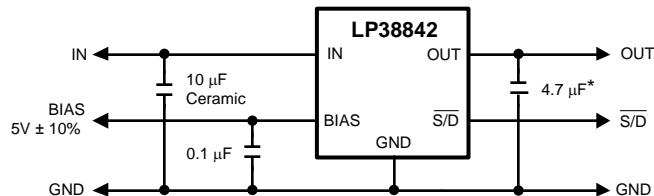
### FEATURES

- Ideal for Conversion from 1.8V or 1.5V Inputs
- Designed for use with low ESR Ceramic Capacitors
- 0.8V, 1.2V and 1.5V Standard Voltages Available
- Ultra Low Dropout Voltage (115mV at 1.5A typ)
- 1.5% Initial Output Accuracy
- Load Regulation of 0.1%/A (typical)
- 30nA Quiescent Current in Shutdown (typical)
- Low Ground Pin Current at all Loads
- Over Temperature/Over Current Protection
- Available in 5 Lead TO-220 and DDPAK/TO-263 Packages
- $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Junction Temperature Range

### APPLICATIONS

- ASIC Power Supplies In:
  - Desktops, Notebooks, and Graphics Cards, Servers
  - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

### TYPICAL APPLICATION CIRCUIT



\* Minimum value required if Tantalum capacitor is used (see Application Hints).

### DESCRIPTION

The LP38842 is a high current, fast response regulator which can maintain output voltage regulation with minimum input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: Vbias provides voltage to drive the gate of the N-MOS power transistor, while Vin is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low Vin voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of these devices makes them suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The parts are available in TO-220 and DDPAK/TO-263 packages.

**Dropout Voltage:** 115 mV (typ) at 1.5A load current.

**Quiescent Current:** 30 mA (typ) at full load.

**Shutdown Current:** 30 nA (typ) when S/D pin is low.

**Precision Output Voltage:** 1.5% room temperature accuracy.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## CONNECTION DIAGRAM

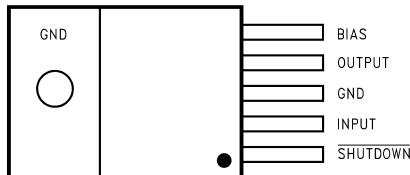


Figure 1. TO-220, Top View

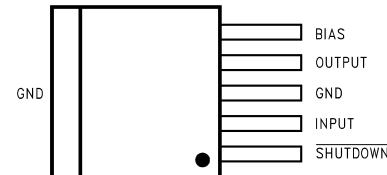
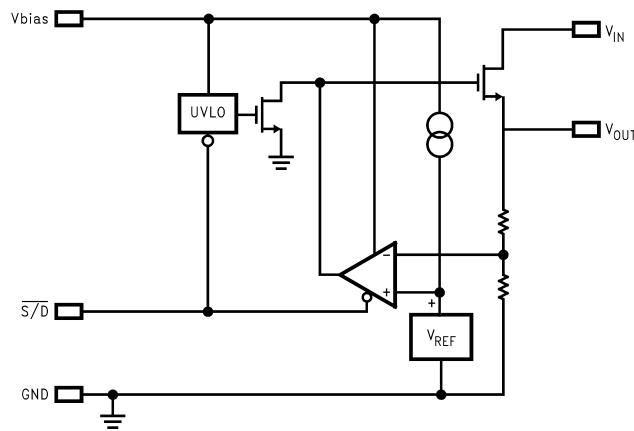


Figure 2. DDPAK/TO-263, Top View

## Pin DESCRIPTIONS

Pin Name	Description
BIAS	The bias pin is used to provide the low current bias voltage to the chip which operates the internal circuitry and provides drive voltage for the N-FET.
OUTPUT	The regulated output voltage is connected to this pin.
GND	This is both the power and analog ground for the IC. Note that both pin three and the tab of the TO-220 and DDPAK/TO-263 packages are at ground potential. Pin three and the tab should be tied together using the PC board copper trace material and connected to circuit ground.
INPUT	The high current input voltage which is regulated down to the nominal output voltage must be connected to this pin. Because the bias voltage to operate the chip is provided separately, the input voltage can be as low as a few hundred millivolts above the output voltage.
SHUTDOWN	This provides a low power shutdown function which turns the regulated output OFF. Tie to $V_{BIAS}$ if this function is not used.

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS <sup>(1)(2)</sup>**

Storage Temperature Range	-65°C to +150°C
Lead Temp. (Soldering, 5 seconds)	260°C
ESD Rating Human Body Model <sup>(3)</sup> Machine Model <sup>(4)</sup>	2 kV 200V
Power Dissipation <sup>(5)</sup>	Internally Limited
V <sub>IN</sub> Supply Voltage (Survival)	-0.3V to +6V
V <sub>BIAS</sub> Supply Voltage (Survival)	-0.3V to +7V
Shutdown Input Voltage (Survival)	-0.3V to +7V
I <sub>OUT</sub> (Survival)	Internally Limited
Output Voltage (Survival)	-0.3V to +6V
Junction Temperature	-40°C to +150°C

- (1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but **do not** ensure specific performance limits. For specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.
- (2) If Military/Aerospace specified devices are required, contact the Texas Instruments Semiconductor Sales Office/Distributors for availability and specifications.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.
- (4) The machine model is a 220 pF capacitor discharged directly into each pin.
- (5) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink thermal values.  $\theta_{J-A}$  for TO-220 devices is 65°C/W if no heatsink is used. If the TO-220 device is attached to a heatsink, a  $\theta_{J-S}$  value of 4°C/W can be assumed.  $\theta_{J-A}$  for DDPAK/TO-263 devices is approximately 35°C/W if soldered down to a copper plane which is at least 1 square inches in area. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

**RECOMMENDED OPERATING CONDITIONS**

V <sub>IN</sub> Supply Voltage	(V <sub>OUT</sub> + V <sub>DO</sub> ) to 5.5V
Shutdown Input Voltage	0 to +5.5V
I <sub>OUT</sub>	1.5A
Operating Junction Temperature Range	-40°C to +125°C
V <sub>BIAS</sub> Supply Voltage	4.5V to 5.5V
V <sub>OUT</sub>	0.8V to 1.5V

## ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for  $T_J = 25^\circ\text{C}$ , and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified:  $V_{IN} = V_O(\text{NOM}) + 1\text{V}$ ,  $V_{BIAS} = 4.5\text{V}$ ,  $I_L = 10\text{ mA}$ ,  $C_{IN} = 10\text{ }\mu\text{F CER}$ ,  $C_{OUT} = 22\text{ }\mu\text{F CER}$ ,  $C_{BIAS} = 1\text{ }\mu\text{F CER}$ ,  $V_{S/D} = V_{BIAS}$ . Min/Max limits are specified through testing, statistical correlation, or design.<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ <sup>(2)</sup>	Max	Units
$V_O$	Output Voltage Tolerance	10 mA < $I_L$ < 1.5A $V_O(\text{NOM}) + 1\text{V} \leq V_{IN} \leq 5.5\text{V}$ $4.5\text{V} \leq V_{BIAS} \leq 5.5\text{V}$	0.788 <b>0.776</b>	0.8	0.812 <b>0.824</b>	V
			1.182 <b>1.164</b>	1.2	1.218 <b>1.236</b>	
			1.478 <b>1.455</b>	1.5	1.523 <b>1.545</b>	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation <sup>(3)</sup>	$V_O(\text{NOM}) + 1\text{V} \leq V_{IN} \leq 5.5\text{V}$		0.01		%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation <sup>(4)</sup>	10 mA < $I_L$ < 1.5A		0.1	0.4 <b>1.1</b>	%/A
$V_{DO}$	Dropout Voltage <sup>(5)</sup>	$I_L = 1.5\text{A}$		115	175 <b>315</b>	mV
$I_Q(V_{IN})$	Quiescent Current Drawn from $V_{IN}$ Supply	10 mA < $I_L$ < 1.5A		30	35 <b>40</b>	mA
		$V_{S/D} \leq 0.3\text{V}$		0.06	1 <b>30</b>	$\mu\text{A}$
$I_Q(V_{BIAS})$	Quiescent Current Drawn from $V_{BIAS}$ Supply	10 mA < $I_L$ < 1.5A		2	4 <b>6</b>	mA
		$V_{S/D} \leq 0.3\text{V}$		0.03	1 <b>30</b>	$\mu\text{A}$
$I_{SC}$	Short-Circuit Current	$V_{OUT} = 0\text{V}$		4		A
<b>Shutdown Input</b>						
$V_{SDT}$	Output Turn-off Threshold	Output = ON		0.7	1.3	V
		Output = OFF	<b>0.3</b>	0.7		
$T_d$ (OFF)	Turn-OFF Delay	$R_{LOAD} X C_{OUT} \ll T_d$ (OFF)		20		$\mu\text{s}$
$T_d$ (ON)	Turn-ON Delay	$R_{LOAD} X C_{OUT} \ll T_d$ (ON)		15		
$I_{S/D}$	S/D Input Current	$V_{S/D} = 1.3\text{V}$		1		$\mu\text{A}$
		$V_{S/D} \leq 0.3\text{V}$		-1		
$\theta_{J-A}$	Junction to Ambient Thermal Resistance	TO-220, No Heatsink		65		$^\circ\text{C}/\text{W}$
		DDPAK/TO-263, 1 sq.in Copper		35		
<b>AC Parameters</b>						
PSRR ( $V_{IN}$ )	Ripple Rejection for $V_{IN}$ Input Voltage	$V_{IN} = V_{OUT} + 1\text{V}$ , $f = 120\text{ Hz}$		80		dB
		$V_{IN} = V_{OUT} + 1\text{V}$ , $f = 1\text{ kHz}$		65		
PSRR ( $V_{BIAS}$ )	Ripple Rejection for $V_{BIAS}$ Voltage	$V_{BIAS} = V_{OUT} + 3\text{V}$ , $f = 120\text{ Hz}$		58		
		$V_{BIAS} = V_{OUT} + 3\text{V}$ , $f = 1\text{ kHz}$		58		
$e_n$	Output Noise Density	$f = 120\text{ Hz}$		1		$\mu\text{V}/\sqrt{\text{Hz}}$
		$BW = 10\text{ Hz} - 100\text{ kHz}$ $V_{OUT} = 1.5\text{V}$		150		
				90		$\mu\text{V}$ (rms)

- (1) If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.
- (2) Typical numbers represent the most likely parametric norm for  $25^\circ\text{C}$  operation.
- (3) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
- (4) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
- (5) Dropout voltage is defined as the minimum input to output differential required to maintain the output with 2% of nominal value.

### TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $C_{IN} = 10 \mu\text{F}$  CER,  $C_{OUT} = 22 \mu\text{F}$  CER,  $C_{BIAS} = 1 \mu\text{F}$  CER,  $S/D$  Pin is tied to  $V_{BIAS}$ ,  $V_{OUT} = 1.2\text{V}$ ,  $I_L = 10\text{mA}$ ,  $V_{BIAS} = 5\text{V}$ ,  $V_{IN} = V_{OUT} + 1\text{V}$ .

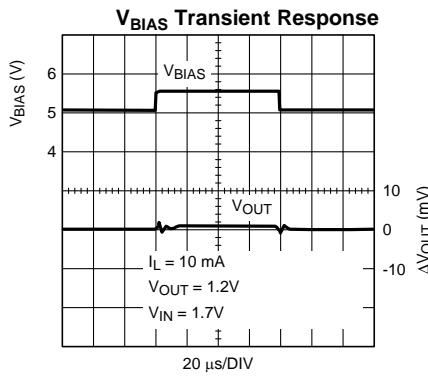


Figure 3.

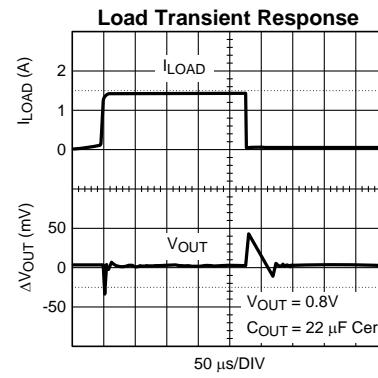


Figure 4.

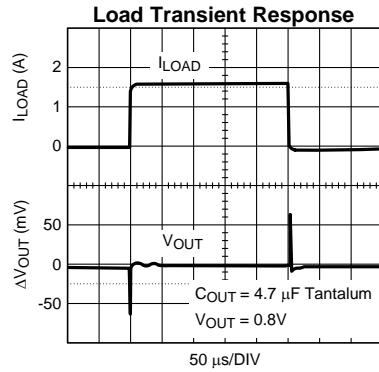


Figure 5.

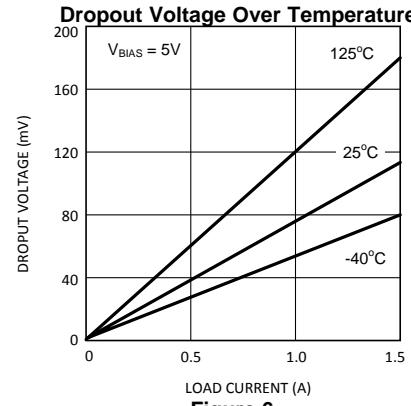


Figure 6.

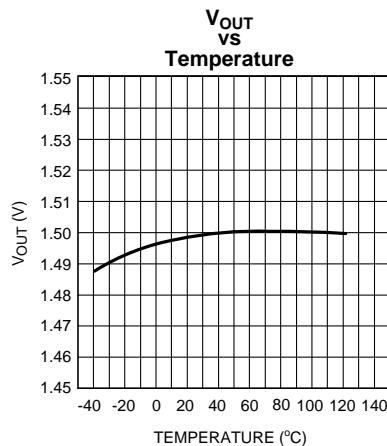


Figure 7.

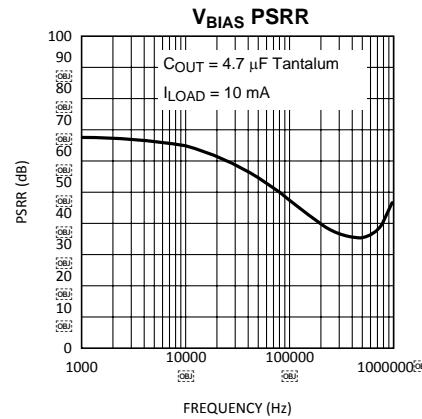


Figure 8.

### TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $C_{IN} = 10 \mu\text{F}$  CER,  $C_{OUT} = 22 \mu\text{F}$  CER,  $C_{BIAS} = 1 \mu\text{F}$  CER,  $\overline{S/D}$  Pin is tied to  $V_{BIAS}$ ,  $V_{OUT} = 1.2\text{V}$ ,  $I_L = 10\text{mA}$ ,  $V_{BIAS} = 5\text{V}$ ,  $V_{IN} = V_{OUT} + 1\text{V}$ .

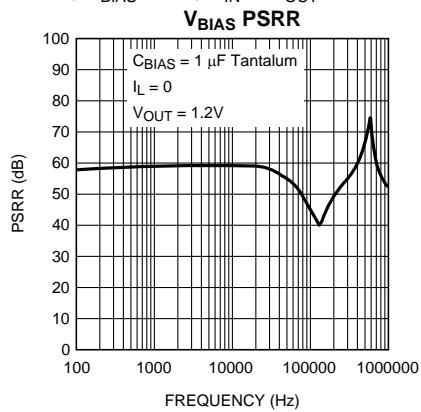


Figure 9.

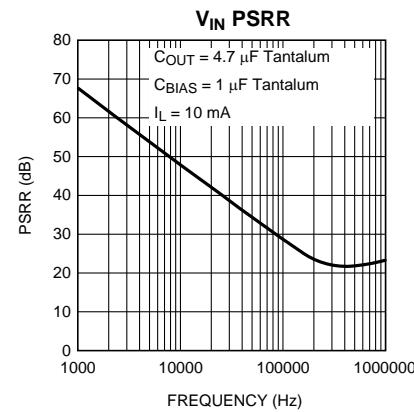


Figure 10.

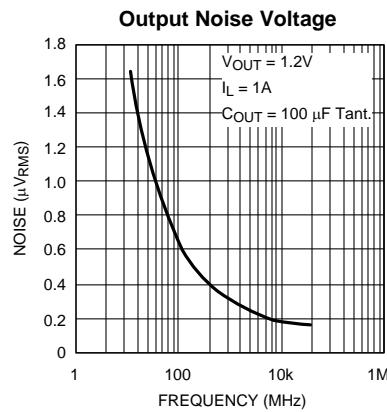


Figure 11.

## Application Hints

### EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the [TYPICAL APPLICATION CIRCUIT](#).

### OUTPUT CAPACITOR

An output capacitor is required on the LP3884X devices for loop stability. The minimum value of capacitance necessary depends on type of capacitor: if a solid Tantalum capacitor is used, the part is stable with capacitor values as low as 4.7 $\mu$ F. If a ceramic capacitor is used, a minimum of 22  $\mu$ F of capacitance must be used (capacitance may be increased without limit). The reason a larger ceramic capacitor is required is that the output capacitor sets a pole which limits the loop bandwidth. The Tantalum capacitor has a higher ESR than the ceramic which provides more phase margin to the loop, thereby allowing the use of a smaller output capacitor because adequate phase margin can be maintained out to a higher crossover frequency. The tantalum capacitor will typically also provide faster settling time on the output after a fast changing load transient occurs, but the ceramic capacitor is superior for bypassing high frequency noise.

The output capacitor must be located less than one centimeter from the output pin and returned to a clean analog ground. Care must be taken in choosing the output capacitor to ensure that sufficient capacitance is provided over the full operating temperature range. If ceramics are selected, only X7R or X5R types may be used because Z5U and Y5F types suffer severe loss of capacitance with temperature and applied voltage and may only provide 20% of their rated capacitance in operation.

### INPUT CAPACITOR

The input capacitor is also critical to loop stability because it provides a low source impedance for the regulator. The minimum required input capacitance is 10  $\mu$ F ceramic (Tantalum not recommended). The value of  $C_{IN}$  may be increased without limit. As stated above, X5R or X7R must be used to ensure sufficient capacitance is provided. The input capacitor must be located less than one centimeter from the input pin and returned to a clean analog ground.

### BIAS CAPACITOR

The 0.1 $\mu$ F capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

### BIAS VOLTAGE

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 - 5.5V to assure proper operation of the part.

### UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the regulator output from turning on if the bias voltage is below approximately 4V.

### SHUTDOWN OPERATION

Pulling down the shutdown ( $\overline{S/D}$ ) pin will turn-off the regulator. Pin  $\overline{S/D}$  must be actively terminated through a pull-up resistor (10 k $\Omega$  to 100 k $\Omega$ ) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to  $V_{BIAS}$  if not used.

### POWER DISSIPATION/HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN})I_{GND} \quad (1)$$

where  $I_{GND}$  is the operating ground current of the device.

The maximum allowable temperature rise ( $T_{R\max}$ ) depends on the maximum ambient temperature ( $T_{A\max}$ ) of the application, and the maximum allowable junction temperature ( $T_{J\max}$ ):

$$T_{R\max} = T_{J\max} - T_{A\max} \quad (2)$$

The maximum allowable value for junction to ambient Thermal Resistance,  $\theta_{JA}$ , can be calculated using the formula:

$$\theta_{JA} = T_{R\max} / P_D \quad (3)$$

These parts are available in TO-220 and DDPAK/TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of  $\theta_{JA}$  calculated above is  $\geq 60 \text{ }^{\circ}\text{C/W}$  for TO-220 package and  $\geq 60 \text{ }^{\circ}\text{C/W}$  for DDPAK/TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable  $\theta_{JA}$  falls below these limits, a heat sink is required.

## HEATSINKING TO-220 PACKAGE

The thermal resistance of a TO-220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of  $\theta_{JA}$  will be same as shown in next section for DDPAK/TO-263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$$\theta_{HA} \leq \theta_{JA} - \theta_{CH} - \theta_{JC} \quad (4)$$

In this equation,  $\theta_{CH}$  is the thermal resistance from the case to the surface of the heat sink and  $\theta_{JC}$  is the thermal resistance from the junction to the surface of the case.  $\theta_{JC}$  is about  $3 \text{ }^{\circ}\text{C/W}$  for a TO-220 package. The value for  $\theta_{CH}$  depends on method of attachment, insulator, etc.  $\theta_{CH}$  varies between  $1.5 \text{ }^{\circ}\text{C/W}$  to  $2.5 \text{ }^{\circ}\text{C/W}$ . If the exact value is unknown,  $2 \text{ }^{\circ}\text{C/W}$  can be assumed.

## HEATSINKING DDPAK/TO-263 PACKAGE

The DDPAK/TO-263 package uses the copper plane on the PCB as a heatsink. The tab of this package is soldered to the copper plane for heat sinking. The graph below shows a curve for the  $\theta_{JA}$  of DDPAK/TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

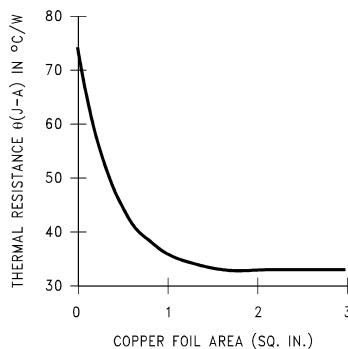


Figure 12.  $\theta_{JA}$  vs Copper (1 Ounce) Area for DDPAK/TO-263 package

As shown in the graph below, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for  $\theta_{JA}$  for the DDPAK/TO-263 package mounted to a PCB is  $32 \text{ }^{\circ}\text{C/W}$ .

Figure 13 shows the maximum allowable power dissipation for DDPAK/TO-263 packages for different ambient temperatures, assuming  $\theta_{JA}$  is  $35 \text{ }^{\circ}\text{C/W}$  and the maximum junction temperature is  $125 \text{ }^{\circ}\text{C}$ .

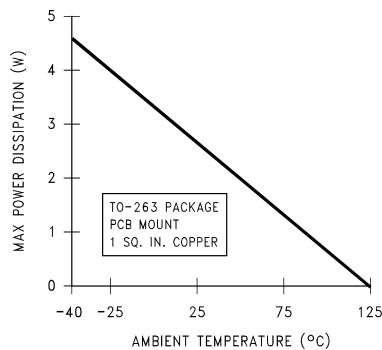


Figure 13. Maximum power dissipation vs ambient temperature for DDPAK/TO-263 package

## REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format .....	8

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38842S-0.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	SN	Level-3-245C-168 HR	-40 to 125	LP38842S -0.8	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
LP38842S-1.2/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	SN	Level-3-245C-168 HR	-40 to 125	LP38842S -1.2	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
LP38842S-1.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	SN	Level-3-245C-168 HR	-40 to 125	LP38842S -1.5	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
LP38842SX-1.2/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	SN	Level-3-245C-168 HR	-40 to 125	LP38842S -1.2	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
LP38842SX-1.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	SN	Level-3-245C-168 HR	-40 to 125	LP38842S -1.5	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
LP38842T-1.2/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 125	LP38842T -1.2	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
LP38842T-1.5/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 125	LP38842T -1.5	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

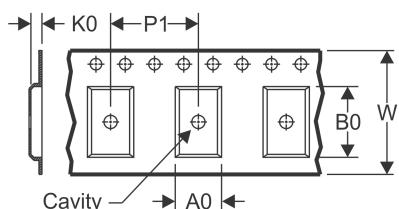
---

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

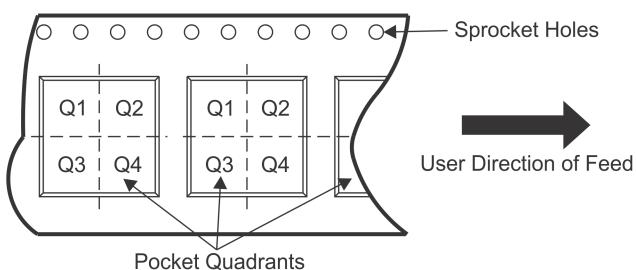
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38842SX-1.2/NOPB	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP38842SX-1.5/NOPB	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38842SX-1.2/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP38842SX-1.5/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

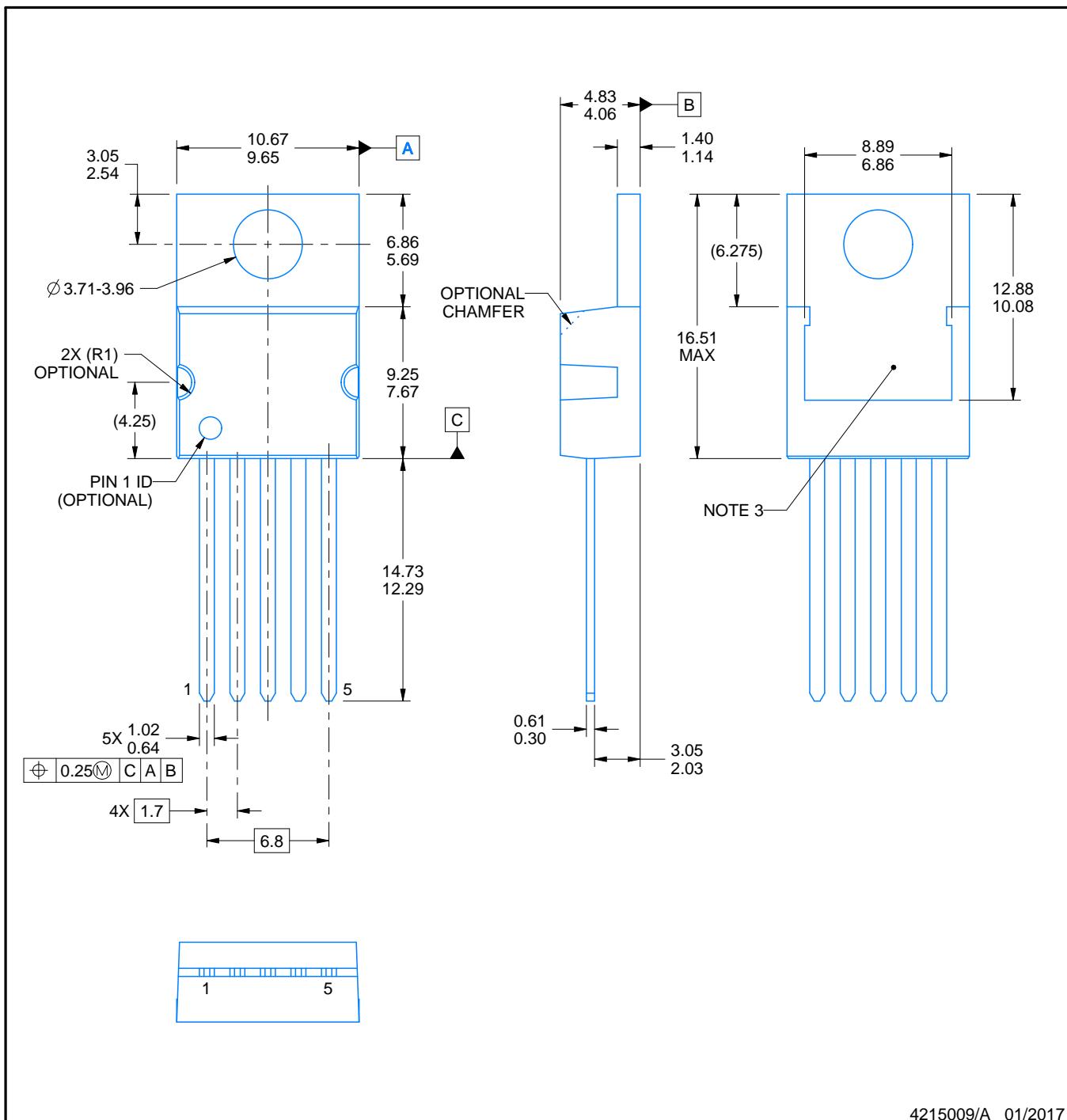


# PACKAGE OUTLINE

**KC0005A**

**TO-220 - 16.51 mm max height**

TO-220



4215009/A 01/2017

**NOTES:**

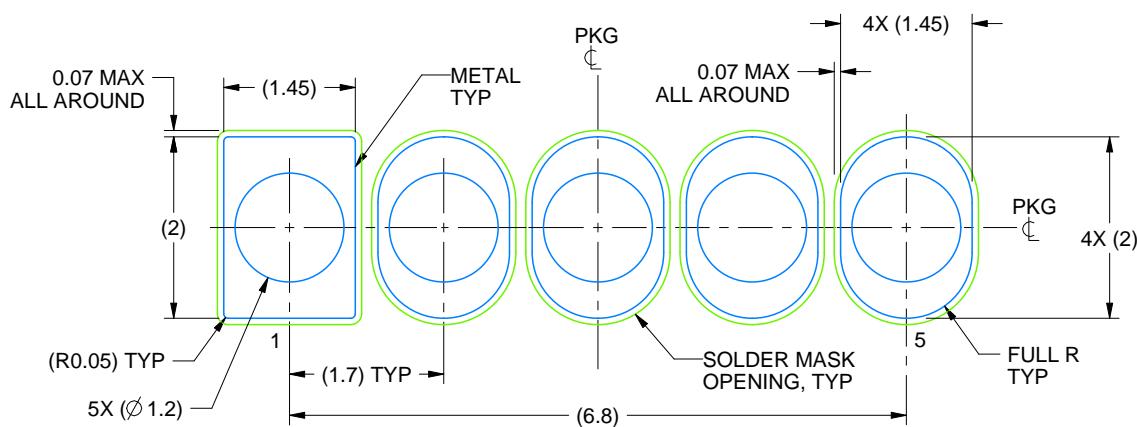
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.

# EXAMPLE BOARD LAYOUT

KC0005A

TO-220 - 16.51 mm max height

TO-220

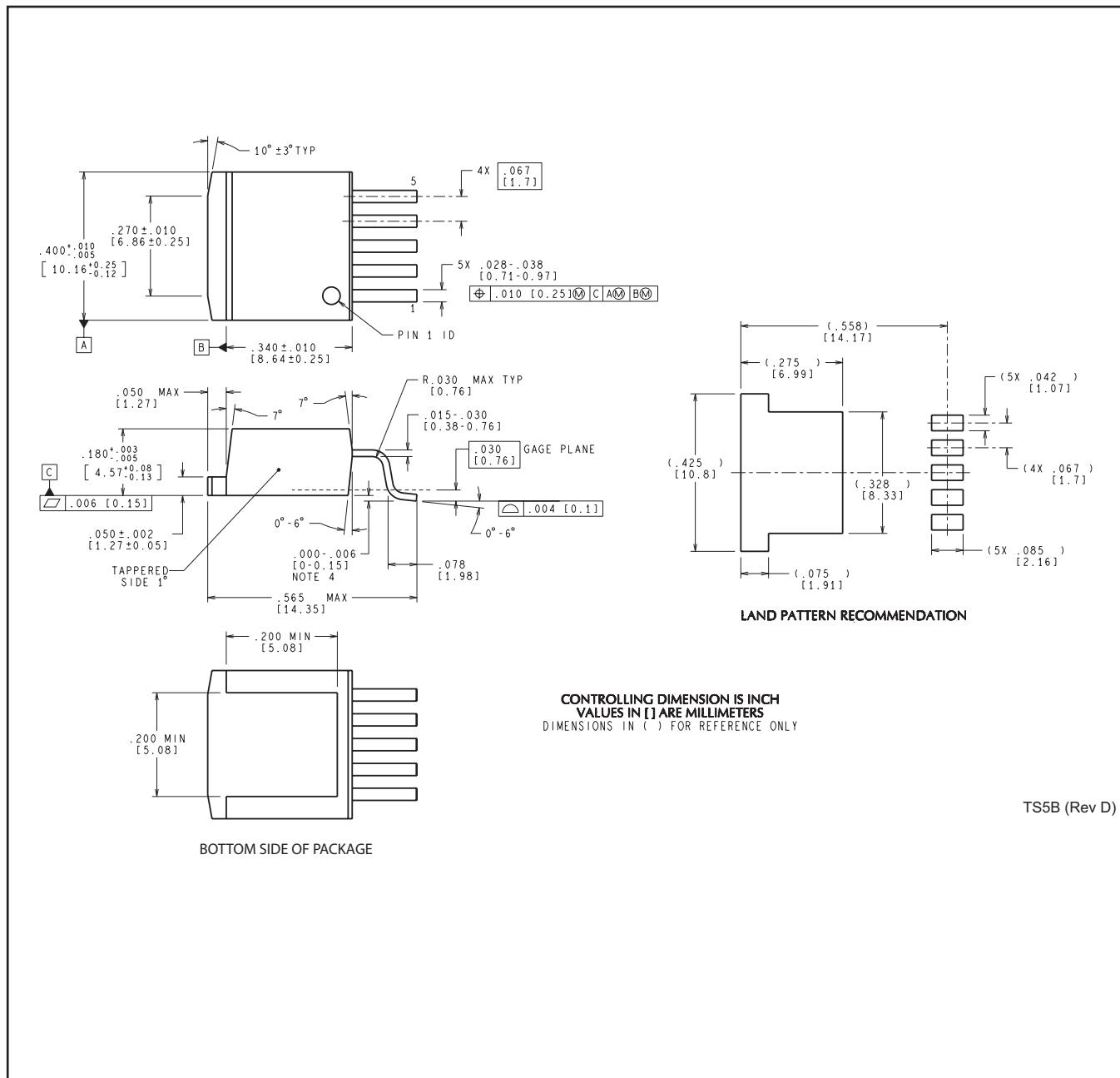


LAND PATTERN  
NON-SOLDER MASK DEFINED  
SCALE:12X

4215009/A 01/2017

## MECHANICAL DATA

KT0005B



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated