

Single-chip Type with built-in FET Switching Regulator Series

Flexible Step-down Switching Regulators with Built-in Power MOSFET



BD9006F/HFP, BD9007F/HFP, BD9009HFP

No.12027ECT35

● Overview

The high-accuracy frequency flexible step-down switching regulator is a switching regulator with built-in POWER MOS FET, which withstands high pressure. The operational frequency is freely configurable with external resistance. It features a wide input voltage range (7V~35V) and a high frequency accuracy of $\pm 5\%$ (BD9006F/HFP, BD9009HFP, $f=200\sim 500\text{kHz}$), Furthermore, an external synchronization input pin enables synchronous operation with external clock.

● Features

- 1) Minimal external components
- 2) Wide input voltage range: 7V~35V
- 3) Frequency voltage accuracy: $\pm 5\%$ (BD9006F/HFP, BD9009HFP, $f=200\sim 500\text{kHz}$)
 $\pm 20\%$ (BD9007F/HFP)
- 4) Built-in P-ch POWER MOS FET
- 5) Output voltage setting enabled with external resistor: 0.8V~ V_{IN}
- 6) Reference voltage accuracy: 0.8V $\pm 2\%$
- 7) Wide operating temperature range: $-40^{\circ}\text{C}\sim +105^{\circ}\text{C}$
- 8) Low dropout: 100% ON duty cycle
- 9) Standby mode supply current: 0 μA (Typ.)
- 10) Oscillation frequency variable with external resistor: 50~500kHz
- 11) External synchronization enabled
- 12) Soft start function: soft start time fixed to 5ms (Typ.)
- 13) Built-in overcurrent protection circuit
- 14) Built-in thermal shutdown protection circuit
- 15) High-power HRP7 package mounted (BD9006HFP, BD9007HFP, BD9009HFP)
- 16) Compact SOP8 package mounted (BD9006F, BD9007F)

● Applications

All fields of industrial equipment, such as Flat TV, printer, DVD, car audio, car navigation, and communication such as ETC, AV, and OA.

● Product lineup

Item	BD9006F/HFP	BD9007F/HFP	BD9009HFP
Output Current	2A	2A	4A
Input Range	7V~35V	7V~35V	7V~35V
Oscillation Frequency Range	50~500kHz	50~500kHz	50~500kHz
Oscillation Frequency Accuracy	$\pm 5\%$	$\pm 20\%$	$\pm 5\%$
External Synchronous Function	Provided	Provided	Provided
Standby Function	Provided	Provided	Provided
Operating Temperature	$-40^{\circ}\text{C}\sim +105^{\circ}\text{C}$	$-40^{\circ}\text{C}\sim +105^{\circ}\text{C}$	$-40^{\circ}\text{C}\sim +105^{\circ}\text{C}$
Package	SOP8/HRP7	SOP8/HRP7	HRP7

● Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Power Supply Voltage		VIN	36	V
Output Switch Pin Voltage		VSW	VIN	V
Output Switch Current	BD9006F/HFP, BD9007F/HFP	ISW	2 *1	A
	BD9009HFP		4 *1	
EN/SYNC Pin Voltage		VEN/SYNC	VIN	V
RT, FB, INV Pin Voltage		VRT, VFB, VINV	7	
Power Dissipation	HRP7	Pd	5.5 *2	W
	SOP8		0.69 *3	W
Operating Temperature Range		Topr	-40~+105	°C
Storage Temperature Range		Tstg	-55~+150	°C
Maximum Junction Temperature		Tjmax	150	°C

*1 Should not exceed Pd-value.

*2 Reduce by 44mW/°C over 25°C, when mounted on 2-layer PCB of 70x70x1.6mm³
(PCB incorporates thermal via. Copper foil area on the reverse side of PCB: 10.5x10.5mm²)*3 Reduce by 5.52mW/°C over 25°C, when mounted on 2-layer PCB of 70x70x1.6mm³

● Recommended Operating Range

Parameter	BD9006F/HFP	BD9007F/HFP	BD9009HFP	Unit
Operating Power Supply Voltage	7~35	7~35	7~35	V
Output Switch Current	~2	~2	~4	A
Output Voltage (min pulse width)	250	250	360	ns
Oscillation Frequency	50~500	50~500	50~500	kHz
Oscillation Frequency set Resistance	27~360	27~360	27~360	kΩ

● Possible Operating Range

Parameter	BD9006F/HFP	BD9007F/HFP	BD9009HFP	Unit
Operating Power Supply Voltage	5~35	5~35	5~35	V

● Electrical Characteristics

◎BD9006F/HFP (Unless otherwise specified, Ta=25°C, VIN=13.2V, VEN/SYNC=5V)

Parameter	Symbol	Spec Values			Unit	Conditions
		Min.	Typ.	Max.		
Standby Circuit Current	ISTB	-	0	10	μA	VEN/SYNC=0V
Circuit Current	Iq	-	4	6.5	mA	Io=0A, RT=51kΩ, VINV=0.7V
【SW Block】						
POWER MOS FET ON Resistance	RON	-	0.3	0.6	Ω	ISW=50mA
Operating Output Current Of Overcurrent Protection	IOLIMIT	2	4	-	A	
Output Leak Current	IOLAK	-	0	30	μA	VIN=35V, VEN/SYNC=0V
【Error Amp Block】						
Reference Voltage 1	VREF1	0.784	0.800	0.816	V	VFB=VINV
Reference Voltage 2	VREF2	0.780	0.800	0.820	V	VIN=10~16V, VFB=VINV
Reference Voltage Input Regulation	ΔVREF	-	0.5	-	%	
Input Bias Current	IB	-1	-	-	μA	VINV=0.6V
Maximum FB Voltage	VFBH	2.2	2.4	-	V	VINV=0V
Minimum FB Voltage	VFBL	-	0.5	0.6	V	VINV=2V
FB Sink Current	IFBSINK	-0.47	-1.16	-2.45	mA	VFB=1V, VINV=1V
FB Source Current	IFBSOURCE	1	5	15	mA	VFB=1V, VINV=0.6V
Soft Start Time	TSS	3	5	9	mS	Ta=-40~105°C
【Oscillator Block】						
Oscillation Frequency	FOSC	285	300	315	kHz	VIN=7V, RT=51kΩ
Frequency Input Regulation	ΔFOSC	-	0.5	-	%	VIN=7~16V
【Enable/Sync Input Block】						
Output ON Voltage	VENON	2.6	-	-	V	VEN/SYNC Sweep Up, Ta=-40~105°C
Output OFF Voltage	VENOFF	-	-	0.8	V	VEN/SYNC Sweep Down, Ta=-40~105°C
Sink Current	IEN/SYNC	-	35	90	μA	
External Sync Frequency	FSYNC	495	500	505	kHz	RT=51kΩ, EN/SYNC=500kHz, Duty 50%

* Not designed to be radiation resistant.

©BD9007F/HFP (Unless otherwise specified, Ta=25°C, VIN=13.2V, VEN/SYNC=5V)

Parameter	Symbol	Spec Values			Unit	Conditions
		Min.	Typ.	Max.		
Standby Circuit Current	ISTB	-	0	10	μA	VEN/SYNC=0V
Circuit Current	IQ	-	4	6.5	mA	IO=0A,RT=51kΩ,VINV=0.7V
【SW Block】						
POWER MOS FET ON Resistance	RON	-	0.3	0.6	Ω	ISW=50mA
Operating Output Current Of Overcurrent Protection	IOLIMIT	2	4	-	A	
Output Leak Current	IOLIAK	-	0	30	μA	VIN=35V, VEN/SYNC=0V
【Error Amp Block】						
Reference Voltage 1	VREF1	0.784	0.800	0.816	V	VFB=VINV
Reference Voltage 2	VREF2	0.780	0.800	0.820	V	VIN=10~16V,VFB=VINV
Reference Voltage Input Regulation	ΔVREF	-	0.5	-	%	
Input Bias Current	IB	-1	-	-	μA	VINV=0.6V
Maximum FB Voltage	VFBH	2.2	2.4	-	V	VINV=0V
Minimum FB Voltage	VFBL	-	0.5	0.6	V	VINV=2V
FB Sink Current	IFBSINK	-0.47	-1.16	-2.45	mA	VFB=1V,VINV=1V
FB Source Current	IFBSOURCE	1	5	15	mA	VFB=1V,VINV=0.6V
Soft Start Time	TSS	3	5	9	mS	Ta=-40~105°C
【Oscillator Block】						
Oscillation Frequency	FOSC	240	300	360	kHz	VIN=7V,RT=51kΩ
Frequency Input Regulation	ΔFOSC	-	0.5	-	%	VIN=7~16V
【Enable/Sync Input Block】						
Output ON Voltage	VENON	2.6	-	-	V	VEN/SYNC Sweep Up,a=-40~105°C
Output OFF Voltage	VENOFF	-	-	0.8	V	VEN/SYNC Sweep,own,Ta=-40~105°C
Sink Current	IEN/SYNC	-	35	90	μA	
External Sync Frequency	FSYNC	495	500	505	kHz	RT=51kΩ, EN/SYNC=500kHz,Duty 50%

* Not designed to be radiation resistant.

©BD9009HFP (Unless otherwise specified, Ta=25°C, VIN=13.2V, VEN/SYNC=5V)

Parameter	Symbol	Spec Values			Unit	Conditions
		Min.	Typ.	Max.		
Standby Circuit Current	ISTB	-	0	10	μA	VEN/SYNC=0V
Circuit Current	IQ	-	4.2	6.5	mA	IO=0A,RT=51kΩ,VINV=0.7V
【SW Block】						
POWER MOS FET ON Resistance	RON	-	0.24	0.5	Ω	ISW=50mA
Operating Output Current Of Overcurrent Protection	IOLIMIT	4	7	-	A	
Output Leak Current	IOLIAK	-	0	30	μA	VIN=35V, VEN/SYNC=0V
【Error Amp Block】						
Reference Voltage 1	VREF1	0.784	0.800	0.816	V	VFB=VINV
Reference Voltage 2	VREF2	0.780	0.800	0.820	V	VIN=10~16V,VFB=VINV
Reference Voltage Input Regulation	ΔVREF	-	0.5	-	%	
Input Bias Current	IB	-1	-	-	μA	VINV=0.6V
Maximum FB Voltage	VFBH	2.2	2.4	-	V	VINV=0V
Minimum FB Voltage	VFBL	-	0.5	0.6	V	VINV=2V
FB Sink Current	IFBSINK	-0.47	-1.16	-2.45	mA	VFB=1V,VINV=1V
FB Source Current	IFBSOURCE	1	5	15	mA	VFB=1V,VINV=0.6V
Soft Start Time	TSS	3	5	9	mS	Ta=-40~105°C
【Oscillator Block】						
Oscillation Frequency	FOSC	285	300	315	kHz	VIN=7V,RT=51kΩ
Frequency Input Regulation	ΔFOSC	-	0.5	-	%	VIN=7~16V
【Enable/Sync Input Block】						
Output ON Voltage	VENON	2.6	-	-	V	VEN/SYNC Sweep Up,Ta=-40~105°C
Output OFF Voltage	VENOFF	-	-	0.8	V	VEN/SYNC Sweep Down,Ta=-40~105°C
Sink Current	IEN/SYNC	-	35	90	μA	
External Sync Frequency	FSYNC	495	500	505	kHz	RT=51kΩ,EN/SYNC=500kHz,Duty 50%

* Not designed to be radiation resistant.

●Reference Data

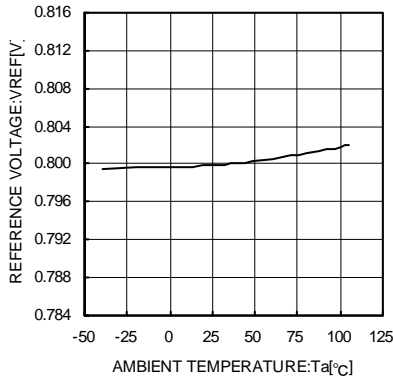


Fig.1 Output reference voltage vs. Ambient temperature (All series)

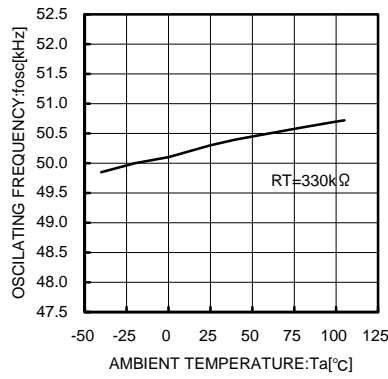


Fig.2 Frequency vs. Ambient temperature (All series)

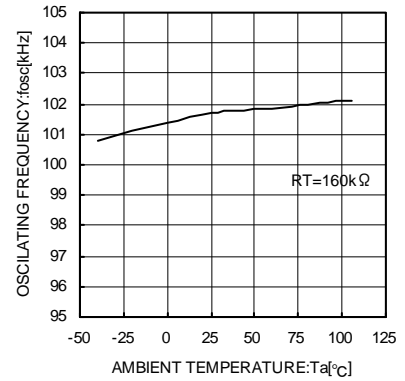


Fig.3 Frequency vs. Ambient temperature (All series)

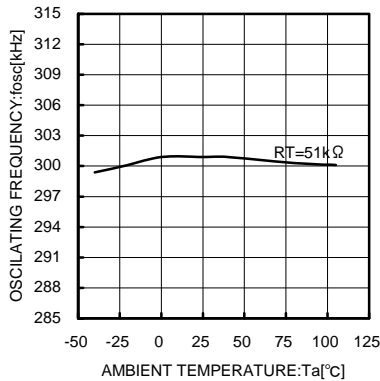


Fig.4 Frequency vs. Ambient temperature (All series)

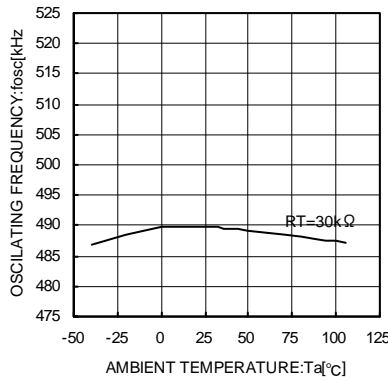


Fig.5 Frequency vs. Ambient temperature (All series)

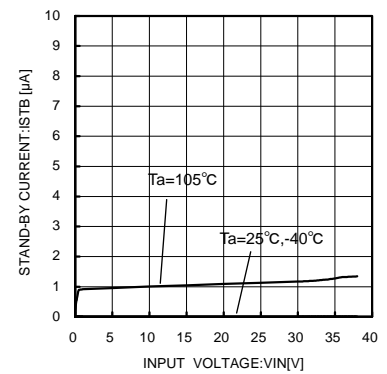


Fig.6 Standby Current (BD9006F/HFP, BD9007F/HFP)

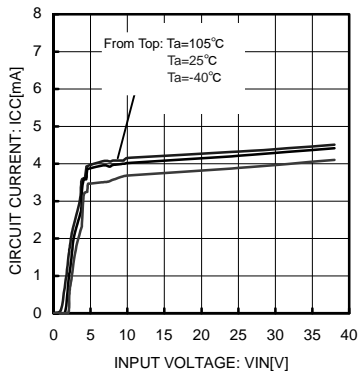


Fig.7 Circuit Current (BD9006F/HFP, BD9007F/HFP)

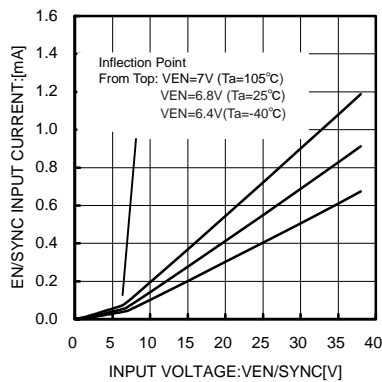


Fig.8 EN/SYNC Input Current (All series)

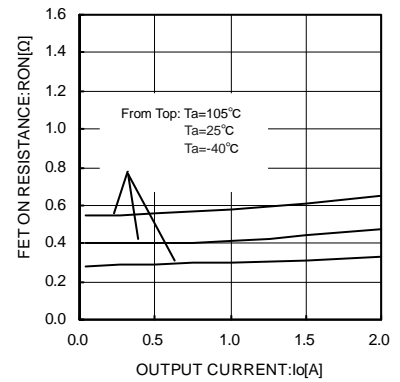


Fig.9 ON Resistance VIN=7V (BD9006F/HFP, BD9007F/HFP)

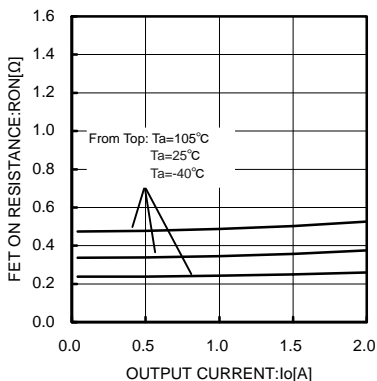


Fig.10 ON Resistance VIN=13.2V (BD9006F/HFP, BD9007F/HFP)

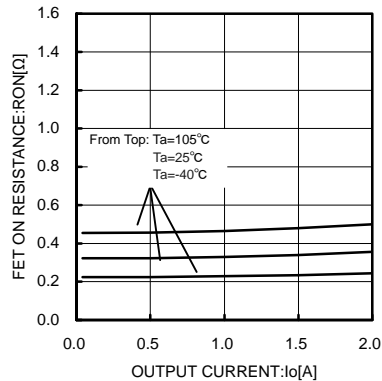


Fig.11 ON Resistance VIN=35V (BD9006F/HFP, BD9007F/HFP)

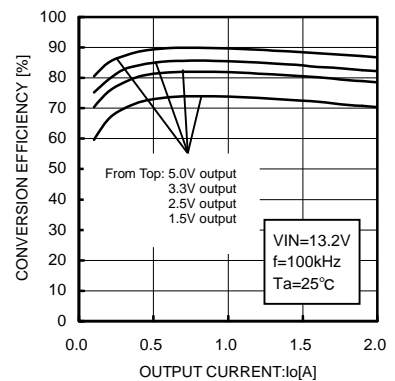


Fig.12 Efficiency f=100kHz (BD9006F/HFP, BD9007F/HFP)

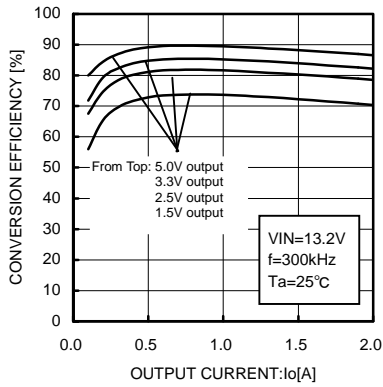


Fig.13 Efficiency f=300kHz (BD9006F/HFP, BD9007F/HFP)

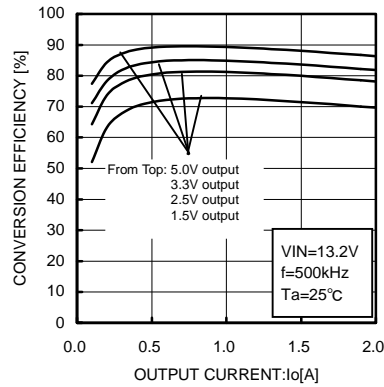


Fig.14 Efficiency f=500kHz (BD9006F/HFP, BD9007F/HFP)

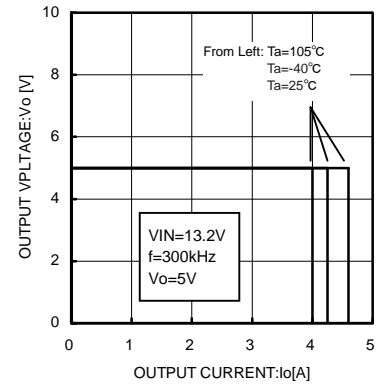


Fig.15 Over-current Protection Operation Current (BD9006F/HFP, BD9007F/HFP)

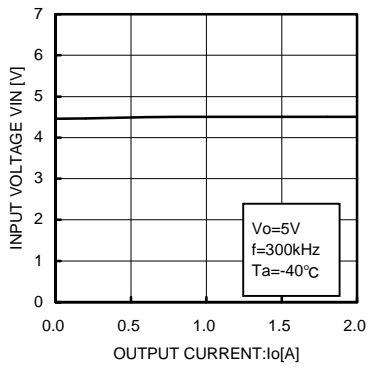


Fig.16 The lowest voltage of possible operation Ta=-40°C (BD9006F/HFP, BD9007F/HFP)

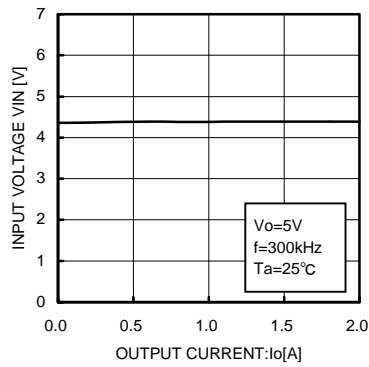


Fig.17 The lowest voltage of possible operation Ta=25°C (BD9006F/HFP, BD9007F/HFP)

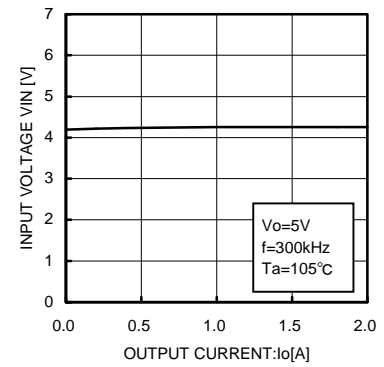


Fig.18 The lowest voltage of possible operation Ta=105°C (BD9006F/HFP, BD9007F/HFP)

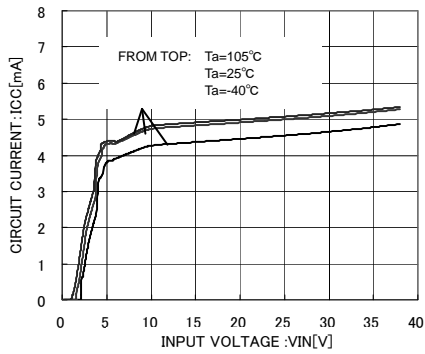


Fig.19 Circuit Current (BD9009HFP)

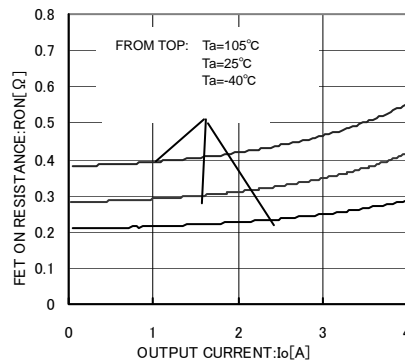


Fig.20 ON Resistance VIN=7V (BD9009HFP)

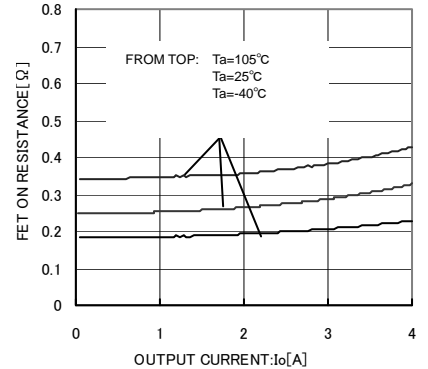


Fig.21 ON Resistance VIN=13.2V (BD9009HFP)

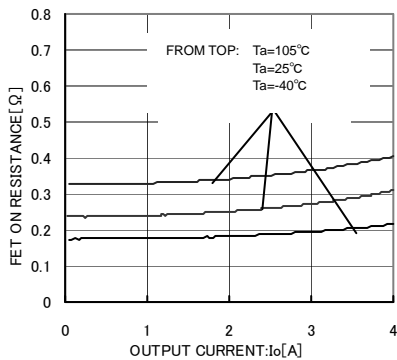


Fig.22 ON Resistance VIN=35V (BD9009HFP)

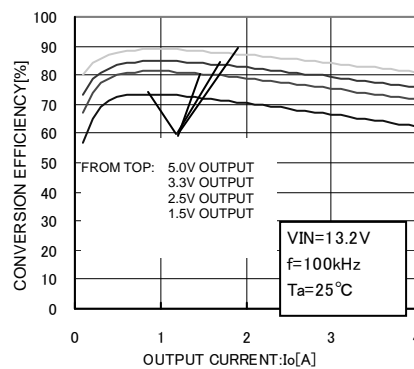


Fig.23 Efficiency f=100kHz (BD9009HFP)

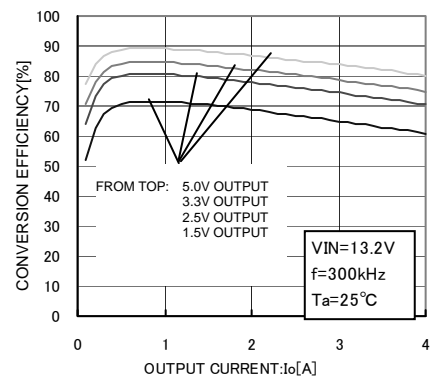


Fig.24 Efficiency f=300kHz (BD9009HFP)

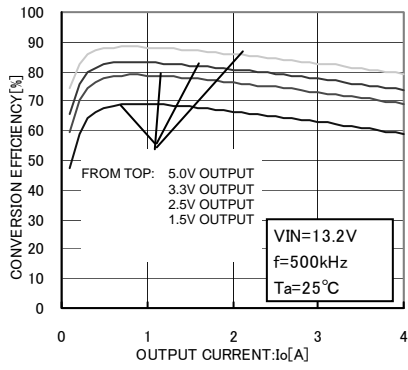


Fig.25 Efficiency f=500kHz (BD9009HFP)

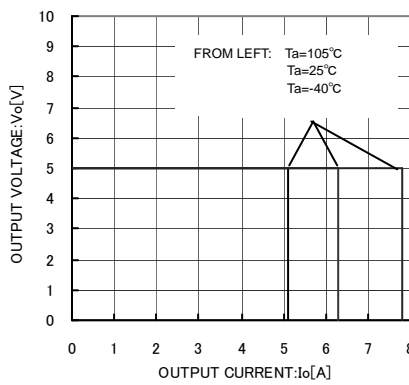


Fig.26 Over-current Protection Operation Current (BD9009HFP)

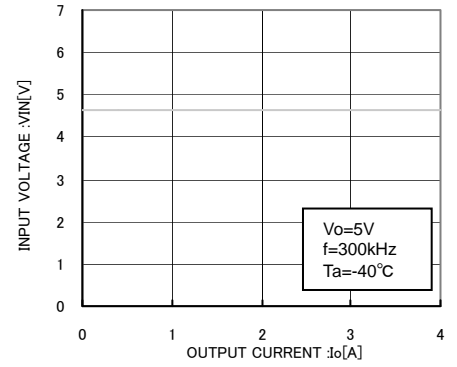


Fig.27 The lowest voltage of possible operation Ta=-40°C (BD9009HFP)

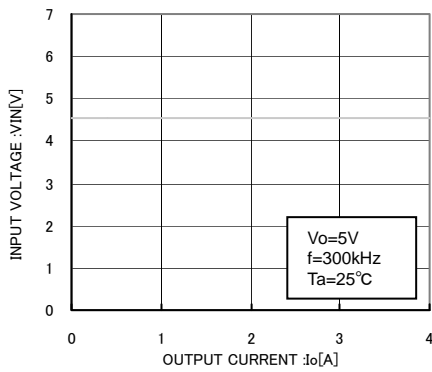


Fig.28 The lowest voltage of possible operation Ta=25°C (BD9009HFP)

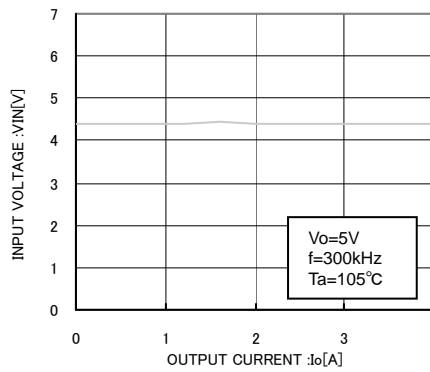


Fig.29 The lowest voltage of possible operation Ta=105°C (BD9009HFP)

●Block Diagrams / Application circuit / PIN assignment

(BD9006F/BD9007F)

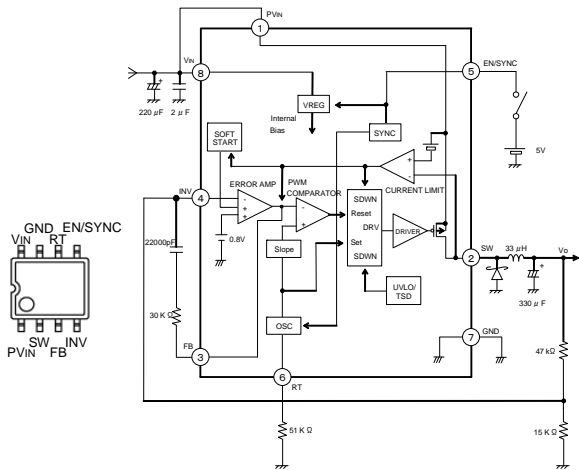


Fig.30

No.	Pin name	Function
1	PVIN	Power system power supply input
2	SW	Output
3	FB	Error Amp output
4	INV	Output voltage feedback
5	EN/SYNC	Enable/Synchronizing pulse input
6	RT	Frequency setting resistor connection
7	GND	Ground
8	VIN	Power supply input

* VIN and PVIN must be shorted before use

(BD9006HFP/BD9007HFP)

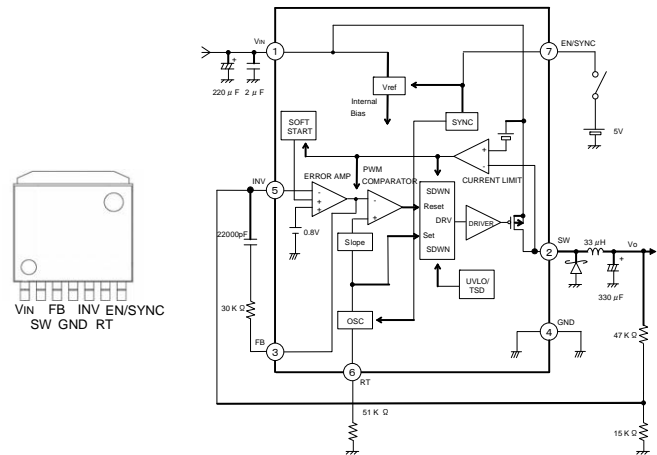


Fig.31

No.	Pin name	Function
1	VIN	Power supply input
2	SW	Output
3	FB	Error Amp output
4	GND	Ground
5	INV	Output voltage feedback
6	RT	Frequency setting resistor connection
7	EN/SYNC	Enable/Synchronizing pulse input
8	FIN	Ground

(BD9009HFP)

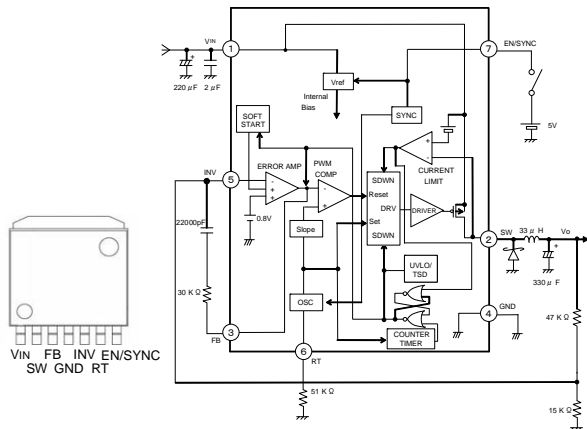


Fig.32

No.	Pin name	Function
1	VIN	Power supply input
2	SW	Output
3	FB	Error Amp output
4	GND	Ground
5	INV	Output voltage feedback
6	RT	Frequency setting resistor connection
7	EN/SYNC	Enable/Synchronizing pulse input
8	FIN	Ground

● Description of operations

• ERROR AMP

The ERROR AMP block is an error amplifier used to input the reference voltage (0.8V Typ.) and the INV pin voltage. The output FB pin controls the switching duty and output voltage V_o . These INV and FB pins are externally mounted to facilitate phase compensation. Inserting a capacitor and resistor between these pins enables adjustment of phase margin. (Refer to recommended examples on pages 13~15.)

• SOFT START

The SOFT START block provides a function to prevent the overshoot of the output voltage V_o through gradually increasing the normal rotation input of the error amplifier when power supply turns ON to gradually increase the switching Duty. The soft start time is set to 5msec (Typ.).

• SYNC

By making the "EN/SYNC" terminal less than 0.8V, the circuit can be shut down.

Furthermore, by applying pulse with higher frequency than the configured oscillation frequency to the "EN/SYNC" terminal, external sync is possible. (Sync possible with double the configured frequency-configured frequency or 500kHz)

• OSC(Oscillator)

This circuit generates the pulse wave to be input to the slope, and by connecting resistance to "RT", 50~500kHz oscillating frequency can be configured. (Refer to p.13 Fig.40)

• slope

This block generates saw tooth waves from the clock generated by the OSC. The generated saw tooth waves are sent to PWM COMPARATOR.

• PWM COMPARATOR

The PWM COMPARATOR block is a comparator to make comparison between the FB pin and internal saw tooth wave and output a switching pulse.

The switching pulse duty varies with the FB value.

min Duty width : 250ns(BD9006F/HFP,BD9007HFP)

min Duty width : 360ns(BD9009HFP)

• TSD (Thermal Shut Down)

In order to prevent thermal destruction/thermal runaway of the IC, the TSD block will turn OFF the output when the chip temperature reaches approximately 150°C or more. When the chip temperature falls to a specified level, the output will be reset. However, since the TSD is designed to protect the IC, the chip junction temperature should be provided with the thermal shutdown detection temperature of less than approximately 150°C.

• CURRENT LIMIT

While the output POWER P-ch MOS FET is ON, if the voltage between drain and source (ON resistance \times load current) exceeds the reference voltage internally set with the IC, this block will turn OFF the output to latch. The overcurrent protection detection values have been set as shown below:

BD9009/HFP . . . 7A (Typ.)

BD9006F/HFP, BD9007F/HFP . . . 4A (Typ.)

Furthermore, since BD9006F/HFP,BD9007F/HFP overcurrent protection is an automatically reset, after the output is turned OFF and latched, the latch will be reset with the RESET signal output by each oscillation frequency.

When BD9009HFP over current protection circuit operates, output is turned off immediately, and then this IC restart to operate after 4096/fosc sec.

However, this protection circuit is only effective in preventing destruction from sudden accident. It does not support for the continuous operation of the protection circuit (e.g. if a load, which significantly exceeds the output current capacitance, is normally connected). Furthermore, since the overcurrent protection detection value has negative temperature characteristics, consider thermal design.

● Timing Chart

(All series)

• Basic Operation

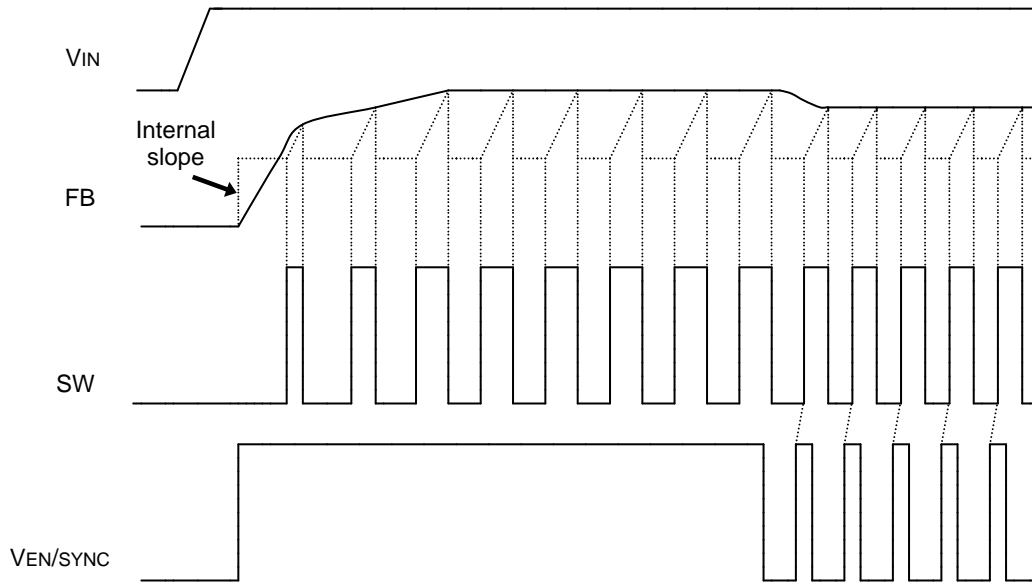


Fig.33

• Over Current Protection Operation

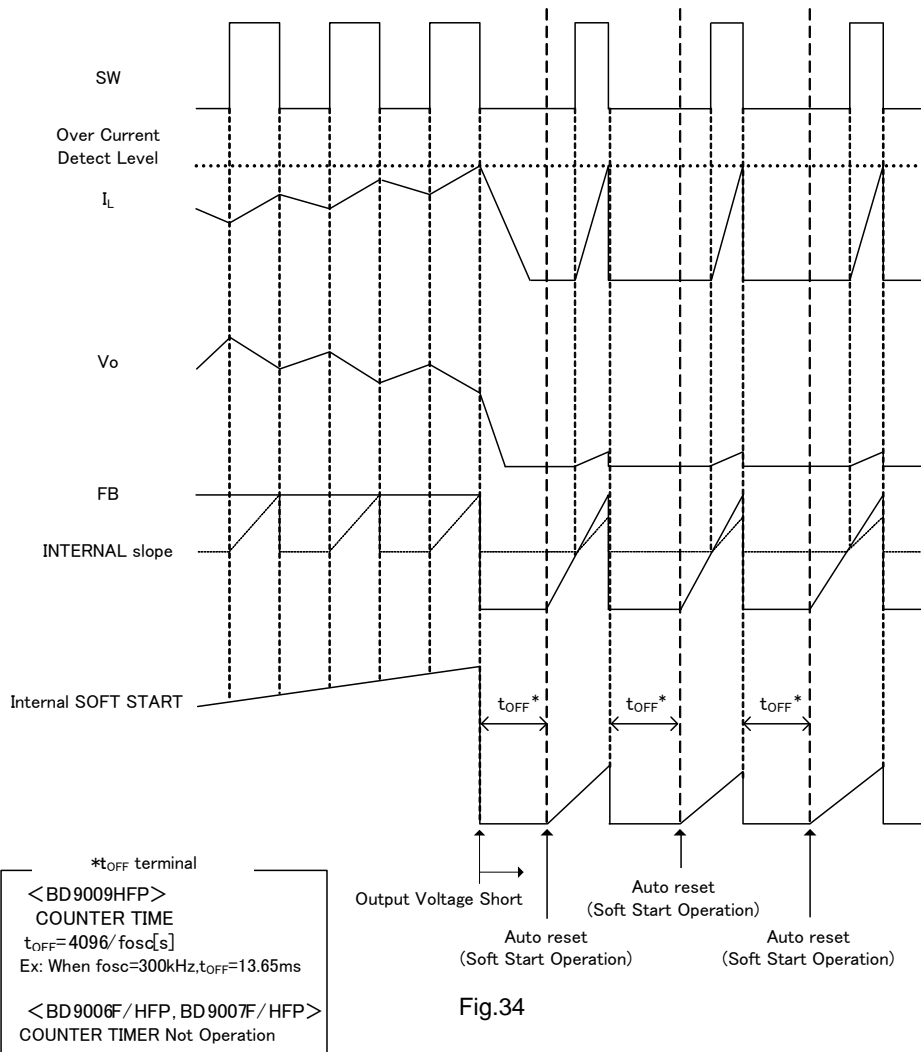


Fig.34

● External synchronizing function

In order to activate the external synchronizing function, connect the frequency setting resistor to the RT pin and then input a synchronizing signal to the EN/SYNC pin. As the synchronizing signal, input a pulse wave higher than a frequency determined with the setting resistor (RT).

However, the external sync frequency should be configured at less than double the configured frequency.

(ex.) When the configured frequency is 100kHz, the external sync frequency should be less than 200kHz.

Furthermore, the pulse wave's LOW voltage should be under 0.8V and the HIGH voltage over 2.6V (when the HIGH voltage is over 6V the EN/SYNC input current increases [see p.4 Fig.8]), the through rate of stand-up (and stand-down) under $20V/\mu S$.

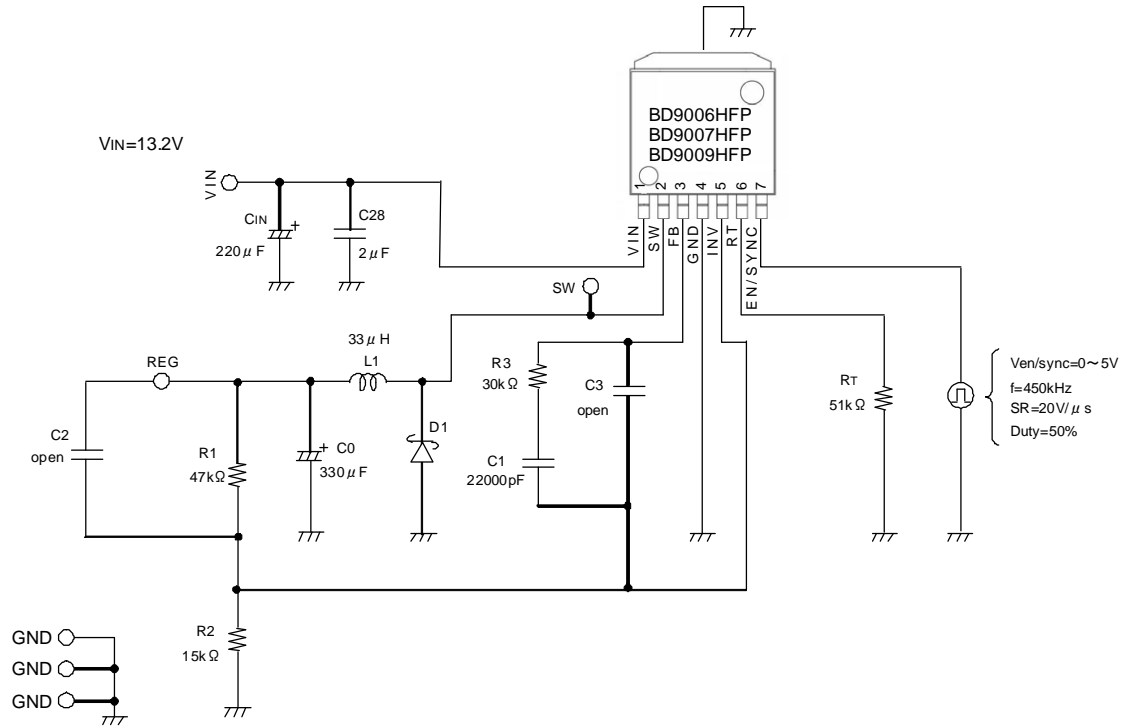


Fig.35 External Sync Sample Circuit
($V_o=3.3V$, $I_o=1A$, $f=300kHz$, EN/SYNC=450kHz)

●Description of external components

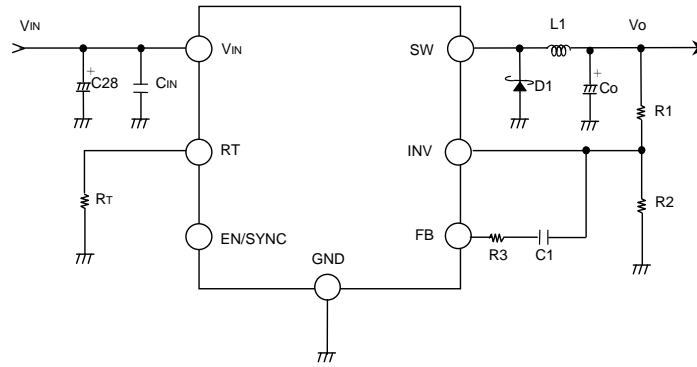


Fig.36

Design Procedure	Sample Calculations
<p>Vo=Output voltage, VIN (Max.)=Maximum input voltage Io (Max.)=Maximum load current, f=Oscillation frequency</p>	<p>When Vo=3.3V, VIN (Typ.)=13.2V Io(Max.)=1A and f=300kHz</p>
<p>1. Setting or output voltage Output voltage can be obtained by the formula shown below:</p> $Vo=0.8 \times (1+R1/R2)$ <p>Use the formula to select the R1 and R2. Furthermore, set the R2 to 30kΩ or less. Select the current passing through the R1 and R2 to be small enough for the output current.</p>	<p>When Vo=3.3V and R2=15kΩ</p> $3.3=0.8 \times (1+R1/15k\Omega)$ $R1=46.875k\Omega \approx 47k\Omega$ <p style="text-align: right;"><u>R1=47kΩ</u></p>
<p>2. Selection of coil (L1) The value of the coil can be obtained by the formula shown below:</p> $L1=(VIN-Vo) \times Vo / (VIN \times f \times \Delta Io)$ <p>ΔIo: Output ripple current ΔIo should typically be approximately 20 to 30% of Io.</p> <p>If this coil is not set to the optimum value, normal (continuous) Oscillation may not be achieved. Furthermore, set the value of the coil with an adequate margin so that the peak current passing through the coil will not exceed the rated current of the coil.</p>	<p>When VIN=13.2V, Vo=3.3V, Io=1A and f=300kHz, L1=(13.2-3.3) × 3.3 / {13.2 × 300k × (1 × 0.3)} =27.5μH ≈ 33μH</p> <p style="text-align: right;"><u>L1=33μH</u></p>
<p>3. Selection of output capacitor (Co) The output capacitor can be determined according to the output ripple voltage ΔVo(p-p) required. Obtain the required ESR value by the formula shown below and then select the capacitance.</p> $\Delta IL=(VIN-Vo) \times Vo / (L \times f \times VIN)$ $\Delta Vpp=\Delta IL \times ESR+(\Delta IL \times Vo) / (2 \times Co \times f \times VIN)$ <p>Set the rating of the capacitor with an adequate margin to the output voltage. Also, set the maximum allowable ripple current with an adequate margin to ΔIL. Furthermore, the output rise time should be shorter than the soft start time. Select the output capacitor having a value smaller than that obtained by the formula shown below.</p> $C_{MAX} = \frac{3.0m \times (I_{LIMIT}-I_o(Max))}{V_o}$ <p>I_{LIMIT} : 2A (BD9006F/HFP, BD9007F/HFP),4A (BD9009HFP) If this capacitances is not optimum, faulty startup may result.</p> <p>(※3.0m is soft start time(min).)</p>	<p>VIN=13.2V, Vo=3.3V, L=33μH, f=300kHz ΔIL=(13.2-3.3) × 3.3 / (33 × 10⁻⁶ × 300 × 10³ × 13.2) =0.25</p> <p style="text-align: right;"><u>ΔIL=0.25A</u></p> <p>When I_{LIMIT}: 2A, Io(Max)=1A, Vo=3.3V</p> $C_{MAX} = 3.0m \times (2-1) / 3.3$ $\approx 910\mu$ <p style="text-align: right;"><u>C_{MAX}=910μF</u></p>

Design Method	Sample Calculations
<p>4. Selection of diode (D1) Set diode rating with an adequate margin to the maximum load current. Also, make setting of the rated inverse voltage with an adequate margin to the maximum input voltage.</p> <p>A diode with a low forward voltage and short reverse recovery time will provide high efficiency.</p>	<p>When $V_{IN(max.)}=35V$ $I_{o(max.)}=2A$</p> <p>Diode ratings must include: Current over 2A Withstand minimum 35V</p>
<p>5. Selection of input capacitor (C_{IN}, C28) Two capacitors, ceramic capacitor C_{IN} and bypass capacitor C28 should be inserted between the V_{IN} and GND. Be sure to insert a ceramic capacitor of 2 to 10μF for the C_{IN}. The capacitor C28 should have a low ESR and a significantly large ripple current. The ripple current I_{RMS} can be obtained by the following formula:</p> $I_{RMS}=I_o \times \sqrt{V_o \times (V_{IN}-V_o)/V_{IN}^2}$ <p>Select capacitors that can accept this ripple current. If the capacitance of C_{IN} and C28 is not optimum, the IC may malfunction.</p>	<p>When $V_{IN}=13.2V$, $V_o=3.3V$ and $I_o=1A$:</p> $I_{RMS}=1 \times \sqrt{3.3 \times (13.2-3.3)/(13.2)^2}$ <p style="text-align: right;"><u>$I_{RMS}=0.433A$</u></p>
<p>6. Setting of oscillating frequency Referring Fig.40 on the following page, select R for the oscillating frequency to be used.</p>	<p>When $f=300kHz$ From p.13 Fig.40, a resistance of $R_T=51k\Omega$ is selected. <u>$R_T=51k\Omega$</u></p>
<p>7. Setting of phase compensation (R3 and C1) The phase margin can be set through inserting a capacitor or a capacitor and resistor between the INV pin and the FB pin. Each set value varies with the output coil, capacitance, I/O voltage, and load. Therefore, set the phase compensation to the optimum value according to these conditions. (For details, refer to Application circuit on page.13~) If this setting is not optimum, output oscillation may result.</p>	<p>※Please contact us if there are any questions regarding phase compensation configuration.</p>

※The set values listed above are all reference values. On the actual mounting of the IC, the characteristics may vary with the routing of wirings and the types of parts in use. In the connection, it is recommended to thoroughly verify these values on the actual system prior to use.

●Directions for pattern layout of PCB

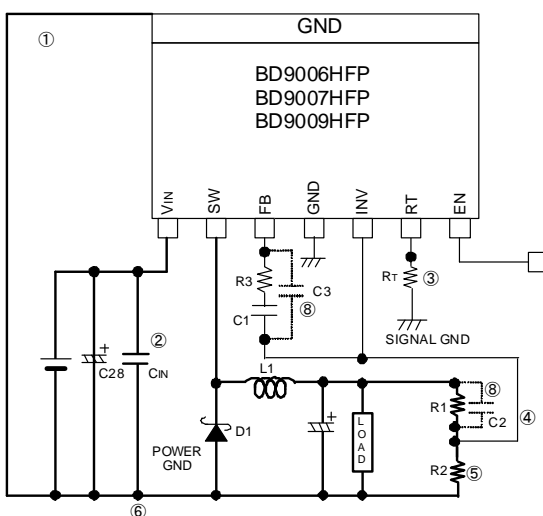


Fig.37

- ① Arrange the wirings shown by heavy lines as short as possible in a broad pattern.
- ② Locate the input ceramic capacitor C_{IN} as close to the V_{IN}-GND pin as possible.
- ③ Locate the R_T as close to the GND pin as possible.
- ④ Locate the R1 and R2 as close to the INV pin as possible, and provide the shortest wiring from the R1 and R2 to the INV pin.
- ⑤ Locate the R1 and R2 as far away from the L1 as possible.
- ⑥ Separate POWER GND (Schottky diode, I/O capacitor's GND) and SIGNAL GND (R_T, GND), so that SW noise doesn't have an effect on SIGNAL GND at all.
- ⑦ Design the POWER wire line as wide and short as possible.
- ⑧ Additional pattern for C2 and C3 expand compensation flexibility.

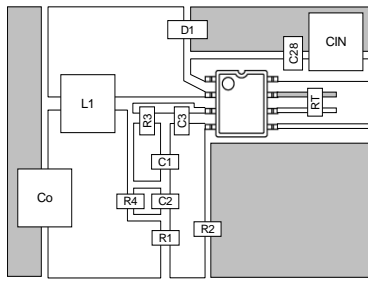


Fig.38 BD9006F, BD9007F Reference Layout Pattern

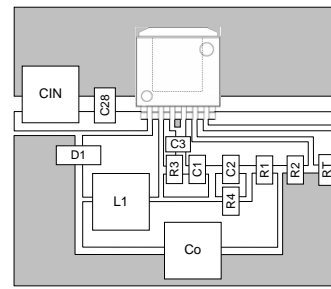


Fig.39 BD9006HFP, BD9007HFP, BD9009HFP Reference Layout Pattern

※As shown above, design the GND pattern as large as possible within inner layer.
 ※Gray zones indicate GND.

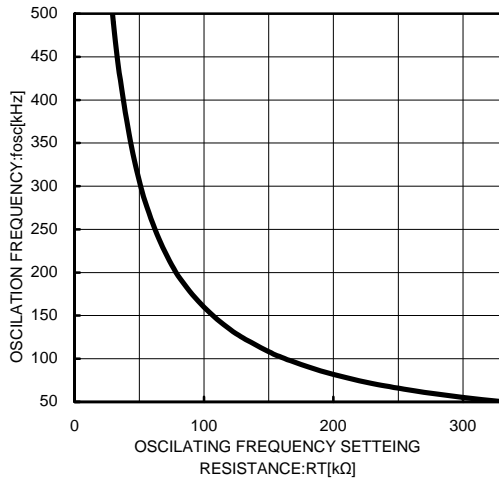


Fig.40 RT Resistance Values vs. Oscillating Frequency

RT[kΩ]	fosc[kHz]	RT[kΩ]	fosc[kHz]
27	537	100	160
30	489	110	146
33	449	120	134
36	415	130	124
39	386	150	108
43	353	160	102
47	324	180	91
51	300	200	82
56	275	220	75
62	250	240	69
68	229	270	61
75	209	300	55
82	192	330	50
91	174	360	46

※The values in the graph for oscillating frequency are Typical values, and variance of ±5% for BD9006F/HFP, BD9009HFP and ±20% for BD9007F/HFP should be considered.

●Phase Compensation setting procedure

1. Application stability conditions

The following section describes the stability conditions of the negative feedback system.

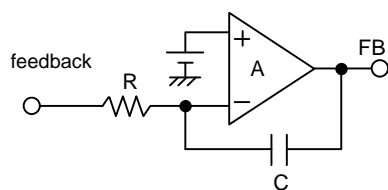
Since the DC/DC converter application is sampled according to the switching frequency, GBW (frequency at 0-dB gain) of the overall system should be set to 1/10 or less of the switching frequency. The following section summarizes the targeted characteristics of this application.

- At a 1 (0-dB) gain, the phase delay is 150° or less (i.e. the phase margin is 30° or more).
- The GBW for this occasion is 1/10 or less of the switching frequency.

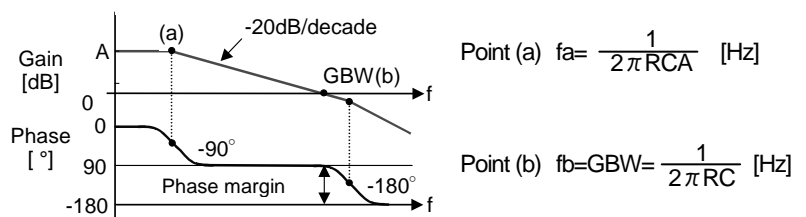
Responsiveness is determined with restrictions on the GBW. To improve responsiveness, higher switching frequency should be provided.

Replace a secondary phase delay (-180°) with a secondary phase lead by inserting two-phase leads, to ensure the stability through the phase compensation. Furthermore, the GBW (i.e., frequency at 0-dB gain) is determined according to phase compensation capacitance provided for the error amplifier. Consequently, in order to reduce the GBW, increase the capacitance value.

(1) Typical integrator (low pass filter)



(2) Open loop characteristics of integrator

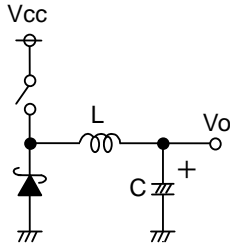


Since the error amplifier is provided with (1) or (2) phase compensation, the low pass filter is applied. In the case of the DC/DC converter application, the R becomes a parallel resistance of the feedback resistance.

2. For output capacitors having high ESR, such as electrolyte capacitor

For output capacitors that have high ESR (i.e., several Ω), the phase compensation setting procedure becomes comparatively simple. Since the DC/DC converter application has a LC resonant circuit attached to the output, a -180° phase-delay occurs in that area. If ESR component is present, however a +90° phase-lead occurs to shift the phase delay to -90°. Since the phase delay should be set within 150°, it is a very effective method but tends to increase the ripple component of the output voltage.

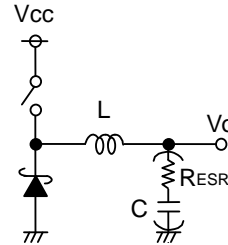
(1) LC resonant circuit



$$f_r = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]}$$

At this resonance point, a -180° phase-delay occurs.

(2) With ESR provided



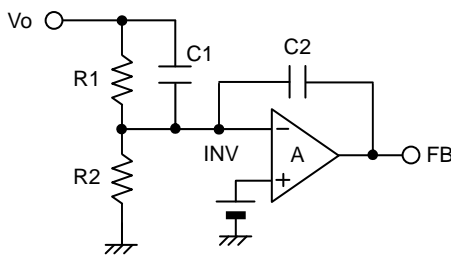
$$f_r = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]: Resonance}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR}C} \text{ [Hz]: Phase lead}$$

A -90° phase-delay occurs.

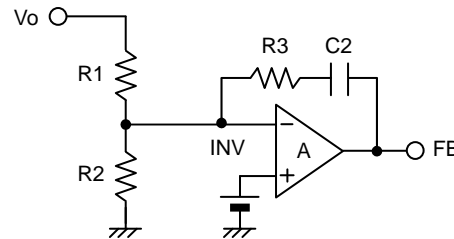
According to changes in phase characteristics, due to the ESR, only one phase lead should be inserted. For this phase lead, select either of the methods shows below:

(3) Insert Feedback Resistance in the C.



$$\text{Phase lead } f_z = \frac{1}{2\pi C1R1} \text{ [Hz]}$$

(4) Insert the R3 in integrator.



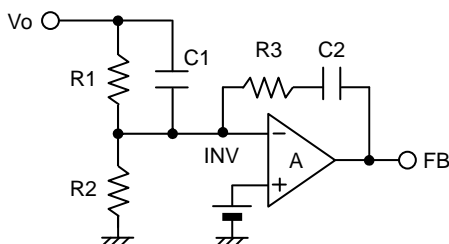
$$\text{Phase lead } f_z = \frac{1}{2\pi C2R3} \text{ [Hz]}$$

To cancel the LC resonance, the frequency to insert the phase lead should be set close to the LC resonant frequency. The setting above have is estimated. Consequently, the setting may be adjusted on the actual system. Furthermore, since these characteristics vary with the layout of PCB loading conditions, precise calculations should be made on the actual system.

3. For output capacitors having low ESR, such as low impedance electrolyte capacitor or OS-CON

In order to use capacitors with low ESR (i.e., several tens of mΩ), two phase-leads should be inserted so that a -180° phase-delay, due to LC resonance, will be compensated. The following section shows a typical phase compensation procedure.

(1) Phase compensation with secondary phase lead



$$\text{Phase lead : } f_{z1} = \frac{1}{2\pi R1C1} \text{ [Hz]}$$

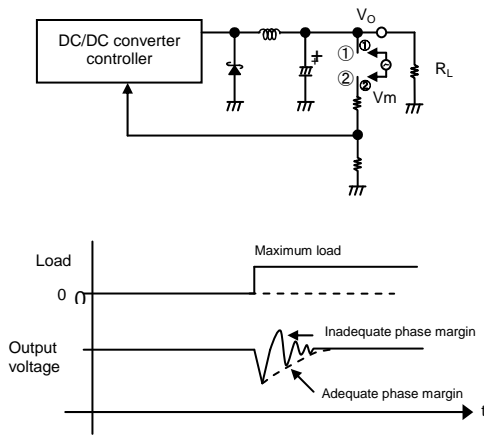
$$\text{Phase lead : } f_{z2} = \frac{1}{2\pi R3C2} \text{ [Hz]}$$

$$\text{LC resonant : } f_r = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]}$$

To set phase lead frequency, insert both of the phase leads close to the LC resonant frequency. According to empirical rule, setting the phase lead frequency fZ2 with R3 and C2 lower than the LC resonant frequency fr, and the phase lead frequency fZ1 with the R1 and C1 higher than the LC resonant frequency fr, will provide stable application conditions.

<Reference> Measurement of open loop of the DC/DC converter

To measure the open loop of the DC/DC converter, use the gain phase analyzer or FRA to measure the frequency characteristics.



<Procedure>

1. Check to ensure output causes no oscillation at the maximum load in closed loop.
2. Isolate ① and ② and insert \$V_m\$ (with amplitude of approximately 100mVpp).
3. Measure (probe) the oscillation of ① to that of ②.

Furthermore, the phase margin can also be measured with the load responsiveness. Measure variations in the output voltage when instantaneously changing the load from no load to the maximum load. Even though ringing phenomenon is caused, due to low phase margin, no ringing takes place. Phase margin is provided. However, no specific phase margin can be probed.

※Please contact us if you have any questions regarding phase compensation.

●Heat Loss

For thermal design, be sure to operate the IC within the following conditions.

(Since the temperatures described hereunder are all guaranteed temperature, take margin into account.)

1. The ambient temperature \$T_a\$ is to be 105°C or less.
2. The chip junction temperature \$T_j\$ is to be 150°C or less.

The chip junction temperature \$T_j\$ can be considered in the following two patterns:

To obtain \$T_j\$ from the IC surface temperature \$T_c\$ in actual use state,
 $T_j = T_c + \theta_j - c \times W$

< Reference value > $\theta_j - c$: HRP7 7°C/W
 SOP8 32.5°C/W

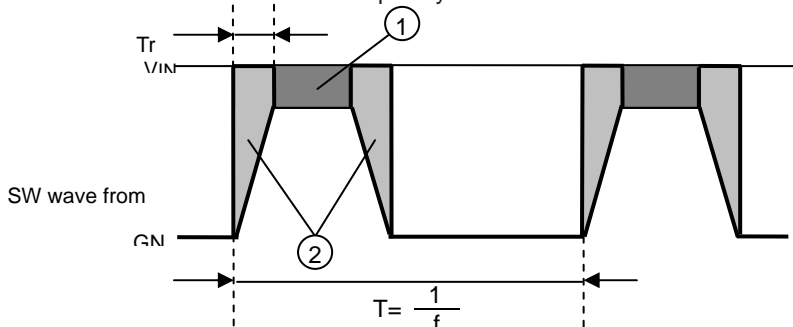
To obtain \$T_j\$ from the ambient temperature \$T_a\$
 $T_j = T_a + \theta_j - a \times W$

< Reference. value > $\theta_j - a$: HRP7 89.3°C/W Single piece of IC
 54.3°C/W 2-layer PCB (Copper foil area on the front side of PCB: 15×15mm²)
 22.7°C/W 2-layer PCB (Copper foil area on the front side of PCB: 70×70mm²)
 PCB size: 70×70×1.6mm³
 (PCB incorporates thermal via.)
 Copper foil area on the front side of PCB: 10.5×10.5mm²
 SOP8 222.2°C/W Single piece of IC
 181.8°C/W 1-layer PCB
 PCB size: 70×70×1.6mm³

The heat loss \$W\$ of the IC can be obtained by the formula shown below:

$$W = R_{on} \times I_o^2 \times \frac{V_o}{V_{IN}} + V_{IN} \times I_{CC} + T_r \times V_{IN} \times I_o \times f$$

\$R_{on}\$: ON resistance of IC (refer to page.4,5) \$I_o\$: Load current
 \$V_o\$: Output voltage \$V_{IN}\$: Input voltage \$I_{CC}\$: Circuit current (refer to page.2,3)
 \$T_r\$: Switching rise/fall time (approximately 20nsec)
 \$f\$: Oscillation frequency



$$\begin{aligned} \text{① } & R_{on} \times I_o^2 \\ \text{② } & 2 \times \frac{1}{2} \times T_r \times \frac{1}{T} \times V_{IN} \times I_o \\ & = T_r \times V_{IN} \times I_o \times f \end{aligned}$$

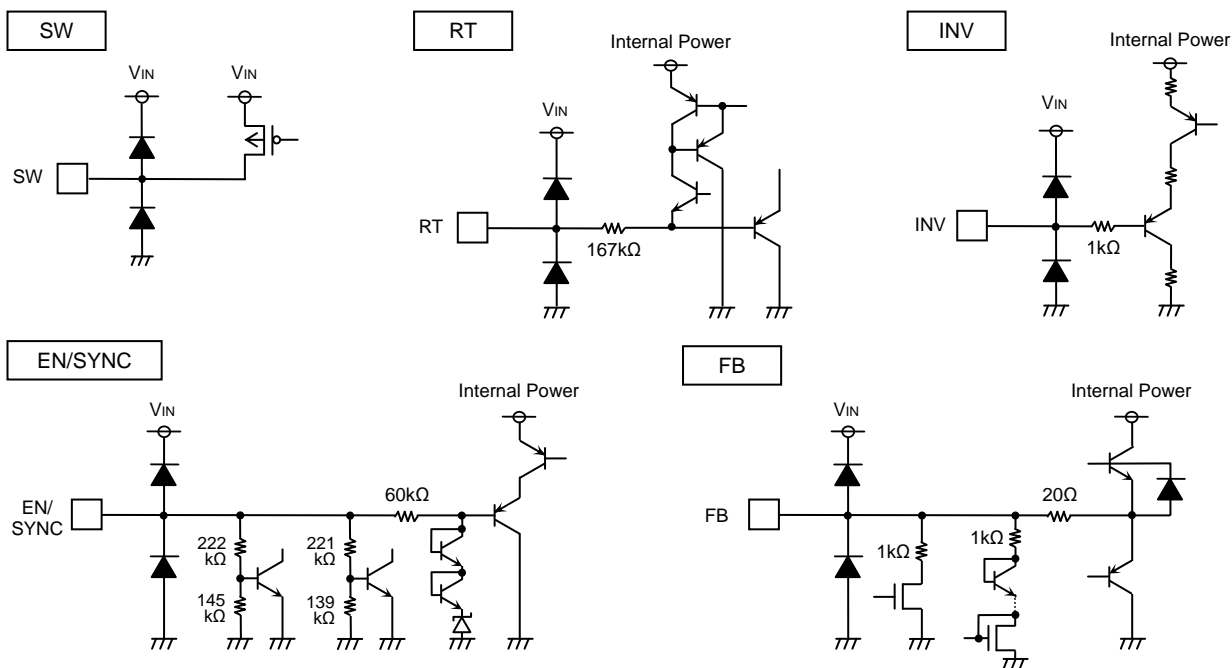


Fig.41 Equivalent circuit

●Cautions on use

1. Absolute maximum ratings

If excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. GND potential

Ground-GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals should be lower than the GND potential voltage including electric transients.

3. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4. Inter-pin shorts and mounting errors

When attaching to the set substrate, pay special attention to the direction and proper placement of the IC. If the IC is attached incorrectly, it may be destroyed.

Furthermore, when using the IC with VIN and EN/SYNC terminals shorted, and the 5-pin (SOP8 package) or 7-pin (HRP7 package) EN/SYNC terminal and 6-pin RT terminal are shorted, the IC may also be damaged when VIN>7V.

5. Operation in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6. Inspection with set printed circuit board

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

7. IC pin input (Fig. 42)

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

- When GND>pin A and GND>pin B, the P-N junction operates as a parasitic diode.
- When pin B >GND>pin A, the P-N junction operates as a parasitic transistor. Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

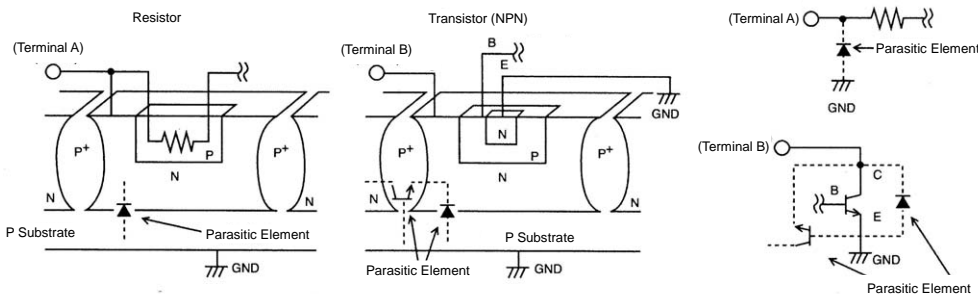


Fig.42 Typical simple construction of monolithic IC

8. GND wiring pattern

It is recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB, so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause on fluctuations in voltages of the small-signal GND. Prevent fluctuations in the GND wiring pattern of external parts.

9. Temperature protection (thermal shut down) circuit

This IC has a built-in temperature protection circuit to prevent the thermal destruction of the IC. As described above, be sure to use this IC within the power dissipation range. Should a condition exceeding the power dissipation range continue, the chip temperature T_j will rise to activate the temperature protection circuit, thus turning OFF the output power element. Then, when the tip temperature T_j falls, the circuit will be automatically reset. Furthermore, if the temperature protection circuit is activated under the condition exceeding the absolute maximum ratings, do not attempt to use the temperature protection circuit for set design.

10. On the application shown below, if there is a mode in which V_{IN} and each pin potential are inverted, for example, if the V_{IN} is short-circuited to the Ground with external diode charged, internal circuits may be damaged. To avoid damage, it is recommended to insert a backflow prevention diode in the series with V_{IN} or a bypass diode between each pin and V_{IN} .

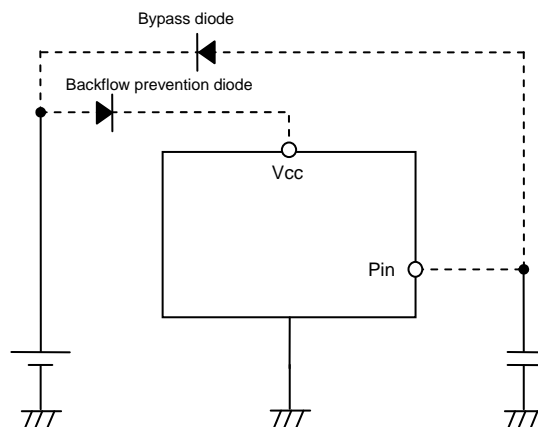
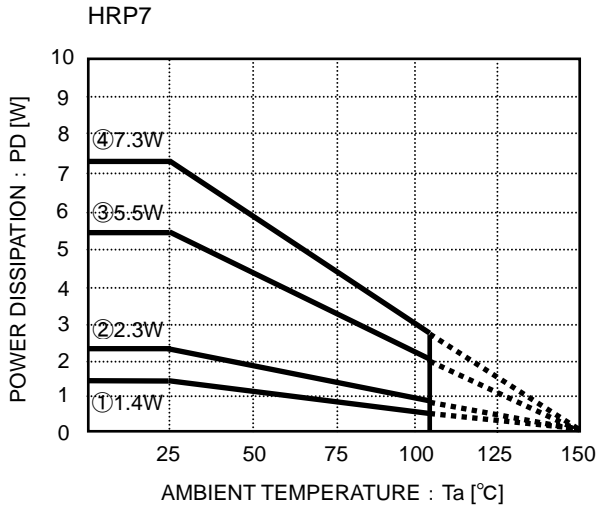


Fig.43

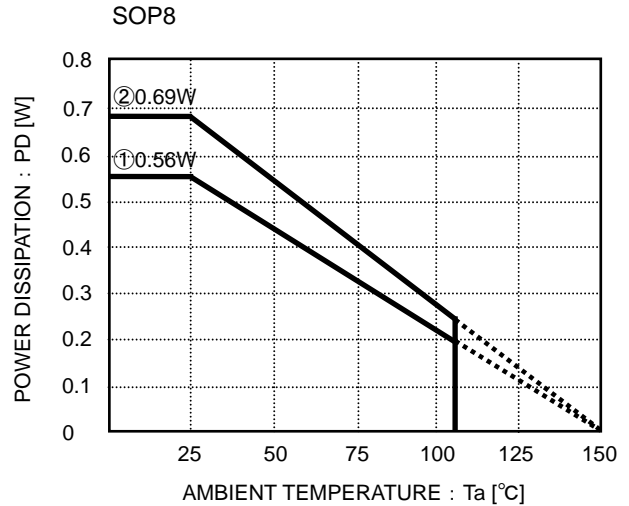
11. This IC is designed that over current protection circuit operates at start up and normal operation. Therefore at start up when this IC's total load current (sum of load current and charge current to output capacitor) is exceeded 2A(BD9006F/HFP,BD9007F/HFP Minimum load current ability) ,4A(BD9009HFP Minimum load current ability), over current protection circuit operates, and this IC's start up times are excessive time.If this case is occurred, output capacitor is recommended to change small value.
12. When this IC starts up with output-GND short, SW output current is exceeded 2A(BD9006F/HFP,BD9007F/HFP) , 4A(BD9009HFP), and this IC may be destroyed. When VIN input voltage is under 7V with output-GND short, over current protection may don't operates.Please don't use this IC in these cases.

● Thermal reduction characteristics



- ① Single piece of IC
PCB Size: 70x70x1.6mm³ (PCB incorporates thermal via)
Copper foil area on the front side of PCB: 10.5x10.5mm²
- ② 2-layer PCB (Copper foil area on the reverse side of PCB: 15x15mm²)
- ③ 2-layer PCB (Copper foil area on the reverse side of PCB: 70x70mm²)
- ④ 4-layer PCB (Copper foil area on the reverse side of PCB: 70x70mm²)

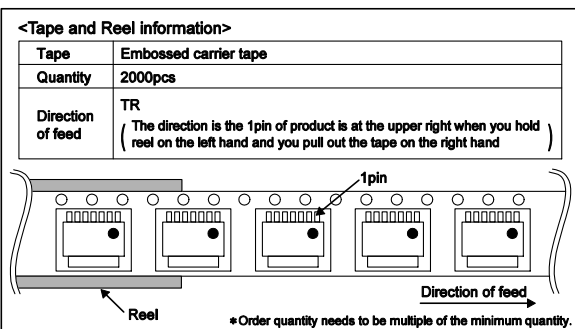
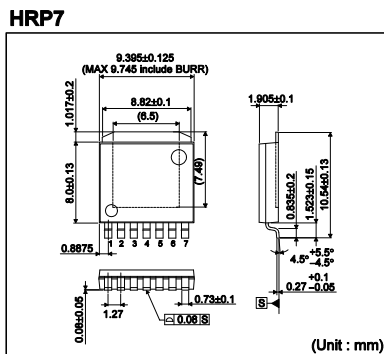
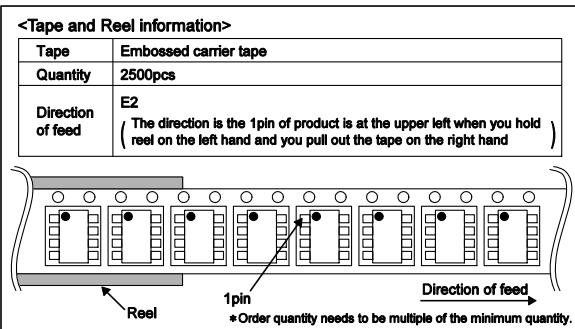
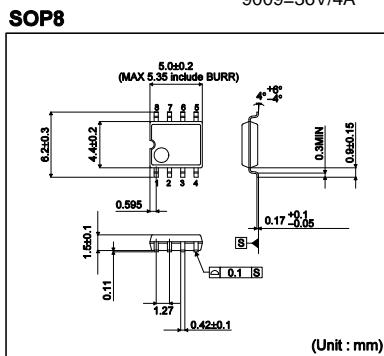
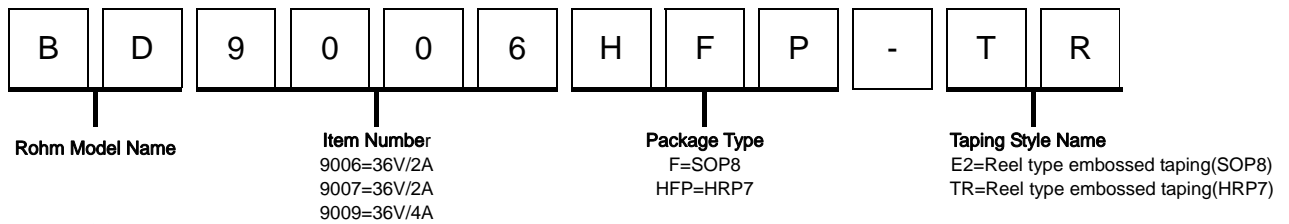
Fig.44



- ① Single piece of IC
- ② When mounted on ROHM standard PCB
(Glass epoxy PCB of 70mmx70mmx1.6mm)

Fig.45

● Ordering Name Selection



ご注意

ローム製品取扱い上の注意事項

1. 本製品は一般的な電子機器（AV 機器、OA 機器、通信機器、家電製品、アミューズメント機器等）への使用を意図して設計・製造されております。従いまして、極めて高度な信頼性が要求され、その故障や誤動作が人の生命、身体への危険若しくは損害、又はその他の重大な損害の発生に関わるような機器又は装置（医療機器^(Note 1)、輸送機器、交通機器、航空宇宙機器、原子力制御装置、燃料制御、カーアクセサリを含む車載機器、各種安全装置等）（以下「特定用途」という）への本製品のご使用を検討される際は事前にローム営業窓口までご相談くださいますようお願い致します。ロームの文書による事前の承諾を得ることなく、特定用途に本製品を使用したことによりお客様又は第三者に生じた損害等に関し、ロームは一切その責任を負いません。

(Note 1) 特定用途となる医療機器分類

日本	USA	EU	中国
CLASS III	CLASS III	CLASS II b	Ⅲ類
CLASS IV		CLASS III	

2. 半導体製品は一定の確率で誤動作や故障が生じる場合があります。万が一、かかる誤動作や故障が生じた場合であっても、本製品の不具合により、人の生命、身体、財産への危険又は損害が生じないように、お客様の責任において次の例に示すようなフェールセーフ設計など安全対策をお願い致します。
 - ①保護回路及び保護装置を設けてシステムとしての安全性を確保する。
 - ②冗長回路等を設けて単一故障では危険が生じないようにシステムとしての安全を確保する。
3. 本製品は、一般的な電子機器に標準的な用途で使用されることを意図して設計・製造されており、下記に例示するような特殊環境での使用を配慮した設計はなされておられません。従いまして、下記のような特殊環境での本製品のご使用に関し、ロームは一切その責任を負いません。本製品を下記のような特殊環境でご使用される際は、お客様におかれまして十分に性能、信頼性等をご確認ください。
 - ①水・油・薬液・有機溶剤等の液体中でのご使用
 - ②直射日光・屋外暴露、塵埃中でのご使用
 - ③潮風、Cl₂、H₂S、NH₃、SO₂、NO₂等の腐食性ガスの多い場所でのご使用
 - ④静電気や電磁波の強い環境でのご使用
 - ⑤発熱部品に近接した取付け及び当製品に近接してビニール配線等、可燃物を配置する場合。
 - ⑥本製品を樹脂等で封止、コーティングしてのご使用。
 - ⑦はんだ付けの後に洗浄を行わない場合(無洗浄タイプのフラックスを使用された場合も、残渣の洗浄は確実にを行うことをお勧め致します)、又ははんだ付け後のフラックス洗浄に水又は水溶性洗浄剤をご使用の場合。
 - ⑧本製品が結露するような場所でのご使用。
4. 本製品は耐放射線設計はなされておられません。
5. 本製品単体品の評価では予測できない症状・事態を確認するためにも、本製品のご使用にあたってはお客様製品に実装された状態での評価及び確認をお願い致します。
6. パルス等の過渡的な負荷（短時間での大きな負荷）が加わる場合は、お客様製品に本製品を実装した状態で必ずその評価及び確認の実施をお願い致します。また、定常時での負荷条件において定格電力以上の負荷を印加されますと、本製品の性能又は信頼性が損なわれるおそれがあるため必ず定格電力以下でご使用ください。
7. 許容損失(Pd)は周囲温度(Ta)に合わせてディレーティングしてください。また、密閉された環境下でご使用の場合は、必ず温度測定を行い、ディレーティングカーブ範囲内であることをご確認ください。
8. 使用温度は納入仕様書に記載の温度範囲内であることをご確認ください。
9. 本資料の記載内容を逸脱して本製品をご使用されたことによって生じた不具合、故障及び事故に関し、ロームは一切その責任を負いません。

実装及び基板設計上の注意事項

1. ハロゲン系（塩素系、臭素系等）の活性度の高いフラックスを使用する場合、フラックスの残渣により本製品の性能又は信頼性への影響が考えられますので、事前にお客様にてご確認ください。
2. はんだ付けはリフローはんだを原則とさせていただきます。なお、フロー方法でのご使用につきましては別途ロームまでお問い合わせください。
詳細な実装及び基板設計上の注意事項につきましては別途、ロームの実装仕様書をご確認ください。

応用回路、外付け回路等に関する注意事項

1. 本製品の外付け回路定数を変更してご使用になる際は静特性のみならず、過渡特性も含め外付け部品及び本製品のバラツキ等を考慮して十分なマージンをみて決定してください。
2. 本資料に記載された応用回路例やその定数などの情報は、本製品の標準的な動作や使い方を説明するためのもので、実際に使用する機器での動作を保証するものではありません。従いまして、お客様の機器の設計において、回路やその定数及びこれらに関連する情報を使用する場合には、外部諸条件を考慮し、お客様の判断と責任において行ってください。これらの使用に起因しお客様又は第三者に生じた損害に関し、ロームは一切その責任を負いません。

静電気に対する注意事項

本製品は静電気に対して敏感な製品であり、静電放電等により破壊することがあります。取り扱い時や工程での実装時、保管時において静電気対策を実施の上、絶対最大定格以上の過電圧等が印加されないようにご使用ください。特に乾燥環境下では静電気が発生しやすくなるため、十分な静電対策を実施ください。(人体及び設備のアース、帯電物からの隔離、イオナイザの設置、摩擦防止、温湿度管理、はんだごてのこて先のアース等)

保管・運搬上の注意事項

1. 本製品を下記の環境又は条件で保管されますと性能劣化やはんだ付け性等の性能に影響を与えるおそれがありますのでこのような環境及び条件での保管は避けてください。
 - ①潮風、Cl₂、H₂S、NH₃、SO₂、NO₂等の腐食性ガスの多い場所での保管
 - ②推奨温度、湿度以外での保管
 - ③直射日光や結露する場所での保管
 - ④強い静電気が発生している場所での保管
2. ロームの推奨保管条件下におきましても、推奨保管期限を経過した製品は、はんだ付け性に影響を与える可能性があります。推奨保管期限を経過した製品は、はんだ付け性を確認した上でご使用頂くことを推奨します。
3. 本製品の運搬、保管の際は梱包箱を正しい向き（梱包箱に表示されている天面方向）で取り扱ってください。天面方向が遵守されずに梱包箱を落下させた場合、製品端子に過度なストレスが印加され、端子曲がり等の不具合が発生する危険があります。
4. 防湿梱包を開封した後は、規定時間内にご使用ください。規定時間を経過した場合はベーク処置を行った上でご使用ください。

製品ラベルに関する注意事項

本製品に貼付されている製品ラベルにQRコードが印字されていますが、QRコードはロームの社内管理のみを目的としたものです。

製品廃棄上の注意事項

本製品を廃棄する際は、専門の産業廃棄物処理業者にて、適切な処置をしてください。

外国為替及び外国貿易法に関する注意事項

本製品は外国為替及び外国貿易法に定める規制貨物等に該当するおそれがありますので輸出する場合には、ロームにお問い合わせください。

知的財産権に関する注意事項

1. 本資料に記載された本製品に関する応用回路例、情報及び諸データは、あくまでも一例を示すものであり、これらに関する第三者の知的財産権及びその他の権利について権利侵害がないことを保証するものではありません。従いまして、上記第三者の知的財産権侵害の責任、及び本製品の使用により発生するその他の責任に関し、ロームは一切その責任を負いません。
2. ロームは、本製品又は本資料に記載された情報について、ローム若しくは第三者が所有又は管理している知的財産権その他の権利の実施又は利用を、明示的にも黙示的にも、お客様に許諾するものではありません。

その他の注意事項

1. 本資料の全部又は一部をロームの文書による事前の承諾を得ることなく転載又は複製することを固くお断り致します。
2. 本製品をロームの文書による事前の承諾を得ることなく、分解、改造、改変、複製等しないでください。
3. 本製品又は本資料に記載された技術情報を、大量破壊兵器の開発等の目的、軍事利用、あるいはその他軍用用途目的で使用しないでください。
4. 本資料に記載されている社名及び製品名等の固有名詞は、ローム、ローム関係会社若しくは第三者の商標又は登録商標です。

一般的な注意事項

1. 本製品をご使用になる前に、本資料をよく読み、その内容を十分に理解されるようお願い致します。本資料に記載される注意事項に反して本製品をご使用されたことによって生じた不具合、故障及び事故に関し、ロームは一切その責任を負いませんのでご注意願います。
2. 本資料に記載の内容は、本資料発行時点のものであり、予告なく変更することがあります。本製品のご購入及びご使用に際しては、事前にローム営業窓口で最新の情報をご確認ください。
3. ロームは本資料に記載されている情報は誤りがないことを保証するものではありません。万が一、本資料に記載された情報の誤りによりお客様又は第三者に損害が生じた場合においても、ロームは一切その責任を負いません。

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