CY23EP09

2.5 V or 3.3 V, 10 MHz–220 MHz, Low Jitter, Nine-Output Zero Delay Buffer

Features

- 10 MHz to 220 MHz maximum operating range
- Zero input-output propagation delay, adjustable by loading on CLKOUT pin
- Multiple low-skew outputs
  - 45 ps typical output-output skew
  - One input drives nine outputs, grouped as 4 + 4 + 1
- 25 ps typical cycle-to-cycle jitter
- 15 ps typical period jitter
- Standard and High drive strength options
- Available in space-saving 16-pin 150-mil small outline integrated circuit (SOIC) or 4.4 mm thin shrunk small outline package (TSSOP) packages
- 3.3 V or 2.5 V operation
- Industrial temperature available

Functional Description

The CY23EP09 is a 2.5 V or 3.3 V zero delay buffer designed to distribute high-speed clocks and is available in a 16-pin SOIC or TSSOP package. The -1H version operates up to 220 (200) MHz frequencies at 3.3 V (2.5 V), and has higher drive than the -1 devices. All parts have on-chip PLLs that lock to an input clock on the REF pin. The phase-locked loop (PLL) feedback is on-chip and is obtained from the CLKOUT pad.

There are two banks of four outputs each, which can be controlled by the Select inputs as shown in the Select Input Decoding on page 4. If all output clocks are not required, BankB can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

The PLL enters a power-down mode when there are no rising edges on the REF input (less than ~2 MHz). In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 25 μA of current draw.

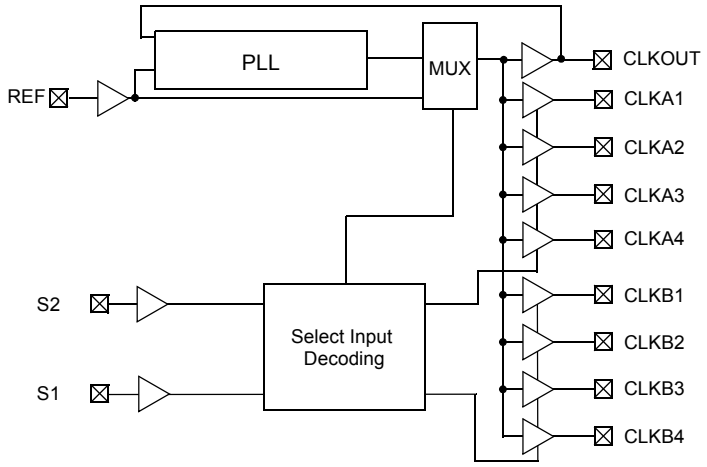
In the special case when S2:S1 is 1:0, the PLL is bypassed and REF is output from DC to the maximum allowable frequency. The part behaves like a non-zero delay buffer in this mode, and the outputs are not tri-stated.

The CY23EP09 is available in different configurations, as shown in the Ordering Information table. The CY23EP09-1 is the base part. The CY23EP09-1H is the high-drive version of the -1, and its rise and fall times are much faster than the -1.

These parts are not intended for 5 V input-tolerant applications

For a complete list of related documentation, click here.

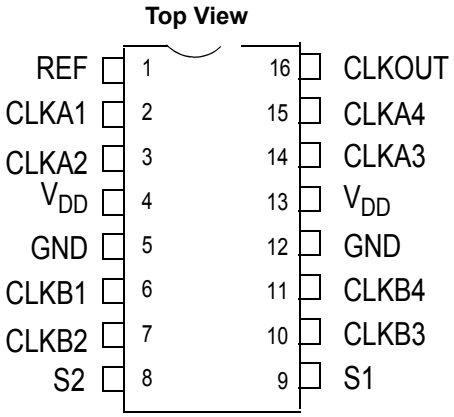
Block Diagram



Contents

Pin Configuration

Figure 1. 16-pin SOIC or TSSOP pinout (Top View)



Pin Definitions

Pin No.	Signal	Description
1	REF [1]	Input reference frequency
2	CLKA1 [2]	Buffered clock output, Bank A
3	CLKA2 [2]	Buffered clock output, Bank A
4	V_{DD}	3.3 V or 2.5 V supply
5	GND	Ground
6	CLKB1 [2]	Buffered clock output, Bank B
7	CLKB2 [2]	Buffered clock output, Bank B
8	S2 [3]	Select input, bit 2
9	S1 [3]	Select input, bit 1
10	CLKB3 [2]	Buffered clock output, Bank B
11	CLKB4 [2]	Buffered clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3 V or 2.5 V supply
14	CLKA3 [2]	Buffered clock output, Bank A
15	CLKA4 [2]	Buffered clock output, Bank A
16	CLKOUT [2]	Buffered output, internal feedback on this pin

Notes
1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.

Select Input Decoding

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT [4]	Output Source	PLL Shutdown
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

The output driving the CLKOUT pin will be driving a total load of 5 pF (internal load) plus any additional load externally connected to this pin. For applications requiring zero input-output delay, the total load on each output pin (including CLKOUT) must be the same. For example, if there is no external load on CLKOUT pin, add 5 pF to each of the remaining outputs to match the internal load on CLKOUT pin. If input-output delay adjustments are required, the CLKOUT load may be changed to vary the delay between the REF input and remaining outputs.

For zero output-output skew, be sure to load all outputs equally. For further information refer to the application note titled “AN1234 – Understanding Cypress’s Zero Delay Buffers”.

Note
4. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Absolute Maximum Conditions

Supply voltage to ground potential .....–0.5 V to 4.6 V
DC input voltage .....V_{SS} – 0.5 V to 4.6 V

Storage temperature ..... –65 °C to 150 °C
Junction temperature ..... 150 °C
Static discharge voltage
(per MIL-STD-883, Method 3015) ..... > 2000 V

Operating Conditions

Parameter	Description	Min	Max	Unit
$V_{DD3.3}$	3.3 V supply voltage	3.0	3.6	V
$V_{DD2.5}$	2.5 V supply voltage	2.3	2.7	V
T_A	Operating temperature (ambient temperature) – Commercial	0	70	°C
	Operating temperature (ambient temperature) – Industrial	–40	85	°C
C_L[5]	Load capacitance, <100 MHz, 3.3 V	–	30	pF
	Load capacitance, <100 MHz, 2.5 V with High drive	–	30	pF
	Load capacitance, <133.3 MHz, 3.3 V	–	22	pF
	Load capacitance, <133.3 MHz, 2.5 V with High drive	–	22	pF
	Load capacitance, <133.3 MHz, 2.5 V with Standard drive	–	15	pF
	Load capacitance, >133.3 MHz, 3.3 V	–	15	pF
	Load capacitance, >133.3 MHz, 2.5 V with High drive	–	15	pF
C_{IN}	Input capacitance[6]	–	5	pF
BW	Closed-loop bandwidth (typical), 3.3 V	1–1.5		MHz
	Closed-loop bandwidth (typical), 2.5 V	0.8		MHz
R_{OUT}	Output impedance (typical), 3.3 V High drive	29		Ω
	Output impedance (typical), 3.3 V Standard drive	41		Ω
	Output impedance (typical), 2.5 V High drive	37		Ω
	Output impedance (typical), 2.5 V Standard drive	41		Ω
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.01	50	ms

Notes
5. Applies to Test Circuit #1.
6. Applies to both REF Clock and internal feedback path on CLKOUT.

Electrical Specifications

3.3 V DC

Parameter	Description	Test Conditions	Min	Max	Unit
V_{DD}	Supply voltage		3.0	3.6	V
V_{IL}	Input LOW voltage		–	0.8	V
V_{IH}	Input HIGH voltage		2.0	V_{DD} + 0.3	V
I_{IL}	Input leakage current	$0 < V_{IN} < V_{IL}$	–	±10	µA
I_{IH}	Input HIGH current	$V_{IN} = V_{DD}$	–	100	µA
V_{OL}	Output LOW voltage	I_{OL} = 8 mA (standard drive)	–	0.4	V
		I_{OL} = 12 mA (High drive)	–	0.4	V
V_{OH}	Output HIGH voltage	I_{OH} = –8 mA (standard drive)	2.4	–	V
		I_{OH} = –12 mA (High drive)	2.4	–	V
I_{DD} (PD mode)	Power down supply current	REF = 0 MHz (Commercial)	–	12	µA
		REF = 0 MHz (Industrial)	–	25	µA
I_{DD}	Supply current	Unloaded outputs, 66-MHz REF	–	30	mA

Electrical Specifications

2.5 V DC

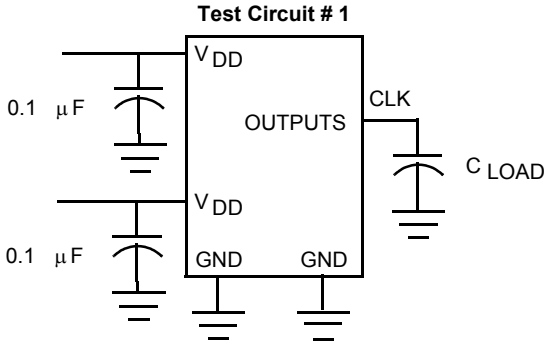
Parameter	Description	Test Conditions	Min	Max	Unit
V_{DD}	Supply voltage		2.3	2.7	V
V_{IL}	Input LOW voltage		–	0.7	V
V_{IH}	Input HIGH voltage		1.7	V_{DD} + 0.3	V
I_{IL}	Input leakage current	$0<V_{IN} < V_{DD}$	–	10	µA
I_{IH}	Input HIGH current	$V_{IN} = V_{DD}$	–	100	µA
V_{OL}	Output LOW voltage	I_{OL} = 8 mA (Standard drive)	–	0.5	V
		I_{OL} = 12 mA (High drive)	–	0.5	V
V_{OH}	Output HIGH voltage	I_{OH} = –8 mA (Standard drive)	V_{DD} – 0.6	–	V
		I_{OH} = –12 mA (High drive)	V_{DD} – 0.6	–	V
I_{DD} (PD mode)	Power down supply current	REF = 0 MHz (Commercial)	–	12	µA
		REF = 0 MHz (Industrial)	–	25	µA
I_{DD}	Supply current	Unloaded outputs, 66-MHz REF	–	45	mA

Thermal Resistance

Parameter [7]	Description	Test Conditions	16-pin SOIC	16-pin TSSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	121	111	°C/W
θ_{JC}	Thermal resistance (junction to case)		53	26	°C/W

Test Circuits

Figure 2. Test Circuit



Note
7. These parameters are guaranteed by design and are not tested.

Electrical Specifications

3.3 V and 2.5 V AC

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Maximum frequency [8] (input/output)	3.3 V High drive	10	–	220	MHz
		3.3 V Standard drive	10	–	167	MHz
		2.5 V High drive	10	–	200	MHz
		2.5 V Standard drive	10	–	133	MHz
T_{IDC}	Input duty cycle	<133.3 MHz	25	–	75	%
		>133.3 MHz	40	–	60	%
$t_2 \div t_1$	Output duty cycle [9]	<133.3 MHz	47	–	53	%
		>133.3 MHz	45	–	55	%
t_3, t_4	Rise, fall time (3.3 V) [9]	Std drive, CL = 30 pF, <100 MHz	–	–	1.6	ns
		Std drive, CL = 22 pF, <133.3 MHz	–	–	1.6	ns
		Std drive, CL = 15 pF, <167 MHz	–	–	0.6	ns
		High drive, CL = 30 pF, <100 MHz	–	–	1.2	ns
		High drive, CL = 22 pF, <133.3 MHz	–	–	1.2	ns
		High drive, CL = 15 pF, >133.3 MHz	–	–	0.5	ns
t_3, t_4	Rise, fall time (2.5 V) [9]	Std drive, CL = 15 pF, <133.33 MHz	–	–	1.5	ns
		High drive, CL = 30 pF, <100 MHz	–	–	2.1	ns
		High drive, CL = 22 pF, <133.3 MHz	–	–	1.3	ns
		High drive, CL = 15 pF, >133.3 MHz	–	–	1.2	ns
t_5	Output to output skew [9]	All outputs equally loaded, 3.3 V supply, 2.5 supply standard drive	–	45	100	ps
		All outputs equally loaded, 2.5 V supply high drive	–	–	110	ps
t_6	Delay, REF rising edge to CLKOUT rising edge [9]	PLL Bypass mode	1.5	–	4.4	ns
		PLL enabled @ 3.3 V	–100	–	100	ps
		PLL enabled @2.5 V	–200	–	200	ps
t_7	Part to part skew [9]	Measured at $V_{DD}/2$. Any output to any output, 3.3 V supply	–	–	±150	ps
		Measured at $V_{DD}/2$. Any output to any output, 2.5 V supply	–	–	±300	ps
t_{LOCK}	PLL lock time [9]	Stable power supply, valid clocks presented on REF and CLKOUT pins	–	–	1.0	ms

Notes
8. For the given maximum loading conditions. See C_L in Operating Conditions Table.
9. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Specifications (continued)

3.3 V and 2.5 V AC

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
T_{JCC}[10, 11]	Cycle-to-cycle jitter, peak	3.3 V supply, >66 MHz, <15 pF	–	25	55	ps
		3.3 V supply, >66 MHz, <30 pF, standard drive	–	65	125	ps
		3.3 V supply, >66 MHz, <30 pF, high drive	–	53	100	ps
		2.5 V supply, >66 MHz, <15 pF, standard drive	–	35	95	ps
		2.5 V supply, >66 MHz, <15 pF, high drive	–	30	65	ps
		2.5 V supply, >66 MHz, <30 pF, high drive	–	75	145	ps
		S2:S1 = 1:0 mode, 3.3 V, <15 pF, standard drive	–	16	–	ps
		S2:S1 = 1:0 mode, 3.3 V, <15 pF, high drive	–	14	–	ps
		S2:S1 = 1:0 mode, 2.5 V, <15 pF, standard drive	–	23	–	ps
		S2:S1 = 1:0 mode, 2.5 V, <15 pF, high drive	–	22	–	ps
T_{PER}[10, 11]	Period jitter, peak	3.3 V supply, 66–100 MHz, <15 pF	–	20	75	ps
		3.3 V supply, >100 MHz, <15 pF	–	15	45	ps
		3.3 V supply, >66 MHz, <30 pF, standard drive	–	40	100	ps
		3.3 V supply, >66 MHz, <30 pF, high drive	–	30	70	ps
		2.5 V supply, >66 MHz, <15 pF, standard drive	–	25	60	ps
		2.5 V supply, 66–100 MHz, <15 pF, high drive	–	25	60	ps
		2.5 V supply, >100 MHz, <15 pF, high drive	–	15	45	ps
		S2:S1 = 1:0 mode, 3.3 V, <15 pF, standard drive	–	28	–	ps
		S2:S1 = 1:0 mode, 3.3 V, <15 pF, high drive	–	24	–	ps
		S2:S1 = 1:0 mode, 2.5 V, <15 pF, standard drive	–	40	–	ps
		S2:S1 = 1:0 mode, 2.5 V, <15 pF, high drive	–	37	–	ps

Notes
10. Parameter is guaranteed by design and characterization. Not 100% tested in production.
11. Typical jitter is measured at 3.3 V or 2.5 V, 29 °C, with all outputs driven into the maximum specified load. Further information regarding jitter specifications may be found in the application note “Understanding Data Sheet Jitter Specifications for Cypress Clock Products.”

Switching Waveforms

Figure 3. Duty Cycle Timing

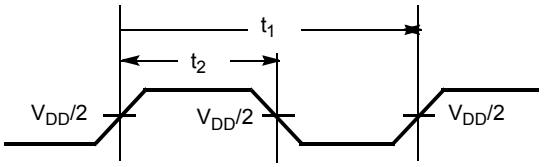


Figure 4. All Outputs Rise/Fall Time

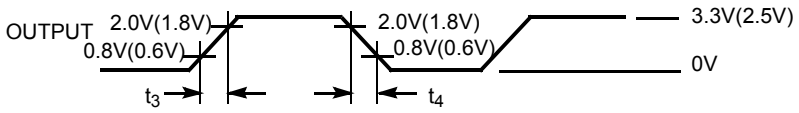


Figure 5. Output-Output Skew

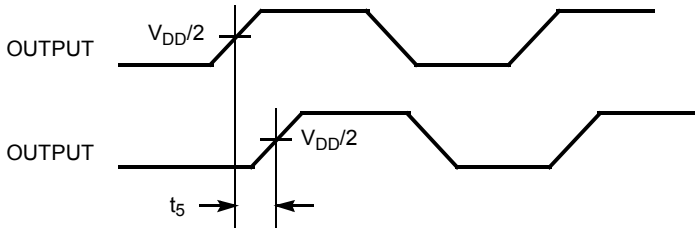


Figure 6. Input-Output Propagation Delay

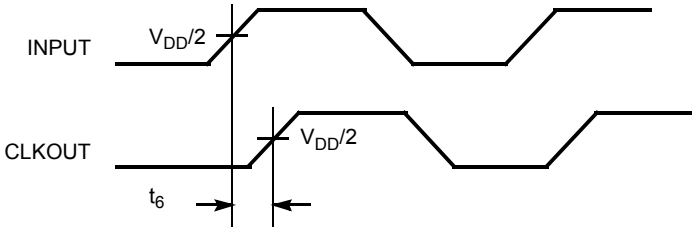
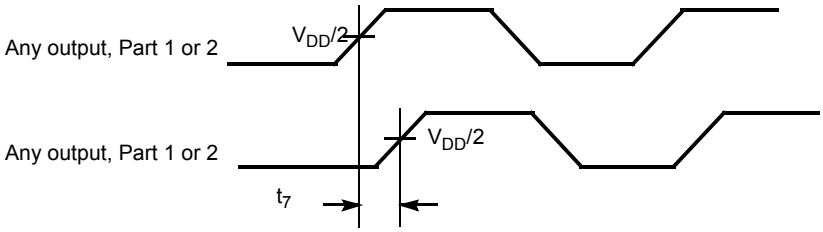
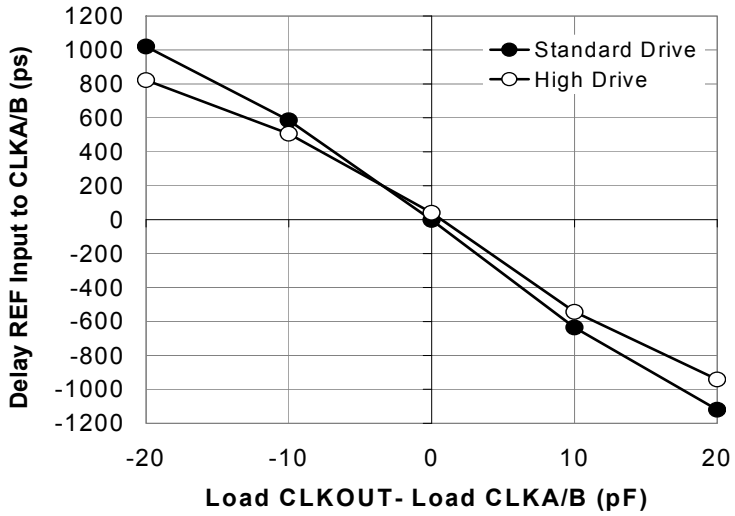


Figure 7. Part-Part Skew



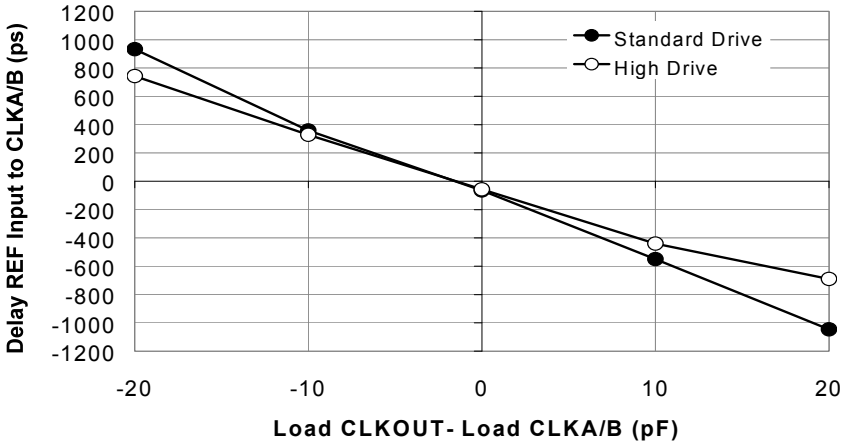
Supplemental Parametric Information

Figure 8. 2.5 V Typical Room Temperature Graph for REF Input to CLKA/CLKB Delay Versus Loading Difference between CLKOUT and CLKA/CLKB



Data is shown for 66 MHz. Delay is a weak function of frequency.

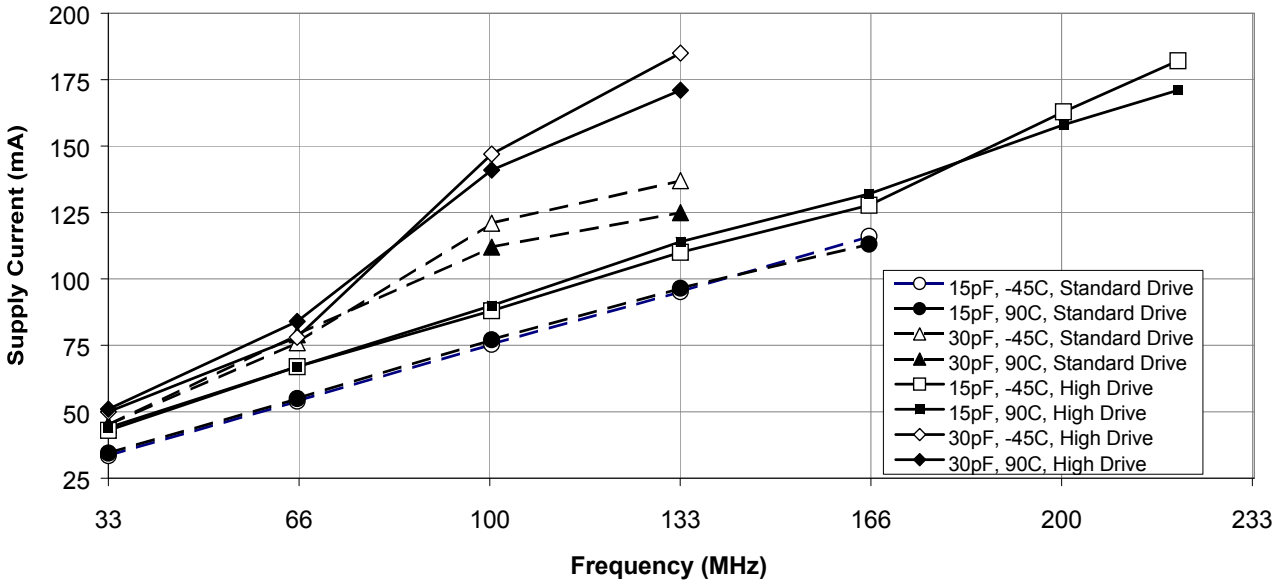
Figure 9. 3.3 V Typical Room Temperature Graph for REF Input to CLKA/CLKB Delay Versus Loading Difference between CLKOUT and CLKA/CLKB



Data is shown for 66 MHz. Delay is a weak function of frequency.

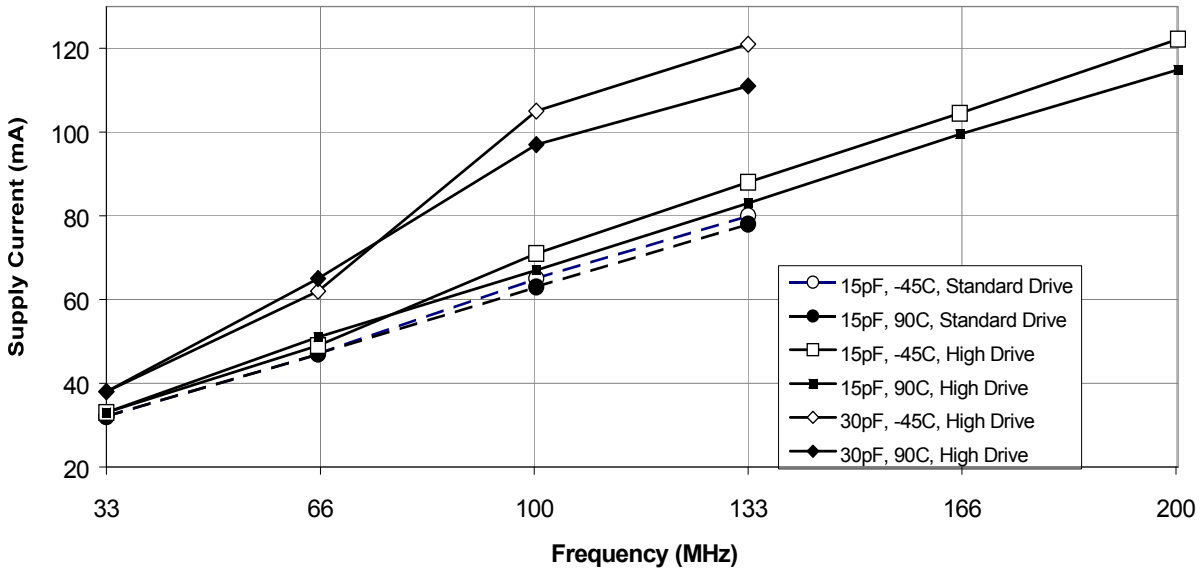
Supplemental Parametric Information (continued)

Figure 10. 3.6 V Measured Supply Current versus Frequency, Drive Strength, Loading, and Temperature



Note that the 30-pF data above 100 MHz is beyond the data sheet specification of 22 pF.

Figure 11. 2.7 V Measured Supply Current Versus Frequency, Drive Strength, Loading, and Temperature



Note that the 30-pF high-drive data above 100bMHz is beyond the data sheet specification of 22 pF.

Supplemental Parametric Information (continued)

Figure 12. Typical 3.3 V Measured Cycle-to-cycle Jitter at 29 °C, versus Frequency, Drive Strength, and Loading

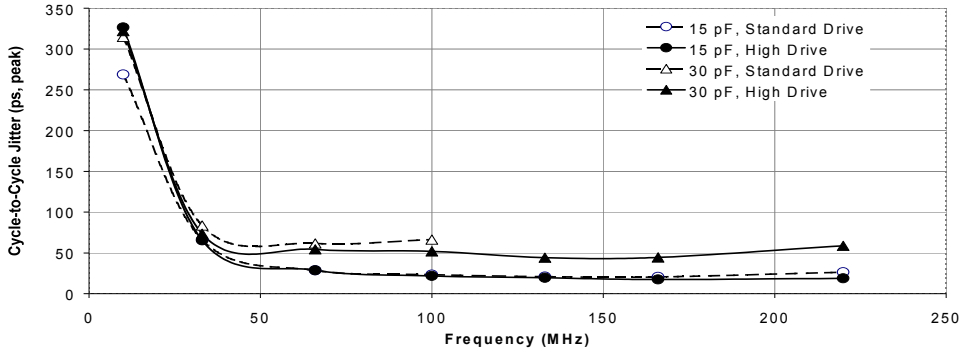


Figure 13. Typical 2.5 V Measured Cycle-to-cycle Jitter at 29 °C, versus Frequency, Drive Strength, and Loading

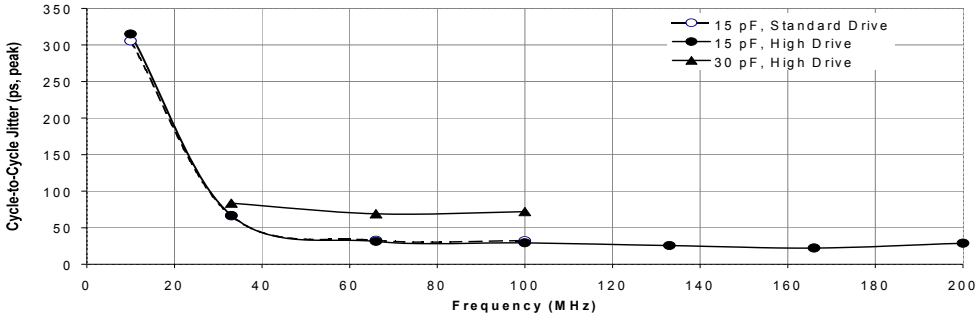


Figure 14. Typical 3.3 V Measured Period Jitter at 29 °C, versus Frequency, Drive Strength, and Loading

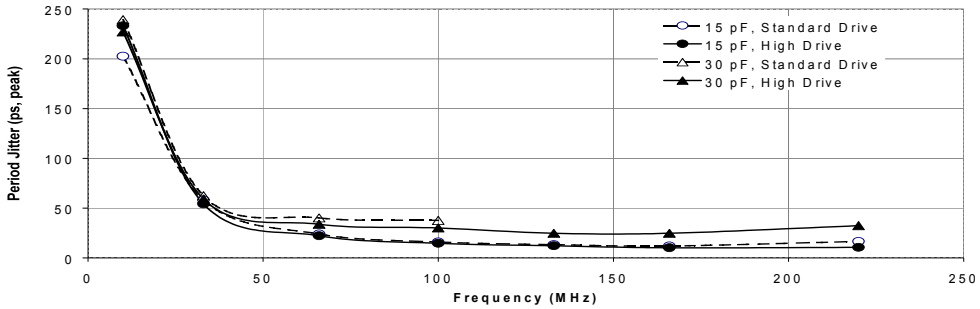
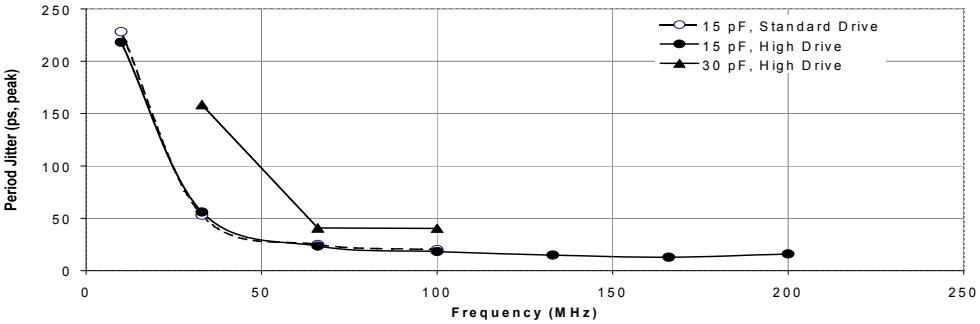
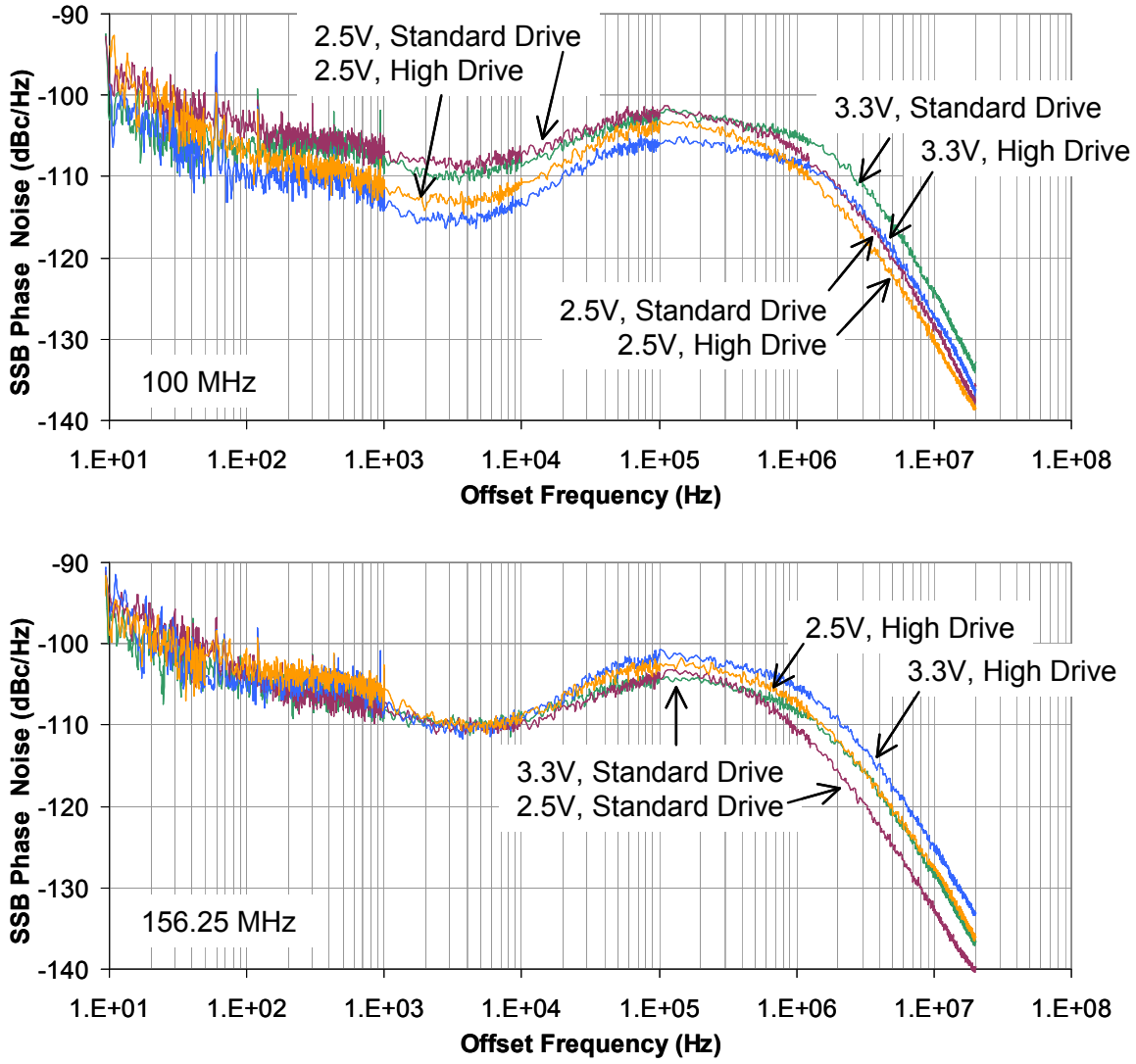


Figure 15. Typical 2.5 V Measured Period Jitter at 29 °C, versus Frequency, Drive Strength, and Loading



Supplemental Parametric Information (continued)

Figure 16. Typical Phase-noise Data at 100 MHz (top) and 156.25 MHz (bottom) across V_{DD} and Drive Strength [12]



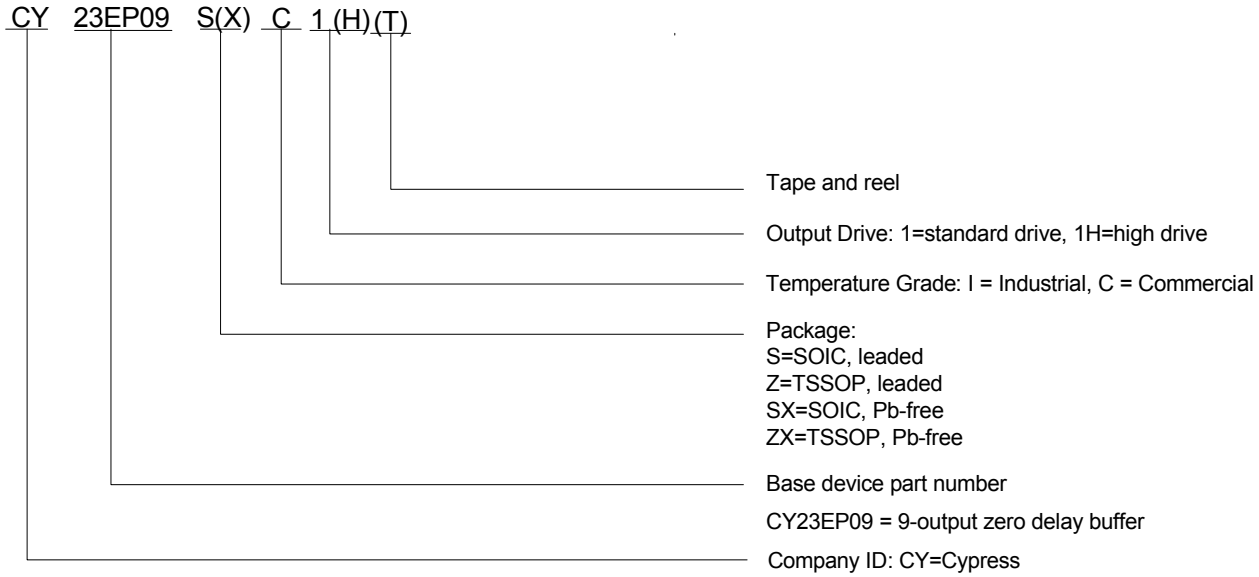
Note

12. Typical jitter is measured at 3.3 V or 2.5 V, 29 °C, with all outputs driven into the maximum specified load. Further information regarding jitter specifications may be found in the application note “Understanding Data Sheet Jitter Specifications for Cypress Clock Products.”

Ordering Information

Ordering Code	Package Type	Operating Range
Pb-free		
CY23EP09SXC-1	16-pin SOIC	Commercial
CY23EP09SXC-1T	16-pin SOIC – Tape and Reel	Commercial
CY23EP09SXI-1	16-pin SOIC	Industrial
CY23EP09SXI-1T	16-pin SOIC – Tape and Reel	Industrial
CY23EP09SXC-1H	16-pin SOIC	Commercial
CY23EP09SXC-1HT	16-pin SOIC – Tape and Reel	Commercial
CY23EP09SXI-1H	16-pin SOIC	Industrial
CY23EP09SXI-1HT	16-pin SOIC – Tape and Reel	Industrial
CY23EP09ZXC-1H	16-pin TSSOP	Commercial
CY23EP09ZXC-1HT	16-pin TSSOP – Tape and Reel	Commercial
CY23EP09ZXI-1H	16-pin TSSOP	Industrial
CY23EP09ZXI-1HT	16-pin TSSOP – Tape and Reel	Industrial

Ordering Code Definitions



Package Diagrams

Figure 17. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068

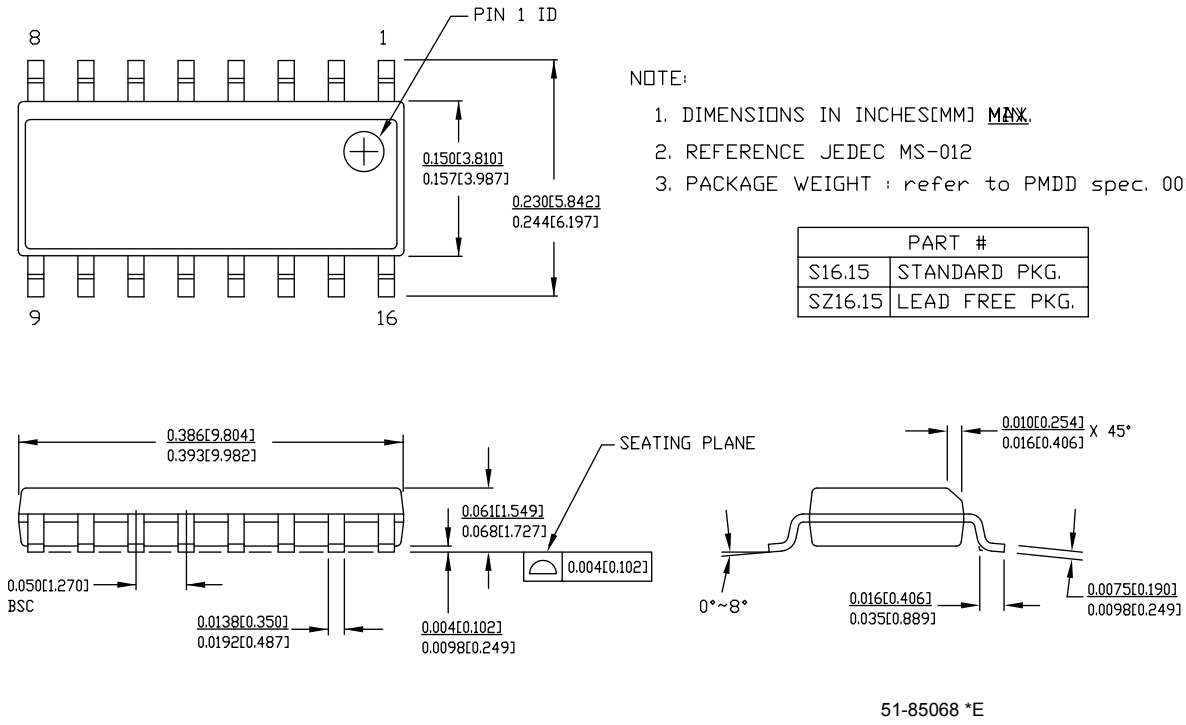
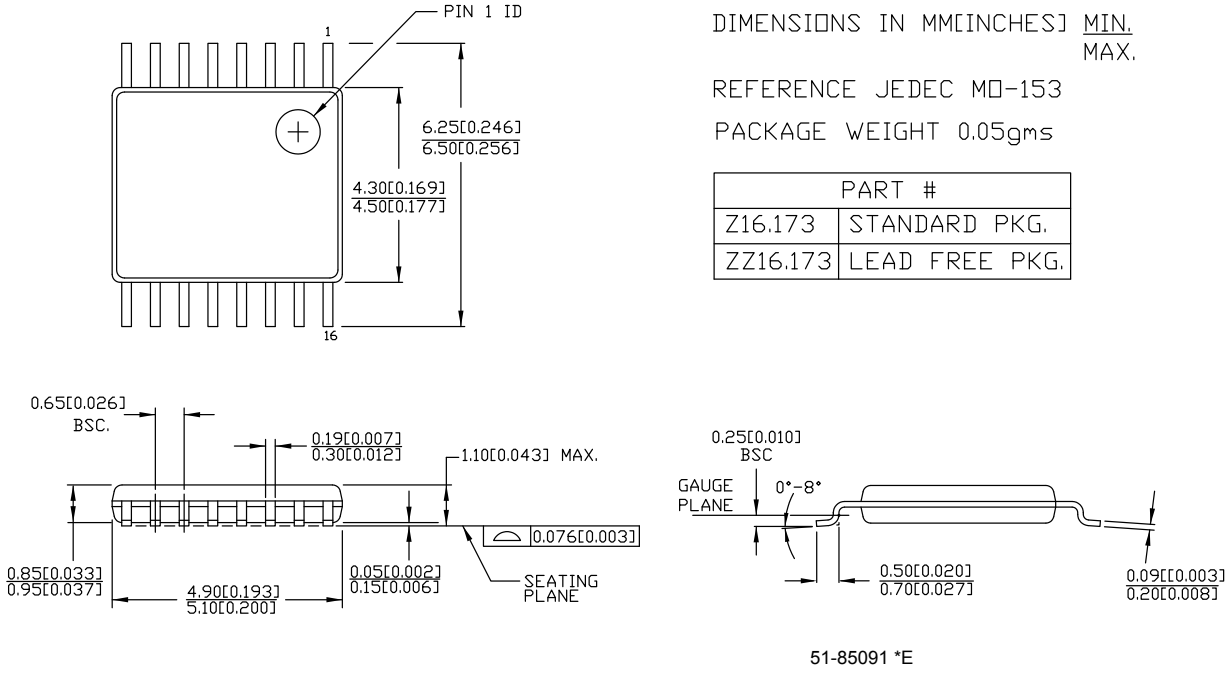


Figure 18. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091



Acronyms

Acronym	Description
PCI	Personal Computer Interconnect
PLL	Phase Locked Loop
SDRAM	Synchronous Dynamic Random Access Memory
SOIC	Small Outline Integrated Circuit
TSSOP	Thin-Shrink Small Outline Package
ZDB	Zero Delay Buffer

Document Conventions

Units of Measure

Symbol	Units of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY23EP09, 2.5 V or 3.3 V, 10 MHz–220 MHz, Low Jitter, Nine-Output Zero Delay Buffer Document Number: 38-07760				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	345446	See ECN	RGL	New data sheet.
*A	355777	See ECN	RGL	Updated Electrical Specifications: Updated values of t_7 parameter (to agree with latest char results).
*B	401036	See ECN	RGL	Changed status from Preliminary to Final. Updated Electrical Specifications: Updated details in “Test Conditions” column corresponding to T_{JCC} and T_{PER} parameters. Updated Supplemental Parametric Information: Added Figure 8. Added Figure 16.
*C	3270178	06/01/2011	BASH	Updated Package Diagrams. Added Acronyms and Units of Measure. Updated to new template.
*D	4400992	06/10/2014	AJU	Updated Operating Conditions: Updated values of Theta Ja and Theta Jc parameters (corresponding to 16-pin TSSOP package). Updated Package Diagrams: spec 51-85068 – Changed revision from *C to *E. spec 51-85091 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*E	4580603	11/26/2014	AJU	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagrams.
*F	5243008	04/26/2016	PSR	Updated Zero Delay and Skew Control: Updated description. Updated Operating Conditions: Removed “Theta Ja”, “Theta Jc” parameters and their details. Removed Note “Theta Ja, EIA JEDEC 51 test board conditions, 2S2P; Theta Jc Mil-Spec 883E Method 1012.1.” and its reference. Added Thermal Resistance. Updated to new template. Completing Sunset Review.
*G	5993917	12/14/2017	AESATMP8	Updated logo and Copyright.

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