# MJD6039, NJVMJD6039T4G

# Darlington Power Transistors

## DPAK For Surface Mount Applications

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, convertors, and power amplifiers.

### Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Monolithic Construction With Built–in Base–Emitter Shunt Resistors
- High DC Current Gain – $h_{FE}$ = 2500 (Typ) @ $I_C$ = 4.0 Adc
- Epoxy Meets UL 94 V–0 @ 0.125 in
- ESD Ratings:
  - Human Body Model, 3B > 8000 V
  - Machine Model, C > 400 V
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- Pb–Free Package is Available*

### MAXIMUM RATINGS

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Collector–Emitter Voltage | $V_{CEO}$ | 80 | Vdc |
| Collector–Base Voltage | $V_{CB}$ | 80 | Vdc |
| Emitter–Base Voltage | $V_{EB}$ | 5 | Vdc |
| Collector Current<br>Continuous<br>Peak | $I_C$ | <br>4<br>8 | Adc |
| Base Current | $I_B$ | 100 | mAdc |
| Total Power Dissipation<br>@ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | <br>20<br>0.16 | <br>W<br>W/°C |
| Total Power Dissipation (Note 1)<br>@ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | <br>1.75<br>0.014 | <br>W<br>W/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | –65 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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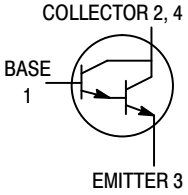
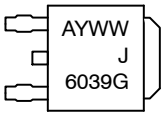
**SILICON POWER TRANSISTORS 4 AMPERES, 80 VOLTS, 20 WATTS**

**DPAK**
**CASE 369C**
**STYLE 1**




### MARKING DIAGRAM




A = Assembly Location
Y = Year
WW = Work Week
J6039 = Device Code
G = Pb–Free Package

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MJD6039T4 | DPAK | 2,500/Tape & Reel |
| MJD6039T4G | DPAK (Pb–Free) | 2,500/Tape & Reel |
| NJVMJD6039T4G | DPAK (Pb–Free) | 2,500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Case | $R_{\theta JC}$ | 6.25 | °C/W |
| Thermal Resistance, Junction−to−Ambient (Note 2) | $R_{\theta JA}$ | 71.4 | °C/W |

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

## ELECTRICAL CHARACTERISTICS ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| Collector−Emitter Sustaining Voltage ($I_C$ = 30 mAdc, $I_B$ = 0) | $V_{CEO(sus)}$ | 80 | – | Vdc |
| Collector−Cutoff Current ($V_{CE}$ = 40 Vdc, $I_B$ = 0) | $I_{CEO}$ | – | 10 | μAdc |
| **ON CHARACTERISTICS** (Note 3) | | | | |
| DC Current Gain ($I_C$ = 1 Adc, $V_{CE}$ = 4 Vdc)<br>($I_C$ = 2 Adc, $V_{CE}$ = 4 Vdc) | $h_{FE}$ | 1000<br>500 | –<br>– | – |
| Collector−Emitter Saturation Voltage ($I_C$ = 2 Adc, $I_B$ = 8 mAdc) | $V_{CE(sat)}$ | – | 2.5 | Vdc |
| Base−Emitter On Voltage ($I_C$ = 2 Adc, $V_{CE}$ = 4 Vdc) | $V_{BE(on)}$ | – | 2.8 | Vdc |
| **DYNAMIC CHARACTERISTICS** | | | | |
| Small−Signal Current Gain ($I_C$ = 0.75 Adc, $V_{CE}$ = 10 Vdc, f = 1 kHz) | $h_{fe}$ | 25 | – | – |
| Output Capacitance ($V_{CB}$ = 10 Vdc, $I_E$ = 0, f = 0.1 MHz) | $C_{ob}$ | – | 100 | pF |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

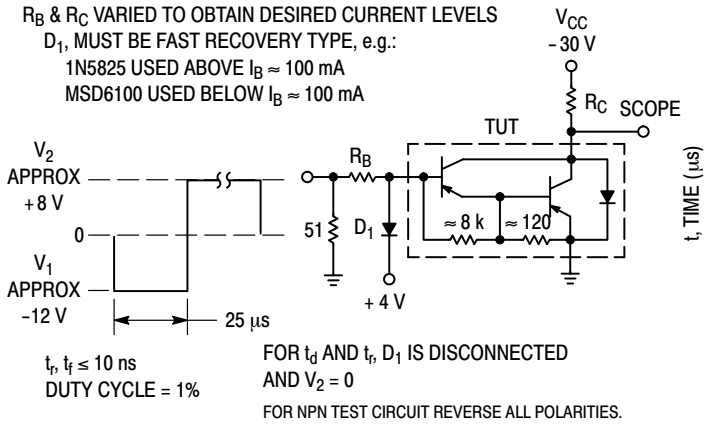



**Figure 1. Switching Times Test Circuit**

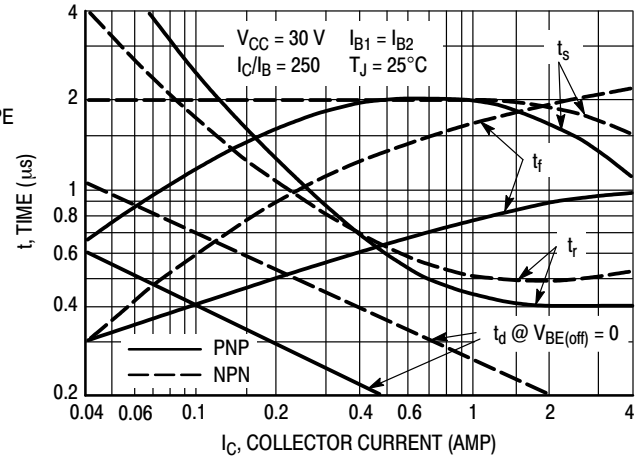



**Figure 2. Switching Times**

## TYPICAL ELECTRICAL CHARACTERISTICS

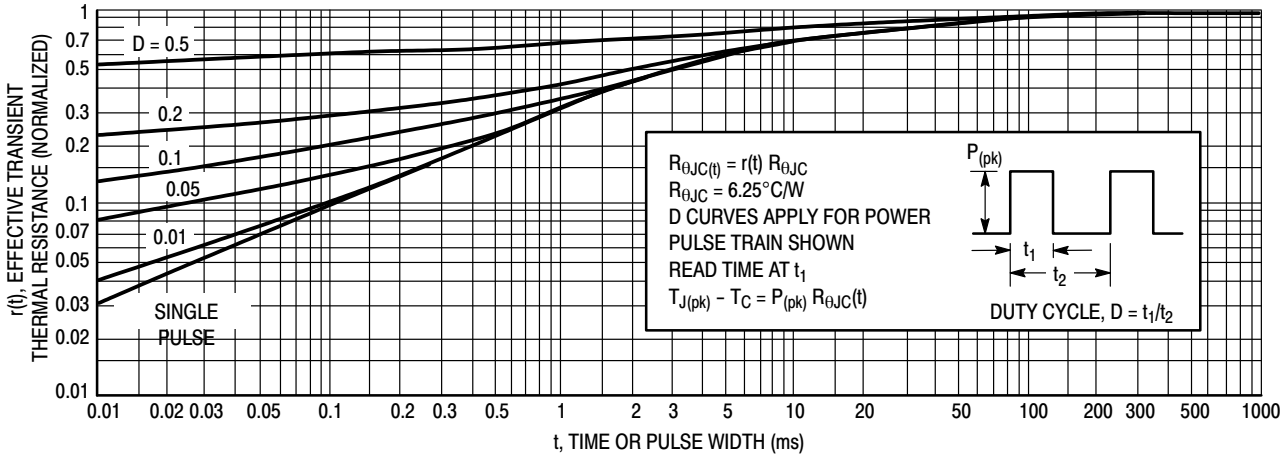



**Figure 3. Thermal Response**

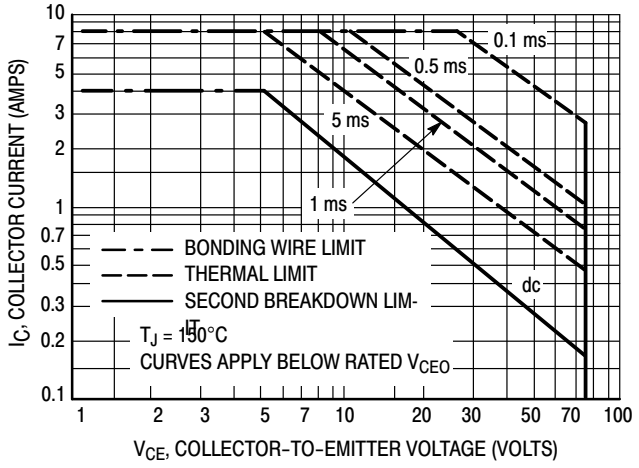



**Figure 4. Maximum Rated Forward Biased Safe Operating Area**

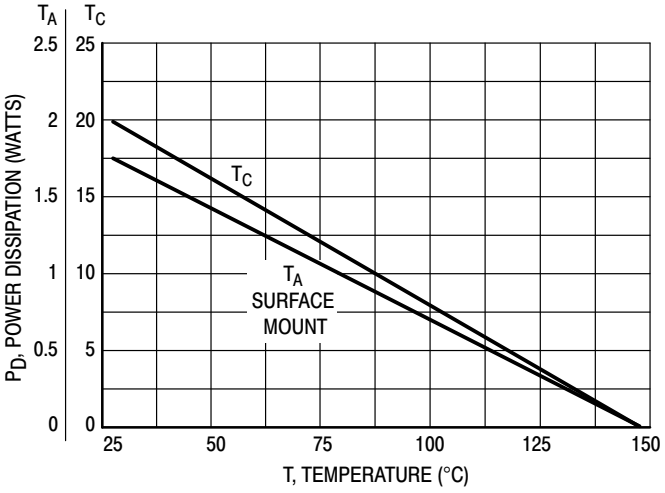



**Figure 5. Power Derating**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 is based on $T_{J(pk)} = 150°C$; $T_C$ is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

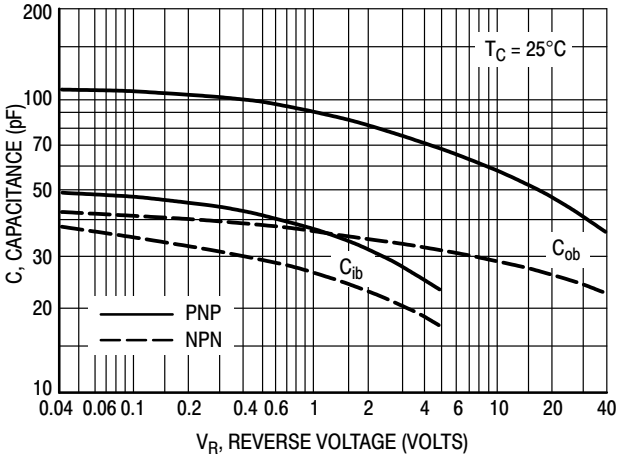



**Figure 6. Capacitance**

## TYPICAL ELECTRICAL CHARACTERISTICS

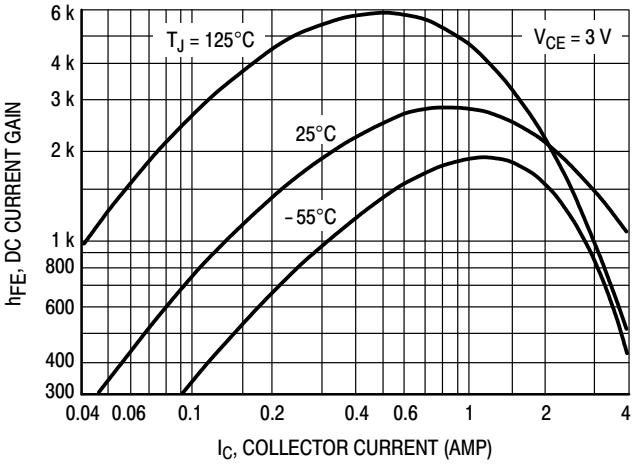



**Figure 7. DC Current Gain**

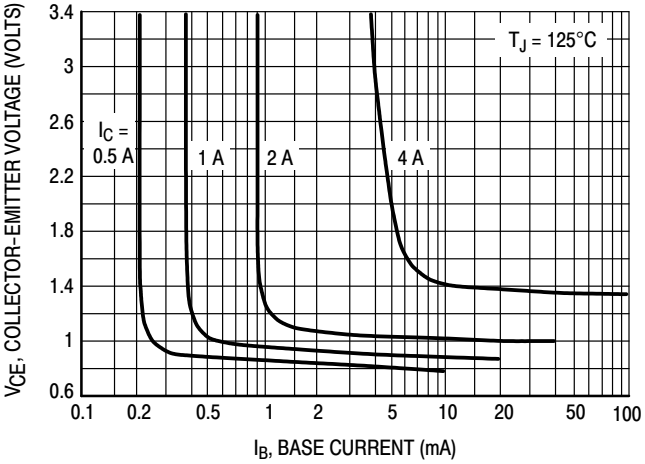



**Figure 8. Collector Saturation Region**

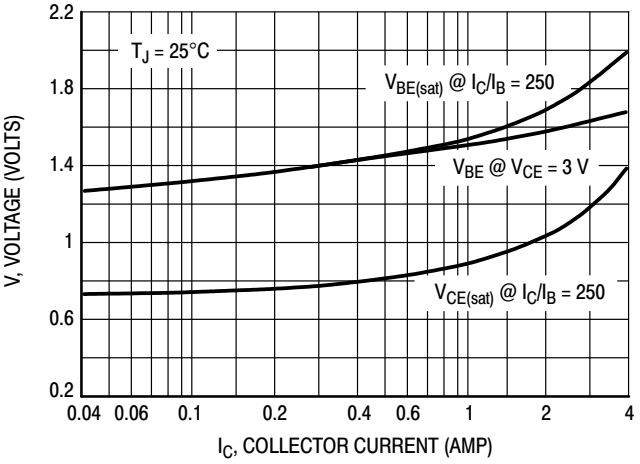



**Figure 9. “On” Voltages**

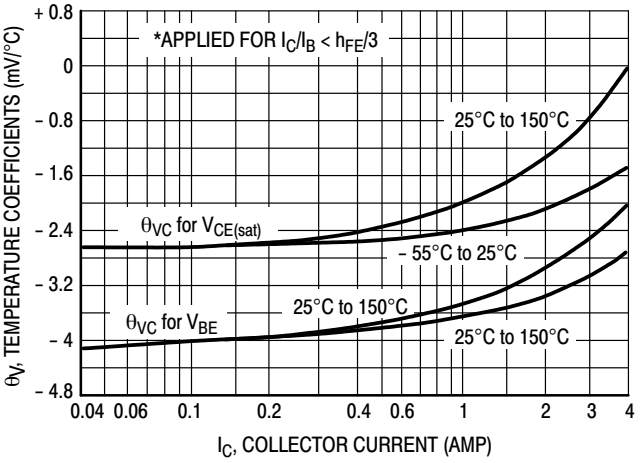



**Figure 10. Temperature Coefficients**

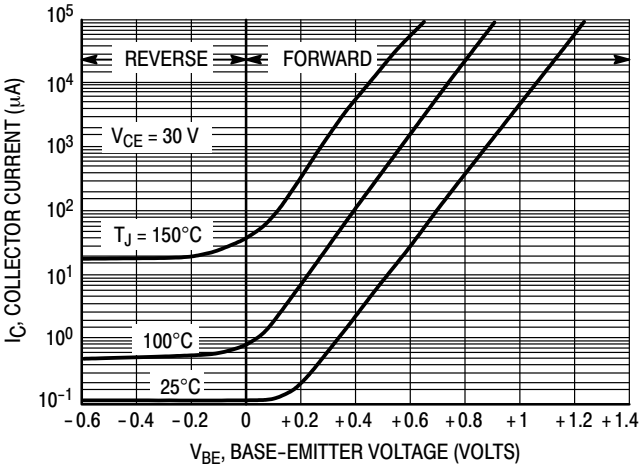



**Figure 11. Collector Cut−Off Region**

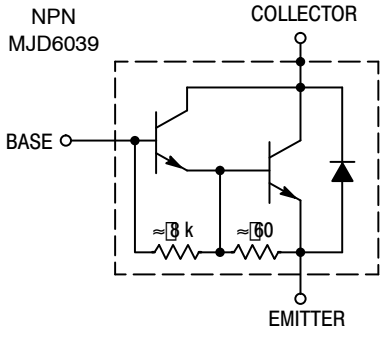
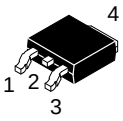


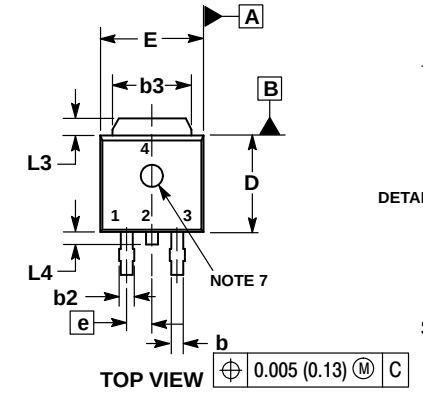

**Figure 12. Darlington Schematic**



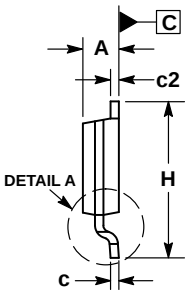

**SCALE 1:1**

**DPAK (SINGLE GAUGE)**
CASE 369C
ISSUE F

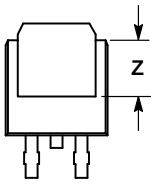
DATE 21 JUL 2015



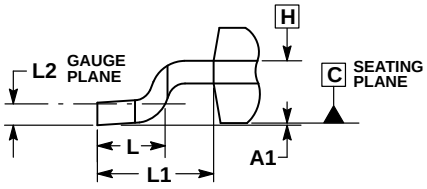

TOP VIEW



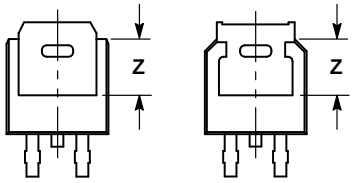

SIDE VIEW




BOTTOM VIEW




DETAIL A
ROTATED 90° CW




BOTTOM VIEW
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.028 | 0.045 | 0.72 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.114 REF | | 2.90 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

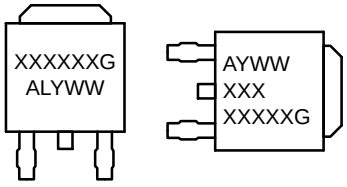
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

### GENERIC MARKING DIAGRAM*

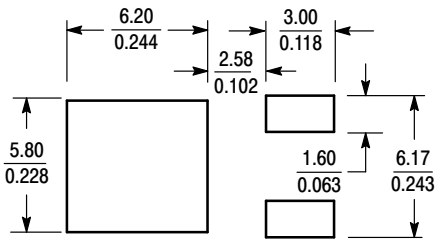



**IC** **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDERING FOOTPRINT*




SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| ISSUE | REVISION | DATE |
|---|---|---|
| O | RELEASED FOR PRODUCTION. REQ. BY L. GAN | 24 SEP 2001 |
| A | ADDED STYLE 8. REQ. BY S. ALLEN. | 06 AUG 2008 |
| B | ADDED STYLE 9. REQ. BY D. WARNER. | 16 JAN 2009 |
| C | ADDED STYLE 10. REQ. BY S. ALLEN. | 09 JUN 2009 |
| D | RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE. | 29 JUN 2010 |
| E | ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA. | 06 FEB 2014 |
| F | ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA. | 21 JUL 2015 |
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