TPS40400 3-V to 20-V PMBus Synchronous Buck Controller

1 Features

- Input Operating Voltage Range: 3 V to 20 V
- PMBus Enabled Analog Controller
- Reference 600 mV ± 1%
- Remote Voltage Sense Amplifier
- Internal 6-V Regulator and 6-V Gate Drive
- Programmable Overcurrent Protection
- Inductor Resistance or Series Resistance Used for Current Sensing
- Programmable Switching Frequency: 200 kHz to 2 MHz
- Powergood Indicator
- Thermal Shutdown
- Programmable Soft-Start
- Internal Bootstrap Diode
- Prebias Output Safe
- 24-Pin QFN Package

2 Applications

- Smart Power Systems
- Power Supply Modules
- Communications Equipment
- Computing Equipment

3 Description

The TPS40400 is a cost-optimized flexible synchronous buck controller that operates from a nominal 3-V to 20-V supply. This controller is an analog PWM controller that allows programming and monitoring through the PMBus™ interface. Flexible features found on this device include programmable soft-start time, programmable short circuit limit, and programmable undervoltage lockout (UVLO).

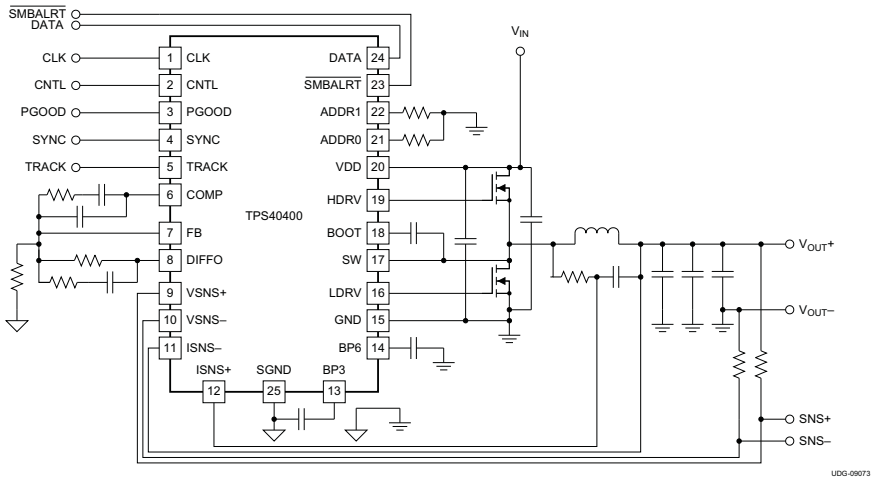
An adaptive anti-cross conduction scheme is used to prevent shoot through current in the power FETs. Gate drive voltage is 6 V to better enhance the power FETs for reduced losses. Short circuit detection occurs by sensing the voltage drop across the inductor or across a resistor placed in series with the inductor. A PMBus programmable threshold is compared to this voltage and is used to detect overcurrent. When the overcurrent threshold is reached, a pulse by pulse current limit scheme is used to limit the current to acceptable levels. If the overcurrent condition persists for more than 7 clock cycles of the converter, a fault condition is declared and the converter shuts down and goes into either a hiccup restart mode or latches off. The behavior can be selected through the PMBus interface. Other PMBus interface features include programmable operating frequency, soft-start time, overvoltage and undervoltage thresholds and the response to those events, output voltage change including margining as well as status monitoring.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS40400	VQFN (24)	3.50 mm × 5.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2015) to Revision D — **Page**

- Changed VQFN (24) package dimensions from: 3.50 mm × 3.50 mm to: 3.50 mm × 5.50 mm ... 1

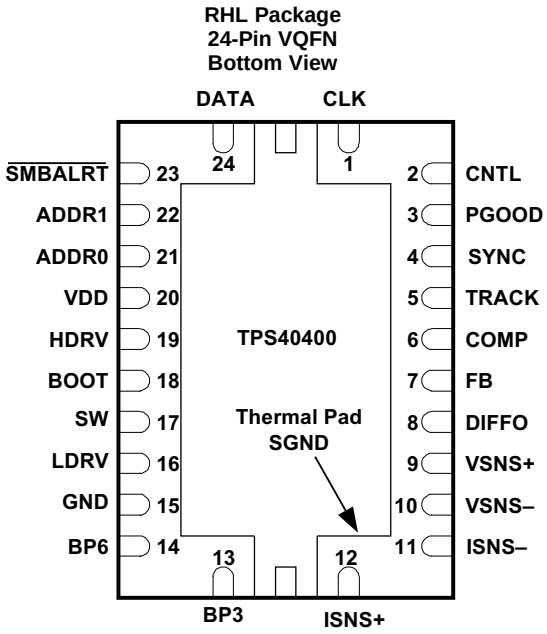
Changes from Revision B (September 2015) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (March 2012) to Revision A — **Page**

- Corrected default values in ON_OFF_CONFIG register map ... 27
- Added Design Example 1 ... 57
- Added Design Example 2 ... 66

5 Pin Configuration and Functions



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
ADDR0	21	I	Low-order address pin for PMBus address configuration. One of eight resistor values must be connected from this pin to SGND to select the low-order octal digit in the PMBus address.
ADDR1	22	I	High-order address pin for PMBus address configuration. One of eight resistor values must be connected from this pin to SGND to select the high-order octal digit in the PMBus address.
BOOT	18	I	Gate drive voltage for the high-side, N-channel MOSFET. A capacitor (100-nF) typical must be connected between this pin and SW.
BP3	13	O	Bypass pin for the internal regulator that supplies power to the internal controls of the device. Normal regulation voltage is 3.3 V. Connect a capacitor with a value of 100-nF or larger from this pin to GND.
BP6	14	O	Bypass pin for the internal regulator that supplies power to the gate drivers. Normal regulation voltage is 6.5 V. Connect a capacitor with a value of 1-μF or larger from this pin to GND.
CLK	1	I	Clock input for the PMBus interface
CNTL	2	I	Logic level input that controls the start-up and shutdown of the converter. PMBus options determine exact functionality.
COMP	6	O	Output of the error amplifier. Used for control loop compensation.
DATA	24	I/O	Data I/O for the PMBus interface
DIFFO	8	O	Output of the unity gain remote voltage sense amplifier. Typically connected to the voltage divider on FB
FB	7	I	Inverting input to the error amplifier. A voltage divider is connected to from the DIFFO pin to the FB pin to sense the output voltage.
GND	15	–	Common connection for the device. This pin should connect to the thermal pad under the device package and to the power stage ground, preferably close to the source of the low-side or rectifier MOSFET. Connections should be arranged so that no high-power level currents flow across the pad connected to the thermal pad on the underside of the device.
HDRV	19	O	Gate drive signal to the high-side MOSFET
ISNS–	11	I	Inverting input to the current sense amplifier
ISNS+	12	I	Noninverting input to the current sense amplifier
LDRV	16	O	Output used to drive the gate of the low-side or rectifier MOSFET.

(1) I = Input, O = Output, P = Supply, G = Ground

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
PGOOD	3	O	Power good output. This is an open-drain output that pulls low when any fault condition exists within the device or when the device is not operating within a user-selectable operating range of the nominal output voltage of the converter.
SGND	PAD	–	Signal ground for the device. Connect the ground of signal level circuits to this pin. Connections should be arranged so that power level currents do not flow in the pad attached to the thermal plane or in the SGND portion of the circuit.
$\overline{\text{SMBALRT}}$	23	O	Output used to signal that PMBus host that the device needs attention.
SW	17	I	This is the common connection for the flying high-side MOSFET driver and also serve as a sense line for the adaptive anti-cross-conduction circuitry
SYNC	4	I	Logic level input to the oscillator inside the device. The oscillator resets on the rising edge of a pulse train applied to this pin and begin a new switching cycle.
TRACK	5	I	Analog input to the noninverting side of the control loop error amplifier. The error amplifier has three inputs (voltage reference, TRACK and soft-start time) to its + side, and the lowest voltage applied to these three inputs dominate and control the output voltage of the whole converter. This pin is to allow the user to configure a voltage divider that allows the device output follow an external reference voltage during start-up.
VDD	20	I	Input power connection for the device. This pin requires a supply voltage of between 3 V to 20 V.
VSNS+	9	I	Noninverting input to the unity gain remote voltage sense amplifier.
VSNS–	10	I	Inverting input to the unity gain remote voltage sense amplifier.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage	VDD	–0.3	22	V
	SW	–5	27	
	BOOT	–0.3	30	
	BOOT-SW, HDRV-SW (Differential from BOOT or HDRV to SW)	–0.3	7	
	VSNS+, TRACK, SYNC, FB	–0.3	7	
	DATA, CLK, CNTL	–0.3	3.6	
	ISNS+, ISNS–	–0.3	15	
	VSNS–	–0.3	0.3	
Output voltage	HDRV	–0.3	30	V
	BP3	–0.3	3.8	
	BP6, COMP, PGOOD, DIFFO, LDRV	–0.3	7	
	$\overline{\text{SMBALRT}}$, ADDR0, ADDR1	–0.3	3.6	
Operating junction temperature, T_J		–40	150	°C
Storage Temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Controller input voltage	3	20	V
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS40400 RHL (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise stated, these specifications apply for –40°C ≤ T_J ≤ 125°C, V_{DD}= 12 Vdc, FREQUENCY_SWITCH = 600 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VDD}	Input voltage range		3		20	V
I_{VDD}	Input operating current	Switching, no driver load		6	15	mA
VOLTAGE REFERENCE						
V_{FB}	Feedback pin voltage default settings		594	600	606	mV
$V_{FB(max)}$	Feedback pin voltage maximum adjustment			750		mV
$V_{FB(min)}$	Feedback pin voltage minimum adjustment			450		mV
$V_{FB(inc)}$	Feedback pin voltage adjustment resolution			2.34		mV
$V_{FB(NL)}$	Maximum nonlinearity error over adjustment range				10	mV
BP6 REGULATOR						
V_{BP6}	6-V regulator output voltage		6.2	6.5	6.8	V
V_{DO6}	Regulator dropout voltage, (V_{VDD} – V_{BP6})	V_{VDD} = 6 V, I_{BP6} = 50 mA			300	mV
I_{BP6}	Regulator current limit		100			mA
BP3 REGULATOR						
V_{BP3}	3.3-V regulator output voltage		3.1	3.3	3.5	V
V_{DO3}	Regulator dropout voltage, (V_{VDD} – V_{BP3})	V_{VDD} = 3 V, I_{BP3} = 5 mA		100	200	mV
OSCILLATOR						
f_{SW}	Switching frequency	Factory default setting	480	600	720	kHz
	Nominal frequency range		200		2000	
	Accuracy	3 V ≤ V_{VDD} ≤ 20 V, 200 kHz ≤ f_{SW} ≤ 2 MHz	–20%		20%	
V_{IH}	SYNC high-level input voltage		2			V
V_{IL}	SYNC low-level input voltage				0.4	
I_{SYNC}	SYNC pin leakage current	V_{SYNC} = 6 V			100	nA
		V_{SYNC} = 0 V			100	
t_{SRISE}	Maximum SYNC rise time[1]		100			ns
t_{SYNC}	Minimum SYNC pulse width		100			ns
V_{RMP}	Ramp amplitude[1]	FREQUENCY_SWITCH = 200 kHz	V_{VDD}/6.6	V_{VDD}/6.5	V_{VDD}/6.3	V
		FREQUENCY_SWITCH = 600 kHz	V_{VDD}/7.0	V_{VDD}/6.8	V_{VDD}/6.6	
		FREQUENCY_SWITCH = 2000 kHz	V_{VDD}/10	V_{VDD}/9.6	V_{VDD}/9.2	
V_{VLY}	Valley voltage[1]			0.9		
f_{SYNC}	SYNC range % of nominal oscillator frequency	200 kHz ≤ f_{SW} ≤ 2 MHz	85%		150%	

(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for –40°C ≤ T_J ≤ 125°C, V_{DD}= 12 Vdc, FREQUENCY_SWITCH = 600 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE WIDTH MODULATOR (PWM)						
D_{MAX}	Maximum duty cycle(1) (2)	FREQUENCY_SWITCH = 600 kHz	90%			
		FREQUENCY_SWITCH = 1.2 MHz	85%			
		FREQUENCY_SWITCH = 2 MHz	75%			
$t_{OFF(min)}$	Minimum OFF time			170	225	ns
$t_{ON(min)}$	Minimum controllable pulse(1)	T_J = 25°C, f_{SW} = 600 kHz			75	ns
SOFT-START						
t_{SS}	Soft-start time(3)	Factory default setting	2.7	3.1	3.5	ms
	Accuracy	600 µs ≤ t_{SS} ≤ 9 ms	–15%		15%	
ERROR AMPLIFIER						
GBWP	Gain bandwidth product(1)		15	20		MHz
A_{OL}	DC gain(1)		60			dB
I_{IBFB}	Input bias current: FB (out of pin)		0		100	nA
I_{IBT}	Input bias current: TRACK (out of pin)		0		250	nA
I_{EAOP}	Output source current	V_{FB} = 0 V, V_{COMP} ≥ 2 V	1			mA
I_{EAOM}	Output sink current	V_{FB} = 2 V, V_{COMP} ≤ 0.3 V	1			
V_{COMPH}	Error amplifier high output voltage	V_{FB} = 0 V	3.8			V
V_{COMPL}	Error amplifier low output voltage	V_{FB} = 2 V			50	mV
$V_{TRACK(ofst)}$	TRACK pin offset voltage		–5		5	mV
CURRENT SENSE AMPLIFIER						
I_{ISNS+}	ISNS+ bias current				200	nA
$I_{ISNS–}$	ISNS– bias current				100	µA
V_{ICM}	Input common-mode range		0.45		15	V
AO_{CM}	Common-mode gain				–80	dB
V_{LIN}	Input linear range, VISNS+ - VISNS-(4)		–45		110	mV
CURRENT LIMIT PROTECTION						
t_{OFF}	Off time between restart attempts			6 × t_{SS}		ms
V_{ILIMTH}	V_{CS+} – $V_{CS–}$ voltage that trips OC fault function	Factory default settings(4), T_J = 25°C	27	30	33	mV
	Threshold accuracy	3 V ≤ V_{VDD} ≤ 20 V, 30 mV ≤ V_{ILIMTH} ≤ 110 mV, T_J = 25°C	–10%		10%	
		3V ≤ V_{VDD} ≤ 20 V, V_{ILIMTH} ≤ 30 mV, T_J = 25°C	–3		3	mV
	Comparator offset	V_{ILIMTH} = 30 mV, T_J = 25°C	–3		3	mV
	Temperature coefficient(1)			4000		ppm/°C
t_{DLYOC}	Overcurrent delay	3-mV overdrive, T_J = 25°C		155		ns
V_{ILIMW}	V_{CS+} – $V_{CS–}$ voltage that sets warning status	Factory default settings, T_J = 25°C	12	15	18	mV
	Threshold accuracy	3 V ≤ V_{VDD} ≤ 20V, 1.9 mV ≤ V_{ILIMTH} ≤ 120 mV, T_J = 25°C	–10%		10%	
		3V ≤ V_{VDD} ≤ 20 V, V_{ILIMTH} < 30 mV, T_J = 25°C	–3		3	mV
	Comparator offset	V_{ILIMTH} = 20 mV, T_J = 25°C	–3		3	mV
	Temperature coefficient(1)			4000		ppm/°C
t_{DLYOCW}	Overcurrent warning delay(1)	3-mV overdrive		250		ns
BOOTSTRAP						
V_{BOOT}	Internal diode voltage drop	I_{BOOT} = 5 mA		0.7	1	V
$I_{BOOT(lk)}$	BOOT diode leakage current(1)	(V_{BOOT} – V_{SW}) = 6 V		1		µA

(2) Operation at 3 V reduces maximum duty cycle by approximately 5%.
(3) See *Application and Implementation* section for more information regarding soft-start time setting.
(4) The entire current ripple waveform must remain within the linear range for current reading results to be accurate. DC current level must be zero or greater for accurate results. Current sense does not support applications that sink current. Transient voltages (such as ripple) are permitted to fall below 0 V, but must be within the specified linear range.

Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for –40°C ≤ T_J ≤ 125°C, V_{DD}= 12 Vdc, FREQUENCY_SWITCH = 600 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO						
$V_{UVLO(on)}$	VDD UVLO turn on threshold(5)	Factory default settings (minimum)	2.475	2.75	3.025	V
	Accuracy(5)	2.25 V ≤ V_{VDD} ≤ 20 V, 2.75 V ≤ VIN_ON ≤ 18 V	–10%		10%	
$V_{UVLO(off)}$	VDD UVLO turnoff threshold(5)	Factory default settings (minimum)	2.25	2.5	2.75	V
	Accuracy(5)	2.25 V < V_{VDD} < 20 V, 2.75 V < VIN_OFF < 17.6 V	–10%		10%	
REMOTE VOLTAGE SENSE AMPLIFIER						
V_{IOFST}	Input offset voltage		–10		10	mV
R_{GAIN}	Gain-setting resistor(1)		48	60	72	kΩ
V_{DIFFO}	Output voltage at DIFFO pin	V_{VDD} > 6.5 V	0		6	V
		V_{VDD} = 5 V	0		4.5	
		V_{VDD} = 3 V	0		2.5	
K_{DIFF}	Differential gain of amplifier		0.995	1	1.005	V/V
V_{AGBWP}	Closed-loop bandwidth(1)		2			MHz
I_{VAOP}	Output source current	V_{SNS+} = V_{DIFFO} = 5 V, $V_{SNS–}$ = 0 V	1			mA
I_{VAOM}	Output sink current	V_{SNS+} = 0 V, $V_{SNS–}$ = 4.5 V, V_{DIFFO} = 5 V	1			mA
POWERGOOD						
V_{PGON}	FB pin voltage upper limit for power good on	Factory default settings		648		mV
	FB pin voltage lower limit for power good on			552		
	Accuracy	540 mV < V_{PGON} < 660 mV	–5%		5%	
V_{PGOFF}	FB pin voltage upper limit for power good off	Factory default settings		660		mV
	FB pin voltage lower limit for power good off			540		
	Accuracy	528 mV < V_{PGOFF} < 672 mV	–5%		5%	
R_{PGD}	Pulldown resistance of PGD pin	V_{FB} = 0, I_{PGOOD} = 5 mA			50	Ω
I_{PGDLK}	Leakage current	Factory default settings , 550 mV < V_{FB} < 650 mV, V_{PGOOD} = 5 V	3		15	µA
t_{PGD}	Delay filter from FB(1)			5		µs
OUTPUT VOLTAGE MARGINING						
MRG_{SLP}	VFB slope during margin voltage transition (6)	Factory default settings	250	214	188	V/s
	Accuracy	3 V < V_{VDD} < 20 V, 600 µs < t_{SS} < 9 ms	–15%		15%	
V_{FBMH}	FB pin voltage after margin high command	Factory default settings	650	660	670	mV
V_{FBML}	FB pin voltage after margin low command	Factory default settings	532	540	548	mV
$V_{FBM(max)}$	Maximum FB pin voltage with margin		742	750	758	mV
$V_{FBM(min)}$	Minimum FB pin voltage with margin		445	450	455	mV
$V_{FB(inc)}$	Resolution of FB steps with margin			2.34		mV
OVERVOLTAGE AND UNDERVOLTAGE DETECTION						
V_{OV}	FB pin overvoltage threshold (OV flag)	Factory default settings	638	672	705	mV
	Accuracy	3 V < V_{VDD} < 20 V, 648 mV < V_{OV} < 690 mV	–5%		5%	
V_{UV}	FB pin undervoltage threshold (UV flag)	Factory default settings	502	528	554	mV
	Accuracy	3 V < V_{VDD} < 20 V, 510 mV < V_{OV} < 552 mV	–5%		5%	
PMBus INTERFACE						
V_{IH}	High-level input voltage, CLK, DATA, CNTL		2.1			V
V_{IL}	Low-level input voltage, CLK, DATA, CNTL				0.8	V
I_{IH}	High-level input current, CLK, DATA, CNTL		–10		10	µA
	CNTL		–12		10	
I_{IL}	Low-level input current, CLK, DATA, CNTL		–10		10	µA
	CNTL		–12		10	

(5) Although specifications appear to overlap, hysteresis is assured for UVLO turnon and turnoff thresholds.
(6) Specified by design. Not production tested.

Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for –40°C ≤ T_J ≤ 125°C, V_{DD}= 12 Vdc, FREQUENCY_SWITCH = 600 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage, DATA, $\overline{SMBALRT}$	3 V ≤ V_{VDD} ≤ 20 V, I_{OUT} = 2 mA			0.4	V
I_{OH}	High-level open-drain leakage current, DATA, $\overline{SMBALRT}$	V_{OUT} = 3.6 V	0		10	µA
C_O (6)	Pin capacitance, CLK, DATA			0.7		pF
f_{PMB}	PMBus operating frequency range	Slave mode	10		400	kHz
PMBus ADDRESSING						
I_{ADD}	ADDX pin current		8.23	9.75	11.21	µA
$V_{ADD(L)}$	Address pin illegal low voltage threshold				0.055	V
MEASUREMENT SYSTEM						
t_{IDLY}	Read delay time (7)		153	192	231	µs
I_{RES}	Current measurement resolution (LSB) (8) (9)			122		µV
I_{RNG}	Current measurement range (9) (10)		–45		110	mV
I_{ACC}	Gain accuracy (11)		–3%		3%	
I_{OFST}	Offset		–3		3	mV
$V_{OUT(res)}$	VOUT measurement resolution (LSB)			15.625		mV
$V_{OUT(rng)}$	VOUT voltage measurement range		0		14	V
$V_{OUT(gain)}$	Gain accuracy (11) (12)		–2		2	LSB
$V_{OUT(gain\_adj)}$	Gain adjustment range through PMBus		–10%		10%	
$V_{OUT(ofst)}$	Offset (11) (12)		–3%		3%	
$V_{OUT(ofst\_adj)}$	Gain adjustment range through PMBus		–125		124	mV
$V_{IN(res)}$	V_{IN} measurement resolution			32.5		mV
$V_{IN(rng)}$	V_{IN} voltage measurement range		3		20	V
$V_{IN(gain)}$	Gain accuracy (11) (12)		–2%		2%	
$V_{IN(gain\_adj)}$	Gain adjustment range through PMBus		–10%		10%	
$V_{IN(offst)}$	Offset (11) (12)		–5.5	–2	1.4	LSB
$V_{IN(offst\_adj)}$	Offset adjustment range through PMBus		–2		1.968	V
THERMAL SHUTDOWN						
T_{JSD}	Junction OT shutdown temperature (12)		135	145	155	°C
T_{JSDH}	Shutdown hysteresis (12)		25	30	35	°C
T_{JWRN}	Junction OT warning threshold (12)		120	130	140	°C
T_{JWRNH}	Junction OT warning temperature hysteresis (12)		15	20	25	°C

(7) All read backs are an average of 16 consecutive measurements – not a rolling average. Time is a delay between parameter updates.
(8) Constrained by the resolution of READ_IOUT command. This presents as the greater of 122 µV/ IOUT_CAL_GAIN or 62.5 mA, the resolution of the READ_IOUT command
(9) Voltage is converted to current by dividing by IOUT_CAL_GAIN, the effective value of the resistance used to sense current in the application. Maximum amount that can be reported through PMBus is 64 A.
(10) Current reading is only supported to 0 average. Voltage transients to –45 mV are taken into account when computing this average.
(11) PMBus commands provide for calibration of each device on an individual basis for improved overall system accuracy.
(12) Specified by design. Not production tested.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{HDHI}	High-side driver pullup resistance	(V_{BOOT} – V_{SW}) = 6.4 V, I_{HDRV} = –100 mA, T_J = 25°C		1.25	2.5	Ω
R_{HDLO}	High-side driver pulldown resistance	(V_{BOOT} – V_{SW}) = 6.4 V, I_{HDRV} = 100 mA, T_J = 25°C		1.3	2.6	Ω
R_{LDHI}	Low-side driver pullup resistance	T_J = 25°C		1.25	2.5	Ω
R_{LDLO}	Low-side driver pulldown resistance	T_J = 25°C		0.8	1.5	Ω
t_{HRISE}	High-side driver rise time(1)	C_{LOAD} = 2.2 nF		6	12.1	ns
t_{HFALL}	High-side driver fall time(1)	C_{LOAD} = 2.2 nF	6.3	12.6		ns
t_{LRISE}	Low-side driver rise time(1)	C_{LOAD} = 2.2 nF	6	12.1		ns
t_{LFALL}	Low-side driver fall time(1)	C_{LOAD} = 2.2 nF	4	8		ns
t_{DT}	Anti-cross conduction time	MFR_SPECIFIC_00 bit 0 = 0, (short dead time.)	20		50	ns
I_{SW}	SW pin leakage current (out of pin)	V_{SW} = 0 V			1	µA

(1) Specified by Design. Not production tested.

6.7 Dissipation Ratings(1)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT (°C/W)	AIRFLOW	T_A = 25°C POWER RATING (W)	T_A = 85°C POWER RATING (W)
24-Pin Plastic QFN (RHL)	31.1	Natural Convection	3.21	1.29
	25.2	200 LFM	3.96	1.58
	23	400 LFM	4.36	1.74

(1) Ratings based on JEDEC High Thermal Conductivity (High K) Board. For more information on the test method, see TI Technical Brief SZZA017.

6.8 Typical Characteristics

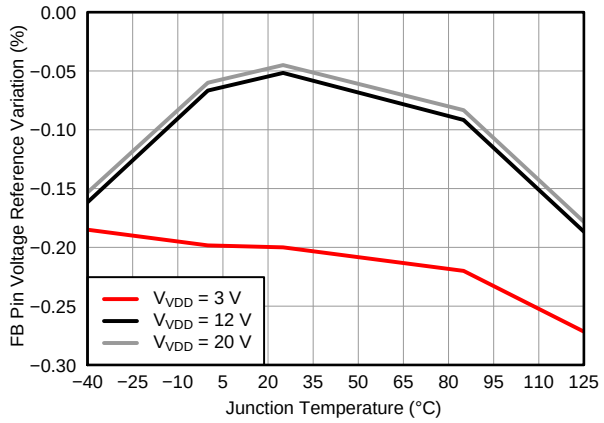


Figure 1. FB Pin Voltage Reference Variation vs Junction Temperature

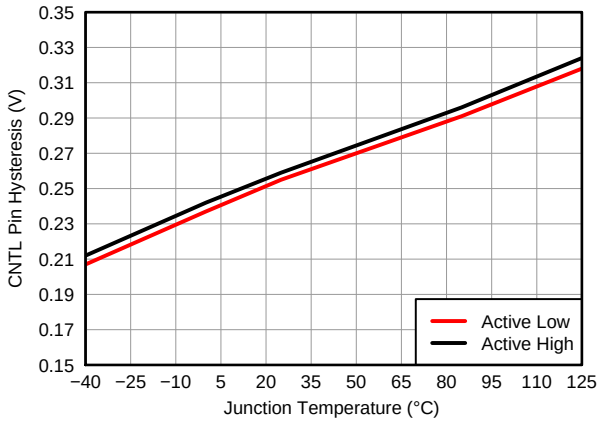


Figure 2. CRTL Pin Hysteresis vs Junction Temperature

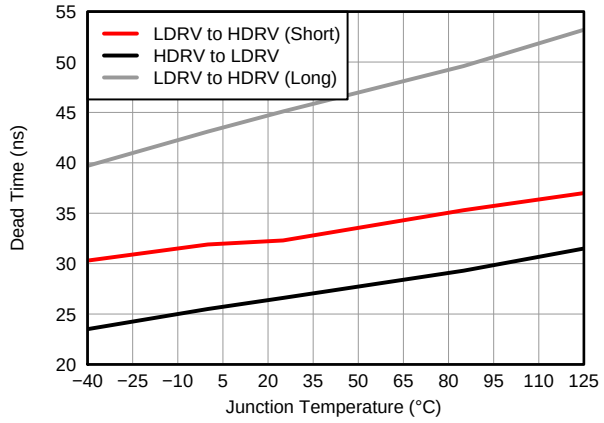


Figure 3. Dead Time vs. Junction Temperature

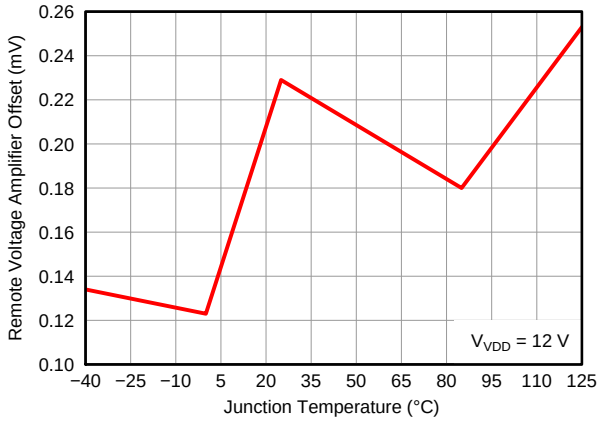


Figure 4. Remote Voltage Amplifier Offset vs Junction Temperature

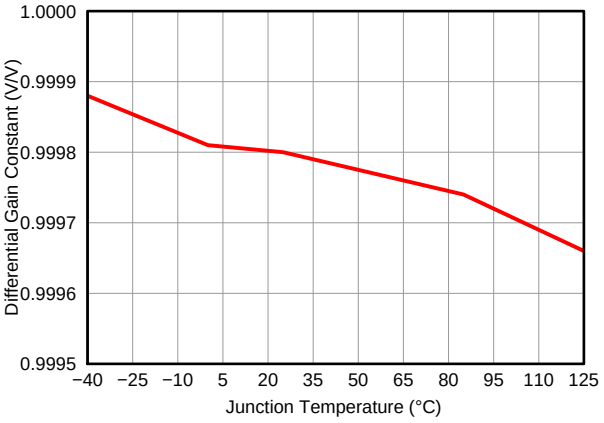


Figure 5. Remote Voltage Amplifier Gain vs Junction Temperature

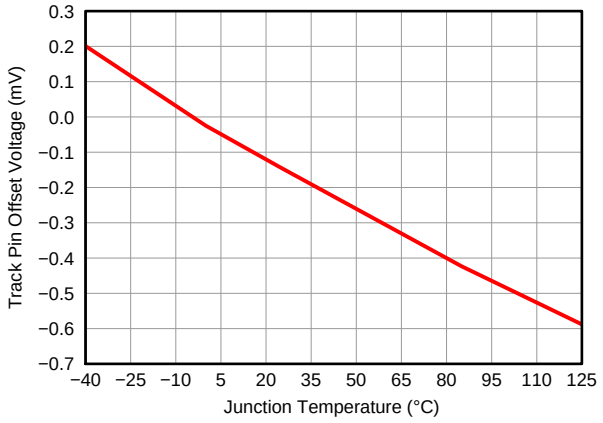


Figure 6. TRACK Pin Offset Voltage vs Junction Temperature

Typical Characteristics (continued)

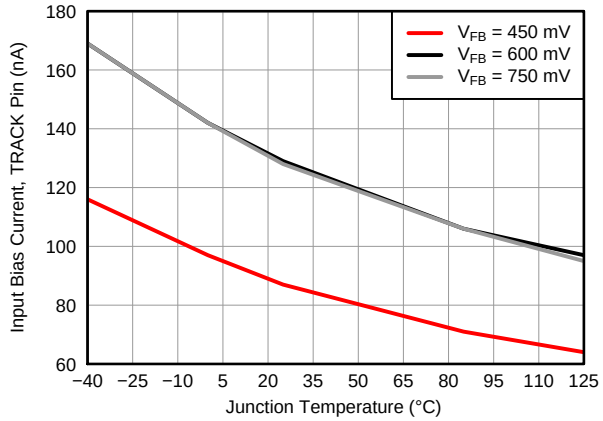


Figure 7. TRACK Pin Input Bias Current vs Junction Temperature

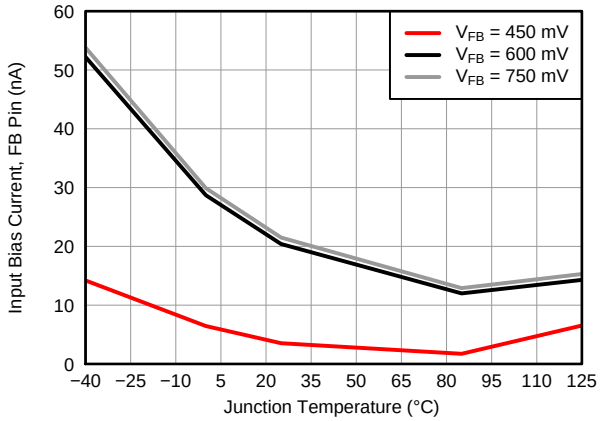


Figure 8. FB pin Input Bias Current vs Junction Temperature

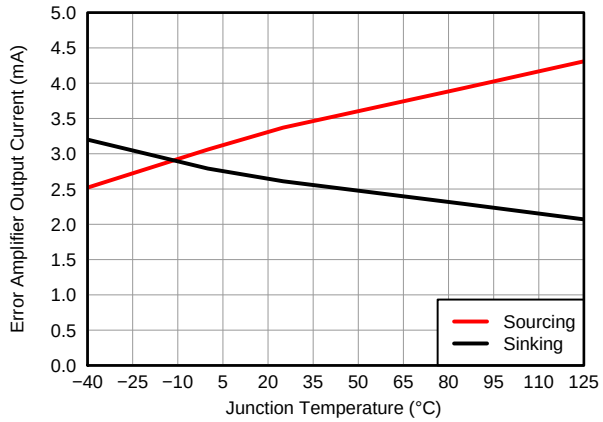


Figure 9. Error Amplifier Output Current vs Junction Temperature

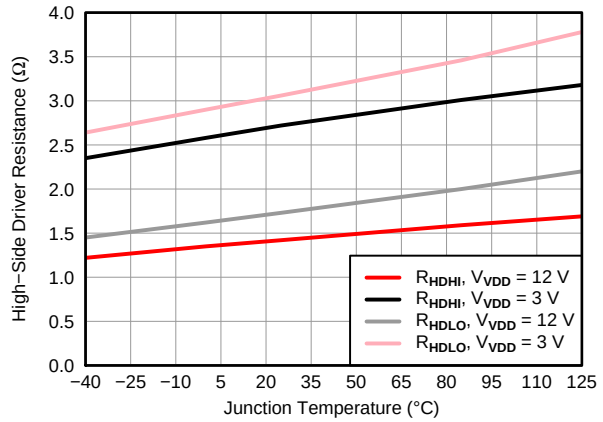


Figure 10. High-Side Driver Resistance vs Junction Temperature

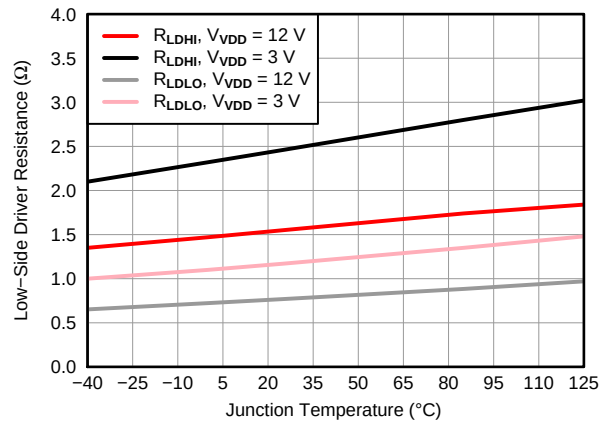


Figure 11. Low-Side Driver Resistance vs Junction Temperature

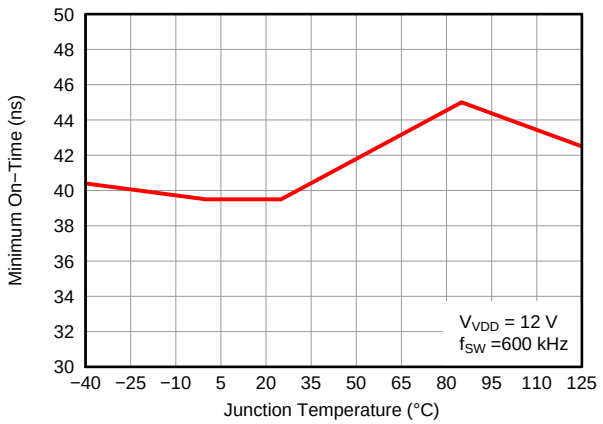


Figure 12. Minimum ON-Time vs Junction Temperature

Typical Characteristics (continued)

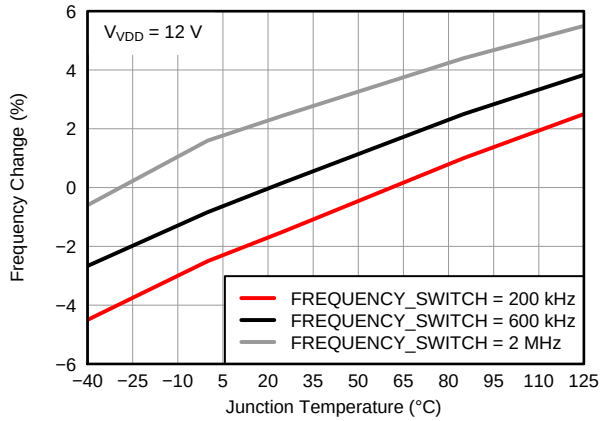


Figure 13. Switching Frequency Change vs Junction Temperature

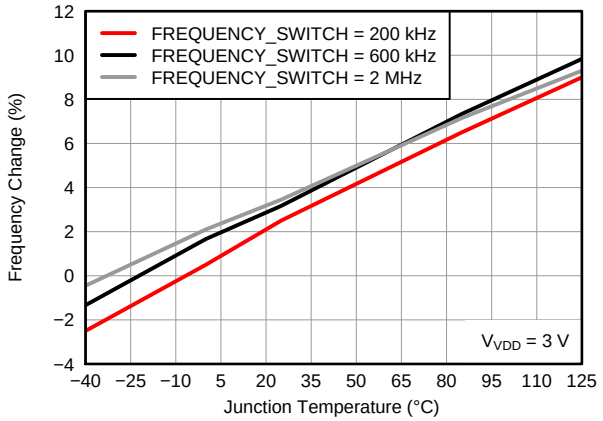


Figure 14. Switching Frequency Change vs Junction Temperature

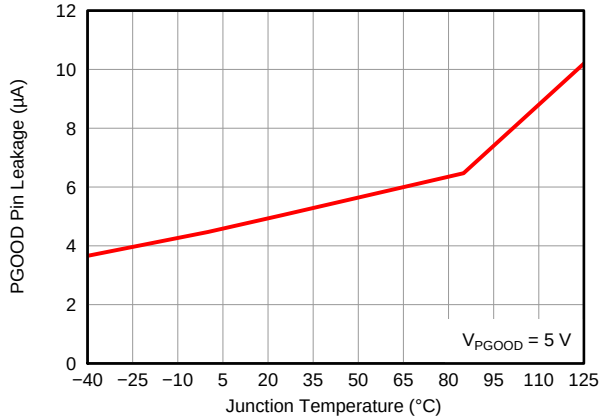


Figure 15. PGOOD Pin Current Leakage vs Junction Temperature

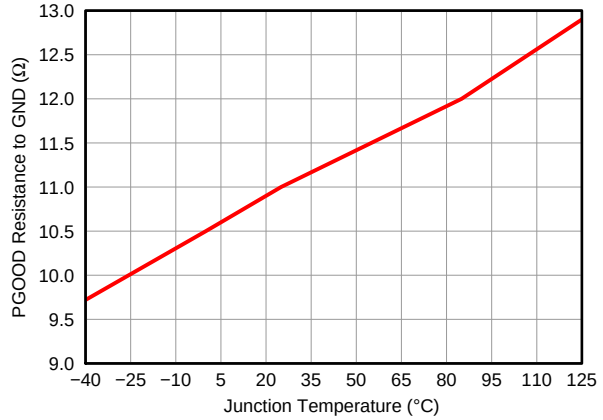


Figure 16. PGOOD Resistance to GND vs Junction Temperature

7 Detailed Description

7.1 Overview

Timing and electrical characteristics of the PMBus can be found in the PMB Power Management Protocol Specification, Part 1, revision 1.1 available at http://pmbus.org. The TPS40400 supports both the 100-kHz and 400-kHz bus timing requirements. The TPS40400 does not stretch pulses on the PMBus when communicating with the master device.

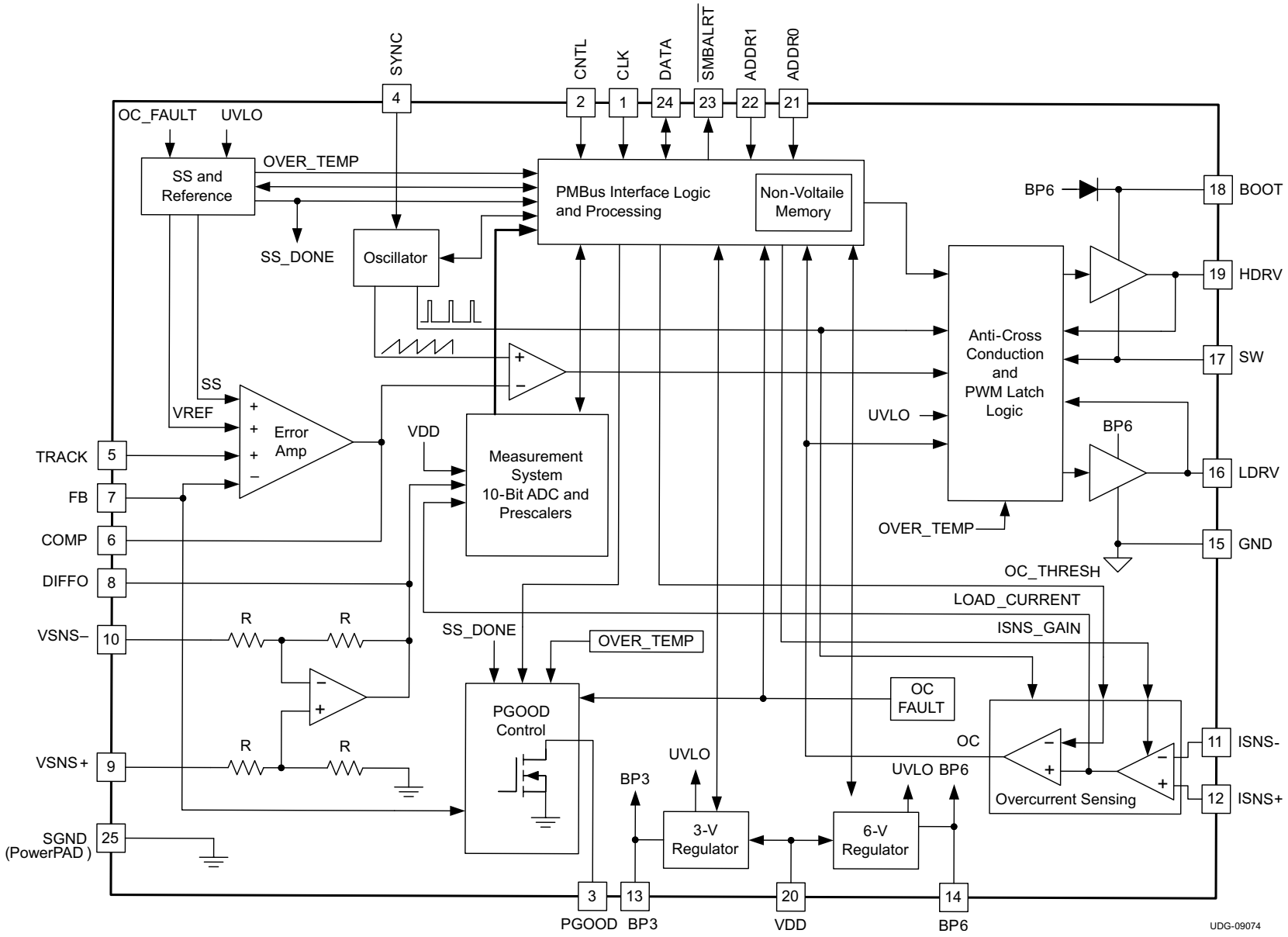
Communication over the TPS40400 device PMBus interface can either support the Packet Error Checking (PEC) scheme or not. If the master supplies CLK pulses for the PEC byte, it is used. If the CLK pulses are not present before a STOP, the PEC is not used.

The TPS40400 supports a subset of the commands in the PMBus 1.1 specification. Most all of the controller parameters can be programmed using the PMBus and stored as defaults for later use. All commands that require data input or output use the literal format. The exponent of the data words is fixed at a reasonable value for the command and altering the exponent is not supported. Direct format data input or output is not supported by the TPS40400. See the *PMBus Functionality and Additional Set-Up* section for specific details.

The TPS40400 also supports the SMBALERT response protocol. The SMBALERT response protocol is a mechanism by which a slave (the TPS40400) can alert the bus master that it experienced a fault condition. The master processes this event and simultaneously accesses all slave devices on the bus (that support the protocol) through the alert response address. Only the slave that caused the alert acknowledges this request. The host performs a modified receive byte operation to get the slave address. At this point, the master can use the PMBus status commands to query the slave that caused the alert. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The TPS40400 contains non-volatile memory that is used to store configuration settings and scale factors. However, the settings programmed into the device are not automatically saved into this non-volatile memory. The STORE_DEFAULT_ALL command must be used to commit the current settings to non-volatile memory as device defaults. The settings that are capable of being stored in non-volatile memory are noted in their detailed descriptions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Voltage Setting

The converter output voltage is set in a way that is similar to a traditional analog controller, by using a voltage divider from the output to the feedback (FB) pin. The output voltage must be divided down to the nominal reference voltage of 600 mV. Figure 17 shows the typical connections for the device. Using the unity gain differential voltage sense amplifier, the TPS40400 can regulate the voltage directly at the load. This method provides better load regulation for output voltages lower than 5-V nominal (see *Electrical Characteristics* table for the maximum output voltage of the differential sense amplifier). For output voltages above this level, connect the output voltage directly to the junction of the R1 resistor and the C1 capacitor, leave DIFFO open, and do not connect the VSNS inputs to the output voltage. In this case, it is also recommended to connect the VSNS+ pin to the BP3 pin and the VSNS– pin to GND. The differential amplifier may also be used as a voltage buffer, provided the electrical specifications are not exceeded

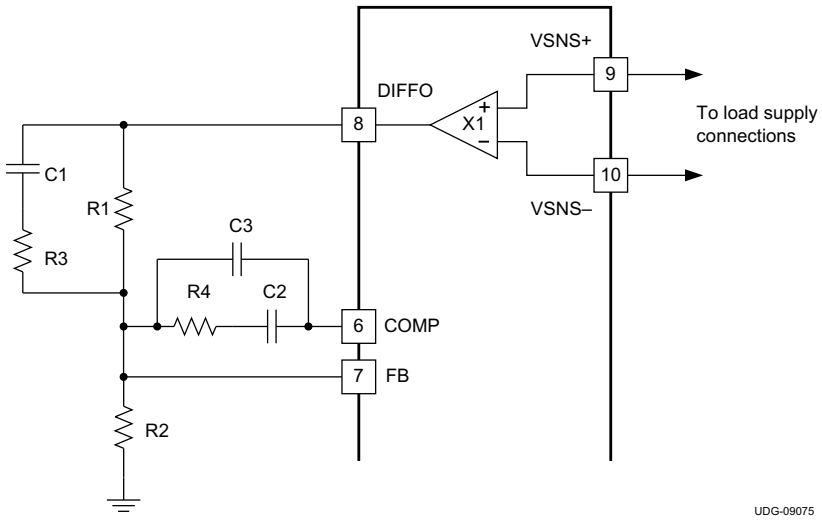


Figure 17. Setting the Output Voltage

The components in Figure 17 that determine the nominal output voltage are R1 and R2. R1 is normally chosen to ensure that the feedback compensation values (R3, R4, C1, C2 and C3) are close to readily available standard values. R2 is then calculated in Equation 1.

$$R2 = V_{FB} \times \left(\frac{R1}{(V_{OUT} - V_{FB})} \right) \quad (1)$$

where

- V_{FB} is the feedback voltage
- V_{OUT} is the desired output voltage
- R1 and R2 are in the same units

The feedback voltage can be changed ±25% from the nominal 600 mV using PMBus commands, allowing the output voltage to vary by the same percentage. See *Output Voltage Adjustment* for further details. After setting the output voltage is set and calculating the values of R1 and R2, calculate the VOUT_SCALE LOOP parameter. The PMBus interface requires this parameter in order to properly adjust the output voltage.

7.3.2 Input Voltage Feedforward

Input voltage feedforward functionality maintains a constant power stage gain as input voltage varies, and provides for very good response to input voltage transient disturbances. The simple constant power stage gain of the device greatly simplifies feedback loop design because loop characteristics remains constant as the input voltage changes, unlike a buck converter without voltage feedforward. For modeling purposes, the gain from the COMP pin to the average voltage at the input of the L-C filter is 6 V/V.

Feature Description (continued)

7.3.3 Output Current Limit and Warning

The TPS40400 device uses a differential current sense scheme to sense the output current. The sense element can be either the series resistance of the power stage filter inductor or a separate current sense resistor. When using the inductor series resistance as in Figure 18, a filter must be used to remove the large AC component of voltage across the inductor and leave only the component of the voltage that appears across the resistance of the inductor. The values of R5 and C4 for the ideal case can be found by Equation 2. The time constant of the R-C filter should be equal to or greater than the time constant of the inductor itself. If the time constants are equal, the voltage appearing across C4 is be the current in the inductor multiplied the inductor resistance. The inductor ripple current is reflected in the voltage across C4 accurately in this case and there is no reason to have a shorter R-C time constant. The time constant of the R-C filter can be made longer than the inductor time constant because this is a voltage mode controller and the current sensing is done for overcurrent detection and output current reporting only. Extending the R-C filter time constant beyond the inductor time constant lowers the AC ripple component of voltage present at the ISNS pins of the device but leaves the correct DC current information intact. This also delays slightly the response to an overcurrent event, but reduces noise in the system leading to cleaner overcurrent performance and current reporting data over the PMBus interface.

$$R5 \times C4 \geq \left(\frac{L}{R_{ESR}} \right) \quad (2)$$

where (from Figure 18)

- R5 and R_{ESR} are in Ω
- C4 is in F (suggest 100 nF
- L is in H

The maximum acceptable voltage across the ISNS pins is 110 mV. Because most inductors have a copper conductor and because copper has a fairly large temperature coefficient of resistance, the resistance of the inductor and the current through the inductor should make a DC voltage less than 110 mV when the inductor is at the maximum temperature for the converter. This also applies for the external resistor shown in Figure 19. The full load output current multiplied by the sense resistor value, must be less that 110 mV at the maximum converter operating temperature.

There is also a constraint on the negative (reverse current) voltage that can be applied to the ISNS pins of the TPS40400 device. The voltage differential from the ISNS+ pin to the ISNS– should not be less than –45 mV. If this condition is not met, inaccurate results from the READ_IOUT command occur. This requirement is intended to limit the ripple voltage. The net current through the inductor must flow towards the load from the input voltage. It is possible for the device to accommodate current sinking, but the device does not support current sinking in overcurrent detection or in the READ_IOUT command.

In all cases, place the component C4 as close as possible to the ISNSx pins to help avoid problems with noise.

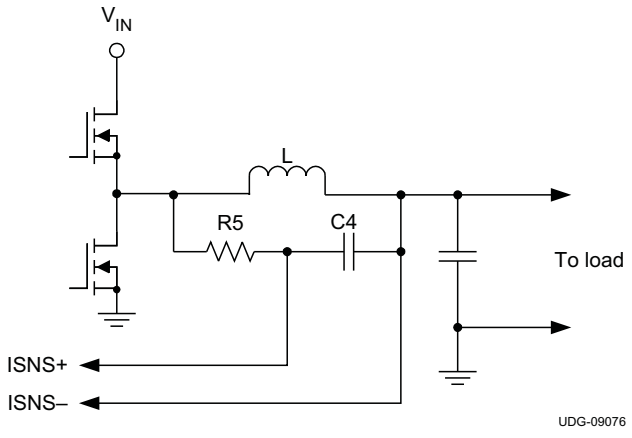


Figure 18. Current Sensing Using Inductor Resistance

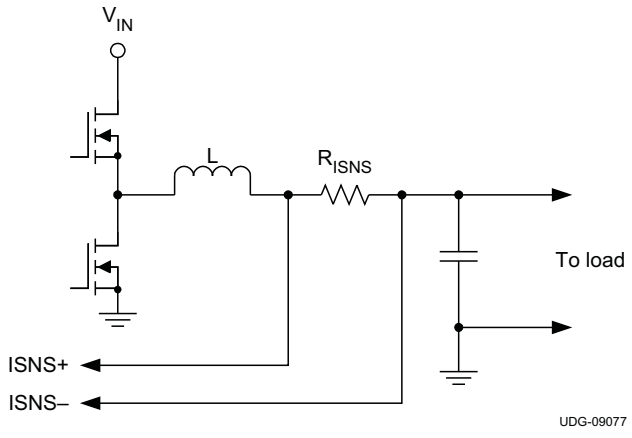


Figure 19. Current Sensing Using Sense Resistor

Feature Description (continued)

After the current sensing method is chosen, determine the resistance of the current sense element. This method allows the proper calculation of thresholds for the overcurrent fault and warning, as well as more accurate reporting of the actual output current. The IOUT_CAL_GAIN command is used to set the value of the sense element resistence of the device. The IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT commands set the levels for the overcurrent warning and fault levels respectively. (See the *PMBus Functionality and Additional Set-Up* section for more details.)

7.3.4 Linear Regulators

Two on-board linear regulators provide power for the internal circuitry of the device. Pin BP3 and BP6 must be bypassed to function properly. The BP3 pin requires a minimum of 100 nF connected between it and GND. The BP6 pin requires approximately 1 µF connected between it and GND.

The external regulator can power other circuits but only if the loads placed on the regulators do not adversely affect operation of the device. Avoid loads with heavy transient currents that can affect the regulator outputs. Transient voltages on these outputs could result in noisy or erratic operation of the TPS40400 device.

It is important to consider current limits. Shorting the BP3 pin to GND damages the BP3 regulator. The BP3 regulator input comes from the BP6 regulator output. The current limit circuit on the BP6 regulator is 100 mA so the total current drawn from both regulators must be less than that. This total current includes the TPS40400 device operating current , $_{VDD}$, plus the gate-drive current required to drive the power MOSFETs. The total available current from two regulators is found in Equation 3 and Equation 4:

$$I_{LIN} = I_{BP6} - (I_{VDD} + I_{GATE}) \quad (3)$$

$$I_{GATE} = f_{SW} \times (Q_{gHIGH} + Q_{gLOW}) \quad (4)$$

where

- I_{LIN} is the total current that can be drawn from BP3 and BP6 in aggregate
- I_{BP6} is the current limit of the BP6 regulator (minimum 100 mA)
- I_{VDD} is the quiescent current of the TPS40400 device (maximum 15 mA)
- I_{GATE} is the gate drive current required by the power MOSFETs
- f_{SW} is the switching frequency
- Q_{gHIGH} is the total gate charge required by the high-side MOSFET
- Q_{gLOW} is the total gate charge required by the low-side MOSFET

7.3.5 PMBus Address

Each device connected to the PMBus interface must have a unique address on the bus acording to the PMBus specification . The TPS40400 device has 64 possible addresses (0 through 63 in decimal) that can be assigned by connecting resistors from the ADDR0 and ADDR1 pins to SGND. The address is set in the form of two octal (0-7) digits, one digit for each pin. ADDR1 is the high-order digit and ADDR0 is the low-order digit.

The E96 series resistors suggested for each digit value are shown in Table 1.

Table 1. E96 Series Resistors

DIGIT	RESISTANCE (kΩ)
0	10
1	15.4
2	23.7
3	36.5
4	54.9
5	84.5
6	130
7	200

The TPS40400 device detects values that are out of range on the ADDR0 and ADDR1 pins. If either pin is detected as having an out of range resistance connected to it, the TPS40400 device continues to respond to PMBus commands at address 127, which is outside of the possible programmed addresses. It is possible (but not recommended) to use the device in this condition, especially if other TPS40400 devices are present on the bus or if another device could possibly occupy the 127 address.

7.3.6 PMBus Connections

The TPS40400 supports both the 100-kHz and 400-kHz bus speeds. Connection for the PMBus interface should follow the *High Power DC specifications* given in section 3.1.3 in the SMBus specification V2.0 for the 400-kHz bus speed or the *Low Power DC specifications* in section 3.1.2. The complete SMBus specification is available from the SMBus web site, smbus.org.

7.3.7 PMBus Functionality and Additional Set-Up

7.3.7.1 Data Format

Three supported PMBus data format commands require representation of a literal number as their argument (commands that set thresholds, set voltages or report those types of settings). A compatible device needs to support only one of these formats. The TPS40400 device supports the *Linear* data format only for these commands. In this format, the data argument consists of two parts, a mantissa and an exponent. The number represented by this argument can be expressed as shown in Equation 5.

$$\text{Value} = \text{Mantissa} \times 2^{\text{exponent}} \tag{5}$$

7.3.7.2 Output Voltage Adjustment

The VOUT_TRIM command adjusts the nominal output voltage of the device. (See the *VOUT_TRIM (22h)* command description for the format of this command as used in the TPS40400 device.) The adjustment range is ±25% from the nominal output voltage. The VOUT_TRIM command is used to trim the final output voltage of the device without relying on high-precision resistors being used as described in the *Figure 17* section. The resolution of the adjustment is 7 bits, with a resulting minimum step size of approximately 0.4%. The output margining function uses this same 7 bit structure so the total combined deviation from the nominal output for margining and VOUT_TRIM is still limited to ±25%. Exceeding this range causes errors.

In order for the PMBus output voltage adjustments to function correctly, the VOUT_SCALE_LOOP parameter must be set properly. VOUT_SCALE_LOOP is a PMBus command (*see Supported PMBus Commands*) that reports the ratio of the voltage divider that sets the nominal output voltage is. The data for this command is the ratio of the divider that is used to set the output voltage. From Figure 17, VOUT_SCALE_LOOP parameter can be calculated using Equation 6.

$$\text{VOUT\_SCALE\_LOOP} = \frac{V_{FB}}{V_{OUT(nom)}} \tag{6}$$

The resolution of the VOUT_SCALE_LOOP command is 0.00195, or slightly less than 0.2% due to the data format of the command (the linear data mode exponent is fixed at –9 for this command). This granularity affects the accuracy of adjustments to the output voltage made using the PMBus (VOUT_TRIM, VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW) as well as setting the overvoltage and undervoltage fault and warning levels. These commands use the VOUT_SCALE_LOOP parameter to calculate the following requirements

- required reference voltage for the requested output voltage
- required thresholds referenced to the FB pin for the requested warning and fault levels

When the VOUT_SCALE_LOOP parameter has been properly set, the commands that adjust the output voltage function properly. The TPS40400 can be in one of three states when considering what the actual output voltage is:

- No output margin
- Margin high
- Margin low

The OPERATION command setting determines the output state. The FB pin reference voltage is calculated as follows in each of these states.

No margin voltage:

$$V_{FB} = \left((VOUT\_TRIM \times VOUT\_SCALE\_LOOP) + 0.6\right) \quad (7)$$

Margin high voltage state:

$$V_{FB} = \left((VOUT\_MARGIN\_HIGH + VOUT\_TRIM) \times VOUT\_SCALE\_LOOP\right) \quad (8)$$

Margin low state:

$$V_{FB} = \left((VOUT\_MARGIN\_LOW + VOUT\_TRIM) \times VOUT\_SCALE\_LOOP\right) \quad (9)$$

where

- V_{FB} is the FB pin voltage
- VOUT_TRIM is the offset voltage in volts to be applied to the output voltage
- VOUT_SCALE_LOOP is the output voltage divider scale parameter
- VOUT_MARGIN_HIGH is the requested margin high voltage
- VOUT_MARGIN_LOW is the requested margin low voltage

For these conditions, the output voltage is shown in Equation 10.

$$V_{OUT} = V_{FB} \times \left(\frac{(R2 + R1)}{R2}\right) \quad (10)$$

where

- V_{FB} is the pin voltage calculated in Equation 7
- R2 and R1 are in consistent units from Figure 17
- VOUT is the output voltage

NOTE

The sum of the margin and trim voltages cannot be more that ±25% from the nominal output voltage. The FB pin voltage can deviate no more that this from the nominal 600 mV.

When using the margin commands, the soft-start time (t_{SS}, set by TON_RISE and the output voltage information available to the device using the VOUT_SCALE_LOOP command) determines the transition rate between any two of the three states (margin high, no margin and margin low) . The transition rate between margin states is the same volts-per-second as the soft-start time, assuming that the user has input the correct value for VOUT_SCALE_LOOP.

7.3.7.3 Overcurrent Threshold

The PMBus interface provides adjustable overcurrent in the TPS40400 device. To function properly, the device requires a value for the current sensing element resistance. Issuing the IOUT_CAL_GAIN command with the argument set to the resistance of the sense element establishes this setting. (See the *IOUT_CAL_GAIN (38h)* command description). The resolution of this command is 30.5 µΩ and the range is 0 to 15.6 mΩ.

Another command, IOUT_CAL_OFFSET (see the *IOUT_CAL_OFFSET (39h)* command description section) can be used to trim out offset errors in the READ_IOUT command results, overcurrent warning and fault level thresholds. The resolution of this command is 62.5 mA Offsets cannot be trimmed closer than half of this amount. The range for this command is -4 A to 3.937 A. Calibrating offsets to a level greater than this is not possible.

After IOUT_CAL_GAIN and IOUT_CAL_OFFSET parameters have been set, the IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT limit commands can be used to set the overcurrent warning and fault thresholds for the device. There are two resolution limiting factors in setting the overcurrent thresholds.

- IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT commands
- Overcurrent DAC can result in lower resolution.

The resolution available in the IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT commands is 500 mA. This limit is the absolute minimum adjustment that can be made to these thresholds.

The overcurrent detection is accomplished using a DAC to set the threshold and a comparator to sense when the actual current level is above that threshold. The resolution of the DAC is 1.875 mV. The resistance of the current sense element and this resolution determine the minimum adjustment that can be made to the overcurrent warning and fault thresholds. That minimum adjustment is given in Equation 11.

$$I_{\Delta OC} = \frac{1.875\,mV}{R_{ISNS}} \tag{11}$$

where

- $I_{\Delta OC}$ is the minimum change that can be made in the overcurrent warning or fault threshold
- R_{ISNS} is the resistance of the current sensing element, either the inductor DC resistance or the resistance of the current sense resistor used

Combining these two resolution limits shows that for current sense elements with a resistance below 3.75 mΩ, the overcurrent resolution is given by Equation 11. For current sense element resistances above 3.75 mΩ, the overcurrent warning and fault resolution is 500 mA.

The TPS40400 device has built in temperature correction for the temperature coefficient of resistance for copper wound inductors used as current sense elements. As the temperature of a copper wound inductor increases, its resistance increases, resulting in a higher DC component of voltage across it for a given current. This leads to a decrease in the current that would actually trip the overcurrent thresholds. The voltages that the device uses to represent the overcurrent thresholds is automatically adjusted higher as the die temperature of the device increases. The temperature coefficient for the increase of the thresholds is chosen close to the temperature coefficient of copper at 4000 ppm/°C. The change in overcurrent threshold voltage from one temperature to another is given in Equation 12.

$$V_{OC2} - V_{OC1} = (T2 - T1) \times (1 + TC_{CU}) \times V_{OC1} \tag{12}$$

where

- V_{OC1} and V_{OC2} are the overcurrent threshold voltages
- T1 and T2 are the corresponding temperatures in °C
- T_{CCU} is the temperature coefficient, 0.004

The change in overcurrent threshold voltages given in Equation 12 maintains the actual overcurrent trip points to a near-constant level only if the die temperature of the device and the copper temperature of the inductor are closely coupled. If the inductor copper temperature rises higher than the die temperature, the overcurrent thresholds appears to decrease and vice versa.

Temperature compensation applied to the overcurrent thresholds must be considered. The threshold voltage must not be or become greater (with the internal temperature compensation) than 110 mV referred to the voltage at the ISNS pins. For instance, when a 10-mΩ resistance inductor is used as the current sense element, a current of 10 A causes a 100-mV DC level at the current sense pins. Initially, this is measurement is within the bounds of the 110 mV limit of the device. However, the temperature compensation of the threshold inside the device raises the effective threshold as the TPS40400 die temperature increases. For a 100°C increase in die temperature, for example, the effective threshold crossed at the ISNS pins to trip an overcurrent is approximately 140 mV at the ISNS pins. The device cannot respond to this level and the result is a failure of the overcurrent mechanism to respond at higher die temperatures. For a given maximum temperature defined by the characteristics of the particular application, Equation 13 shows the maximum overcurrent setting that should be made for the device.

$$I_{MAX} = \frac{V_{ISNS(max)}}{R_{ISNS} \times \left((T_{MAX} - 25) \times (TC_{CU} + 1)\right)} \tag{13}$$

where

- I_{MAX} is the maximum overcurrent threshold setting permissible (using the IOUT_OC_FAULT_LIMIT command) in A
- $V_{ISNS(max)}$ is the maximum allowable voltage differential at the ISNS pins, 120 mV R_{ISNS} is the resistance of the

current sensing element – either inductor or current sense resistor

- T_{MAX} is the maximum junction temperature expected for the TPS40400 device in °C
- TC_{CU} is the temperature coefficient of resistance for copper, 0.004 (13)

Figure 20 shows the variation described in Equation 13; the internal overcurrent threshold as the die temperature increases. In this example, the designated maximum die temperature is 125°C. For the overcurrent threshold to be valid at this temperature (110 mV or below), the maximum overcurrent threshold required using the IOUT_OC_FAULT or IOUT_OC_WARN commands should correspond to no more than 75.7 mV. Equation 13 calculates the current level that achieves this threshold. If the maximum expected die temperature is less than 125°C, then the maximum 25°C overcurrent threshold increases accordingly.

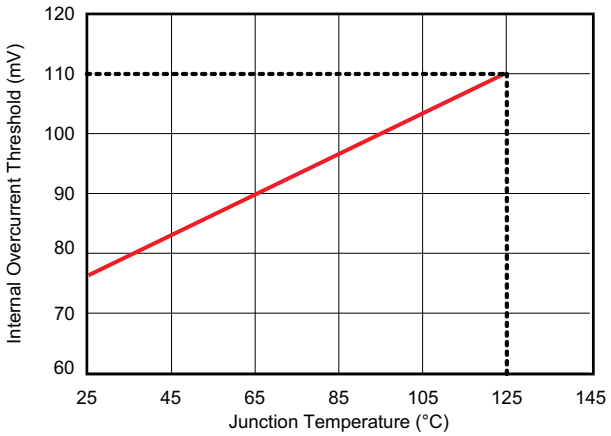


Figure 20. Internal Overcurrent Threshold Variation

7.3.7.4 Output Current Reading

The READ_IOUT command reports the average output current for the converter. The READ_IOUT command can only report positive output current, that is current sourced from the converter. If the converter is sinking current, this command results in a reading of 0 A. Another consideration is the amount of ripple voltage applied to the ISNS pins when the DC voltage level is low (low or no output current). The TPS40400 device averages the ripple voltage measurements when reporting the output current using the READ_IOUT command. Excessive negative ripple voltage ($V_{ISNS+} - V_{ISNS-} < 0$) at the ISNSx pins causes an error in the reported output current. To ensure accurate readings, the differential voltage at these pins should not be allowed to exceed –45 mV.

7.3.7.5 Soft-Start Time

The TPS40400 device supports several soft-start times from 600 µs to 9 ms selected by the TON_RISE PMBus command. See the *TON_RISE (61h)* command description section for full details on the levels and implementation. When selecting the soft-start time, consider the charging current for the output capacitors. In some applications (for example, those with large amounts of output capacitance) this current can lead to problems with nuisance tripping of the overcurrent protection circuitry. To avoid nuisance tripping, include the output capacitor charging current when considering where to set the overcurrent threshold. Equation 14 calculates the output capacitor charging current.

$$I_{CAP} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}}$$

where

- I_{CAP} is the start-up charging current of the output capacitance in A
- V_{OUT} is the output voltage of the converter in V
- C_{OUT} is the total output capacitance in F
- t_{SS} is the selected soft-start time in seconds (14)

After calculating the charging current, calibrate the overcurrent threshold to the sum of the maximum load current and the output capacitor charging current plus some margin. The amount of margin required depends on the individual application, but 25% is a suggested starting point. More or less margin may be required.

7.3.7.6 Power Good

The TPS40400 device includes user selectable power good thresholds. These thresholds determine the voltage at which the PGOOD pin is allowed to go high and the associated PMBus flags are cleared. There are three possible settings. See the *POWER_GOOD_ON (5Eh)* section and *POWER_GOOD_OFF (5Fh)* section command descriptions for complete details. These commands establish symmetrical values above and below the nominal voltage.

Values entered for each threshold should be the voltages corresponding to the threshold below the nominal output voltage. For instance, if the nominal output voltage is 3.3 V, and the desired power good on thresholds are ±5%, the POWER_GOOD_ON command is issued with 2.85 V as the desired threshold. The POWER_GOOD_OFF command must be set to a lower value (higher percentage) than the POWER_GOOD_ON command as well. The VOUT_SCALE_LOOP command must be set to approximately 0.1818 for these examples to work correctly.

The FB pin measures the output voltage to detect the power state. With this method there is the inherent filtering action provided by the compensation network connected from the COMP pin to the FB pin. As the output voltage rises or falls below the nominal value, the error amplifier attempts to force FB to match its reference voltage. When the error amplifier can no longer keep the feedback pin voltage equal to the reference voltage, the FB pin voltage begins to drift away from the reference, and can eventually reach the power good threshold, at which point power good signal is asserted. As a result, the network from the COMP pin to the FB pin should have no purely resistive path.

Power good de-asserts during all start-up sequences, after any fault condition is detected, or whenever the device is turned off or in a disabled state (OPERATION command or CNTL pin put the device into a disabled or off state). The PGOOD pin acts as a diode to GND when the device has no power applied to the VDD pin.

7.3.7.7 Undervoltage Lockout (UVLO)

The TPS40400 device provides flexible user adjustment of the undervoltage lockout threshold and the hysteresis. Two PMBus commands, VIN_ON and VIN_OFF commands allow the user to set these input voltage turn-on and turn-off thresholds independently, with a 500-mV resolution from a minimum of 2.5-V turn-off threshold to a maximum 18-V turn-on threshold. See the *VIN_ON (35h)* and *VIN_OFF (36h)* command description sections for more details.

7.3.7.8 Output Overvoltage and Undervoltage Thresholds

The TPS40400 device has output overvoltage protection and undervoltage protection capability. The comparators that measure the overvoltage conditions and undervoltage conditions use the FB pin as the output sensing point so the filtering effect of the compensation network connected from the COMP pin to the FB pin has an effect on the speed of detection. As the output voltage rises or falls below the nominal value, the error amplifier attempts to force FB to match its reference voltage. When the error amplifier is no longer able to accomplish this match, the FB pin begins to drift and trip the overvoltage threshold or the undervoltage threshold. For this reason the network from the COMP pin to the FB pin should have no purely resistive path.

The VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT commands are used to set the output overvoltage and undervoltage thresholds. There are four possible thresholds that can be set with the undervoltage and overvoltage commands. See the *VOUT_OV_FAULT_LIMIT (40h)* and *VOUT_UV_FAULT_LIMIT (44h)* command description sections for more details.

7.3.7.9 Programmable Fault Responses

For the various fault conditions, the TPS40400 device allows the user to select the fault response. The faults that have programmable responses with the device are overcurrent (see the *VOUT_OV_FAULT_RESPONSE (41h)* command description section), overtemperature, (see the *OT_FAULT_RESPONSE (50h)* command description section), output overvoltage, (see the *VOUT_OV_FAULT_RESPONSE (41h)* command description section) and output undervoltage, (see the *VOUT_UV_FAULT_RESPONSE (45h)* command description section). These commands program the TPS40400 device response to the corresponding fault condition. Possible responses include ignoring the fault, latching off and requiring a reset (either VDD power cycle or a toggling of the CNTL pin and/or OPERATION command status) for the converter to restart. See the *VOUT_OV_FAULT_LIMIT (40h)* and *VOUT_UV_FAULT_LIMIT (44h)* fault response command description section for details on what is available for the specific command.

7.3.7.10 User Data and Adjustable Anti-Cross-Conduction Delay

The TPS40400 device provides a MFR_SPECIFIC_00, command which functions as a scratchpad to store 14 bits of arbitrary data. These bits can represent anything that the user desires and can be stored in EEPROM for non-volatility. Bit 0 of this command selects one of two dead-time settings for the device. The particular setting required for a given application depends upon several values such as total MOSFET gate charge, MOSFET gate resistance, PCB layout quality, temperature).

It is not possible to list specific rules as to when to use which setting, but generally, for MOSFETs with a gate charge above 25 nC, consider a longer dead-time setting. The shorter dead-time setting allows higher efficiency in applications where the MOSFETs are generally small and switch very quickly, but can also lead to minimum amounts of cross conduction in applications with larger, slower switching MOSFETs.

Conversely, using the longer dead-time setting with smaller, faster switching MOSFETs leads to excessive body diode conduction in the low-side MOSFET, leading to a drop in converter efficiency. Bit 1 of this command permanently locks certain parameters from being changed when set to 1. Use this setting with caution. For more detail, see the *MFR_SPECIFIC_00 (D0h)* command description section.

7.4 Device Functional Modes

7.4.1 Continuous Conduction Mode

The TPS40400 device operates in continuous conduction mode (CCM) at a fixed frequency, regardless of the output current.

7.4.2 Operation with CNTL Signal Control

According to the value in the ON_OFF_CONFIG register, the TPS40400 device can be commanded to use the CNTL pin to enable or disable regulation, regardless of the state of the OPERATION command. The minimum input high threshold for the CNTL signal is 2.1 V. The maximum input low threshold for the CNTL signal is 0.8 V. The CNTL pin can be configured as either active high or active low (inverted) logic.

7.4.3 Operation with OPERATION Control

According to the value in the ON_OFF_CONFIG register, TPS40400 device can be commanded to use the OPERATION command to enable or disable regulation, regardless of the state of the CNTL signal.

7.4.4 Operation with CNTL and OPERATION Control

According to the value in the ON_OFF_CONFIG register determines how regulation is enabled or disabled, this device can be commanded to require both a signal on the CNTL pin, and the OPERATION command to enable or disable regulation.

7.4.5 Operation without CNTL or OPERATION Control

According to the value in the ON_OFF_CONFIG register, this device can be commanded to convert power whenever the sensed input voltage is above the programmed UVLO thresholds, VIN_ON and VIN_OFF.

7.4.6 Operation with Output Trim and Margin

The OPERATION command toggles the device between three states:

- Margin None
- Margin Low
- Margin High

In the margin none state, the feedback reference, VREF, is equal to the nominal 600-mV reference, plus any offset defined by the VOUT_TRIM command. In the margin low state, a negative offset defined by the VOUT_MARGIN_LOW command is applied to the feedback reference, moving the converter output voltage down by an equivalent percentage. In the margin high state, a positive offset defined by the VOUT_MARGIN_HIGH command is applied to the feedback reference, moving the converter output voltage up by an equivalent percentage.

7.5 Programming

7.5.1 Supported PMBus Commands

Table 2. Supported PMBus Commands Table

CMD CODE	COMMAND NAME	COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE
01h	*OPERATION*	Can be configured via ON_OFF_CONFIG to be used to turn the output on and off with or without the CNTL pin. Also used to control margin high and margin low.	Margin None. OPERATION does not control On/off.	00h
02h	*ON_OFF_CONFIG*	Configures the combination of CNTL pin input and OPERATION command for turning the output on and off	CNTL only. Active high	17h
03h	*CLEAR_FAULTS*	Clears all fault registers to 00h and releases $\overline{\text{SMB\_ALRT}}$	Write-only	–
10h	*WRITE_PROTECT*	Used to control writing to the device	Allow writes to all registers	00h
11h	*STORE_DEFAULT_ALL*	Stores all current storable register settings into EEPROM as new defaults	Write-only	–
12h	*RESTORE_DEFAULT_ALL*	Restores all storable register settings from EEPROM	Write-only	–
13h	*STORE_DEFAULT_CODE*	Stores individual register settings to EEPROM as new defaults	Write-only	–
14h	*RESTORE_DEFAULT_CODE*	Restores individual register from EEPROM as new defaults	Write-only	–
20h	*VOUT_MODE*	Read-only output mode indicator	Linear. Exponent = –10	16h
22h	*VOUT_TRIM*	Used to apply an offset to the output voltage	$V_{OUT(offst)}$= 0 V	0000h
25h	*VOUT_MARGIN_HIGH*	Used to apply a positive offset to the output voltage in the Margin High state	1.32 V	0547h
26h	*VOUT_MARGIN_LOW*	Used to apply a negative offset to the output voltage in the Margin Low state	1.08 V	0451h
29h	*VOUT_SCALE_LOOP*	Sets the value of the feedback divider ratio	0.5	B900h
33h	*FREQUENCY_SWITCH*	Sets the switching frequency	600 kHz	2813h
35h	*VIN_ON*	Sets the value of the input voltage at which power conversion should start	2.75 V	F00Bh
36h	*VIN_OFF*	Sets the value of the input voltage at which power conversion should stop	2.5 V	F00Ah
38h	*IOUT_CAL_GAIN*	Used to input the current sense element resistance in mΩ	3 mΩ	8862h
39h	*IOUT_CAL_OFFSET*	Used to null offsets in current sense measurements	0.0000 A	E000h
40h	*VOUT_OV_FAULT_LIMIT*	Sets the value of the sensed output voltage which causes an over-voltage fault	1.344 V	0560h
41h	*VOUT_OV_FAULT_RESPONSE*	Sets the converter response to an over-voltage fault	Continue without interruption	04h
44h	*VOUT_UV_FAULT_LIMIT*	Sets the value of the sensed output voltage which causes an under-voltage fault	1.056 V	0439h

Programming (continued)

Table 2. Supported PMBus Commands Table (continued)

CMD CODE	COMMAND NAME	COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE
45h	*VOUT_UV_FAULT_RESPONSE*	Sets the converter response to an under-voltage fault	Continue without interruption	04h
46h	*IOUT_OC_FAULT_LIMIT*	Sets the value of the sensed output current which causes an over-current fault	10 A	F814h
47h	*IOUT_OC_FAULT_RESPONSE*	Sets the converter response to an over-current fault	Continue without interruption	04h
4Ah	*IOUT_OC_WARN_LIMIT*	Sets the value of the sensed output current which causes an over-current warning	7.5 A	F80Fh
50h	*OT_FAULT_RESPONSE*	Sets the converter response to an over-temperature fault	Shutdown and restart when temperature falls by hysteresis	C0h
5Eh	*POWER_GOOD_ON*	Sets the value of the output voltage at which the Power Good signal asserts high	1.104 V	046Ah
5Fh	*POWER_GOOD_OFF*	Sets the value of the output voltage at which the Power Good signal is de-asserted low	1.08 V	0452h
61h	*TON_RISE*	Sets the rise-time of the output voltage at start-up	2.7 ms	E02Bh
78h	*STATUS_BYTE*	Returns one byte summarizing the most critical faults	Read Only	Current Status
79h	*STATUS_WORD*	Returns two bytes summarizing fault and warning conditions	Read Only	Current Status
7Ah	*STATUS_VOUT*	Returns one byte summarizing output voltage fault and warning conditions	Read Only	Current Status
7Bh	*STATUS_IOUT*	Returns one byte summarizing output current fault and warning conditions	Read Only	Current Status
7Dh	*STATUS_TEMPERATURE*	Returns one byte summarizing temperature fault and warning conditions	Read Only	Current Status
7Eh	*STATUS_CML*	Returns one byte summarizing communication, memory and logic fault and warning conditions	Read Only	Current Status
88h	*READ_VIN*	Returns the input voltage in volts	Read Only	Current Status
8Bh	*READ_VOUT*	Returns the output voltage in volts	Read Only	Current Status
8Ch	*READ_IOUT*	Returns the output current in Amperes	Read Only	Current Status
98h	*PMBUS_REVISION*	Returns the PMBus revision to which the device complies	PMBus version 1.1	11h
A0h	*MFR_VIN_MIN*	Describes the minimum input voltage from which the device is able to convert power	3 V	F00Ch
A1h	*MFR_VIN_MAX*	Describes the maximum input voltage from which the device is able to convert power	20 V	F050h
A4h	*MFR_VOUT_MIN*	Describes the minimum output voltage which the converter can supply	0.6 V	0266h

Programming (continued)

Table 2. Supported PMBus Commands Table (continued)

CMD CODE	COMMAND NAME	COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE
A5h	*MFR_VOUT_MAX*	Describes the maximum output voltage which the converter can supply(1)	12 V	3000h
D0h	*MFR_SPECIFIC_00*	User data, write protect extended, and dead-time option selection	25ns, 00h	0000h
D4h	*MFR_SPECIFIC_04* *VOUT_CAL_OFFSET*	Used to apply an offset adjustment to READ_VOUT	0.0000 V	0000h
D5h	*MFR_SPECIFIC_05* *VOUT_CAL_GAIN*	Used to apply a gain adjustment to READ_VOUT	0.00 %	C000h
D6h	*MFR_SPECIFIC_06* *VIN_CAL_OFFSET*	Used to apply an offset adjustment to READ_VIN	0.0000 V	D800h
D7h	*MFR_SPECIFIC_07* *VIN_CAL_GAIN*	Used to apply a gain adjustment to READ_VOUT	0.00 %	C000h
FCh	*MFR_SPECIFIC_44* *DEVICE_CODE*	Identifies the device and revision.	0015h	0015h

(1) The maximum recommended output voltage, using the differential remote sense amplifier is limited to 5.5 V

7.6 Register Maps

7.6.1 OPERATION (01h)

The OPERATION command is used to turn the device output on or off in conjunction with the input from the CONTROL pin. It is also used to set the output voltage to the upper or lower MARGIN voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CONTROL pin instructs the device to change operation modes.

Table 3. OPERATION (01h) Commands

COMMAND	OPERATION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r	r/w	r/w	r/w	r/w	r	r
Function	ON	X	Margin				X	X
Default Value	0	0	0	0	0	0	X	X

7.6.1.1 On

This bit is an enable command to the converter.

- 0: output switching is disabled. Both drivers placed in an off or low state.
- 1: output switching is enabled. The device is allowed to begin power conversion assuming no fault conditions exist.

7.6.1.2 Margin

If Margin Low is enabled, load the value from the VOUT_MARGIN_LOW command. If Margin High is enabled, load the value from the VOUT_MARGIN_HIGH command. (See PMBus specification for more information)

- 00XX: Margin Off
- 0101: Margin Low (Ignore Fault)
- 0110: Margin Low (Act on Fault)
- 1001: Margin High (Ignore Fault)
- 1010: Margin High (Act on Fault)

NOTE

The reference voltages used for overvoltage, undervoltage, and power good detection are derived from the actual reference voltage in effect at the time. It is not possible to set a margin to test for one of these fault conditions. To test for these conditions, force the FB pin to a voltage that trips these fault conditions based on the current reference voltage.

From Margin Low (Act on Fault), output overvoltage (OV) events report in the STATUS registers, but regulation continues, regardless of the VOUT_OV_FAULT_RESPONSE command settings. Output undervoltage faults continue to cause the converter to respond according to the VOUT_UV_FAULT_RESPONSE command settings.

Likewise, from Margin High (Act on Fault), output undervoltage (UV) events report in the STATUS registers, but regulation continues regardless of the VOUT_UV_FAULT_RESPONSE command settings. Output overvoltage faults continue to cause the converter to respond according to the settings in the VOUT_OV_FAULT_RESPONSE command.

7.6.2 ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CNTL pin input and serial bus commands needed to turn the unit on and off. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 4. ON_OFF_CONFIG (02h) Commands

COMMAND	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r
Function	X	X	X	pu	cmd	cpr	pol	cpa
Default Value	X	X	X	1	0	1	1	1

7.6.2.1 Pu

The pu bit sets the default to either operate any time power is present or for the on/off to be controlled by CNTL pin and PMBus OPERATION command. This bit is used in conjunction with the 'cp', 'cmd', and 'on' bits to determine start up.

Table 5. Pu

BIT VALUE	ACTION
0	Device powers up any time power is present regardless of state of the CNTL pin.
1	Device does not power up until commanded by the CNTL pin and OPERATION command as programmed in bits [2:0] of the ON_OFF_CONFIG register.

7.6.2.2 Cmd

The cmd bit controls how the device responds to the OPERATION command.

Table 6. Cmd

BIT VALUE	ACTION
0	Device ignores the “on” bit in the OPERATION command.
1	Device responds to the “on” bit in the OPERATION command.

7.6.2.3 Cpr

The cpr bit sets the CNTL pin response. This bit is used in conjunction with the 'cmd', 'pu', and 'on' bits to determine start up.

Table 7. Cpr

BIT VALUE	ACTION
0	Device ignores the CNTL pin. On/off is controlled only by the OPERATION command.
1	Device requires the CNTL pin to be asserted to start the unit.

7.6.2.4 Pol

The pol bit controls the polarity of the CONTROL pin. For a change to become effective, the contents of the ON_OFF_CONFIG register must be stored to non-volatile memory using either the SOR_DEFAULT_ALL or STORE_DEFAULT_CODE commands and the device power cycled. Simply writing a new value to this bit does not change the polarity of the CNTL pin.

Table 8. Pol

BIT VALUE	ACTION
0	CNTL pin is active low.
1	CNTL pin is active high.

7.6.2.5 Cpa

The cpa bit sets the CNTL pin action when turning the device off. This bit is read internally and cannot be modified by the user.

Table 9. Cpa

BIT VALUE	ACTION
1	Turn off the output and stop transferring energy to the output as fast as possible.

7.6.3 CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT signal output if the device is asserting the SMBALERT signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately reset and the host notified by the usual means.

7.6.4 WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to the device configuration or operation. All supported command parameters may have their parameters read, regardless of the WRITE_PROTECT settings. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 10. WRITE_PROTECT (10h) Commands

COMMAND	WRITE_PROTECT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	X	X	X	X	X
Function	bit7	bit6	bit5	X	X	X	X	X
Default Value	0	0	0	X	X	X	X	X

Table 11. Bit5

BIT VALUE	ACTION
0	Enable all writes as permitted in bit6 or bit7
1	Disable all writes except the WRITE_PROTECT, OPERATION and ON_OFF_CONFIG. (bit6 and bit7 must be 0 to be valid data)

Table 12. Bit6

BIT VALUE	ACTION
0	Enable all writes as permitted in bit5 or bit7
1	Disable all writes except for the WRITE_PROTECT and OPERATION commands. (bit5 and bit7 must be 0 to be valid data)

Table 13. Bit7

BIT VALUE	ACTION
0	Enable all writes as permitted in bit5 or bit6
1	Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data)

In any case, only one of the three bits may be set at any one time. Attempting to set more than one bit results in an alert being generated and the cml bit is STATUS_WORD being set.

7.6.5 STORE_DEFAULT_ALL (11h)

The STORE_DEFAULT_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.

It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed.

EEPROM programming faults cause the device to NACK and set the 'cml' bit in the STATUS_BYTE and the 'oth' bit in the STATUS_CML registers.

7.6.6 RESTORE_DEFAULT_ALL (12h)

The RESTORE_DEFAULT_ALL command restores all of the storable register settings from EEPROM memory.

Do not use this command while the device is actively switching. If this command is used during active switching, the device stops switching the output drivers and the output voltage drops. Depending on loading conditions, the output voltage could reach an undervoltage level and trigger an undervoltage fault response if programmed to do so. The TPS40400 device will not prevent the user from issuing this command during regulation, but it is not recommended as it results in a restart that could disrupt power sequencing requirements in more complex systems. It is strongly recommended that the device be stopped before issuing this command.

NOTE

Issuing RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE to a device which has *latched-off* due to a fault, causes the device to re-enter regulation immediately, without necessitating a toggle of the CNTL signal or OPERATION ON bit.

7.6.7 STORE_DEFAULT_CODE (13h)

The STORE_DEFAULT_CODE command instructs the PMBus core to store the contents of the programming register whose Command Code matches the value in the data byte into memory as the new default value.

Table 14. STORE_DEFAULT_CODE (13h) Commands

COMMAND	STORE_DEFAULT_CODE							
Bit Position	7	6	5	4	3	2	1	0
Access	w	w	w	w	w	w	w	w
Function	Command code							

EEPROM programming faults cause the device to NACK and set the ‘cml’ bit in the STATUS_BYTE and the ‘oth’ bit in the STATUS_CML registers. It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed.

It is permitted to use the STORE_DEFAULT_CODE command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable, undesirable or even catastrophic results. It is recommended to turn off the device output before issuing this command.

NOTE

Not all supported commands have non-volatile memory back-up. The user should avoid issuing a STORE_DEFAULT_CODE or RESTORE_DEFAULT_CODE to commands without non-volatile memory support. This situation can cause the device to become unresponsive. The TPS40400 rejects STORE_DEFAULT_CODE or RESTORE_DEFAULT_CODE attempts to unsupported or read-only registers, but does not prevent the user from attempting to issue these commands to supported, writeable, registers without non-volatile memory back-up, such as the OPERATION command.

7.6.8 RESTORE_DEFAULT_CODE (14h)

The RESTORE_DEFAULT_CODE command instructs the PMBus core to overwrite the programming register whose Command Code matches the value in the data byte, with the default value.

Table 15. RESTORE_DEFAULT_CODE (14h) Commands

COMMAND	RESTORE_DEFAULT_CODE							
Bit Position	7	6	5	4	3	2	1	0
Access	w	w	w	w	w	w	w	w
Function	Command code							

The RESTORE_DEFAULT_CODE command should not be used while the device is switching because the device stops switching and restarts. During the restart, the low-side driver turns on for an extended time period and could damage loads that are sensitive to the power rail sinking current. If this is of no concern then the command may be used while the device is switching.

NOTE

A VIN_UV fault may be triggered when RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE command is set. The firmware workaround is accomplished by verifying that, upon completion of a RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE command, the sole source asserting SMB_ALERT is STATUS_BYTE[3] (VIN_UV). If so, issue a CLEAR_FAULTS command. Any other source asserting SMB_ALERT under these circumstances (that is, completion of RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE) would indicate an actual fault condition.

7.6.9 VOUT_MODE (20h)

The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit mode and 5-bit exponent parameter, as shown below. The 3-bit mode sets whether the device uses the Linear or Direct modes for output voltage related commands. The 5-bit parameter sets the exponent value for the linear data mode. The mode and exponent parameters are set and do not permit the user to change the values.

Table 16. VOUT_MODE (20h) Commands

COMMAND	VOUT_MODE							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Mode			Exponent				
Default Value	0	0	0	1	0	1	1	0

7.6.9.1 Mode

Value fixed at 000, linear mode.

7.6.9.2 Exponent

Value fixed at 11011, Exponent for Linear mode values is –10.

7.6.10 VOUT_TRIM (22h)

The VOUT_TRIM command is used to apply a fixed offset voltage to the output voltage command value. It is most typically use by the end user to trim the output voltage at the time the PMBus device is assembled into the end user system. It is vital that the VOUT_SCALE_LOOP comand is set correctly in order to obtaining correct results. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal).

$$V_{OUT(offst)} = VOUT\_TRIM \times 2^{-10} \quad (15)$$

The maximum value of $V_{OUT(offst)}$ is ±25% of nominal VOUT. Nominal V_{OUT} is set by external resistors and the 600 mV error amplifier reference. The valid range in 2s complement for this command is –4000h to 3FFF. The high order two bits of the high byte must both be either 0 or 1. They cannot have different values. If a value outside of the ±25% is given with this command, the TPS40400 device sets the output voltage to the upper or lower limit depending on the direction of the setting, assert SMBALRT, set the CML bit in STATUS_BYTE and the invalid data bit STATUS_CML.

Table 17. VOUT_TRIM (22h) Commands

COMMAND	VOUT_TRIM															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r(1)	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Bits are sign extend only and are not otherwise programmable.

7.6.11 VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command sets the target voltage which the output changes to when the OPERATION command is set to "Margin High". The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal). The actual output voltage commanded by a margin high command can be found by:

$$V_{OUT(MH)} = (VOUT\_MARGIN\_HIGH + VOUT\_TRIM) \times 2^{-10} \quad (16)$$

The maximum margin range is ±25% of nominal VOUT. Nominal VOUT is set by external resistors and a 600 mV error amplifier reference and does not include the offset generated by VOUT_TRIM. It is critical that the correct value be programmed into VOUT_SCALE_LOOP for the correct margin value to be calculated. Error checking is not performed when the VOUT_MARGIN_HIGH command is issued. The error checking is done when the OPERATION command is issued calling for a margin high state. At that time, values outside the ±25% range is treated as invalid data and causes the set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The output voltage is then set to to the upper or lower limit depending on the direction of the setting. The device state can be restored to power up defaults by issuing either the RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE commands.

Table 18. VOUT_MARGIN_HIGH (25h) Commands

COMMAND	VOUT_MARGIN_HIGH															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	1	0	1	0	0	0	1	1	1

The default value of VOUT_MARGIN_HIGH is 0x547 or 1351. This corresponds to a default margin high voltage of 1.32 V with the default VOUT_SCALE_LOOP value of 0.5 and external resistor selection to give 1.2 V nominal output voltage.

7.6.12 VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command sets the target voltage which the output changes to when the OPERATION command is set to "Margin Low". The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal). The actual output voltage commanded by a margin high command can be found by:

$$V_{OUT(ML)} = \left(VOUT\_MARGIN\_LOW + VOUT\_TRIM\right) \times 2^{-10} \quad (17)$$

The maximum margin range is ±25% of nominal VOUT. Nominal VOUT is set by external resistors and a 600 mV error amplifier reference and does not include the offset generated by VOUT_TRIM. It is critical that the correct value be programmed into VOUT_SCALE_LOOP for the correct margin value to be calculated. Error checking is not performed when the VOUT_MARGIN_LOW command is issued. The error checking is done when the OPERATION command is issued calling for a margin high state. At that time, values outside the ±25% range is treated as invalid data and causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The output voltage is then set to the upper or lower limit depending on the direction of the setting. The device state can be restored to power up defaults by issuing either the RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE commands.

Table 19. VOUT_MARGIN_LOW (26h) Commands

COMMAND	VOUT_MARGIN_LOW															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	1

The default value of VOUT_MARGIN_LOW is 0x451 or 1105. This corresponds to a default margin high voltage of 1.08 V with the default VOUT_SCALE_LOOP value of 0.5 and external resistor selection to give 1.2 V nominal output voltage.

7.6.13 VOUT_SCALE_LOOP (29h)

VOUT_SCALE_LOOP is equal to the feedback resistor ratio. The nominal output voltage is set by a resistor divider and the internal 600mV reference voltage. The default value of VOUT_SCALE_LOOP is 0.5 meaning that the reference voltage is one half of the output voltage. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The correct setting for the VOUT_SCALE_LOOP parameter is shown in Equation 18.

$$VOUT\_SCALE\_LOOP = \frac{V_{FB}}{V_{OUT(nom)}} \tag{18}$$

It is important that this parameter is set correctly because it has an effect on several other parameters. Any parameter that operates on or reports output voltage depends on the correct setting of this parameter for correct results to be obtained.

Table 20. VOUT_SCALE_LOOP (29h) Commands

COMMAND	VOUT_SCALE_LOOP															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent						Mantissa									
Default Value	1	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0

7.6.13.1 Exponent

Value fixed at –9 (dec).

7.6.13.2 Mantissa

Default value is 256 (dec). When combined with the exponent, the overall value of VOUT_SCALE_LOOP is 0.5 (dec). The maximum value for the mantissa is 512 for a VOUT_SCALE_LOOP value of 1.

7.6.14 FREQUENCY_SWITCH (33h)

The FREQUENCY_SWITCH command sets the switching frequency. TPS40400 device only supports frequencies from 200 kHz to 2 MHz. Values written within the supported frequency range is rounded up to the nearest supported increment. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

There are 14 distinct supported frequencies:

- 200 kHz
- 300 kHz
- 400 kHz
- 500 kHz
- **600 kHz (default)**
- 700 kHz
- 800 kHz
- 900 kHz
- 1.0 MHz
- 1.2 MHz
- 1.4 MHz
- 1.6 MHz
- 1.8 MHz
- 1.9 MHz

The data word that accompanies this command is divided into a fixed 5-bit exponent and an 11-bit mantissa. The 5 most significant bits of the mantissa are fixed, while the lower six bits may be altered.

Table 21. FREQUENCY_SWITCH (33h) Commands

COMMAND	FREQUENCY_SWITCH															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1

7.6.14.1 Exponent

Fixed at 5(dec)

7.6.14.2 Mantissa

The upper five bits are fixed at 0.
The lower six bits are writeable with a default value of 19 (dec).

7.6.15 VIN_ON (35h)

The VIN_ON command sets the value of the input voltage at which the unit should start operation assuming all other required start-up conditions are met. Values are mapped to the nearest supported increment. Values outside the supported range are treated as invalid data and cause the device set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The value of VIN_ON remains unchanged on an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 22. Supported VIN_ON Values

SUPPORTED VIN_ON VALUES			
2.75[(1)]	6.50	10.50	14.50
3.00	7.00	11.00	15.00
3.50	7.50	11.50	15.50
4.00	8.00	12.00	16.00
4.50	8.50	12.50	16.50
5.00	9.00	13.00	17.00

(1) Default setting

Table 22. Supported VIN_ON Values (continued)

SUPPORTED VIN_ON VALUES			
5.50	9.50	13.50	17.50
6.00	10.00	14.00	18.00

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5-bit exponent and an 11-bit mantissa. The four most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

Table 23. VIN_ON (35h) Commands

COMMAND	VIN_ON															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	1

7.6.15.1 Exponent

–2 (dec), fixed.

7.6.15.2 Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 11 (dec).

7.6.16 VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop operation. Values are mapped to the nearest supported increment. Values outside the supported range is treated as invalid data and causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The value of VIN_ON remains unchanged during an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 24. Supported VIN_OFF Values

SUPPORTED VIN_OFF VALUES			
2.50(1)	6.50	10.50	14.50
3.00	7.00	11.00	15.00
3.50	7.50	11.50	15.50
4.00	8.00	12.00	16.00
4.50	8.50	12.50	16.50
5.00	9.00	13.00	17.00
5.50	9.50	13.50	17.50
6.00	10.00	14.00	

(1) Default setting

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON resultx in the new value being rejected, SMBALERT being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5 bit exponent and an 11 bit mantissa. The 4 most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

Table 25. VIN_OFF (36h) Commands

COMMAND	VIN_OFF															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	0

7.6.16.1 Exponent

–2 (dec), fixed.

7.6.16.2 Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 10 (dec)

7.6.17 IOUT_CAL_GAIN (38h)

The IOUT_CAL_GAIN is the ratio of the voltage at the current sense element to the sensed current. The units are Ohms (Ω). The effective current sense element can be the DC resistance of the inductor or a separate current sense resistor. The default setting is 3 mΩ, and the resolution is 30.5 μΩ. The range is 0 to 15.6 mΩ. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 26. IOUT_CAL_GAIN (38h) Commands

COMMAND	IOUT_CAL_GAIN															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	0	0	0	1	0	0	0	0	1	1	0	0	0	1	0

7.6.17.1 Exponent

–15 (dec), fixed.

7.6.17.2 Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 98 (dec)

7.6.18 IOUT_CAL_OFFSET (39h)

The IOUT_CAL_OFFSET is used to compensate for offset errors in the READ_IOUT results and the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT thresholds. The units are amps. The default setting is 0 amps. The resolution of the argument for this command is 62.5 mA and the range is +3937.5mA to -4000 mA. Values written outside of this range alias into the supported range. For example, 1110 0100 0000 0001 has an expected value of –63.0625 amps, but results in 1110 0111 1111 0001 which is –0.9375 A. This occurs because the read-only bits are fixed. The Exponent is always –4 and the 5 msb bits of the Mantissa are always equal to the sign bit. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 27. IOUT_CAL_OFFSET (39h) Commands

COMMAND	IOUT_CAL_OFFSET															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

7.6.18.1 Exponent

–4 (dec), fixed.

7.6.18.2 Mantissa

MSB is programmable with sign, next 4 bits are sign extend only.
Lower six bits are programmable with a default value of 0 (dec)

7.6.19 VOUT_OV_FAULT_LIMIT (40h)

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage that causes an output overvoltage fault. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The effective value of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal) so the effective overvoltage trip point requested is:

$$V_{OUT(OV\_req)} = VOUT\_OV\_FAULT\_LIMIT \times 2^{-10} \quad (19)$$

The VOUT_OV_FAULT_LIMIT has two data bytes formatted as 2's complement binary integer. The actual values for the VOUT_ OV_FAULT_LIMIT trip point are set to fixed percentages of nominal V_{OUT}. There are four fixed percentages of the nominal V_{OUT} that are supported for overvoltage trip points.

- 108%
- 110%
- **112% (default)**
- 115%

For example, for a 1.2V nominal output, VOUT_OV_FAULT_LIMIT can be set to 1.296 V, 1.32 V, 1.344 V or 1.38 V. Values within the supported range is set to the nearest fixed percentage. It is critical that the correct value be programmed into VOUT_SCALE_LOOP for the correct overvoltage fault trip point to be calculated. Values outside the supported range results in the corresponding extreme value to be selected. No error conditions are reported

Table 28. VOUT_OV_FAULT_LIMIT (40h) Commands

COMMAND	VOUT_OV_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0	0

7.6.20 VOUT_OV_FAULT_RESPONSE (41h)

Description: The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to a VOUT_OV_FAULT_LIMIT fault. The device also:

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT_OV fault bit in the STATUS_VOUT register, and

- Notifies the host via $\overline{\text{SMBALRT}}$ pin

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

A one-byte unsigned binary data argument is used with this command:

Table 29. VOUT_OV_FAULT_RESPONSE (41h) Commands

COMMAND	VOUT_OV_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/W	r/w	r/w	r/w	r/w	r	r	r
Function	RSP[1]	RSP[0]	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	0	0	0	0	0	1	0	0

7.6.20.1 RSP[1:0]

Output voltage overvoltage response

00: The device continues operation without interruption.

01: The device continues operation for four switching cycles. If the fault is still present, the device shuts down and responds according to RS[2:0].

10: The device shuts down and responds according to RS[2:0].

11: The device shuts down and attempts to restart.

7.6.20.2 RS[2:0]

Output voltage overvoltage retry setting

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal start-up (soft-start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted.

7.6.21 VOUT_UV_FAULT_LIMIT (44h)

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage that causes an output undervoltage fault. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The effective value of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal) so the effective overvoltage trip point requested is:

$$V_{OUT(UV\_req)} = VOUT\_UV\_FAULT\_LIMIT \times 2^{-10} \quad (20)$$

The VOUT_UV_FAULT_LIMIT has two data bytes formatted as two's complement binary integer. The actual values for VOUT_ UV_FAULT_LIMIT trip point are set to fixed percentages of nominal VOUT. There are four fixed percentages of V_{OUT} that are supported for overvoltage trip points.

- 92%
- 90%
- **88% (default)**
- 85%

For example, for a 1.2 V nominal output, VOUT_UV_FAULT_LIMIT can be set to 1.104 V, 1.08 V, 1.056 V or 1.02 V. Values within the supported range are set to the nearest fixed percentage. It is critical that the correct value be programmed into VOUT_SCALE_LOOP for the correct overvoltage fault trip point to be calculated. Values outside the supported range results in the corresponding extreme value to be selected. No error conditions are reported.

The VOUT_UV_FAULT_LIMIT command has two bytes formatted as a two's compliment binary integer:

Table 30. VOUT_UV_FAULT_LIMIT (44h) Commands

COMMAND	VOUT_UV_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	1

7.6.22 VOUT_UV_FAULT_RESPONSE (45h)

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to a VOUT_UV_FAULT_LIMIT fault. The device also:

- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT UV Fault bit in the STATUS_VOUT register, and
- Notifies the host via $\overline{\text{SMBALRT}}$ pin

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

A one-byte unsigned binary data word is used with this command:

Table 31. VOUT_UV_FAULT_RESPONSE (45h) Commands

COMMAND	VOUT_UV_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r	r	r
Function	RSP[1]	RSP[0]	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	0	0	0	0	0	1	0	0

7.6.22.1 RSP[1:0]

Output voltage undervoltage response

00: The device continues operation without interruption.

01: The device continues operation for four switching cycles. If the fault is still present, the device shuts down and responds according to RS[2:0].

10: The device shuts down and responds according to RS[2:0].

11: The device shuts down and attempts to restart.

7.6.22.2 RS[2:0]

Output voltage undervoltage retry setting

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal start-up (soft-start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted.

7.6.23 IOUT_OC_FAULT_LIMIT (46h)

The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current fault condition. The IOUT_OC_FAULT_LIMIT should be set to equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causea the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the SMBALRT signal. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The IOUT_OC_FAULT_LIMIT takes a two-byte data word formatted as follows:

Table 32. IOUT_OC_FAULT_LIMIT (46h) Commands

COMMAND	IOUT_OC_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	0

7.6.23.1 Exponent

–1 (dec), fixed.

7.6.23.2 Mantissa

The upper five bits are fixed at 0.
The lower six bits are programmable with a default value of 20 (dec)

The actual output current for a give mantissa and exponent is shown in Equation 21.

$$I_{OUT(oc)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (21)$$

The default output fault current setting is 10 A. Values of $I_{OUT(oc)}$ can range between 0 A and 35 A in 500-mA increments.

7.6.24 IOUT_OC_FAULT_RESPONSE (47h)

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT fault. The device also:

- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the IOUT/POUT bit in the STATUS_WORD
- Sets the IOUT OC Fault bit in the STATUS_IOUT register, and
- Notifies the host as described in section 10.2.2 of the PMBus Specification.

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 33. IOUT_OC_FAULT_RESPONSE (47h) Commands

COMMAND	IOUT_OC_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r	r	r
Function	RSP[1]	RSP[0]	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	0	0	0	0	0	1	0	0

7.6.24.1 RSP[1:0]

00: The device continues operation without interruption

01: This is unsupported and causes a data error.

10: The device continues operation for four switching cycles. If the fault is still present, the device shuts down and responds according to RS[2:0].

11: The device shuts down and attempts to restart.

7.6.24.2 RS[2:0]

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal start-up (soft-start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted.

7.6.25 IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning. When this current level is exceeded the device:

- Sets the OTHER bit in the STATUS_BYTE
- Sets the OCW bit in the STATUS_WORD
- Sets the IOUT overcurrent Warning (OCW) bit in the STATUS_IOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALRT}}$

The IOUT_OC_WARN_LIMIT threshold should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the $\overline{\text{SMBALRT}}$ signal. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The IOUT_OC_WARN_LIMIT takes a two byte data word formatted as follows:

Table 34. IOUT_OC_WARN_LIMIT (4Ah) Commands

COMMAND	IOUT_OC_WARN_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1

7.6.25.1 Exponent

–1 (dec), fixed

7.6.25.2 Mantissa

The upper five bits are fixed at 0.
Lower six bits are programmable with a default value of 15 (dec)

The actual output warning current level for a give mantissa and exponent is:

$$I_{OUT(oc)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (22)$$

The default output fault current setting is 10A. Values of $I_{OUT(oc)}$ can range from 0 A to 35 A in 500 mA increments. The default output warning current setting is 7.5A.

7.6.26 OT_FAULT_RESPONSE (50h)

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an output over temperature fault. The temperature sensed is the die temperature of the TPS40400 device only. No other temperature sensors are provided. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands. The OT_FAULT_LIMIT parameter is not programmable and is therefore not supported in the PMBus command set. When an over temperature fault condition is sensed, the device:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT FAULT bit in the STATUS_TEMPERATURE register, and
- Notifies the host by asserting the $\overline{\text{SMBALRT}}$ signal

A one-byte unsigned binary data word is used with this command:

Table 35. OT_FAULT_RESPONSE (50h) Commands

COMMAND	OT_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r/w	r	r	r	r	r	r
Function	X	OTF_RS	X	X	X	X	X	X
Default Value	1	1	0	0	0	0	0	0

7.6.26.1 OTF_RS

Over temperature fault retry setting

0: A zero value for the Retry setting indicates that the unit does not attempt to restart.

1: A one value for the Retry setting indicates that the unit goes through a normal start-up (soft-start) when the die temperature falls below the hysteresis band limit. (See the *Electrical Characteristics* table).

7.6.27 POWER_GOOD_ON (5Eh)

The POWER_GOOD_ON command sets the value of the output voltage at which the PGOOD output pin (open drain) is asserted high. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands. The actual implementation is a window comparator with symmetrical thresholds above and below the nominal. This command sets both the upper and lower power good threshold at the same time. The parameter passed with this command is always the lower threshold (less than the nominal output) and is mapped to the closest supported percentages of the nominal output voltage in Table 36.

Table 36. Supported POWER_GOOD_ON Levels

THRESHOLD	
LOW	HIGH
95%	105%
92%(1)	108%
90%	110%

(1) Default value

For example, with a 1.2 V nominal output voltage, the POWER_GOOD_ON command can set the lower threshold to 1.14 V, 1.104 V or 1.08 V. Doing this automatically sets the upper thresholds to 1.26 V, 1.296 V and 1.32 V respectively.

The effective value of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal) so the effective lower power good turn on threshold requested is:

$$V_{OUT(PGOOD\_ON)} = POWER\_GOOD\_ON \times 2^{-10} \quad (23)$$

The nominal output voltage is set by external resistors and a 600-mV error amplifier reference. It is critical that the correct value be programmed into VOUT_SCALE_LOOP in order to correctly select the desired POWER_GOOD_ON threshold.

Normally, the POWER_GOOD_ON threshold is set higher than the POWER_GOOD_OFF threshold. If the POWER_GOOD_ON threshold is set to a value equal to or less than the POWER_GOOD_OFF threshold, the device:

- Sets the CML bit in the STATUS_BYTE
- Sets the Invalid data bit in STATUS_CML
- Notifies the host via $\overline{\text{SMBALRT}}$ pin

It is the user's responsibility to ensure that the chosen POWER_GOOD_ON and POWER_GOOD_OFF thresholds are reasonable with respect to each other. For values written outside the supported ranges are ACK'ed but causes the $\overline{\text{SMBALRT}}$ line to assert and the CML bit to be set in the STATUS_WORD. The invalid data bit is also set in the STATUS_CML results. The actual POWER_GOOD_ON threshold is set to the nearest supported extreme value. For instance, with VOUT_SCALE_LOOP set to 0.5 for a typical 1.2-V output supply, setting POWER_GOOD_ON to 0.5 results in the threshold being set to the 90% value.

The POWER_GOOD_ON command has two data bytes formatted as two’s complement binary integer:

Table 37. POWER_GOOD_ON Commands

COMMAND	POWER_GOOD_ON															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	0	0	1	1	0	1	0	1	0

The default value sets the power good turn on threshold to 1.1035V which maps to the 92% low threshold and 108% high threshold.

7.6.28 POWER_GOOD_OFF (5Fh)

The POWER_GOOD_OFF command sets the value of the output voltage at which the PGOOD output pin (open drain output) is de-asserted low. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands. The actual implementation is a window comparator with symmetrical thresholds above and below the nominal. This command sets both the upper and lower power good threshold at the same time. The parameter passed with this command is always the lower threshold (less than the nominal output) and is mapped to the closest supported percentages of the nominal output voltage below:

Table 38. Supported POWER_GOOD_OFF Levels

SUPPORTED POWER_GOOD_OFF LEVELS	
LOW THRESHOLD	HIGH THRESHOLD
92%	108%
90%(1)	110%
88%	112%

(1) Default value

For example, with a 1.2 V nominal output voltage, the POWER_GOOD_OFF command can set the lower threshold to 1.104 V, 1.0 8V or 1.056 V. Doing this automatically sets the upper thresholds to 1.296 V, 1.32 V and 1.344 V respectively.

The effective value of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal) so the effective lower power good turn on threshold requested are:

$$V_{OUT(PGOOD\_OFF)} = POWER\_GOOD\_OFF \times 2^{-10} \quad (24)$$

The nominal output voltage is set by external resistors and a 600 mV error amplifier reference. It is critical that the correct value be programmed into VOUT_SCALE_LOOP for the correct POWER_GOOD_ON threshold to be selected.

Normally, the POWER_GOOD_ON threshold is set higher than the POWER_GOOD_OFF threshold. If the POWER_GOOD_ON threshold is set to a value equal to or less than the POWER_GOOD_OFF threshold, the device:

- Sets the CML bit in the STATUS_BYTE
- Sets the Invalid data bit in STATUS_CML
- Notifies the host via $\overline{\text{SMBALRT}}$ pin

It is the user's responsibility to make sure that chsen POWER_GOOD_ON and POWER_GOOD_OFF thresholds are reasonable with respect to each other. For values written outside the supported ranges are ACK'ed but cause the $\overline{\text{SMBALRT}}$ line to assert and the CML bit to be set in the STATUS_WORD. The invalid data bit is also set in the STATUS_CML results. The actual POWER_GOOD_OFF threshold is set to the nearest supported extreme value. For instance, with VOUT_SCALE_LOOP set to 0.5 for a typical 1.2-V output supply, setting POWER_GOOD_OFF to 0.5 results in the threshold being set to the 88% value.

The POWER_GOOD_OFF command has two data bytes formatted as two's complement binary integer:

Table 39. POWER_GOOD_OFF (5Fh) Commands

COMMAND	POWER_GOOD_OFF															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1	0

The default value sets the power good turn off threshold to 1.08 V which maps to the 90% low threshold and 108% high threshold.

7.6.29 TON_RISE (61h)

The TON_RISE command sets the time in ms, from when the output starts to rise until the voltage has entered the regulation band. There are several discreet settings that this command supports. Commanding a value other than one of these values results in the nearest supported value being selected.

The supported TON_RISE times over PMBus are as follows. Note that the actual soft-start time is longer than the entered value. Typically the nominal value seen in operation is approximately 15% longer that the time entered.

- 600 µs
- 900 µs
- 1.2 ms
- 1.8 ms
- **2.7 ms (default value)**
- 4.2 ms
- 6.0 ms
- 9.0 ms

A value of 0 ms instructs the unit to bring its output voltage to the programmed regulation value as quickly as possible. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The TON_RISE command is formatted as a linear mode two's complement binary integer.

Table 40. TON_RISE (61h) Commands

COMMAND	TON_RISE															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	1

7.6.29.1 Exponent

–4 (dec), fixed.

7.6.29.2 Mantissa

The upper two bits are fixed at 0.
The lower five bits are programmable with a default value of 43 (dec)

7.6.30 STATUS_BYTE (78h)

The STATUS_BYTE command returns one byte of information with a summary of the most critical device faults. For TPS40400 device, 4 fault bits is flagged in this particular command: output over-voltage, output over-current, over-temperature, and output under-voltage. The STATUS_BYTE reports communication faults in the CML bit. Other communication faults set the NONE OF THE ABOVE bit.

Table 41. STATUS_BYTE (78h) Commands

COMMAND	STATUS_BYTE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMPERATURE	CML	NONE OF THE ABOVE
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OFF:

The device is not providing power to the output, regardless of the reason. In the TPS40400 device, this flag means that the converter is not enabled.

VOUT_OV:

An output overvoltage fault has occurred.

IOUT_OC:

An output over current fault has occurred.

VIN_UV:

An input undervoltage fault has occurred.

TEMPERATURE:

A temperature fault or warning has occurred.

CML:

A **C**ommunications, **M**emory or **L**ogic fault has occurred.

NONE OF THE ABOVE:

A fault or warning not listed in bit1 through bits 1-7 has occurred, for example an undervoltage condition or an over current warning condition

7.6.31 STATUS_WORD (78h)

The STATUS_WORD command returns two bytes of information with a summary of the device's fault/warning conditions. The low byte is identical to the STATUS_BYTE above. The additional byte reports the warning conditions for output overvoltage and overcurrent, as well as the power good status of the converter.

Table 42. STATUS_WORD (78h) Commands

COMMAND	STATUS_WORD (LOW BYTE)							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMPERATURE	CML	NONE OF THE ABOVE
Default Value	0	x	0	0	0	0	0	0

A "1" in any of the low byte (STATUS_BYTE) bit positions indicates that:

OFF:

The device is not providing power to the output, regardless of the reason. In the TPS40400 device, this flag warns that the converter is not enabled.

VOUT_OV:

An output overvoltage fault has occurred.

IOUT_OC:

An output over current fault has occurred.

VIN_UV:

An input undervoltage fault has occurred.

TEMPERATURE:

A temperature fault or warning has occurred.

CML:

A **C**ommunications, **M**emory or **L**ogic fault has occurred.

NONE OF THE ABOVE:

A fault or warning not listed in bits 1-7 has occurred

Table 43. STATUS_WORD (78h) Commands

COMMAND	STATUS_WORD (HIGH BYTE)							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	VOUT	IOUT/POUT	X	X	$\overline{\text{POWER\_GOOD}}$	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of the high byte bit positions indicates that:

VOUT:

An output voltage fault or warning has occurred

IOUT/POUT:

An output current warning or fault has occurred. The PMBus specification states that this also applies to output power. The TPS40400 device does not support output power warnings or faults.

$\overline{\text{POWER\_GOOD}}$:

The power good signal is negated.

7.6.32 STATUS_VOUT (7Ah)

The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults. The TPS40400 device supports only the VOUT_OV Fault and VOUT_UV Fault bits of this register.

Table 44. STATUS_VOUT (7Ah) Commands

COMMAND	STATUS_VOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	VOUT OV Fault	X	X	VOUT UV Fault	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

VOUT OV Fault:

The device detects an output voltage rise above the VOUT_OV_FAULT_LIMIT threshold.

VOUT UV Fault:

The device detects an output voltage fall below the VOUT_UV_FAULT_LIMIT threshold.

7.6.33 STATUS_IOUT (7Bh)

The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults. The TPS40400 device supports only the IOUT_OC Fault and IOUT_OC Warning bits of this register.

Table 45. STATUS_IOUT (7Bh) Commands

COMMAND	STATUS_IOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	IOUT_OV Fault	X	IOUT OC Warning	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

IOUT_OV Fault:

The device detects an output current rise above the level set by IOUT_OC_FAULT_LIMIT.

VOUT_UV Fault:

The device detects an output current rise relating to the level set by IOUT_OC_WARN_LIMIT.

7.6.34 STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the converter temperature related faults. The TPS40400 device supports only the OT Fault and OT Warning bits of this register.

Table 46. STATUS_TEMPERATURE (7Dh) Commands

COMMAND	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	OT Fault	OT Warning	X	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OT Fault:

The device die temperature has exceeded the preset fault threshold.

OT Warning:

The device die temperature has exceeded the preset warning threshold.

7.6.35 STATUS_CML (7Eh)

The STATUS_CML command returns one byte of information relating to the status of the converter's communication related faults. The bits of this register supported by the TPS40400 device are:

Invalid/Unsuppported Command, Invalid/Unsupported Data, Packet Error Check Failed and Other Communication Fault.

Table 47. STATUS_CML (7Eh) Commands

COMMAND	STATUS_CML							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Invalid/Unsuppported Command	Invalid/Unsupported Data	Packet Error Check Failed	X	X	X	Other Communication Fault	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

Invalid/Unsupported Command:

An invalid or unsupported command has been received.

Invalild/Unsupported Data

Invalid or unsupported data has been received

Packet Error Check Failed

A packet has failed the CRC error check.

Other Communication Fault

Some other communication fault or error has occurred

7.6.36 READ_VIN (88h)

The READ_VIN commands returns two bytes of data in the linear data format that represent the input voltage applied to the VDD pin of the device. The data format is as follows:

Table 48. READ_VIN (88h) Commands

COMMAND	READ_VIN															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0

The input voltage is scaled before it reaches the internal analog to digital converter so that resolution of the input voltage read back is 31.25mV. The input voltage can be found using Equation 25.

$$V_{IN} = \text{Mantissa} \times 2^{\text{Exponent}} \times \left(1 + \text{READ\_VIN\_CAL\_GAIN}\right) + \text{READ\_VIN\_CAL\_OFFSET} \quad (25)$$

7.6.36.1 Exponent

Fixed at –5.

7.6.36.2 Mantissa

The lower 10 bits are the result of the ADC conversion of the input voltage. The 11th bit is fixed at 0 because only positive numbers are considered valid.

READ_VIN_CAL_GAIN comes from the MFR_SPECIFIC_06 command

READ_VIN_CAL_OFFSET comes from the MFR_SPECIFIC_07 command

7.6.37 READ_VOUT (8Bh)

The READ_VOUT commands returns two bytes of data in the linear data format that represent the output voltage of the device. The output voltage is sensed at the ISNS- pin so voltage drop to the load is not accounted for. The data format is as follows:

Table 49. READ_VOUT (8Bh) Commands

COMMAND	READ_VOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The setting of the VOUT_MODE affects the results of this command as well. VOUT_MODE is set to linear mode with an exponent of –10 and cannot be altered. The output voltage can be found by:

$$V_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \times \left(1 + \text{READ\_VOUT\_CAL\_GAIN}\right) + \text{READ\_VOUT\_CAL\_OFFSET} \quad (26)$$

7.6.37.1 Exponent

Fixed at -10 by VOUT_MODE

7.6.37.2 Mantissa

Bits 13 (bit 5 in high order byte) through 4 are the result of the ADC conversion of the ouput voltage. The effective LSB using this scheme is 15.625 mV.

READ_VOUT_CAL_GAIN is derived from the MFR_SPECIFIC_05 command

READ_VOUT_CAL_OFFSET is derived from the MFR_SPECIFIC_04 command

7.6.38 READ_IOUT (8Ch)

The READ_IOUT commands returns two bytes of data in the linear data format that represent the output current of the device. The output current is sensed at the ISNS+ and ISNS– pins. The data format is as follows:

Table 50. READ_IOUT (8Ch) Commands

COMMAND	READ_IOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

The output current is scaled before it reaches the internal analog to digital converter so that resolution of the output current read is 62.5 mA, though resolution may be less depending on the setting of IOUT_CAL_GAIN. The maximum value that can be reported is 64 A. It is mandatory that the IOUT_CAL_GAIN and IOUT_CAL_OFFSET parameters are sset correctly in order to obtain accurate results. The output current can be found by using Equation 27.

$$I_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \tag{27}$$

7.6.38.1 Exponent

Fixed at -4.

7.6.38.2 Mantissa

The lower 10 bits are the result of the ADC conversion of the input voltage. The 11th bit is fixed at 0 because only positive numbers are considered valid.

7.6.39 PMBUS_REVISION (98h)

The PMBUS_REVISION command returns a single, unsigned binary byte that indicates that the TPS40400 device is compliant with the 1.1 revision of the PMBus specification.

Table 51. PMBUS_REVISION (98h) Commands

COMMAND	PMBUS_REVISION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Default Value	0	0	0	1	0	0	0	1

7.6.40 MFR_VIN_MIN (A0h)

The MFR_VIN_MIN command returns a two-byte linear formatted result that indicates the minimum voltage from which the TPS40400 device is able to convert power. The data is formatted as follows:

Table 52. MFR_VIN_MIN (A0h) Commands

COMMAND	MFR_VIN_MIN															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0

The minimum input voltage can be found using Equation 28.

$$V_{IN} = \text{Mantissa} \times 2^{\text{Exponent}} \tag{28}$$

This equates to 3 V when evaluated with the default values. The TPS40400 device begins to convert power at a minimum input of 2.75-V.

7.6.40.1 Exponent

Fixed at –2.

7.6.40.2 Mantissa

Fixed at 12.

7.6.41 MFR_VIN_MAX (A1h)

The MFR_VIN_MAX returns a two-byte linear formatted result that represents the maximum specified operating voltage for the TPS40400 device. The data is formatted as follows:

Table 53. MFR_VIN_MAX (A1h) Commands

COMMAND	MFR_VIN_MAX															
Format																
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	1	0	1	0	0	0	0

The maximum input voltage can be found from:

$$V_{IN(min)} = Mantissa \times 2^{Exponent} \quad (29)$$

This equals 20 V when evaluated with the default values.

7.6.41.1 Exponent

Fixed at –2.

7.6.41.2 Mantissa

Fixed at 80.

7.6.42 MFR_VOUT_MIN (A4h)

This command returns a two byte result that represents the minimum output voltage the TPS40400 device supports.

Table 54. MFR_VOUT_MIN (A4h) Commands

COMMAND	MFR_VOUT_MIN															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default Value	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0

The setting of the VOUT_MODE affects the results of this command. VOUT_MODE is set to linear mode with an exponent of -10 and cannot be altered. The minimum nominal output voltage can be found by:

$$V_{OUT(max)} = Mantissa \times 2^{Exponent} \quad (30)$$

This equals to 600 mV using the pre-set values. Using VOUT_TRIM, it is possible to adjust this voltage down to approximately 450 mV.

7.6.42.1 Exponent

Fixed at –10.

7.6.42.2 Mantissa

Fixed at 614.

7.6.43 MFR_VOUT_MAX (A5h)

The command returns a two-byte result that represents the maximum output voltage that the TPS40400 device supports.

Table 55. MFR_VOUT_MAX (A5h) Commands

COMMAND	MFR_VOUT_MAX															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default Value	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

The setting of the VOUT_MODE affects the results of this command. VOUT_MODE is set to linear mode with an exponent of –10 and cannot be altered. The maximum nominal output voltage can be found by:

$$V_{OUT(max)} = \text{Mantissa} \times 2^{\text{Exponent}} \quad (31)$$

This evaluates to 12 V using the pre-set values.

7.6.43.1 Exponent

Fixed at –10.

7.6.43.2 Mantissa

Fixed at 12288

7.6.44 MFR_SPECIFIC_00 (D0h)

The MFR_SPECIFIC_00 command is used for storing arbitrary user data and for selecting a dead time or anti-cross conduction time for the TPS40400 device. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

This command take a two byte unsigned binary argument as follows.

Table 56. MFR_SPECIFIC_00 (D0h) Commands

COMMAND	MFR_SPECIFIC_00															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	USER_DATA								USER_DATA						WPE	DTC
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.6.44.1 Dead-Time Control Setting (DTC)

- 0: Fast. Dead time ≅ 25 ns
- 1: Slow. Dead time ≅ 50 ns

7.6.44.2 WPE

Write protect extension. Writing a 1 to this bit position **permanently locks** the following parameters:

- IOUT_CAL_GAIN
- IOUT_CAL_OFFSET
- FREQUENCY_SWITCH
- IOUT_OC_FAULT_LIMIT

- MFR_SPECIFIC_00

NOTE

Subsequent to setting the WPE bit, either a STORE_DEFAULT_ALL or STORE_DEFAULT_CODE (for MFR_SPECIFIC_00) PMBus command must be issued in order to prevent the WPE bit from being cleared when the device is subjected to a reset-restart operation.

7.6.45 MFR_SPECIFIC_01 (D1h)

This command is used for trimming internal components of the TPS40400 device and is not recommended for general use.

7.6.46 MFR_SPECIFIC_02 (D2h)

This command is used for trimming internal components of the TPS40400 device and is not recommended for general use.

7.6.47 MFR_SPECIFIC_03 (D3h)

This command is used for trimming internal components of the TPS40400 device and is not recommended for general use.

7.6.48 MFR_SPECIFIC_04 (D4h)

This command applies an offset to the READ_VOUT command results to calibrate out offset errors in the on board measurement system. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 57. MFR_SPECIFIC_04 (D4h) Commands

COMMAND	MFR_SPECIFIC_04															
Format	Linear, two's compliment binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Bits are sign extension only and are not otherwise programmable.

Default value: 0

$$READ\_VOUT\_CAL\_OFFSET = Mantissa \times 2^{Exponent} \quad (32)$$

- Exponent is fixed at 2^{-10} by VOUT_MODE
- LSB value is 975 µV
- Range -125 mV to 124 mV

7.6.49 MFR_SPECIFIC_05 (D5h)

This command applies a gain correction to the READ_VOUT command results to calibrate out gain errors in the on board measurement system. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 58. MFR_SPECIFIC_05 (D5h) Commands

COMMAND	MFR_SPECIFIC_05															
Format	Linear, two's compliment binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r(1)	r(1)	r(1)	r(1)	r(1)	r/w	r/w	r/w	r/w	r/w

(1) Bits are sign extension only and are not otherwise programmable.

Table 58. MFR_SPECIFIC_05 (D5h) Commands (continued)

COMMAND	MFR_SPECIFIC_05															
Function	Exponent					Mantissa										
Default Value	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Default value: 0

$$READ\_VOUT\_CAL\_GAIN = Mantissa \times 2^{Exponent}$$

- Exponent is fixed at -8
- LSB value is 0.4%
- Range -0.125 to 0.121 (33)

7.6.50 MFR_SPECIFIC_06 (D6h)

This command applies an offset to the READ_VIN command results to calibrate out offset errors in the on board measurement system. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 59. MFR_SPECIFIC_06 (D6h) Commands

COMMAND	MFR_SPECIFIC_06															
Format	Linear, two's compliment binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r(1)	r(1)	r(1)	r(1)	r(1)	r/w	r(1)	r(1)	r(1)	r(1)	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0

(1) Bits are sign extension only and are not otherwise programmable.

Default value: 0

$$READ\_VIN\_CAL\_OFFSET = Mantissa \times 2^{Exponent}$$

- Exponent is fixed at -5
- LSB value is 32 mV
- Range -2 V to 1.968 V (34)

7.6.51 MFR_SPECIFIC_07 (D7h)

This command applies a gain correction to the READ_VIN command results to calibrate out gain errors in the on board measurement system. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Table 60. MFR_SPECIFIC_07 (D7h) Commands

COMMAND	MFR_SPECIFIC_07															
Format	Linear, two's compliment binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r(1)	r(1)	r(1)	r(1)	r(1)	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Bits are sign extension only and are not otherwise programmable.

Default value: 0

$$READ\_VIN\_CAL\_GAIN = Mantissa \times 2^{Exponent}$$

- Exponent is fixed at -8
- LSB value is 0.4%
- Range -0.125V to 10.121 (35)

7.6.52 MFR_SPECIFIC_44 (FCh)

This command returns a two byte unsigned binary 12-bit device identifier code and 4-bit revision code in the following format.

Table 61. MFR_SPECIFIC_44 (FCh) Commands

COMMAND	MFR_SPECIFIC_44															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Identifier Code												Revision Code			
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1

This command is oriented toward providing similar information to the DEVICE_ID command but for devices that do not support block read and write functions.

7.6.52.1 Identifier Code

Fixed at 1(dec)

7.6.52.2 Revision Code

Starts at 0 and increments as revisions progress.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS40400 device is a step-down DC-DC controller with integrated MOSFET drivers. Input voltage, output voltage and output current telemetry, parametric configuration, and protection features are programmable via the PMBus interface. The device is typically paired with two power MOSFETs and an L-C filter output stage to convert a higher DC voltage to a lower DC voltage. The available output current of a converter using the TPS40400 controller is limited by the choice of power stage components, and over-current protection levels. The maximum allowable over-current protection threshold is 35 A. Use the following design procedure to select component values for a TPS40400 converter. A Loop Compensation Calculator tool is available at www.ti.com to calculate the control loop compensation components, required for stability. The TPS40400 is also supported by Texas Instruments Fusion Digital Power Designer, a graphical software tool set designed to simplify programming, monitoring and configuration of the TPS40400 device via the PMBus interface.

8.2 Typical Applications

8.2.1 TPS40400 12-V Input, 1.2-V Output, 20-A (maximum) Output Current Converter

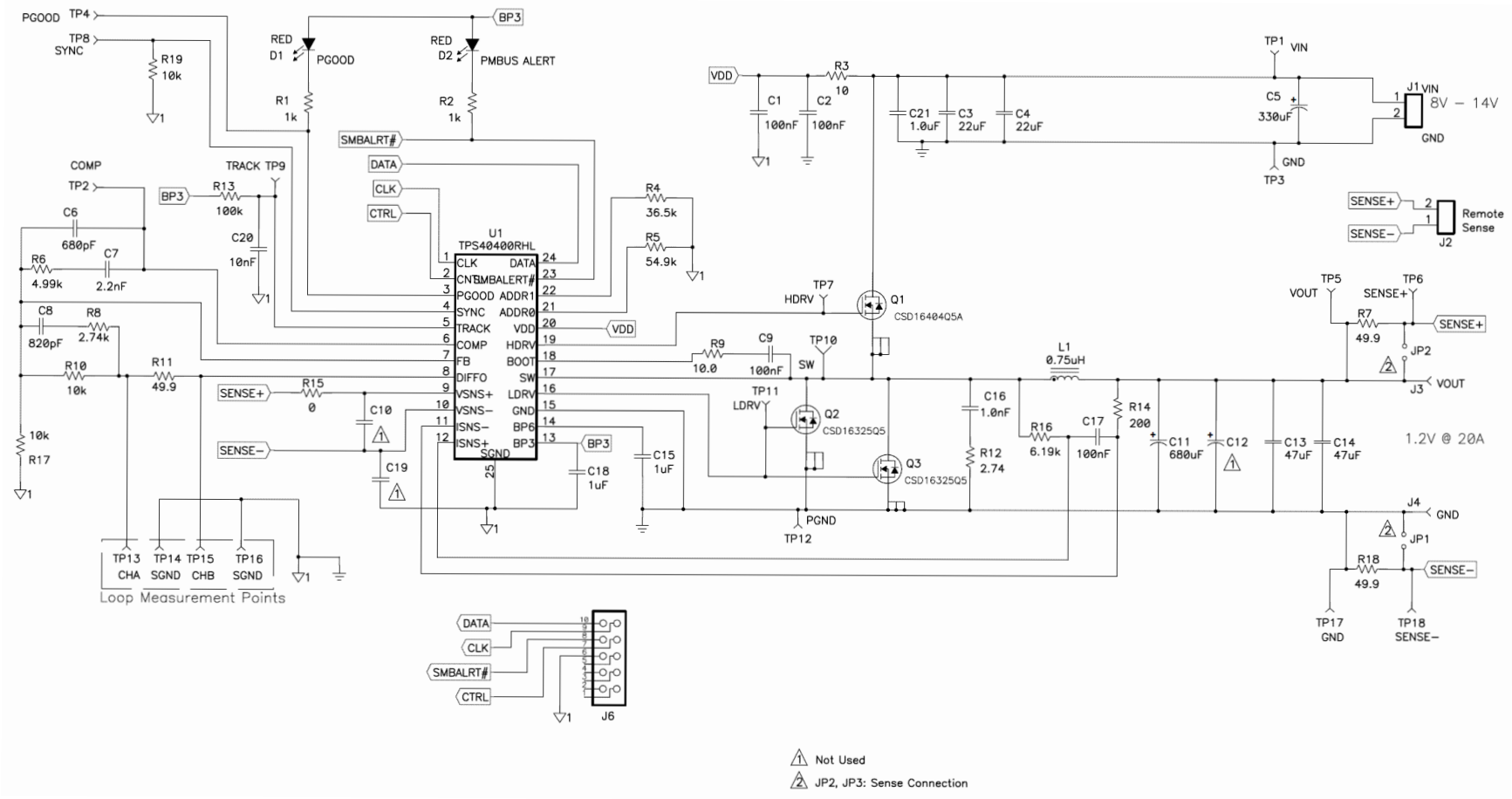


Figure 21. Typical Application Schematic, TPS40400

8.2.1.1 Design Requirements

The following example shows the design process and component selection for a synchronous buck converter using the TPS40400. The design goal parameters are listed in Table 62.

Table 62. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current	V_{IN} = 8 V, I_{OUT} = 20 A		3.6		A
	No load input current	V_{IN} = 12 V, I_{OUT} = 0 A		60		mA
$V_{IN(start)}$	V_{IN} start voltage			7		V
$V_{IN(stop)}$	V_{IN} stop voltage			5		V
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage	V_{IN} = 12 V, I_{OUT} = 20 A	1.08	1.2	1.32	V
	Line regulation	8 ≤ V_{IN} ≤ 14 V, I_{OUT} = 20 A			0.5%	
	Load regulation	V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 20 A			0.5%	
Vout_ripple	Output ripple voltage	V_{IN} = 12 V, I_{OUT} = 20 A			50	mV_{P-P}
Iout	Output current	8 ≤ V_{IN} ≤ 14	0		20	A
I_{OCP}	Output over current inception point	V_{IN} = 12 V	21	25	29	A
SS	Soft-start time	(default)		2.8		ms
	Transient response					
ΔI	Load step	10 A ≤ I_{OUT} ≤ 20 A		10		A
	Load slew rate			1		A/µS
	Overshoot			120		mV
	Settling time			20		µs
SYSTEM CHARACTERISTICS						
f_{SW}	Switching frequency			300		kHz
η_{PK}	Peak efficiency	V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 20 A		90%		
η	Full load efficiency	V_{IN} = 12 V, I_{OUT} = 20 A		85%		
T_{OPER}	Operating temperature range	8 ≤ V_{IN} ≤ 14 V, 0 A ≤ I_{OUT} ≤ 20 A	–40		60	°C

8.2.1.1.1 Design Example List of Materials

Table 63 lists of materials for the 12-V Input, 1.2-V Output, 20-A (maximum) Output Current Converter design.

Table 63. List of Materials

REFERENCE DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C1, C2, C9, C17	4	100 nF	Ceramic, 25 V, X7R, 10%	0603	Std	Std
C11	1	680 µF	Tantalum, 6.3 V, 10%	7343 (D)	TPSE687K006R0045	AVX
C13, C14	2	47 µF	Ceramic, 6.3 V, X7R, 10%	1210	Std	Std
C15, C18	2	1 µF	Ceramic, 16 V, X7R, 10%	0805	Std	Std
C16	1	1.0 nF	Ceramic, 25 V, X7R, 10%	0603	Std	Std
C20	1	10 nF	Ceramic, 50 V, X7R, 10%	0603	Std	Std
C21	1	1.0 µF	Ceramic, 25 V, X7R, 10%	1206	Std	Std
C3, C4	2	22 µF	Ceramic, 25 V, X7R, 10%	1210	Std	Std
C5	1	330 µF	Aluminum, 25 V, 150 mΩ, FC series	10 mm x 12 mm	EEVFC1E331P	Panasonic
C6	1	680 pF	Ceramic, 50 V, X7R, 10%	0603	Std	Std
C7	1	2.2 nF	Ceramic, 50 V, X7R, 10%	0603	Std	Std
C8	1	820 pF	Ceramic, 50 V, X7R, 10%	0603	Std	Std
D1, D2	2	RED	LED, Red, 20-mA, 6-mcd	0603	LTST-C190CKT	Lite On
J1, J2	2	D120/2DS	Terminal block, 2-pin, 15-A, 5.1mm	0.40 inch x 0.35 inch	ED120/2DS	On Shore Technology
J3, J4	2	L35	Type L - copper single conductor, one-hole mount	0.813 inch x 0.375 inch	L35	Thomas and Betts
J6	1	86479-3	Male right angle 2 x 5-pin, 100mil spacing	0.607 inch x 0.484 inch	86479-3	AMP
JP1, JP2	2	PEC02SAAN	Header, 2-pin, 100 mil Spacing	0.100 inch x 2	PEC02SAAN	Sullins
L1	1	0.75 µH	Inductor, SMT, 0.75 µH, 1.2 mΩ, 31A	0.512 x 0.571 inch	PG0077.801	Pulse
Q1	1	CSD16404Q5A	MOSFET, N-channel, 25 V, 20 A, 4.1 mΩ	QFN5X6mm	CSD16404Q5A	TI
Q2, Q3	2	CSD16325Q5	MOSFET, N-channel, 25 V, 33 A, 1.7 mΩ	QFN-8 POWER	CSD16325Q5	TI
R1, R2	2	1 kΩ	Resistor, 1/16-W, 5%	0603	Std	Std
R10, R17, R19	3	10 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R12	1	2.74 kΩ	Resistor, 1/8W, 1%	1206	Std	Std
R13	1	100 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R14	1	200 Ω	Resistor, 1/16W, 1%	0603	Std	Std
R15	1	0 Ω	Resistor, 1/16W, 1%	0603	Std	Std
R16	1	6.19 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R3, R9	2	10 Ω	Resistor, 1/16W, 1%	0603	Std	Std
R4	1	36.5 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R5	1	54.9 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R6	1	4.99 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R7, R11, R18	3	49.9 Ω	Resistor, 1/16W, 1%	0603	Std	Std
R8	1	2.74 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
U1	1	TPS40400RHL	3.0 V to 20 V PMBus synchronous buck controller	QFN-24	TPS40400RHL	TI

8.2.1.2 Detailed Design Procedure

The following design example is for an output of 1.2 V at 20-A maximum, with an input range of 8 V to 14 V.

8.2.1.2.1 Selecting a Switching Frequency

This design example is calculated for a switching frequency of 300 kHz to improve efficiency. The switching frequency can be changed with the Fusion GUI, but some components may need to be revised at other switching frequencies.

8.2.1.2.2 Output Inductor, L_{OUT}

The output inductor value is determined by the peak-to-peak ripple at high line, and in this case a value of 30% of output current maximum is used.

$$L_{OUT} = \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{14 - 1.2}{0.3 \times 20} \times \frac{1}{300\,kHz} = 610\,nH \tag{36}$$

For this design a 750-nH inductor from Pulse (PG0077.801) was selected. The actual ripple current should now be recalculated using the actual inductance value.

$$I_{RIPPLE} = di = dt \times \frac{V_L}{L} = 3.05\,\mu \times \frac{1.2}{0.75\,\mu} = 4.88\,A_{P-P} \tag{37}$$

With this ripple current, the inductor RMS and peak current values can be calculated.

The RMS value of a zero-average triangular wave is given by Equation 38.

$$I_{RMS} = \sqrt{(I_{DC})^2 + (I_{AC})^2} = \sqrt{(20)^2 + \left(\frac{4.88}{\sqrt{12}}\right)^2} = 20.05\,A_{RMS} \tag{38}$$

At maximum load and maximum line, the peak inductor current is given by Equation 39.

$$I_{PEAK} = I_{DC} + \frac{I_{P-P}}{2} = 20 + \frac{4.88}{2} = 22.44\,A_{PEAK} \tag{39}$$

The DCR of the selected inductor (from the data sheet) is 1.2 mΩ. Inductor conduction losses are described in Equation 40.

$$P = I^2 \times R = (I_{RMS})^2 \times DCR = (20.05)^2 \times 1.2\,m\Omega = 0.482\,W \tag{40}$$

8.2.1.2.3 Output Capacitance, C_{OUT}

The selection of the output capacitor is typically affected by the output transient response requirement. Equation 41 and Equation 42 can be used to over-estimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance. The estimate of C_{OUT} based on overshoot is shown in Equation 41.

$$V_{OVERSHOOT} < \frac{\Delta I_{OUT}}{C_{OUT}} \times \Delta t = \frac{\Delta I_{OUT}}{C_{OUT}} \times \frac{\Delta I_{OUT} \times L_O}{V_{OUT}} = \frac{(\Delta I_{OUT})^2 \times L_O}{V_{OUT} \times C_{OUT}} \tag{41}$$

The estimate of C_{OUT} based on undershoot is shown in Equation 42.

$$V_{UNDERSHOOT} < \frac{\Delta I_{OUT}}{C_{OUT}} \times \Delta t = \frac{\Delta I_{OUT}}{C_{OUT}} \times \frac{\Delta I_{OUT} \times L_O}{(V_{IN} - V_{OUT})} = \frac{(\Delta I_{OUT})^2 \times L_O}{(V_{IN} - V_{OUT}) \times C_{OUT}} \tag{42}$$

When $V_{IN(min)} > 2 \times V_{OUT}$, use the overshoot equation ($V_{Overshoot}$) to calculate minimum output capacitance. When $V_{IN(min)} < 2 \times V_{OUT}$ use the undershoot equation ($V_{Undershoot}$). In this design example, $V_{IN(min)}$ is much larger than $2 \times V_{OUT}$ so Equation 43 is used to determine the required minimum output capacitance.

$$C_{OUT} = \frac{(\Delta I_{OUT})^2 \times L_{OUT}}{V_{OUT} \times V_{OVERSHOOT}} = \frac{(10)^2 \times 750\,nH}{1.2 \times 120\,mV} = 520\,\mu F \tag{43}$$

8.2.1.2.4 The Resistive Component of Output Ripple

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated by Equation 44.

$$ESR_{MAX} = \frac{V_{SPEC} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{SPEC} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}} = \frac{50\,mV - \left(\frac{4.88}{8 \times 521\,\mu F \times 300\,kHz}\right)}{4.88} = 9.45\,m\Omega \tag{44}$$

The factor of 8 in the equation above results from the calculation of capacitor voltage resulting from a triangular current. For this design, a 680-µF, 45-mΩ ESR, 5-nH ESL tantalum and two, 47-µF, 3-mΩ ESR, 0.9-nH ESL ceramic capacitors were selected for a total capacitance of 780 µF.

8.2.1.2.5 Peak Current Rating of the Inductor

With the output capacitance known, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is shown in Equation 45 and the resulting peak inductor current is shown in Equation 46 .

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{1.2 \times (680\,\mu + 2 \times 47\,\mu)}{3.1\,m} = 0.3\,A \quad (45)$$

$$I_{L1(peak)} = I_{OUT(max)} + \left(\frac{I_{RIPPLE}}{2}\right) + I_{CHARGE} = 20 + \left(\frac{4.88}{2}\right) + 0.3 = 23.04\,A \quad (46)$$

8.2.1.2.6 Input Capacitance, C_{IN}

The input capacitor is selected to limit the input ripple voltage to 20% or less of V_{IN}. The ripple voltage is due to the current flowing in the input capacitor's ESR as well as capacitance charging and discharging. To simplify the calculations, an infinitely large series input inductance is assumed. With an infinite inductor, the input capacitor current is calculated to be 5.6 Arms.

For reasons of availability, consider the capacitor EEVFC1E331P, which is an electrolytic, 330-µF, 25-V capacitor with 150-mΩ of ESR and 100-nH ESL. This capacitor has an rms current rating of 670 mA. With the calculated rms value of the capacitor current of 5.6 Arms, this implies that needs to be additional capacitance with a much lower ESR across the input bus in order to divert most of the AC current to this low ESR capacitor.

Another readily available capacitor is selected. A 22-µF, ceramic, 25-V, 10-mΩ ESR, 0.9-nH ESL device, two in parallel. With these capacitors in parallel, the ripple in the electrolytic is well within its rating with a value of 329 mA_{rms}.

8.2.1.2.7 Switching MOSFETs, Q_{HS} and Q_{LS}

The high-side and low-side MOSFETs, Q_{HS} and Q_{LS}, are selected based on several factors including:

- Vds, the drain to source voltage rating. This design requires a 25-V device
- Vgs, the gate to source voltage rating. For the TPS40400 device this voltage is 6.5 V
- Conduction losses, based on $I^2 \times R_{DS(on)}$
- Gate charge, must be low enough to be driven by the PWM controller

These devices are selected:

Table 64. MOSFET Summary

LOCATION	PART NUMBER	VOLTAGE RATING (V)	$R_{DS(on)}$ (mΩ)	GATE CHARGE Q_G(nC)	QTY
High-side	CSD16404Q5A	25	4.1	8	1
Low-side	CSD16325Q5	25	1.7	25	2

Because the selected MOSFETs are switch very quickly, the device is programmed to have the shorter dead-time of 25 ns.

8.2.1.2.8 Device Addressing, R_{ADDR0} and R_{ADDR1}

The PMBus address for the device must be read from the ADDR0 and ADDR1 pins. Each pin has an internal fixed current source and the resulting developed voltage is read and converted to the desired device address. The external resistors R_{ADDR0} and R_{ADDR1} from the address pins to ground set eight possible states for a total of 64 possible addresses. The address states are determined by voltages on the address pins per Table 65.

Table 65. Address Configuration

DIGIT	RESISTANCE (kΩ)
0	10
1	15.4
2	23.7
3	36.5
4	54.9
5	84.5
6	130
7	200

For this design, the address of 34 octal, or 28 decimal is selected arbitrarily. In order to achieve this address, the ADDR0 resistor R5 would be 54.9 kΩ and the ADDR1 resistor R4 would be 36.5 kΩ.

8.2.1.2.9 Current Sense Flter, R16 and C17

Current sensing for the TPS40400 device is typically done by sensing the voltage drop across the output inductor's (L1) DC resistance. In order to do this, the large AC switching voltage forced across L1 must be filtered out so that the measured voltage is only the DC drop. This is done by placing an R-C filter directly across the output choke (high-frequency filter) L1. The R-C combination is chosen such that it provides enough filtering for the application and the time constant is chosen to match that of the output inductor and its ESR, which is shown in Equation 47.

$$\tau = \frac{L1}{DCR} \tag{47}$$

Usually a capacitor value is chosen between 10 nF and 1 µF for this location. A value of 100 nF is arbitrarily chosen, which yields Equation 48.

$$R16 = \frac{L1}{DCR} \times \frac{1}{C} = \frac{750\,nH}{1.2\,m\Omega \times 100\,nF} = 6.25\,k\Omega \tag{48}$$

Choose a standard value of 6.19 kΩ.

The capacitor C17 should be placed as close to the ISNS+ and ISNS– pins as possible to provide good bypass filtering. R16 should be placed close to the inductor to prevent traces with the switch node voltage from being propagated across the PCB and getting close to sensitive pins of the TPS40400 device.

8.2.1.2.10 Voltage Decoupling Capacitors, C_{BP3}, C_{BP6}, and C_{VDD}

Three pins on the TPS40400 device have DC bias voltages. It is necessary to add small decoupling capacitors to these pins. Table 66 shows the recommended minimum values.

Table 66. Voltage Decoupling Capacitor Values

DEVICE LOCATION	RECOMMENDED MINIMUM VALUE	FUNCTION	SELECTED VALUE
C_{BP3}, (C18)	0.1-µF low ESR	V_{CC} for internal controls of the device	1-µF ceramic
C_{BP6}, (C15)	1-µF low ESR	V_{CC} for gate drivers	1-µF ceramic
C_{VDD}, (C1) and (C2)	0.1-µF low ESR	V_{CC} for input power to the device	2 x 100 nF, with additional series 10-Ω filter resistor R3 to filter out switching noise from the power MOSFETs

8.2.1.2.11 Bootstrap Capacitor, C9

Selection of the bootstrap capacitor is based on the total gate charge of the high-side MOSFET and the allowable ripple on the BOOT pin. A ripple of 0.2 V is chosen as maximum for this design. This yields a value described in Equation 49.

$$C_{BOOT} = C9 \geq \frac{Q_{GHS}}{V_{BOOT(ripple)}} \times \frac{8nC}{0.2V} = 40nF \quad (49)$$

Choose a standard value of 100 nF. Additionally, a series resistor R9 is added in order to reducing the turn-on speed of the high-side MOSFET, Q1.

8.2.1.2.12 Snubber R12 and C16

For this design, the snubber function is designed based on an allowable snubber power dissipation. A target value of between 0.25% and 0.5% of the rated output power (P_{OUT}) is used as the starting point for the calculation of the snubber values. Once the snubber values are determined and real hardware is obtained, the snubber values can be adjusted to achieve better results.

$$\frac{Energy}{seconds} = \frac{E}{cycle} \times f_{SW} = 2(events) \times \frac{1}{2} \times C \times V^2 \times 300kHz \quad (50)$$

$$C = \frac{60mW}{V^2 \times 300kHz} = \frac{60mW}{196 \times 300kHz} = 1.02nF \quad (51)$$

$$R = \frac{\frac{Shortest\ Pulse\ Width}{10}}{5 \times C} = \frac{28.6n}{5 \times C} = \frac{28.6n}{5 \times 1n} = 5.72\Omega \quad (52)$$

8.2.1.2.13 Loop Compensaton Components

Using the Texas Instruments SwitcherPro™ design tool and the resulting plant (system) bode plot, a crossover frequency of 20 kHz is selected with 45° of phase margin. The resulting compensation components are listed in Table 67.

Table 67. Component Summary

COMPONENT LOCATION	VALUE
R6	4.99 kΩ
R8	2.74 kΩ
C6	680 pF
C7	2.2 nF
C8	820 pF

8.2.1.2.14 Output Voltage Set Point, R_{BIAS}

The output voltage can be set by choosing and calculating R1 and R_{BIAS}. The V_{OUT} set point is shown in Equation 53.

$$R_{BIAS} = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}} \quad (53)$$

In this design R1 was chosen to be 10 kΩ. R_{BIAS} is calculated to be 10 kΩ.

8.2.1.2.15 Remote Sensing

Remote sensing can be accomplished with the differential amplifier as shown in Figure 22. Resistors RS1 and RS2 (R7 and R18 in the schematic above) are used if the sense connections fail or get damaged. The values of RS1 and RS2 are bound by an upper value such that the voltage drop across them does not introduce appreciable voltage regulation error from the bias current, and a lower value such that the voltage drop in the load wires which appears across these resistors does not dissipate appreciable power. Values between 10 Ω to 50 Ω are usually chosen.

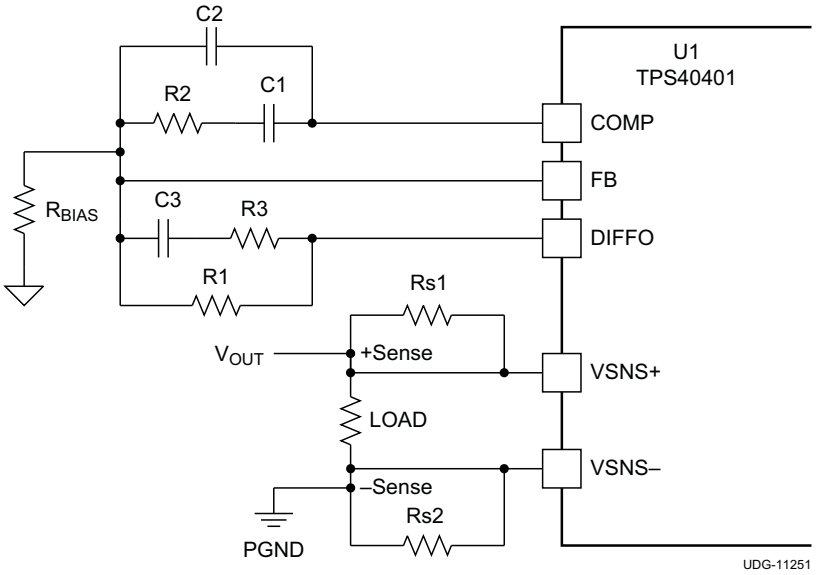


Figure 22. Remote Sense Function

8.2.1.3 Application Curves

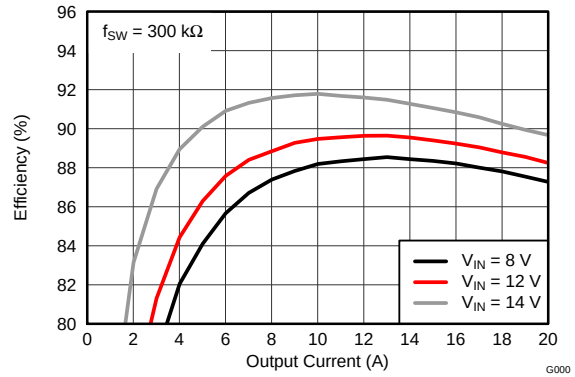


Figure 23. Efficiency

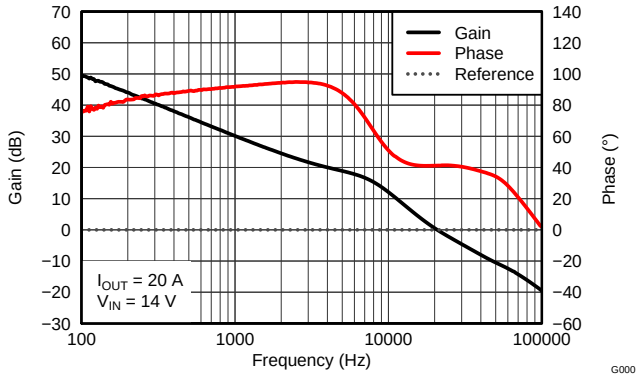


Figure 24. Plant (System) Bode

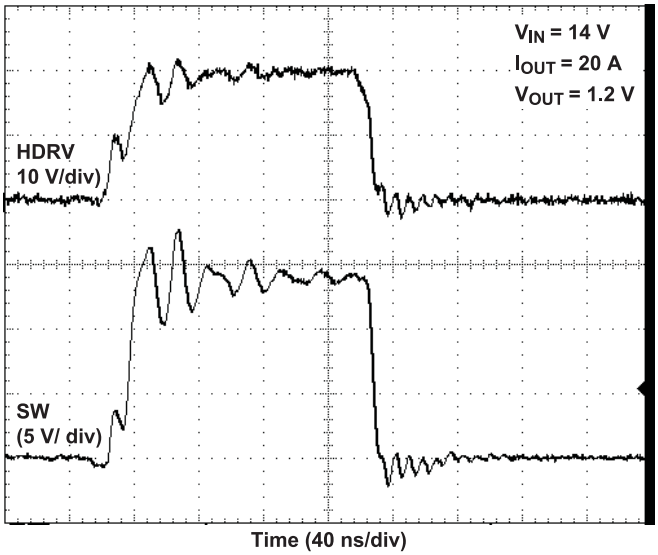


Figure 25. Switching Waveform

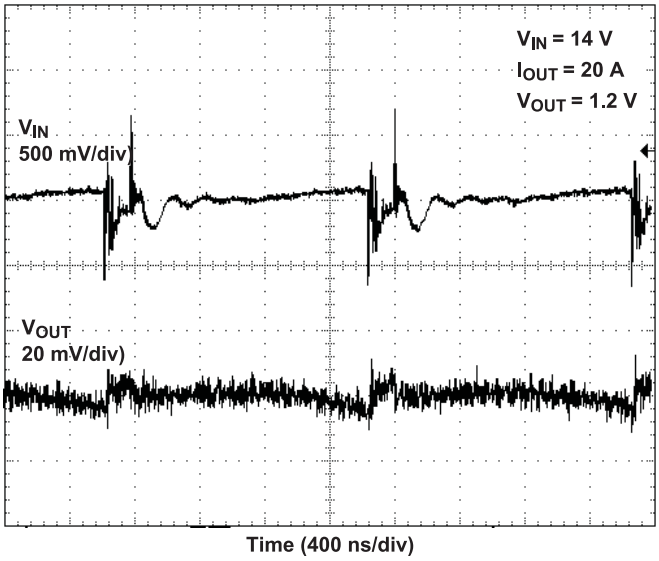


Figure 26. Ripple Waveform

8.2.2 TPS40400 12-V Input 5-V Output, 5-A (Maximum) Output Current Converter Design Example 2

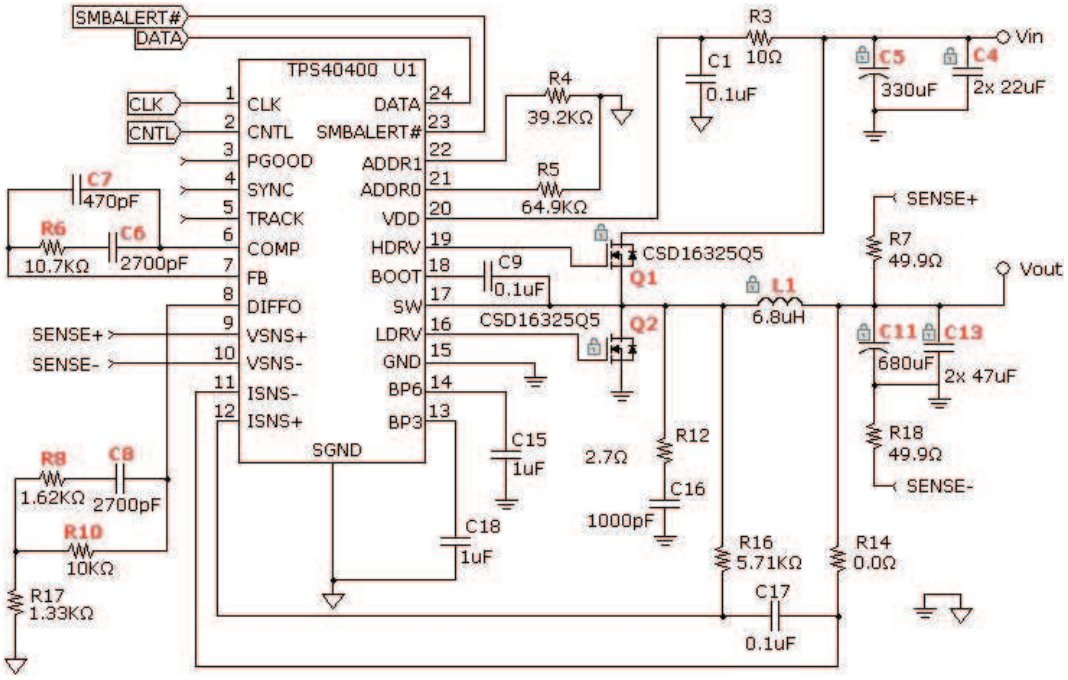


Figure 27. Typical Application Schematic, TPS40400 Design Example 2

8.2.2.1 Design Requirements

Figure 27 shiws the design process and component selection for a synchronous buck converter using the TPS40400 device. The design goal parameters are listed in Table 68.

Table 68. Electrical Parameters

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current	V_{IN} = 8 V, I_{OUT} = 5 A		3.5		A
	No load input current	V_{IN} = 12 V, I_{OUT} = 0 A		60		mA
$V_{IN(start)}$	V_{IN} start voltage			7		V
$V_{IN(stop)}$	V_{IN} stop voltage			6		V
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage	V_{IN} = 12 V, I_{OUT} = 5 A	4.75	5	5.25	V
	Line regulation	8 ≤ V_{IN} ≤,14 V, I_{OUT} = 5 A			0.5%	
	Load regulation	V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 5 A			0.5%	
$V_{OUT(ripple)}$	Output ripple voltage	V_{IN} = 12 V, I_{OUT} = 5 A			50	mV_{P-P}
Iout	Output current	8 ≤ V_{IN} ≤ 14	0		5	A
I_{OCP}	Output over current inception point	V_{IN} = 12 V	6.7	8	9.3	A
SS	Soft-start time	(default)		5		ms
	Transient response					
ΔI	Load step	2 A ≤ I_{OUT} ≤ 5 A		3		A
	Load slew rate			1		A/µS
	Overshoot			500		mV
	Settling time			50		µs

Table 68. Electrical Parameters (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SYSTEM CHARACTERISTICS						
f_{SW}	Switching frequency			300		kHz
η_{PK}	Peak efficiency	V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 5 A		90%		
η	Full load efficiency	V_{IN} = 12 V, I_{OUT} = 5 A		85%		
T_{OPER}	Operating temperature range	8 ≤ V_{IN} ≤ 14 V, 0 A ≤ I_{OUT} ≤ 5 A	–40		60	°C

8.2.2.1.1 List of Materials

Table 69 lists the materials for Design Example 2.

Table 69. List of Materials

REFERENCE DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C1, C2, C9, C17	4	0.1 µF	Ceramic, X7R, 25 V, 20%	0603	Standard	Standard
C3, C4	2	22 µF	Ceramic, X7R, 25 V, 10%	1210	Standard	Standard
C5	1	330 µF	Aluminum, 25 V, 20%	10x12mm	EEVFC1E331P	Panasonic
C6	1	2700 pF	Ceramic, X7R, 10 V, 20%	0603	Standard	Standard
C7	1	470 pF	Ceramic, X7R, 10 V, 20%	0603	Standard	Standard
C8	1	2700 pF	Ceramic, X7R, 10 V, 20%	0603	Standard	Standard
C11	1	680 µF	Tantalum, 6.3 V, 20%	7343 (D)	TPSE6870060045	Standard
C13, C14	2	47 µF	Ceramic, X7R, 6.3 V, 20%	1210	GRM32ER60J476M	Standard
C15, C18	2	1 µF	Ceramic, X7R, 16 V, 20%	0603	Standard	Standard
C16	1	1000 pF	Ceramic, X7R, 25 V, 20%	0603	Standard	Standard
L1	1	6.8 µH	Inductor, 6.8 µH, 12 mΩ		PF0553.682NL	Pulse
Q1	1	CSD16325Q5	Transistor, N-channel MOSFET, 25 V, 100 A, 10 Ω	QFN 5x6	CSD16325Q5	TI
Q2	1	CSD16325Q5	Transistor, N-channel, 25 V, 100 A, 10 Ω	QFN 5x6	CSD16325Q5	TI
R3	1	10 Ω	Resistor, 1/16W, 5%	0603	Standard	Standard
R4	1	39.2 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R5	1	64.9 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R6	1	10.7 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R7, R18	2	49.9 Ω	Resistor, 1/16W, 1%	0603	Standard	Standard
R8	1	1.62 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R10	1	10 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R12	1	2.7 Ω	Resistor, 1/16W, 5%	0603	Standard	Standard
R14	1	0.0 Ω	Resistor, 1/16W, 1%	0603	Standard	Standard
R16	1	5.71 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R17	1	1.33 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
U1	1	TPS40400	3.0V-20V PMBus synchronous buck controller	24-pin QFN	TPS40400RHL	Texas Instruments

8.2.2.2 Application Curves

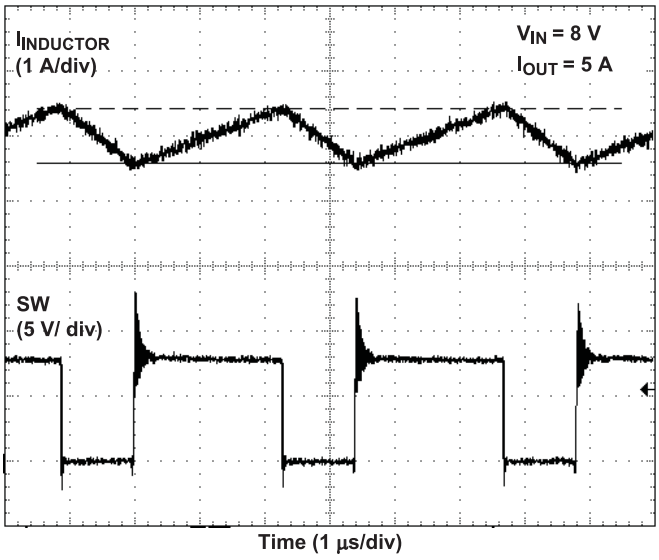


Figure 28. Switching Voltage and Inductor Current Waveform

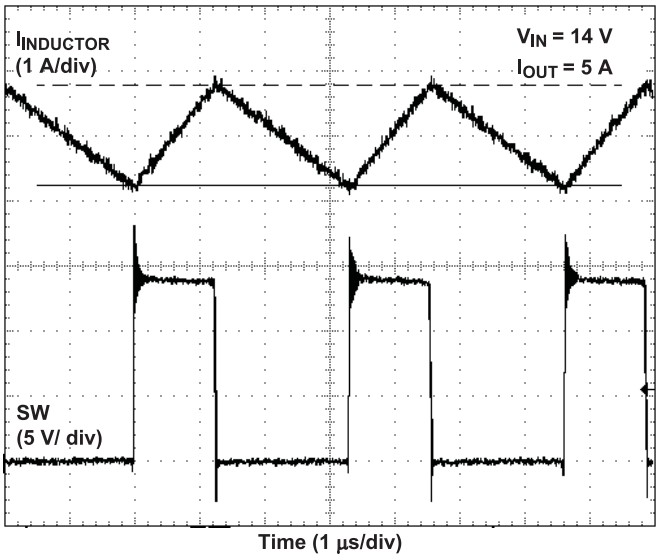


Figure 29. Switching Voltage and Inductor Current Waveform

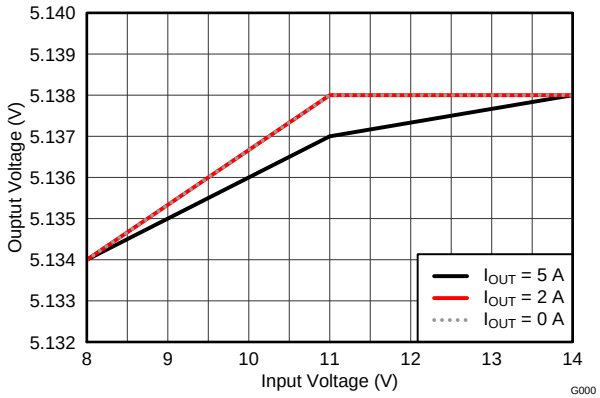


Figure 30. Line Regulation

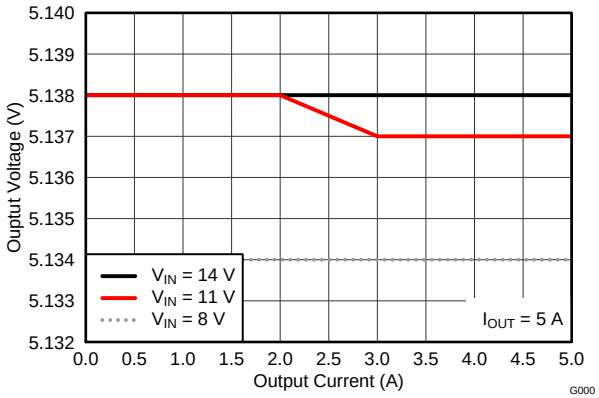


Figure 31. Load Regulation

8.3 Initialization Setup

8.3.1 Internal Configuration

Internal configuration of the TPS40400 device is handled via the PMBus (pins CLK and DATA) and the Fusion Digital Power Designer (GUI interface). An example of the configuration window that is used to make internal configuration changes to the TPS40400 device is shown below in Figure 32.

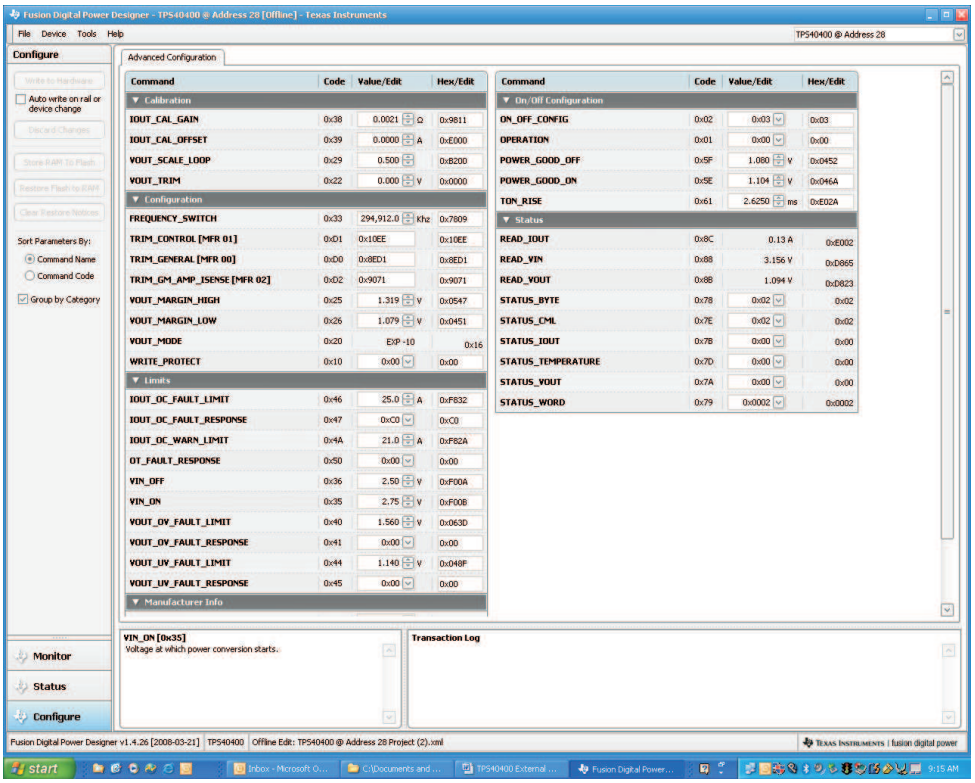


Figure 32. All Configuration Window

Figure 32 shows are the user changeable parameters of the TPS40400 device and these consist of the following sections.

- Calibration
- Configuration
- Limits
- On/Off Configuration

The status section is read only, and consists of data read from the TPS40400 device such as V_{OUT}, I_{OUT}, V_{IN}, and status words. A full description of each command and status word is available in the *Register Maps* section.

Configuration changes can be implemented by changing the value in the **Value/Edit** box of each parameter. Most boxes allow direct parameter changes such as voltage or current, but some boxes such as **IOUT_OC_FAULT_RESPONSE** provide a pop-up configuration window as shown in Figure 33, and others provide a pull-down menu. Select the appropriate radio buttons to make the desired changes.

To implement the changes to the device, click on the [Write to Hardware] button. This stores the changes to the device in volatile memory, so these changes are lost when input power is cycled. To permanently make changes and commit those changes to non-volatile memory, click on the [Store RAM to Flash] button.

Initialization Setup (continued)

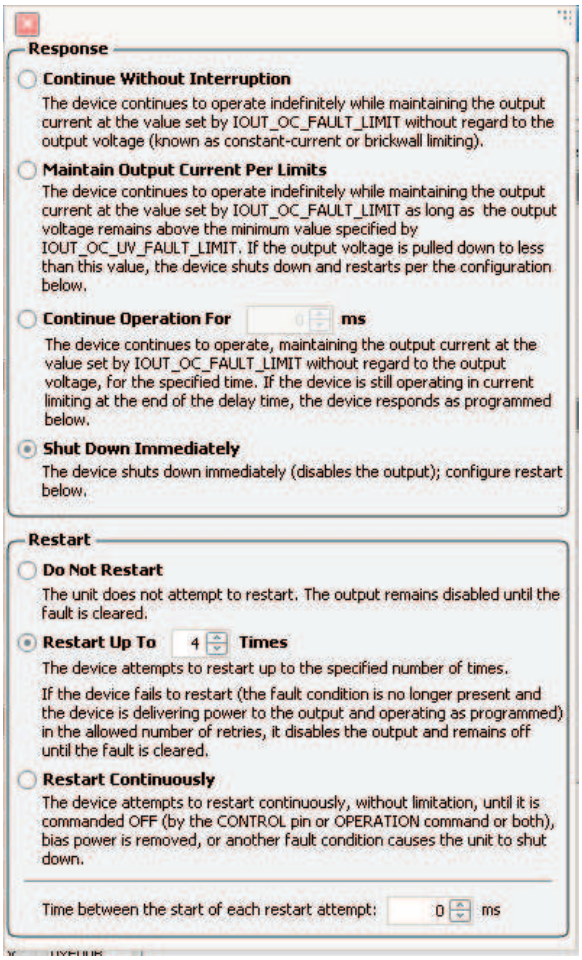


Figure 33. IOUT_OC_FAULT_RESPONSE Configuration Window

9 Power Supply Recommendations

The TPS40400 device operates from an input voltage supply between 3 V and 20 V. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the *Layout* section.

10 Layout

10.1 Layout Guidelines

- As with any switching regulator, there are several paths that conduct fast switching voltages or currents. Minimize the loop area formed by these paths and their bypass connections, and minimize the impedance of these paths. Separate input currents from output currents.
- High-frequency bypassing of the power stage VIN and GND areas is essential. Power stage bypass capacitors from VIN to GND should be as close as physically possible to the power MOSFET device pins, and should be on the same layer as the power MOSFET devices. Connecting bypass connections through vias dramatically increases the impedance of these connections, and can lead to excessive switching noise.
- Ensure that the TPS40400 device is not exposed to voltages or currents higher than its absolute maximum ratings due to switching noise. In many cases, this consideration requires the addition of an R-C snubber network, or provisions to slow the turn-on rate of the high-side MOSFET such as a high-side gate resistor or boot resistor.
- Minimize the SW copper area for best noise performance. Route sensitive traces away from SW and BOOT, as these nets contain fast switching voltages, and lend easily to capacitive coupling.
- Keep the gate drive loop impedance (HDRV-gate-source-SW and LDRV-gate-source-GND) as low as possible. Widen the HDRV and LDRV trace connections to 20 mils as soon as possible once they are away from the TPS40400 device pins.
- Ensure that the PowerPad™ integrated circuit package of the TPS40400 device functions as the ground return for its signal components. Connect the GND pin to the power stage ground, as it functions as a return for the integrated MOSFET drivers. The power stage ground and signal ground returns should only have one single point of connection, at the thermal pad of the TPS40400 device.
- Signal components should be placed close to the TPS40400 device, and terminated to SGND. Signal components include: feedback resistors, frequency compensation components, bypass connections for BP3, BP6, and VDD, and PMBus address selection resistors.
- For proper thermal performance, the TPS40400 PowerPad integrated circuit package must be thermally grounded to internal copper layers through multiple thermal vias, and must have adequate solder coverage after assembly.
- Locate signal components and their connections and terminations to the TPS40400 device far away from the fast switching power nets of the TPS40400 device. Switching noise that is coupled onto signal paths, either directly or through ground returns, can degrade regulator performance. Alternatively, use a small low-pass R-C filter between VIN and VDD to reduce the amount of switching noise coupled into the TPS40400 device VDD pin from the power stage VIN pin.
- The TPS40400 device require good local bypassing on several pins. Locate bypass capacitors for BP3, BP6 and VDD as close as physically possible to the TPS40400 device, Locate bypass capacitors on the same layer to minimize the impedance of these bypass connections and return paths.
- Route the output voltage remote sense lines from the output capacitor bank at the load, back to the VSNS+ and VSNS– pins of the TPS40400 device, as a tightly coupled differential pair. Avoid routing these lines near fast switching nets such as SW, BOOT, or VIN, as these can potentially couple differential-mode noise into the regulation path. As an alternative, locally connect a small coupling capacitor (no greater than 1 nF) to the TPS40400 device to improve noise immunity. Reference the feedback and compensation components to the differential amplifier output, DIFFO. Keep the feedback and compensation components local to the TPS40400 device, away from switching power stage nets.
- Route the output current sense lines from either side of the inductor, back to the TPS40400 device as a tightly coupled differential pair. When using DCR current sensing, with an R-C averaging filter from SW to VOUT, place the sense resistor close to the inductor with a kelvin connection from SW and VOUT under the inductor, and place the capacitor as close as possible to the ISNS+ and ISNS– pins of the TPS40400 device.

10.2 Layout Examples

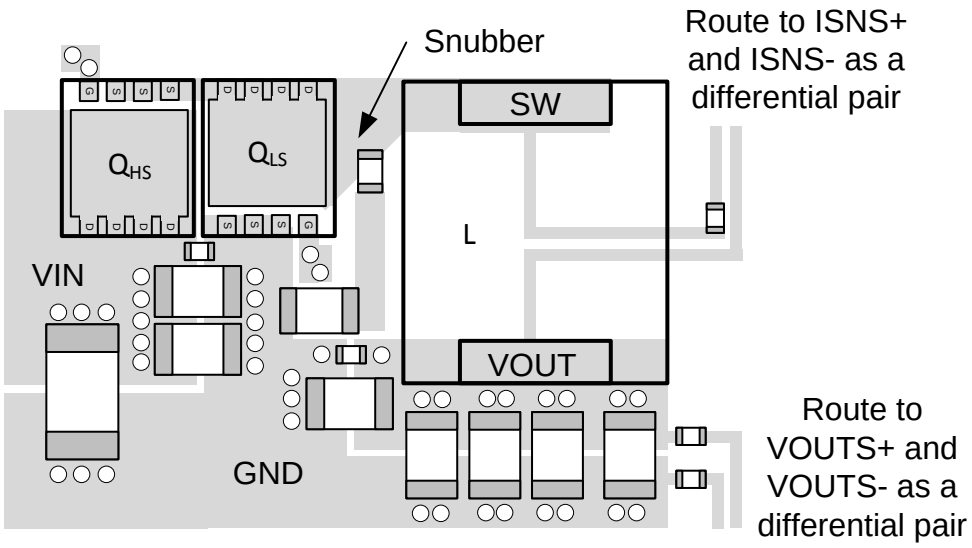


Figure 34. Example Discrete MOSFET Power Stage Layout

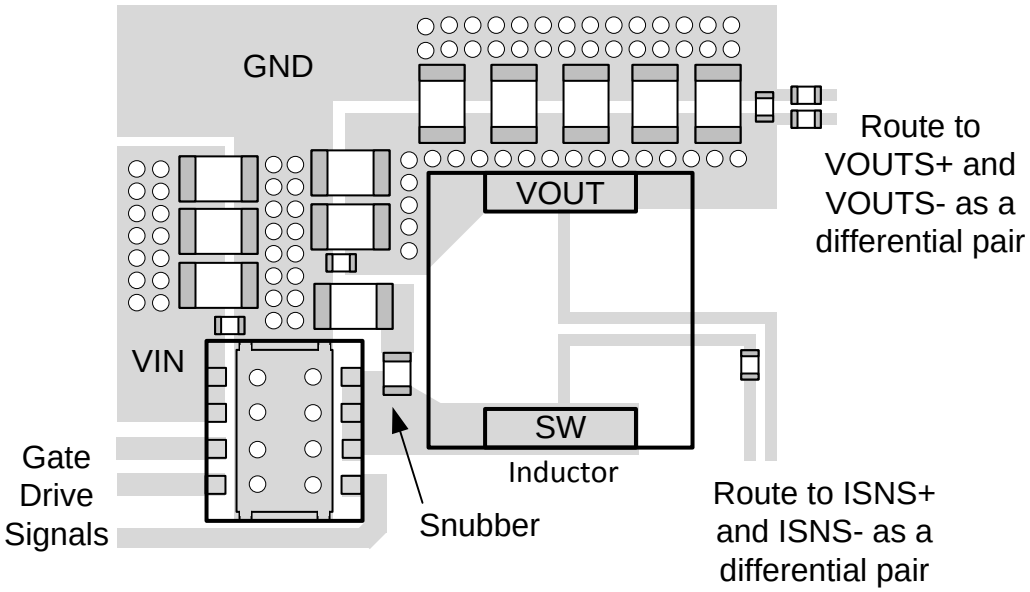


Figure 35. Example Integrated Power Stage Layout

Layout Examples (continued)

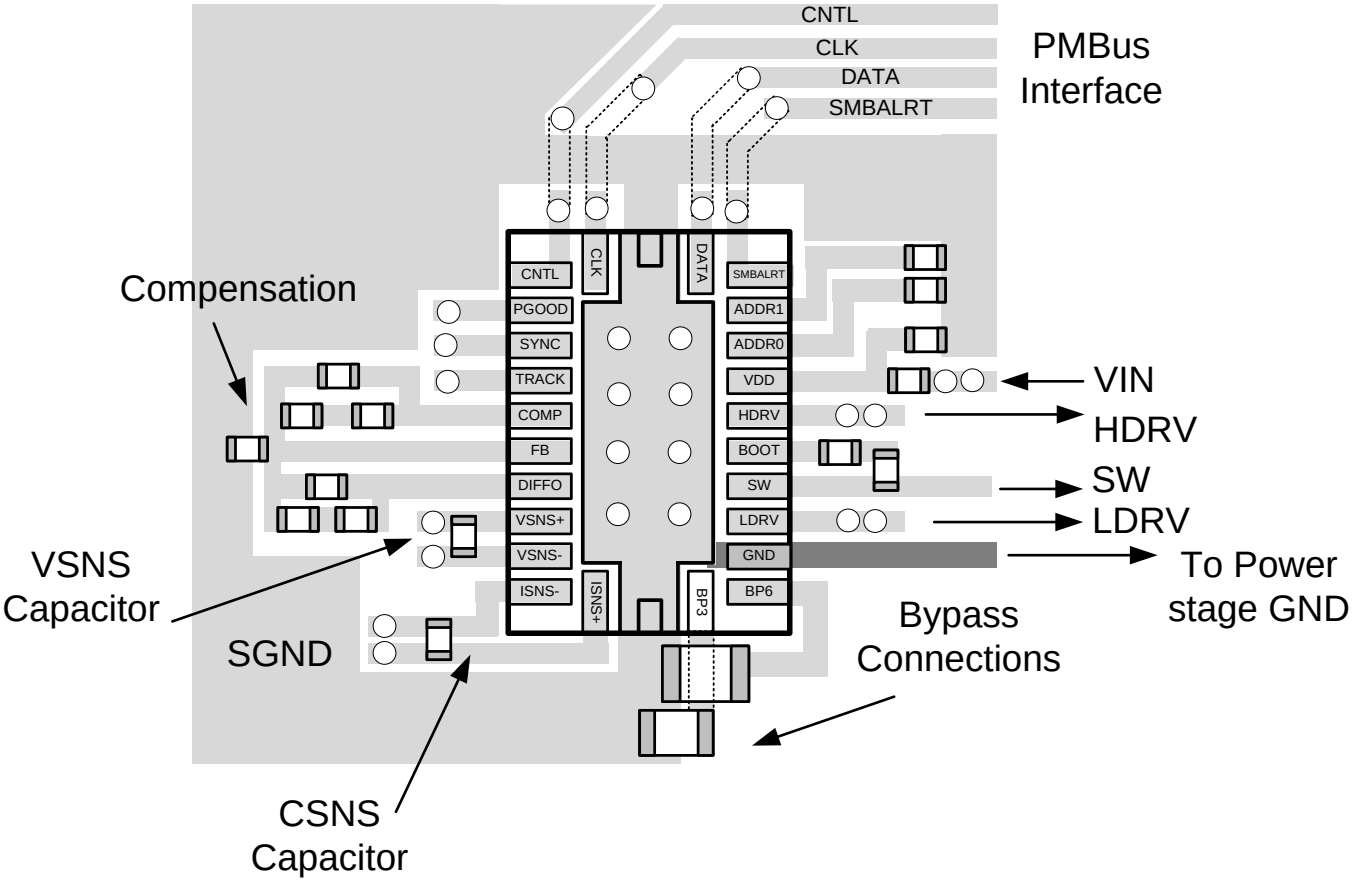


Figure 36. Example Controller Layout

10.3 Thermal Considerations

Power dissipation ratings determine the thermal limitations of any power supply design. In general, power dissipation in the power MOSFETs and output inductor will limit the safe operating area of the design. Consult the manufacturer data sheets for these components to ensure that power dissipation ratings are met with sufficient margin. Additionally, Table 70 shows the power dissipation ratings of the TPS40400 controller device itself.

Table 70. TPS40400 Power Dissipation Ratings

THERMAL IMPEDANCE JUNCTION-TO-AMBIENT (°C/W)	AIRFLOW	T_A = 25°C POWER RATING	T_A = 85°C POWER RATING
31.1	Natural Convection	3.21 W	1.29 W
25.2	200 LFM	3.96 W	1.58 W
23	400 LFM	4.36 W	1.74 W

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

SwitcherPro, PowerPad, E2E are trademarks of Texas Instruments.
PMBus is a trademark of SMIF, Inc..
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40400RHLR	ACTIVE	VQFN	RHL	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	40400	Samples
TPS40400RHLT	ACTIVE	VQFN	RHL	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	40400	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

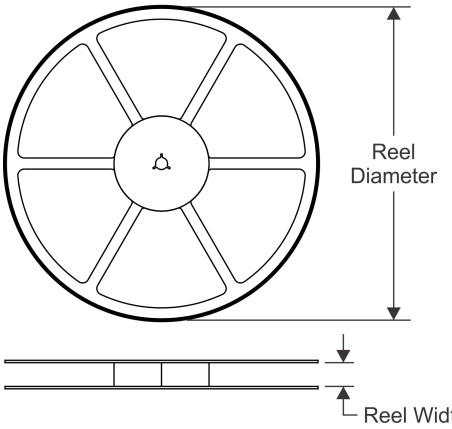
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

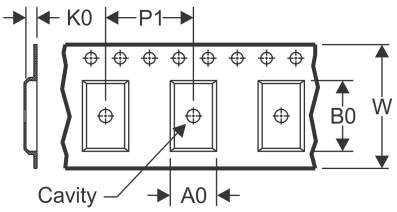
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

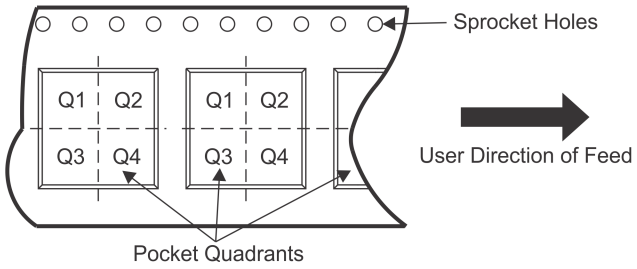


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

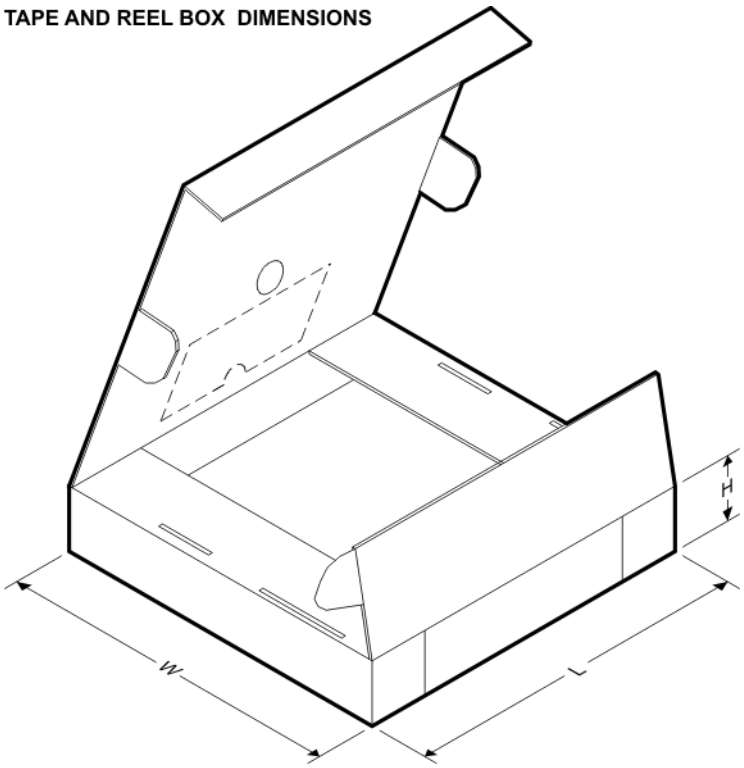
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40400RHLR	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
TPS40400RHLT	VQFN	RHL	24	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

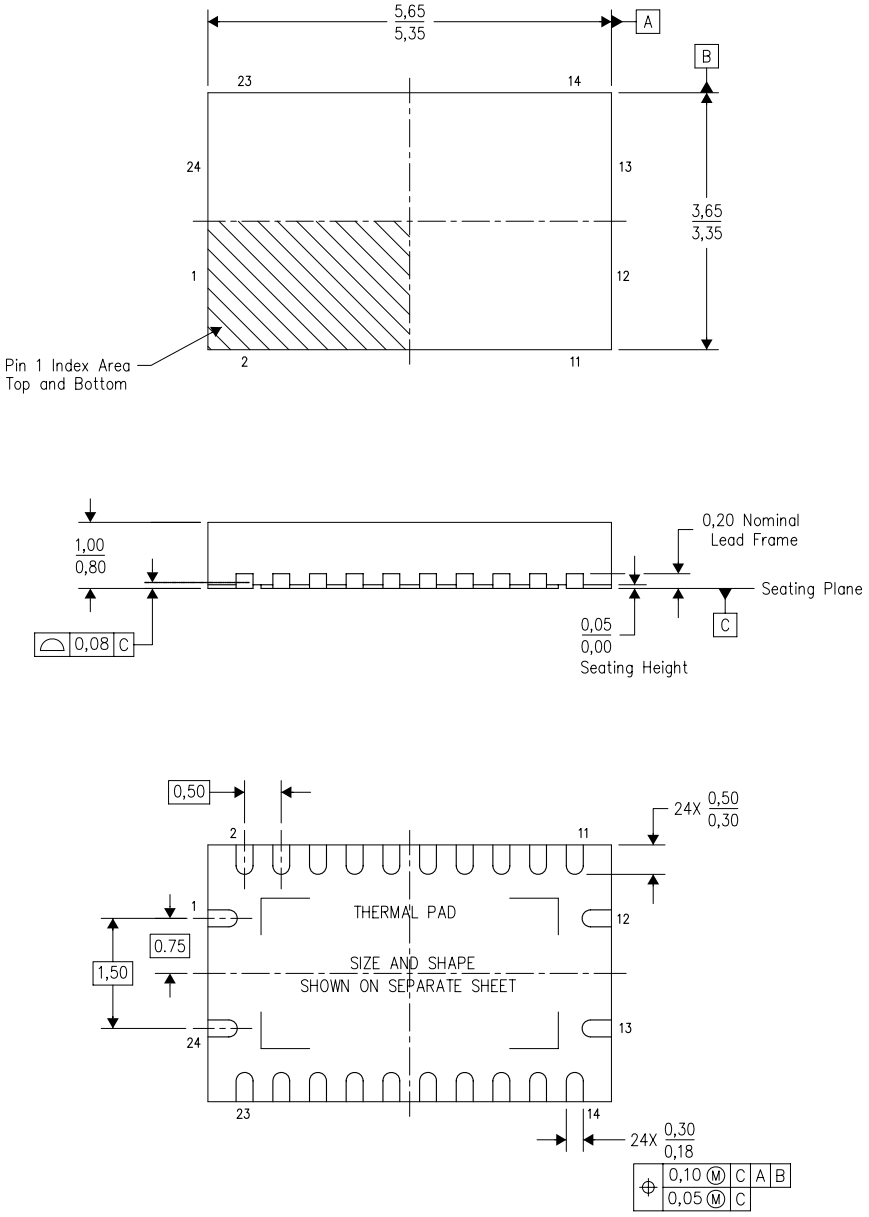
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40400RHLR	VQFN	RHL	24	3000	367.0	367.0	35.0
TPS40400RHLT	VQFN	RHL	24	250	210.0	185.0	35.0

RHL (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4205346–4/J 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. JEDEC MO–241 package registration pending.

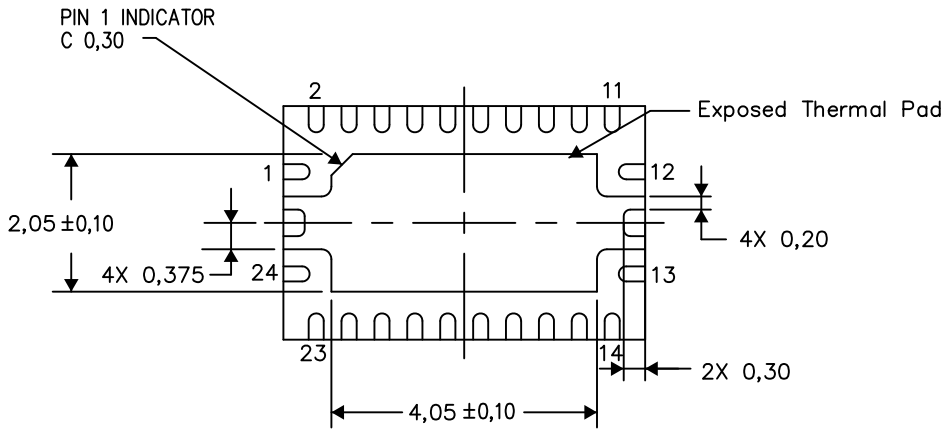
RHL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



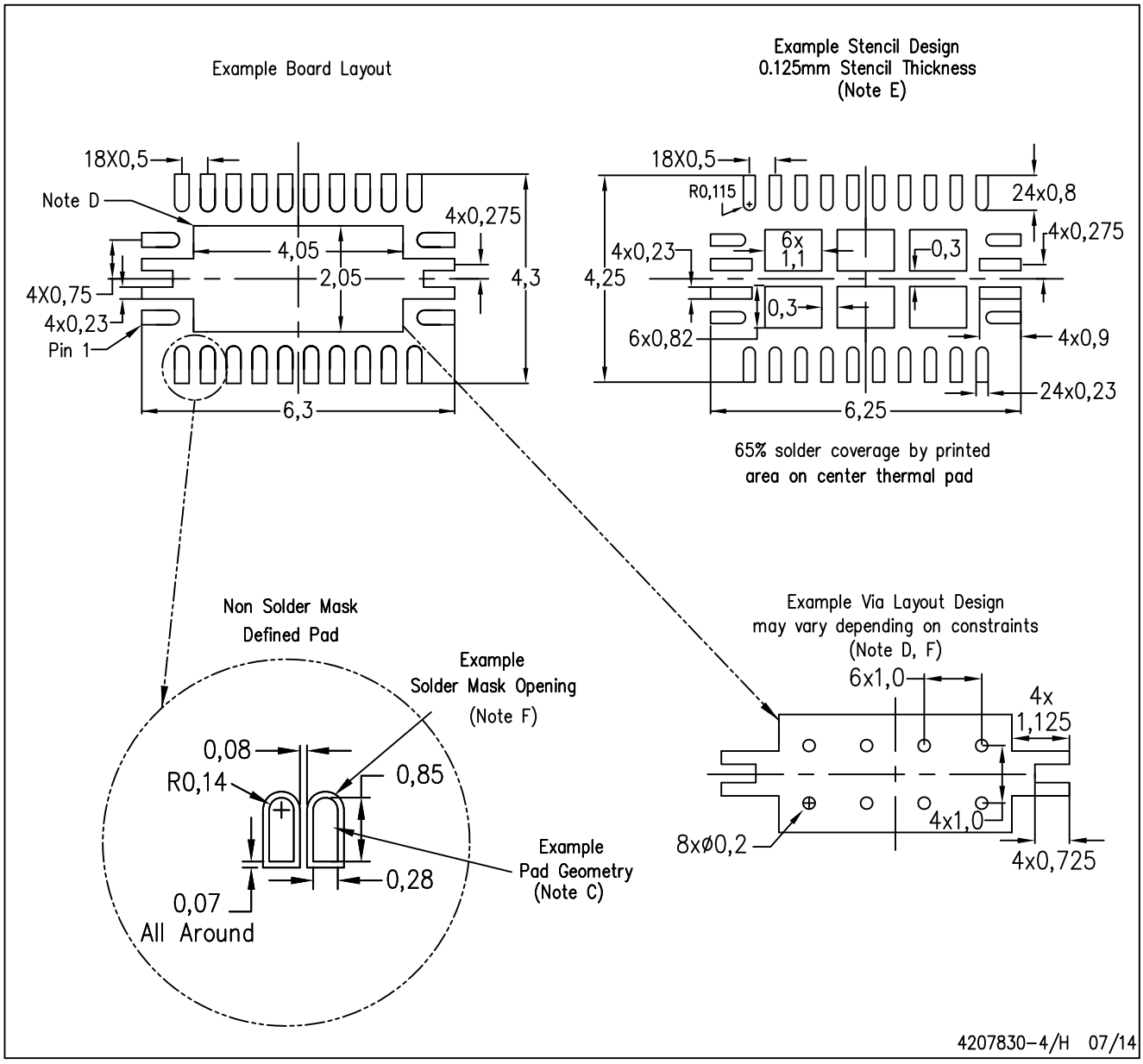
Bottom View

Exposed Thermal Pad Dimensions

4206363–4/N 07/14

NOTE: All linear dimensions are in millimeters

RHL (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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