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# FQP32N20C / FQPF32N20C

## N-Channel QFET® MOSFET

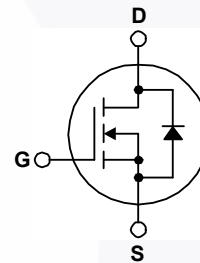
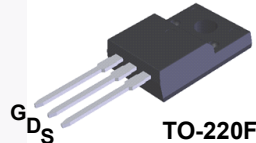
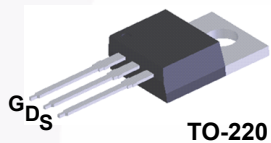
200 V, 28 A, 82 mΩ

### Features

- 28 A, 200 V,  $R_{DS(on)} = 82 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 14 \text{ A}$
- Low Gate Charge (Typ. 82.5 nC)
- Low  $C_{rss}$  (Typ. 185 pF)
- 100% Avalanche Tested

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQP32N20C	FQPF32N20C	Unit
$V_{DSS}$	Drain to Source Voltage	200		V
$I_D$	Drain Current	-Continuous ( $T_C = 25^\circ\text{C}$ )	28.0	28.0 *
		-Continuous ( $T_C = 100^\circ\text{C}$ )	17.8	17.8 *
$I_{DM}$	Drain Current - Pulsed (Note 1)	112	112 *	A
$V_{GSS}$	Gate to Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	955		mJ
$I_{AR}$	Avalanche Current (Note 1)	28.0		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	15.6		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	156	50	W
		- Derate above $25^\circ\text{C}$		W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

\*Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FQP32N20C	FQPF32N20C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.8	2.51	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQP32N20C	FQP32N20C	TO-220	Tube	N/A	50 units
FQPF32N20C	FQPF32N20C	TO-220F	Tube	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.24	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 160\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 14\text{ A}$	--	0.068	0.082	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 14\text{ A}$	--	20	--	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	1700	2220	pF
$C_{oss}$	Output Capacitance		--	400	520	pF
$C_{riss}$	Reverse Transfer Capacitance		--	185	245	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{ V}, I_D = 32\text{ A}, R_G = 25\ \Omega$	--	25	60	ns
$t_r$	Turn-On Rise Time		--	270	550	ns
$t_{d(off)}$	Turn-Off Delay Time		--	245	500	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	210	430
$Q_g$	Total Gate Charge	$V_{DS} = 160\text{ V}, I_D = 32\text{ A}, V_{GS} = 10\text{ V}$	--	82.5	110	nC
$Q_{gs}$	Gate-Source Charge		--	10.5	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	44.5	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	28	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	112	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 28\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 32\text{ A}, di_F / dt = 100\text{ A}/\mu\text{s}$	--	265	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	2.73	--	$\mu\text{C}$

### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2.  $L = 1.4\text{ mH}, I_{AS} = 32\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 28\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

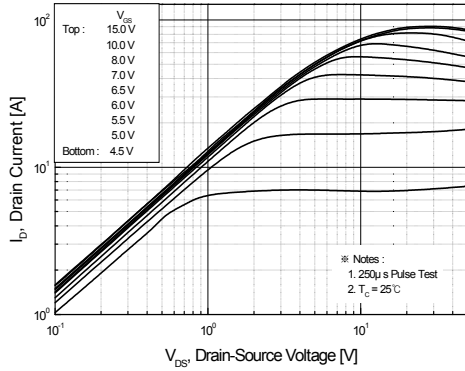


Figure 1. On-Region Characteristics

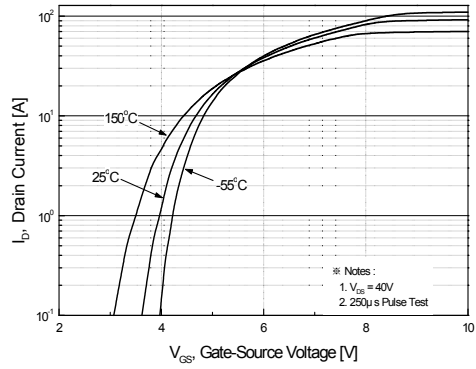


Figure 2. Transfer Characteristics

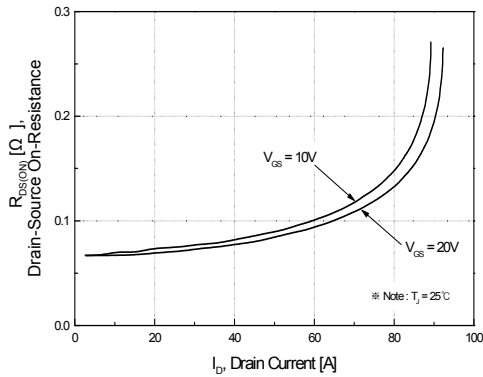


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

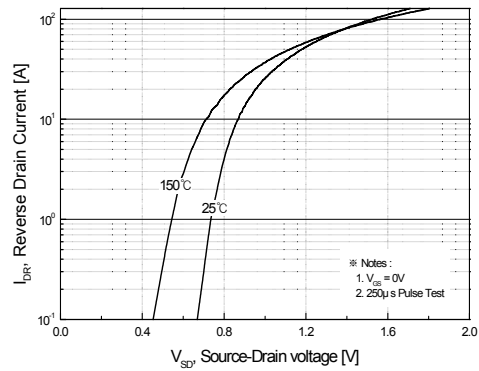


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

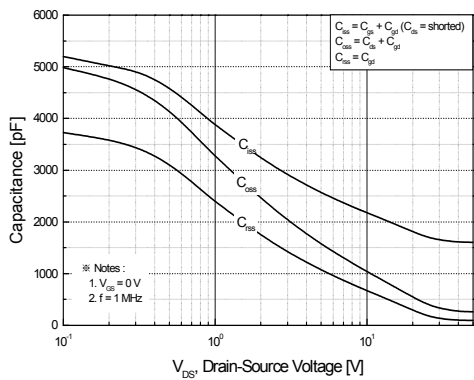


Figure 5. Capacitance Characteristics

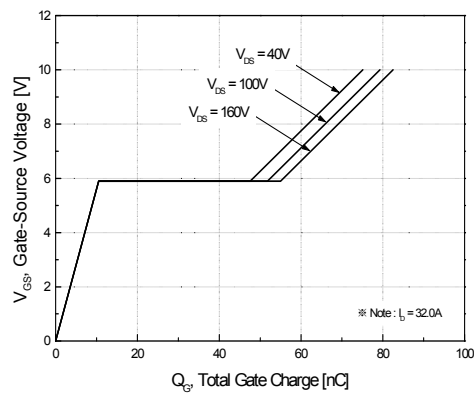
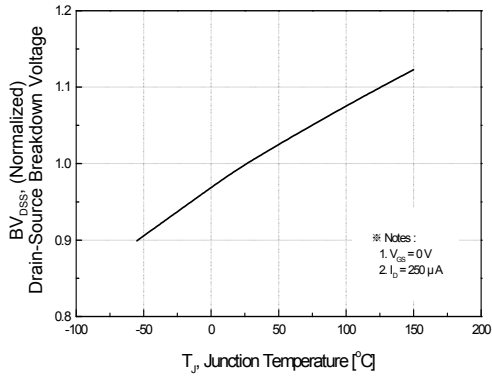
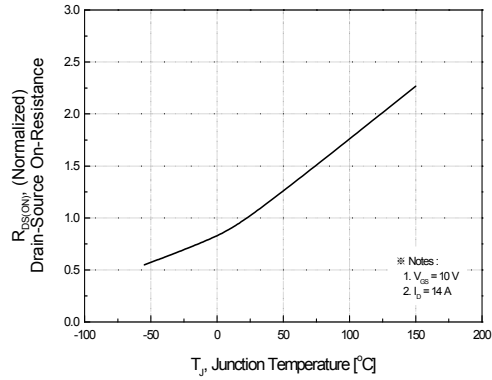


Figure 6. Gate Charge Characteristics

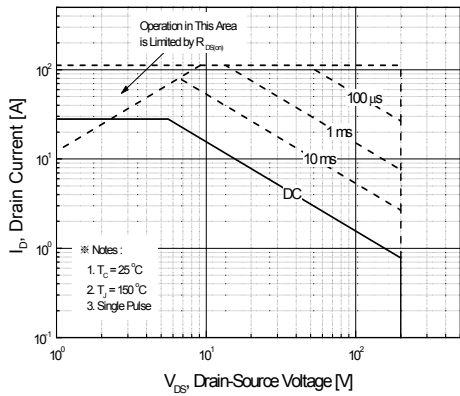
**Typical Characteristics** (Continued)



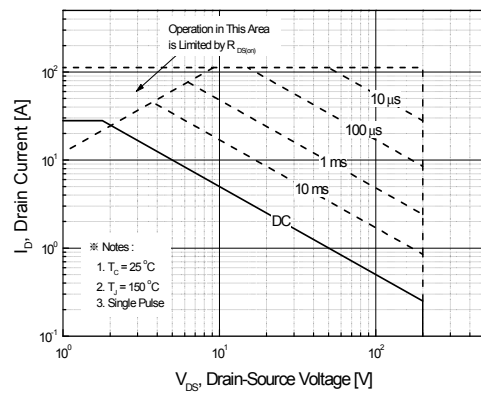
**Figure 7. Breakdown Voltage Variation vs Temperature**



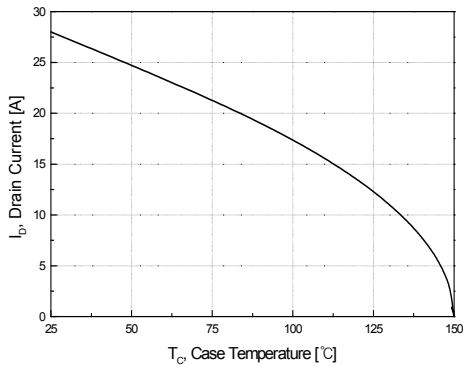
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9-1. Maximum Safe Operating Area for FQP32N20C**

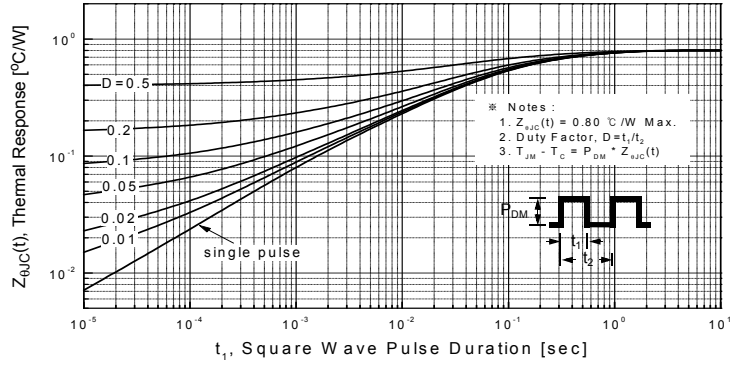


**Figure 9-2. Maximum Safe Operating Area for FQPF32N20C**

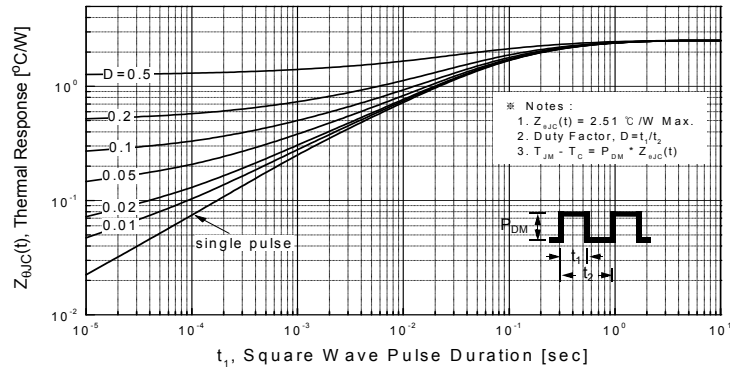


**Figure 10. Maximum Drain Current vs Case Temperature**

**Typical Characteristics** (Continued)

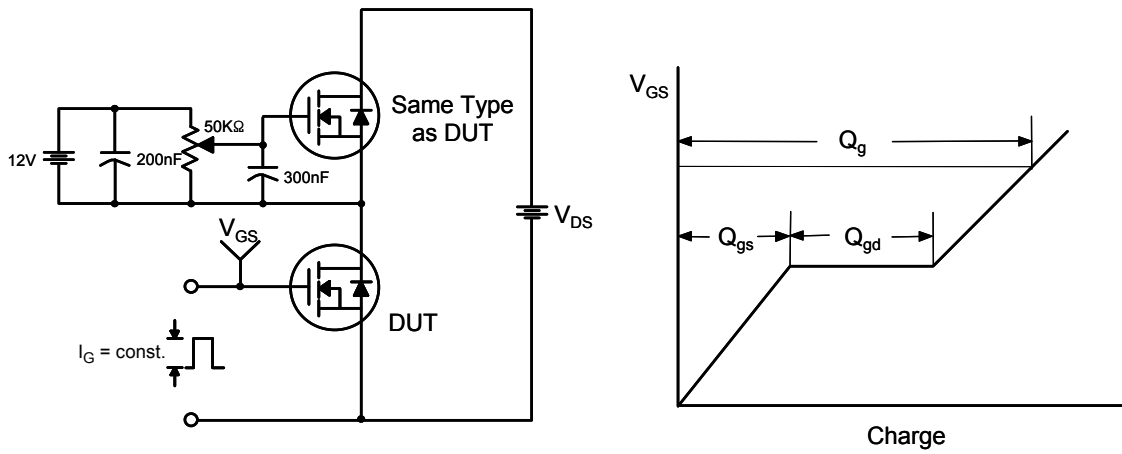


**Figure 11-1. Transient Thermal Response Curve for FQP32N20C**

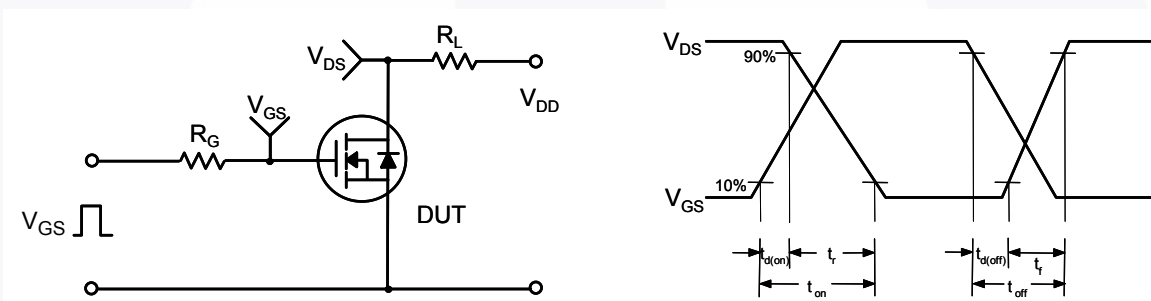


**Figure 11-2. Transient Thermal Response Curve for FQPF32N20C**

**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**



**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**

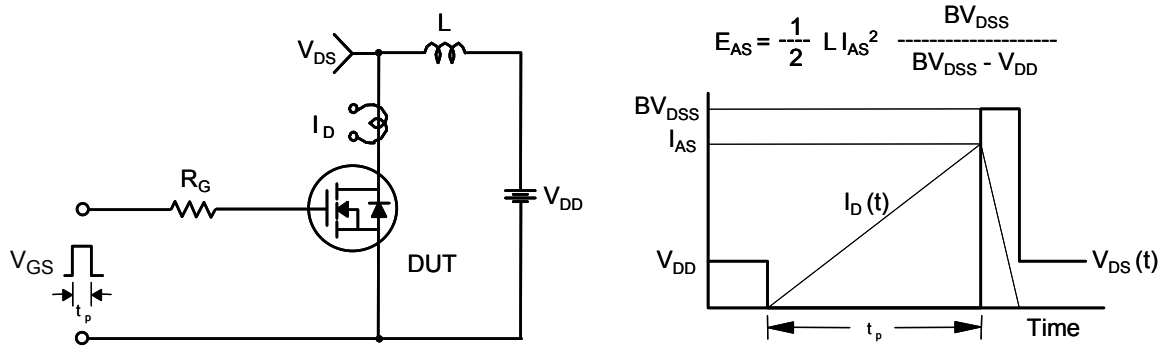
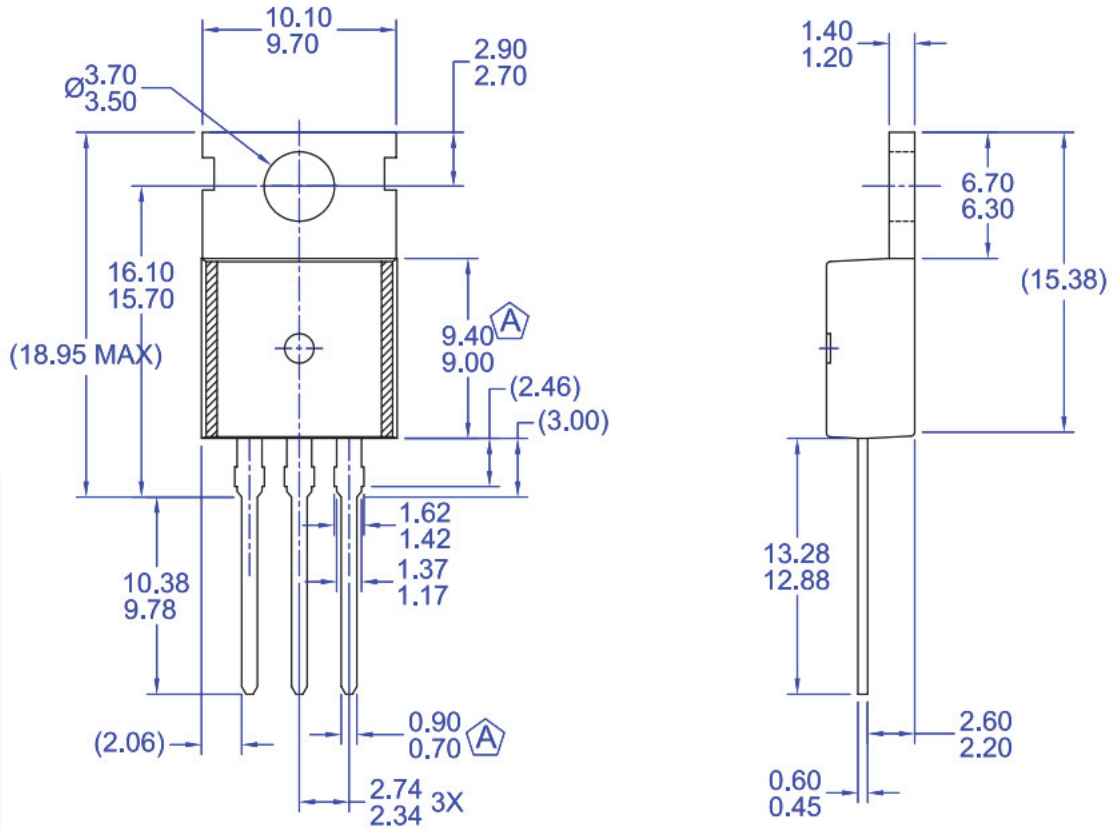


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





**Mechanical Dimensions**



**NOTES:**

- (A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

**Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB**

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## Mechanical Dimensions



### NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

**Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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