

Low Voltage, Fault Protection, SP3T Analog Switch (3:1 Multiplexer/Demultiplexer)

DESCRIPTION

The DG2522 is a low on-resistance SP3T analog switch design to operation from 1.6 V to 5.5 V.

The DG2522 switches signals in either direction with amplitudes up to V_+ . Protection circuit is built in to isolate the signals if any of them swings above V_+ . It guaranteed low leakage level for isolation in power down mode.

Built on Vishay Siliconix's sub-micro CMOS technology, the DG2522 achieves switch on-resistance of 0.8Ω at 4.5 V V_+ with 0.6Ω flatness. It has superior 0.008 % THD (total harmonic distortion) over frequency of 20 Hz to 20 kHz. It provides -59 dB off-Isolation, -65 dB crosstalk at 1 MHz, and 105 MHz -3 dB bandwidth.

The select pin of the control logic input can tolerate voltages above V_+ up to 5.5 V. Logic high 1.8 V is guaranteed over the full V_+ range that makes it compatible with many low voltage digital control circuits.

The features of ultra small package size, wide V_+ range, low on-resistance, low logic threshold, and switch isolation under fault condition make it an ideal device for battery operated devices to handle signals such as audio, video, data stream, and other high accuracy signals.

The DG2522 comes in a small miniQFN-8 lead package of 1.4 mm x 1.4 mm x 0.55 mm. As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device termination and is 100 % RoHS compliant.

FEATURES

- Isolation at $V_+ = 0$ V and signal above V_+
- Logic input tolerates up to 5.5 V
- 1.6 V to 5.5 V operation voltage range
- Guaranteed 1.8 V $V_{TH(high)}$ at $V_+ = 4.5$ V
- 0.008 % total harmonic distortion
- Low switch on-resistance
- 300 mA latch up current per JESD78


RoHS
COMPLIANT

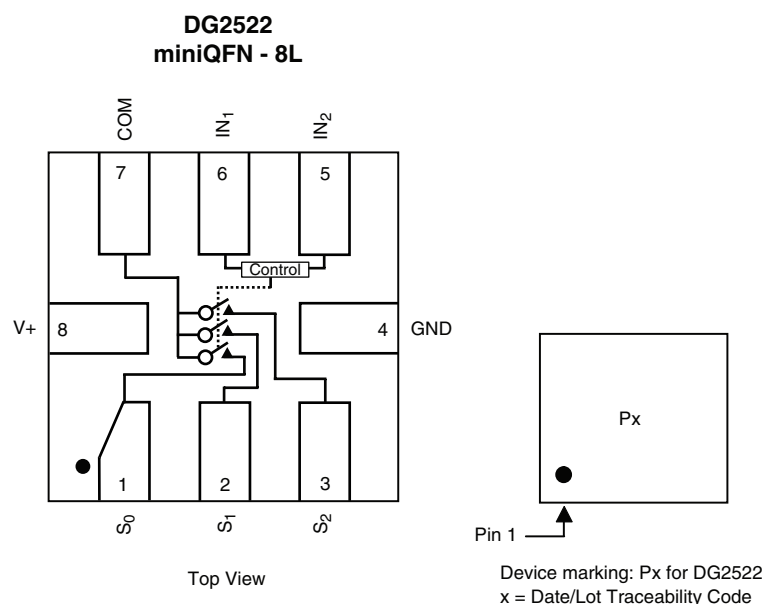
BENEFITS

- Ultra small miniQFN8 package of 1.4 mm x 1.4 mm x 0.55 mm
- High fidelity audio switch
- Reed relay replacement
- Low power consumption

APPLICATIONS

- Cellular phones and PDAs
- GPS and portable media players
- Modems and wireless cards
- Computers peripherals
- Communication and network circuits
- Low voltage data acquisition systems
- Portable instrumentation

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION





TRUTH TABLE DG2522		
IN ₁ (Pin 6)	IN ₂ (Pin 5)	Function
0	0	COM disconnect
1	0	COM (Pin 7) = S ₀ (Pin 1)
0	1	COM (Pin 7) = S ₁ (Pin 2)
1	1	COM (Pin 7) = S ₂ (Pin 3)

ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	miniQFN-8L	DG2522DN-T1-E4

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter		Limit	Unit
Reference to GND	V+	- 0.3 to 6.0	V
	IN, COM, S _x ^a	- 0.3 to (V+ + 0.3)	
Current (Any terminal except S _x or COM)		30	mA
Continuous Current (S _x or COM)		± 300	
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage Temperature (D Suffix)		- 65 to 150	°C
Power Dissipation (Packages) ^b	miniQFN-8L ^c	190	mW

Notes:

- a. Signals on S₀, S₁, S₂ and COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 2.4 mW/°C above 70 °C.



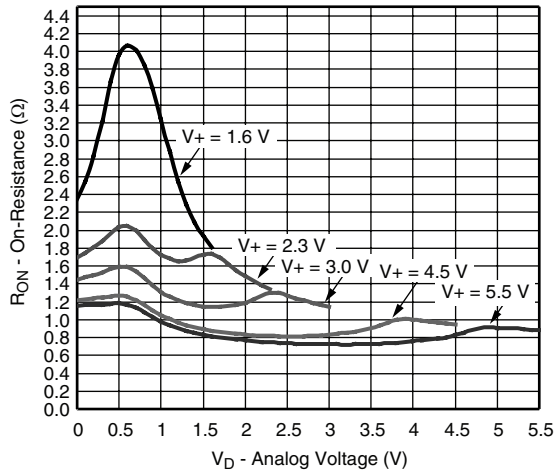
SPECIFICATIONS $V_+ = 5\text{ V}$							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}, \pm 10\%, V_{IN} = 0.6\text{ V}$ or 1.8 V^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Analog Switch							
Analog Signal Range ^d	V_{analog}	$R_{\text{DS(on)}}$	Full	0		V_+	V
On-Resistance	$R_{\text{DS(on)}}$	$V_+ = 4.5\text{ V}, I_{\text{SX}} = 100\text{ mA}, V_{\text{COM}} = 2.5\text{ V}$	Room		0.8	1.1	Ω
		$V_+ = 4.5\text{ V}, I_{\text{SX}} = 100\text{ mA}, V_{\text{COM}} = 2.5\text{ V}$	Full			1.5	
R_{ON} Match	ΔR_{ON}	$V_+ = 4.5\text{ V}, I_{\text{SX}} = 100\text{ mA}, V_{\text{COM}} = 2.5\text{ V}$	Room			0.1	
R_{ON} Resistance Flatness	R_{ON} flatness	$V_+ = 4.5\text{ V}, I_{\text{SX}} = 100\text{ mA}, V_{\text{COM}} = 0.5\text{ V}, 2.5\text{ V}$	Room		0.2	0.6	
Switch Off Leakage Current	$I_{\text{SX(off)}}$	$V_+ = 5.5\text{ V}, V_{\text{SX}} = 1\text{ V}/4.5\text{ V}, V_{\text{COM}} = 4.5\text{ V}/1\text{ V}$	Room	- 20		20	nA
			Full	- 120		120	
	Room		- 20		20		
	Full		- 120		120		
Channel-On Leakage Current	$I_{\text{COM(on)}}$	$V_+ = 4.3\text{ V}, V_{\text{SX}} = V_{\text{COM}} = 4.5\text{ V}/1\text{ V}$	Room	- 20		20	
			Full	- 120		120	
Power Down Leakage		$V_+ = 0\text{ V}, V_{\text{SX}} = 0\text{ V}/5.5\text{ V}, V_{\text{COM}} = 5.5\text{ V}/0\text{ V}$	Room	- 1	0.001	1	μA
			Full	- 25		25	
Digital Control							
Input High Voltage	V_{INH}	$V_+ = 2.7\text{ V}$	Full	1.6			V
		$V_+ = 4.5\text{ V}$	Full	1.8			
Input Low Voltage	V_{INL}		Full			0.6	
Input Capacitance	C_{IN}	$f = 1\text{ MHz}, V_{\text{INX}} = 0\text{ V}$	Room		5		pF
Input Current	I_{INL} or I_{INH}	$V_{\text{IN}} = 0$ or V_+	Full	- 1		1	μA
Dynamic Characteristics							
Break-Before-Make Time ^e	t_{BBM}	$V_+ = 5.0\text{ V}, V_{\text{SX}} = V_+, R_L = 50\ \Omega, C_L = 35\text{ pF}$ (see figure 2)	Room		8		ns
			Full	14			
Enable Turn-On Time ^e	t_{ON}	$V_+ = 5.0\text{ V}, V_{\text{SX}} = V_+, R_L = 50\ \Omega, C_L = 35\text{ pF}$ (see figure 1)	Room		53	75	ns
			Full			85	
Enable Turn-Off Time ^e	t_{OFF}		Room		40	60	
			Full			70	
Charge Injection ^d	Q	$C_L = 1\text{ nF}, R_{\text{GEN}} = 0\ \Omega, V_{\text{GEN}} = 0\text{ V}$	Room		27		pC
Off-Isolation ^d	O_{IRR}	$R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$	Room		- 59		dB
Crosstalk ^d	X_{TALK}	$R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$			- 64		
- 3 dB Bandwidth ^d	BW	$R_L = 50\ \Omega, C_L = 5\text{ pF}$	Room		105		MHz
Source Off Capacitance ^d	$C_{\text{SX(off)}}$	$f = 1\text{ MHz}, V_{\text{NX}} = 0\text{ V}$	Room		17		pF
Drain Off Capacitance ^d	$C_{\text{COM(off)}}$	$f = 1\text{ MHz}, V_{\text{COM}} = 0\text{ V}$	Room		51		
Drain On Capacitance ^d	$C_{\text{COM(on)}}$	$f = 1\text{ MHz}, V_{\text{COM}} = V_{\text{NX}} = 0\text{ V}$	Room		70		
Total Harmonic Distortion ^d	THD	$V_+ = 5\text{ V}, V_{\text{IN}} = 1\text{ V}_{\text{RMS}}, R_L = 600\ \Omega, f = 20\text{ Hz}$ to 20 kHz	Room		0.008		%
Power Supply							
Power Supply Range	V_+			1.6		5.5	V
Power Supply Current	I_+	$V_{\text{IN}} = 0$ or V_+	Full			1.0	μA

Notes:

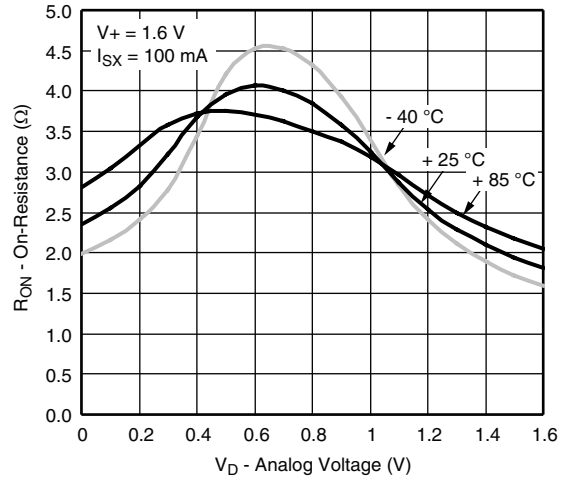
- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, not subjected to production test.
- e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

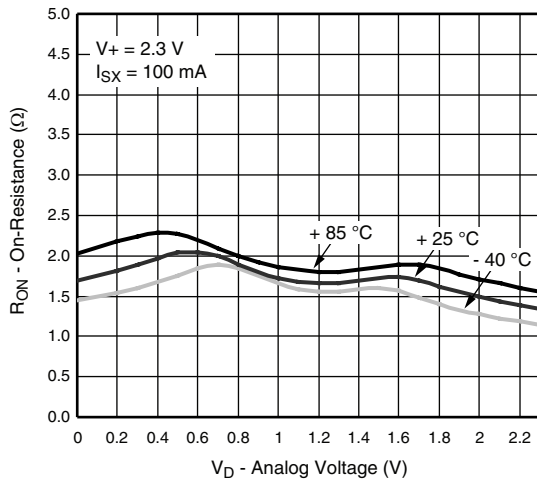
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



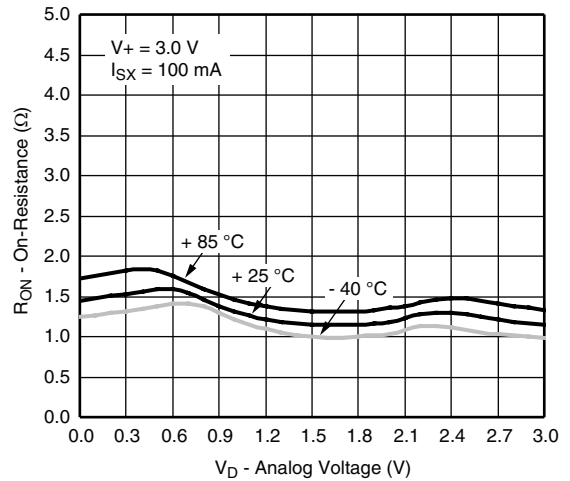
R_{ON} vs. V_D and Single Supply Voltage



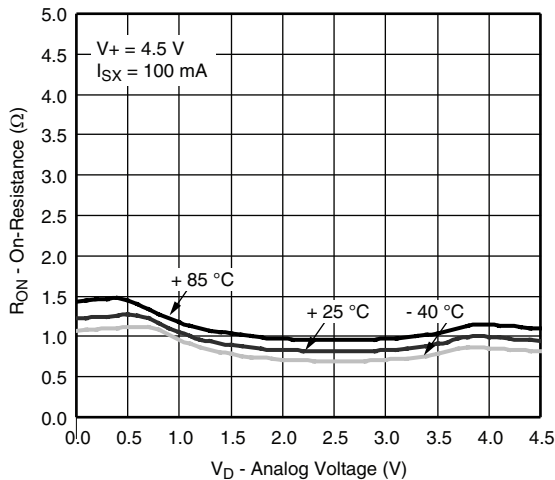
R_{ON} vs. Analog Voltage and Temperature



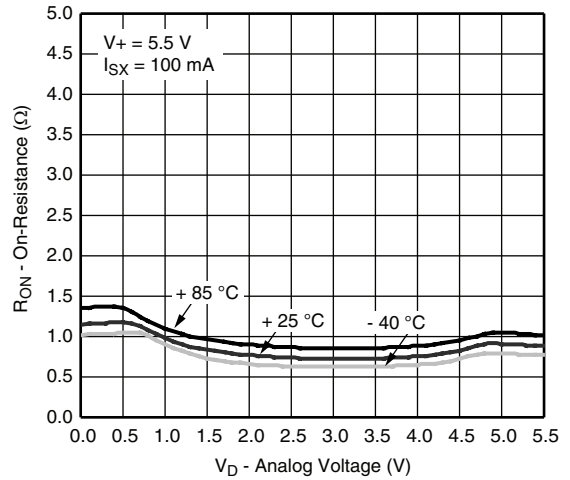
R_{ON} vs. Analog Voltage and Temperature



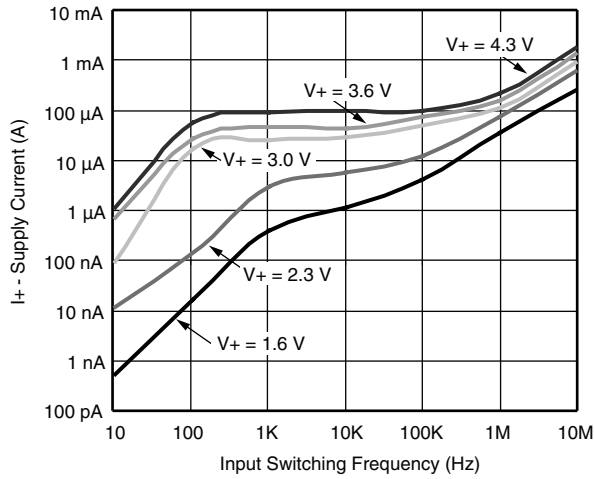
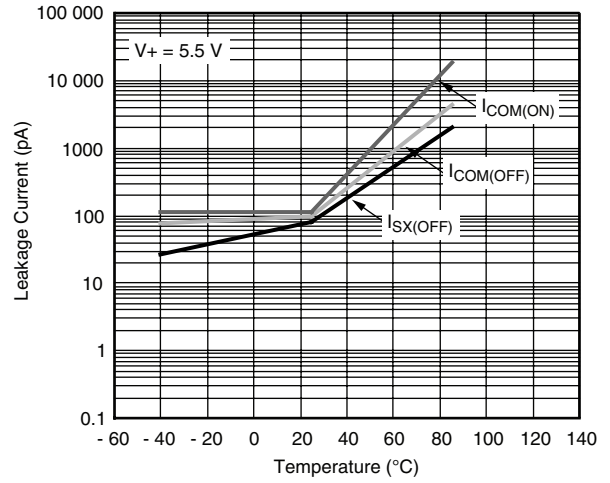
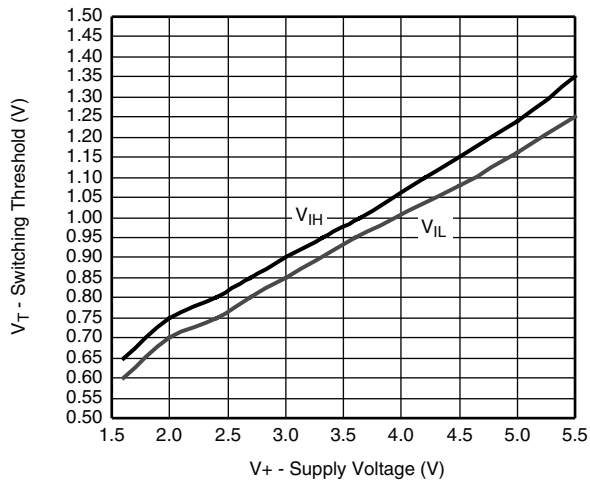
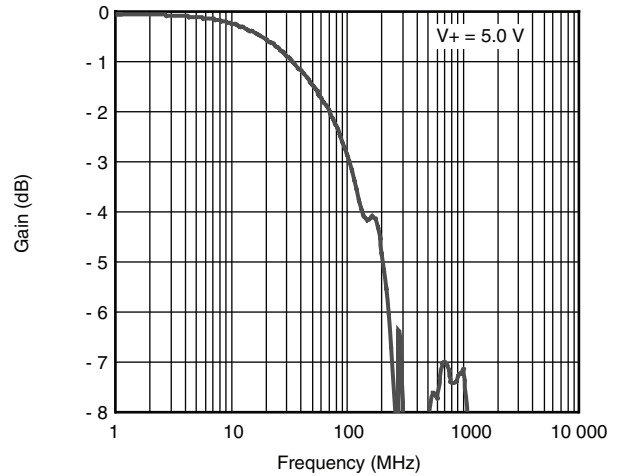
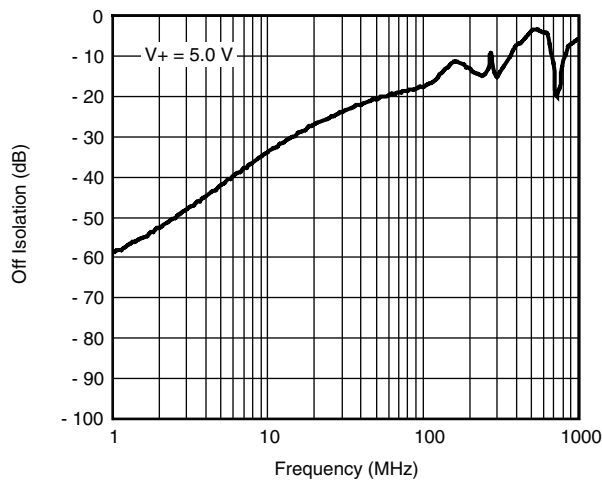
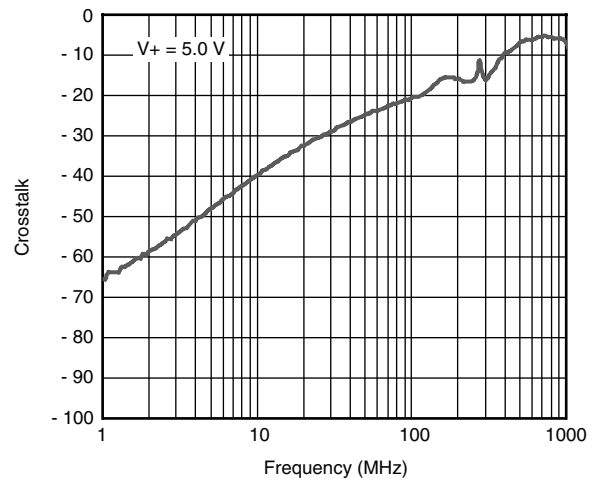
R_{ON} vs. Analog Voltage and Temperature



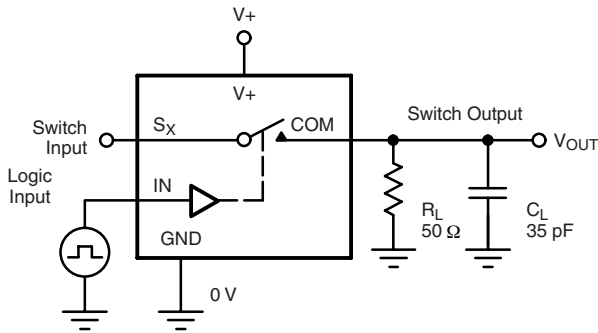
R_{ON} vs. Analog Voltage and Temperature



R_{ON} vs. Analog Voltage and Temperature

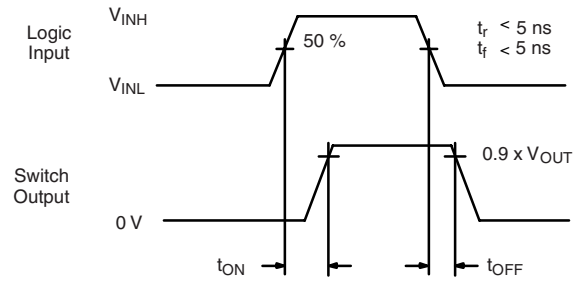
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Supply Current vs. Input Switching Frequency

Leakage Current vs. Temperature

Switching Threshold vs. Supply Voltage

Gain vs. Frequency

Off Isolation vs. Frequency

Crosstalk vs. Frequency

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
 Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

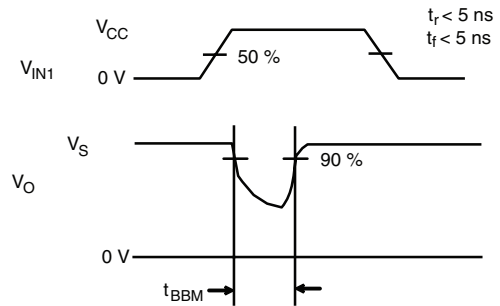
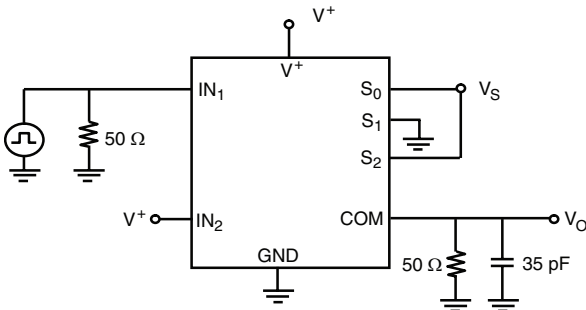


Figure 2. Break-Before-Make (DG2749)

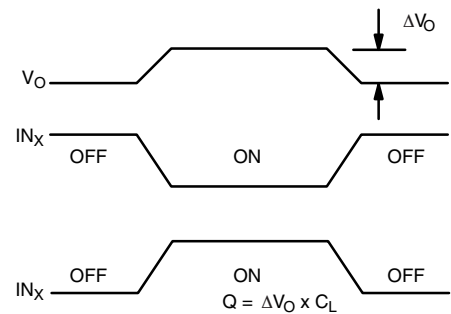
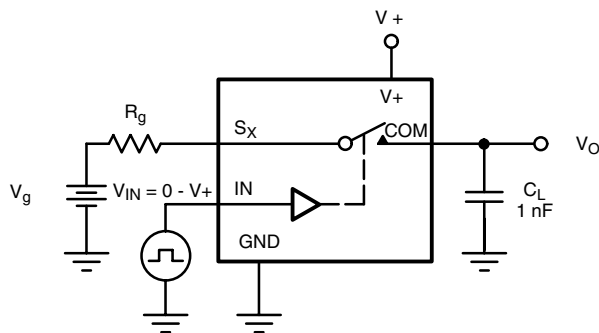
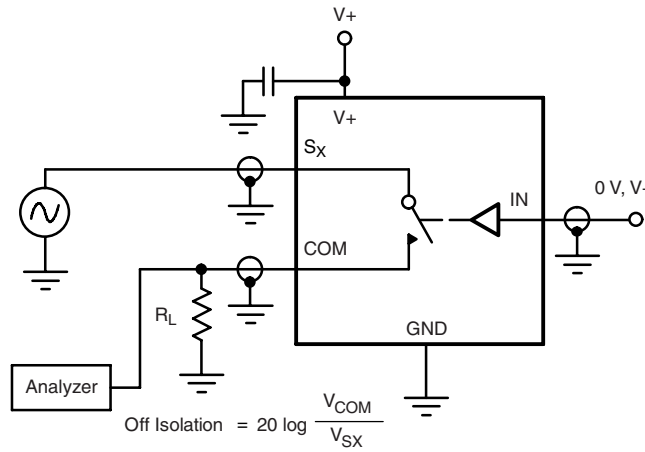
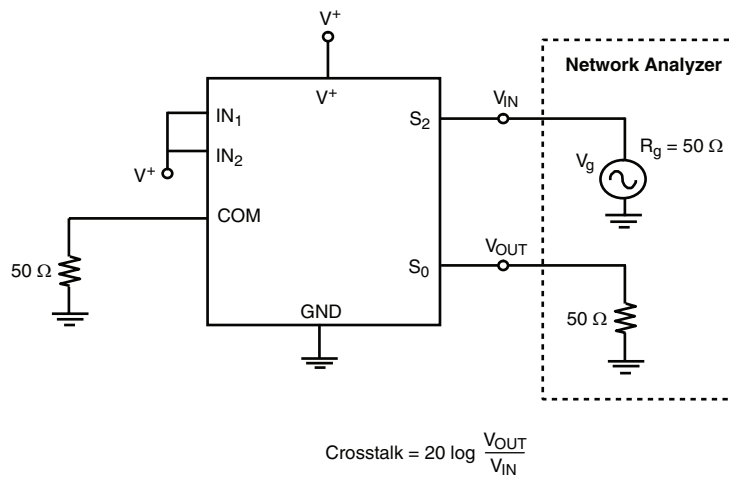
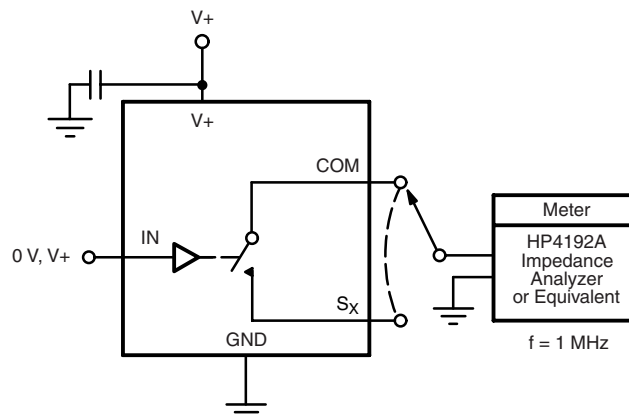
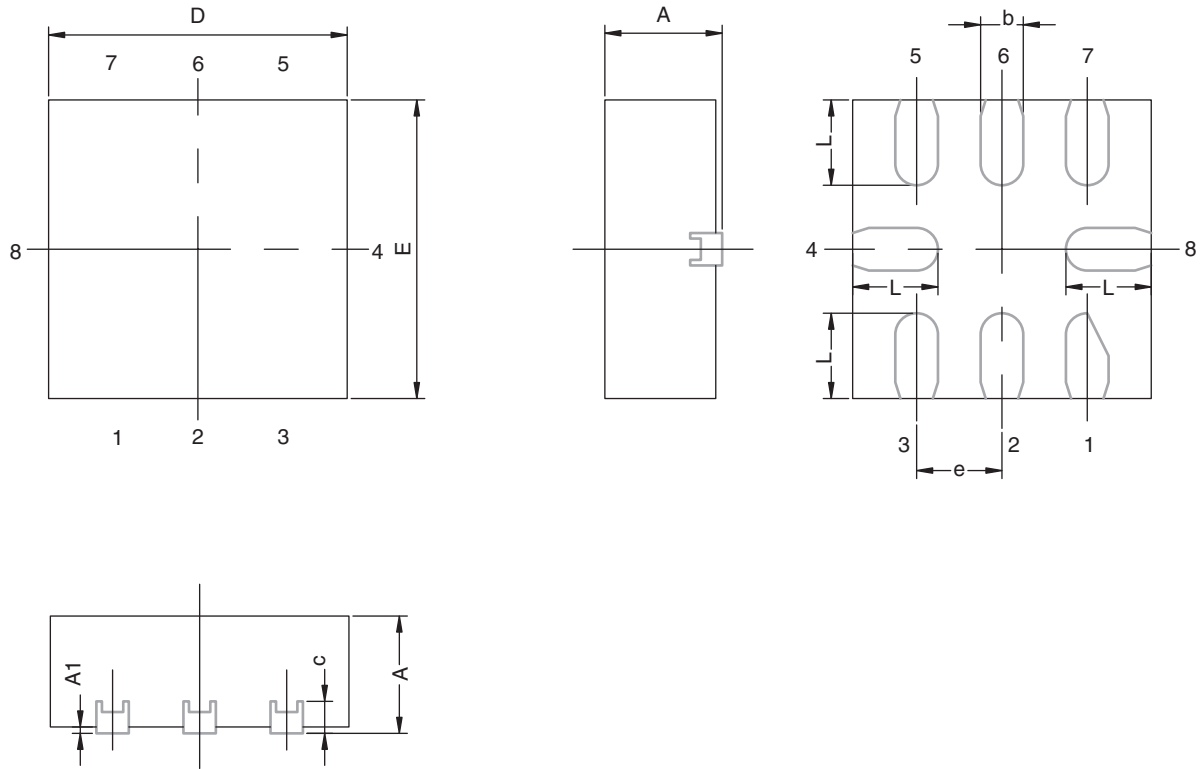


Figure 3. Charge Injection

TEST CIRCUITS

Figure 4. Off-Isolation

Figure 5. Crosstalk

Figure 6. Channel Off/On Capacitance

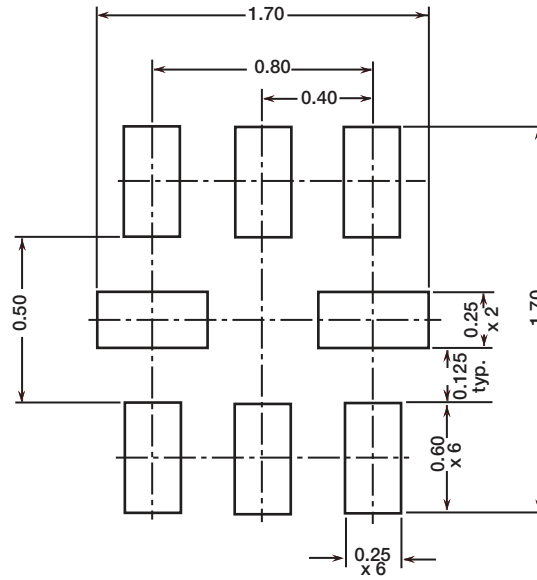
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MINIQFN-8L CASE OUTLINE



DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0.00	-	0.05	0.000	-	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.15 REF			0.006 REF		
D	1.35	1.40	1.45	0.053	0.055	0.057
E	1.35	1.40	1.45	0.053	0.055	0.057
e	0.40 BSC			0.016 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
ECN: C-08336-Rev. A, 05-May-08						
DWG: 5964						

RECOMMENDED MINIMUM PADS FOR MINI QFN 8L



Suggested Minimum Pad
Dimensions in mm



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