LM2941x 1-A Low Dropout Adjustable Regulator

1 Features

- Operating V_{IN} Range: 6 V to 26 V
- Output Voltage Adjustable From 5 V to 20 V
- Dropout Voltage Typically 0.5 V at I_{OUT} = 1 A
- Output Current in Excess of 1 A
- Trimmed Reference Voltage
- Reverse Battery Protection
- Internal Short-Circuit Current Limit
- Mirror Image Insertion Protection
- P^+ Product Enhancement Tested
- TTL, CMOS Compatible ON/OFF Switch
- WSON Space-Saving Package

2 Applications

- Industrial
- Automotive

3 Description

The LM2941 positive voltage regulator features the ability to source 1 A of output current with a typical dropout voltage of 0.5 V and a maximum of 1 V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground pin current when the differential between the input voltage and the output voltage exceeds approximately 3 V. The quiescent current with 1 A of output current and an input-output differential of 5 V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3$ V).

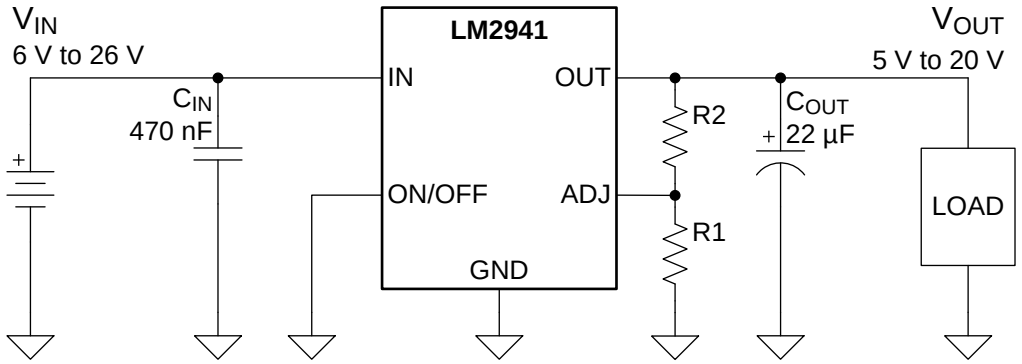
Designed also for vehicular applications, the LM2941 and all regulated circuitry are protected from reverse battery installations or two-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2941	WSON (8)	4.00 mm x 4.00 mm
	TO-263 (5)	10.16 mm x 8.42 mm
	TO-220 (5)	14.986 mm x 10.16 mm
	TO-220 (5)	10.16 mm x 8.51 mm
LM2941C	TO-263 (5)	10.16 mm x 8.42 mm
	TO-220 (5)	14.986 mm x 10.16 mm
	TO-220 (5)	10.16 mm x 8.51 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (December 2014) to Revision I — **Page**

- Changed update pin names to TI nomenclature ... 1

Changes from Revision G (April 2013) to Revision H — **Page**

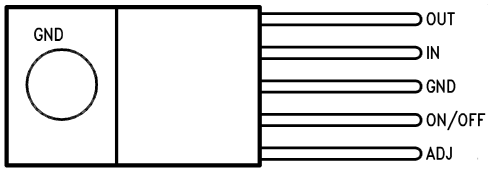
- Added *Device Information* and *ESD Ratings* tables, *Feature Description* section, *Device Functional Modes, Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section; updated *Thermal Info* .. 1

Changes from Revision F (April 2013) to Revision G — **Page**

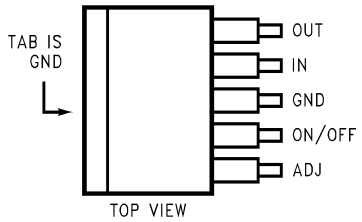
- Changed layout of National Data Sheet to TI format ... 1

5 Pin Configuration and Functions

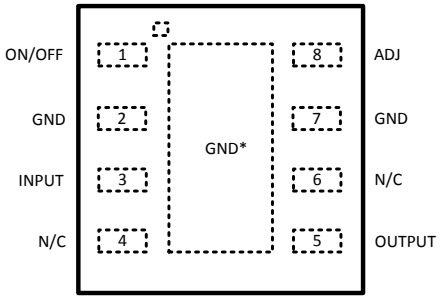
TO-220 (KC) Plastic Package
4 Pins
Top View



TO-263 (KTT) Surface-Mount Package
4 Pins



WSON (NGN)Surface Mount Package
8 Leads
Top View



* TIE TO GND OR LEAVE FLOATING

Pin Functions

PIN				TYPE	DESCRIPTION
NAME	KC	KTT	NGN		
ADJ	1	1	8	I	Sets output voltage
ON/OFF	2	2	1	I	Enable/Disable control
GND	3	3	2, 7	—	Ground
IN	4	4	3	I	Input supply
OUT	5	5	5	O	Regulated output voltage. This pin requires an output capacitor to maintain stability. See the *Detailed Design Procedure* section for output capacitor details.
NC	—	—	4, 6	—	No internal connection. Connect to GND or leave open.

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

		MIN	MAX	UNIT
Input voltage (Survival Voltage, ≤ 100 ms)	LM2941T, LM2941S, LM2941LD		60	V
	LM2941CT, LM2941CS		45	V
Internal power dissipation [3]		Internally Limited		
Maximum junction temperature			150	°C
Soldering remperature[4]	TO-220 (T), Wave, 10 s		260	°C
	TO-263 (S), 30 s		235	°C
	WSON-8 (LD), 30 s		235	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_J(max)$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/R_{\theta JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM2941 will go into thermal shutdown. If the TO-263 package is used, the thermal resistance can be reduced by increasing the PC board copper area thermally connected to the package. The value $R_{\theta JA}$ for the WSON package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (SNOA401). It is recommended that 6 vias be placed under the center pad to improve thermal performance.
(4) Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperature and time are for Sn-Pb (STD) only.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Temperatures	LM2941T	−40	125	°C
	LM2941CT	0	125	
	LM2941S	−40	125	
	LM2941CS	0	125	
	LM2941LD	−40	125	

6.4 Thermal Information

THERMAL METRIC(1)(2)		LM2941LD	LM2941S, LM2941T		UNIT
		WSON (NGN)	TO-263 (KTT)	TO-220 (KC)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.5	41	32.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.2	43.2	25.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	17	22.9	18.3	
ψ_{JT}	Junction-to-top characterization parameter	0.2	11.4	8.5	
ψ_{JB}	Junction-to-board characterization parameter	17.2	21.9	17.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	0.9	0.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_J(max)$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/R_{\theta JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM2941 will go into thermal shutdown. If the TO-263 package is used, the thermal resistance can be reduced by increasing the PC board copper area thermally connected to the package. The value $R_{\theta JA}$ for the WSON package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (SNOA401). It is recommended that 6 vias be placed under the center pad to improve thermal performance.

6.5 Electrical Characteristics: LM2941T, LM2941S, LM2941LD

5 V ≤ V_{OUT} ≤ 20 V, V_{IN} = V_{OUT} + 5 V, C_{OUT} = 22 µF, unless otherwise specified. MIN (minimum) and MAX (maximum) specifications in apply over the full Operating Temperature Range (unless otherwise specified) and typical values apply at T_J = 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference voltage	5 mA ≤ I_{OUT} ≤ 1 A(1)	1.211	1.275	1.339	V
	5 mA ≤ I_{OUT} ≤ 1 A(1), T_J = 25°C	1.237	1.275	1.313	
Line regulation	V_{OUT} + 2 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 5 mA		4	10	mV/V
Load regulation	50 mA ≤ I_{OUT} ≤ 1 A		7	10	mV/V
Output impedance	100 mADC and 20 mArms, f_{OUT} = 120 Hz		7		mΩ/V
Quiescent current	V_{OUT} + 2 V ≤ V_{IN} < 26 V, I_{OUT} = 5 mA		10	20	mA
	V_{OUT} + 2 V ≤ V_{IN} < 26 V, I_{OUT} = 5 mA, T_J = 25°C		10	15	
	V_{IN} = V_{OUT} + 5 V, I_{OUT} = 1 A		30	60	mA
	V_{IN} = V_{OUT} + 5 V, I_{OUT} = 1 A, T_J = 25°C		30	45	
RMS output noise, % of V_{OUT}	10 Hz to 100 kHz, I_{OUT} = 5 mA		0.003%		
Ripple rejection	f_{OUT} = 120 Hz, 1 Vrms, I_L = 100 mA		0.005	0.04	%/V
	f_{OUT} = 120 Hz, 1 Vrms, I_L = 100 mA, T_J = 25°C		0.005	0.02	
Long-term stability			0.4		%/1000 Hr
Dropout voltage	I_{OUT} = 1 A		0.5	1	V
	I_{OUT} = 1 A, T_J = 25°C		0.5	0.8	
	I_{OUT} = 100 mA		110	200	mV
Short-circuit current	V_{IN} max = 26 V(2)	1.6	1.9		A
Maximum line transient	V_{OUT} max 1 V above nominal V_{OUT} R_{OUT} = 100 Ω, t ≤ 100 ms	60	75		V
Maximum operational input voltage		26	31		V_{DC}
Reverse polarity DC input voltage	R_{OUT} = 100 Ω, V_{OUT} ≥ −0.6 V	−15	−30		V
Reverse polarity transient input voltage	t ≤ 100 ms, R_{OUT} = 100 Ω	−50	−75		

(1) The output voltage range is 5 V to 20 V and is determined by the two external resistors, R1 and R2. See Figure 18.
(2) Output current capability will decrease with increasing temperature, but will not go below 1 A at the maximum specified temperatures.

Electrical Characteristics: LM2941T, LM2941S, LM2941LD (continued)

5 V ≤ V_{OUT} ≤ 20 V, V_{IN} = V_{OUT} + 5 V, C_{OUT} = 22 µF, unless otherwise specified. MIN (minimum) and MAX (maximum) specifications in apply over the full Operating Temperature Range (unless otherwise specified) and typical values apply at T_J = 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON/OFF threshold voltage ON	I_{OUT} ≤ 1 A		1.30	0.80	V
ON/OFF threshold voltage OFF	I_{OUT} ≤ 1 A	2	1.3		
ON/OFF threshold current	$V_{ON/OFF}$ = 2 V, I_{OUT} ≤ 1 A		50	300	µA
	$V_{ON/OFF}$ = 2 V, I_{OUT} ≤ 1 A, T_J = 25°C		50	100	

6.6 Electrical Characteristics: LM2941CT, LM2941CS

5 V ≤ V_{OUT} ≤ 20 V, V_{IN} = V_{OUT} + 5 V, C_{OUT} = 22 µF, unless otherwise specified. MIN (minimum) and MAX (maximum) specifications in apply over the full Operating Temperature Range (unless otherwise specified) and typical values apply at T_J = 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference voltage	5 mA ≤ I_{OUT} ≤ 1 A (1)	1.211	1.275	1.339	V
	5 mA ≤ I_{OUT} ≤ 1 A (1), T_J = 25°C	1.237	1.275	1.313	
Line regulation	V_{OUT} + 2 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 5 mA, T_J = 25°C		4	10	mV/V
Load regulation	50 mA ≤ I_{OUT} ≤ 1 A, T_J = 25°C		7	10	mV/V
Output impedance	100 mADC and 20 mArms, f_{OUT} = 120 Hz		7		mΩ/V
Quiescent current	V_{OUT} + 2 V ≤ V_{IN} < 26 V, I_{OUT} = 5 mA, T_J = 25°C		10	15	mA
	V_{IN} = V_{OUT} + 5 V, I_{OUT} = 1 A		30	60	mA
	V_{IN} = V_{OUT} + 5 V, I_{OUT} = 1 A, T_J = 25°C		30	45	
RMS output noise, % of V_{OUT}	10 Hz to 100 kHz I_{OUT} = 5 mA		0.003%		
Ripple rejection	f_{OUT} = 120Hz, 1 Vrms, I_L = 100 mA, T_J = 25°C		0.005	0.02	%/V
Long-term stability			0.4		%/1000 Hr
Dropout voltage	I_{OUT} = 1A		0.5	1	V
	I_{OUT} = 1A, T_J = 25°C		0.5	0.8	
	I_{OUT} = 100 mA		110	200	mV
Short-circuit current	V_{IN} max = 26 V (2), T_J = 25°C	1.6	1.9		A
Maximum line transient	V_{OUT} max 1 V above nominal V_{OUT}, R_{OUT} = 100 Ω, t ≤ 100 ms, , T_J = 25°C	45	55		V
Maximum operational input voltage	T_J = 25°C	26	31		V_{DC}
Reverse polarity DC input voltage	R_{OUT} = 100 Ω, V_{OUT} ≥ −0.6 V, T_J = 25°C	−15	−30		V
Reverse polarity transient input voltage	t ≤ 100 ms, R_{OUT} = 100 Ω, T_J = 25°C	−45	−55		
ON/OFF threshold voltage ON	I_{OUT} ≤ 1 A, T_J = 25°C		1.3	0.8	V
ON/OFF threshold voltage OFF	I_{OUT} ≤ 1 A, T_J = 25°C	2	1.3		
ON/OFF threshold current	$V_{ON/OFF}$ = 2 V, I_{OUT} ≤ 1 A, T_J = 25°C		50	100	µA

(1) The output voltage range is 5 V to 20 V and is determined by the two external resistors, R1 and R2. See Typical Application.
(2) Output current capability will decrease with increasing temperature, but will not go below 1 A at the maximum specified temperatures.

6.7 Typical Characteristics

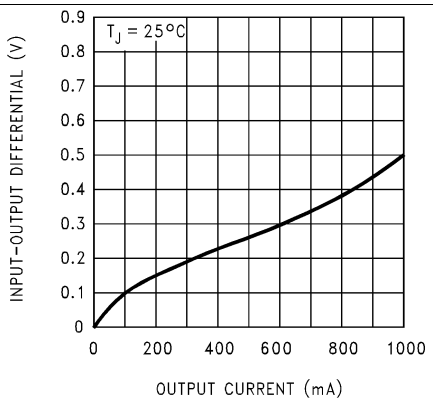


Figure 1. Dropout Voltage

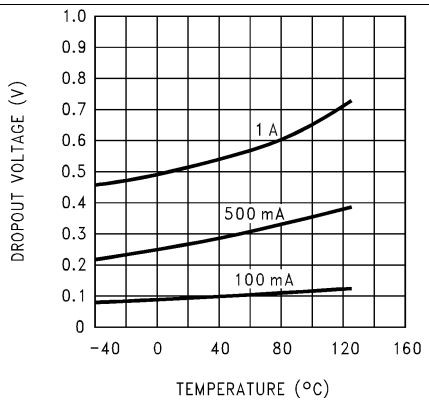


Figure 2. Dropout Voltage vs. Temperature

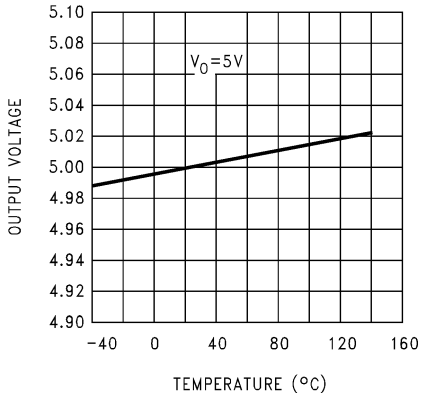


Figure 3. Output Voltage

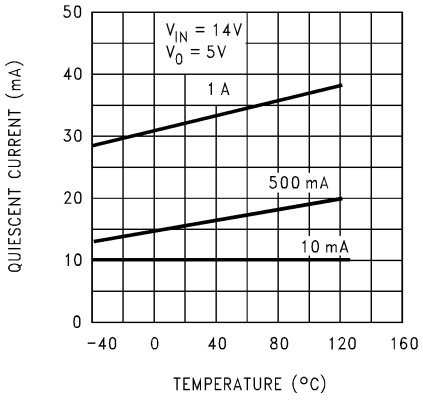


Figure 4. Quiescent Current vs. Temperature

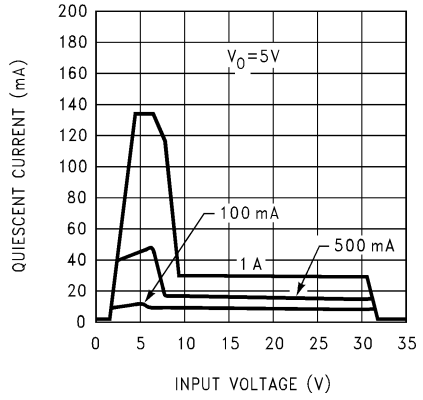


Figure 5. Quiescent Current

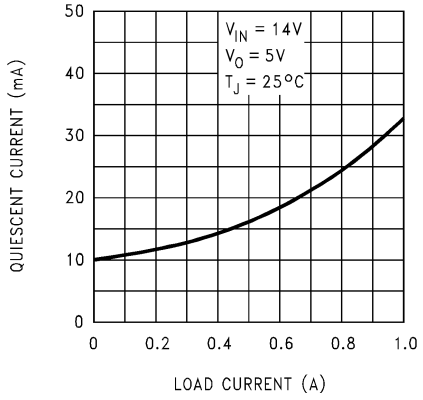


Figure 6. Quiescent Current

Typical Characteristics (continued)

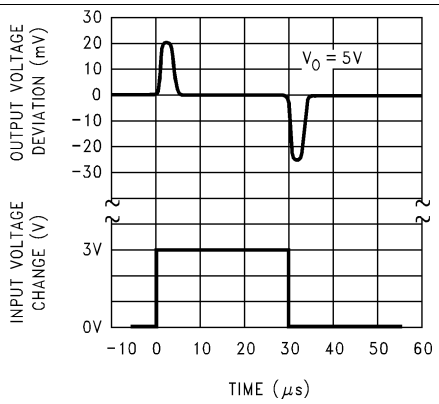


Figure 7. Line Transient Response

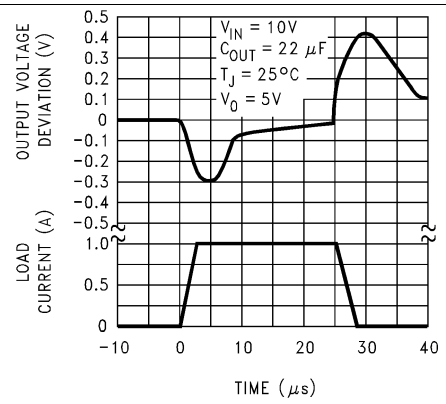


Figure 8. Load Transient Response

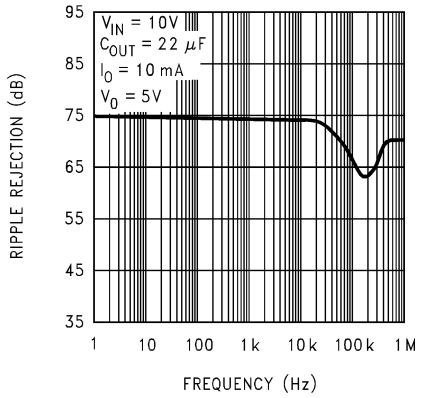


Figure 9. Ripple Rejection

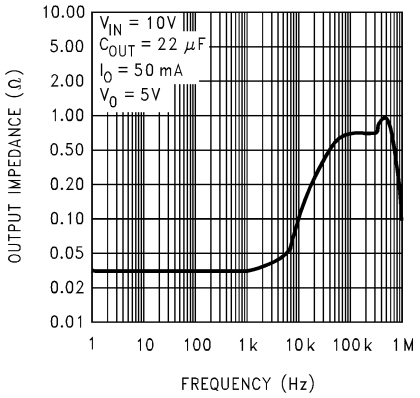


Figure 10. Output Impedance

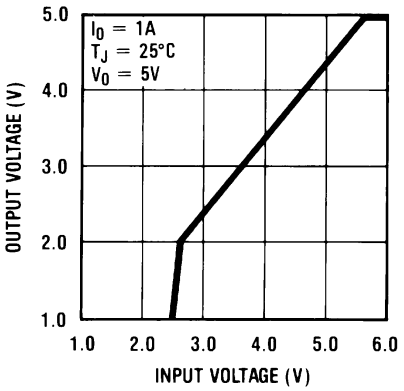


Figure 11. Low Voltage Behavior

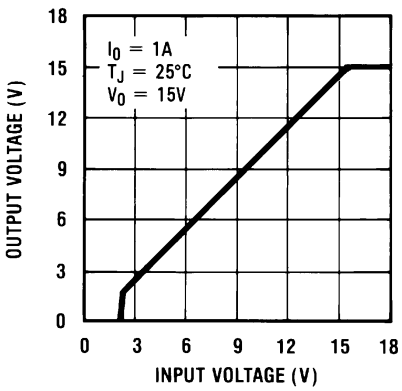


Figure 12. Low Voltage Behavior

Typical Characteristics (continued)

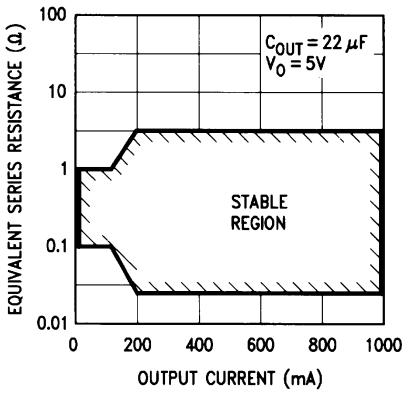


Figure 13. Output Capacitor ESR

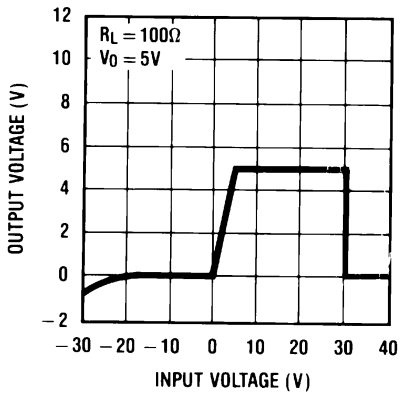


Figure 14. Output at Voltage Extremes

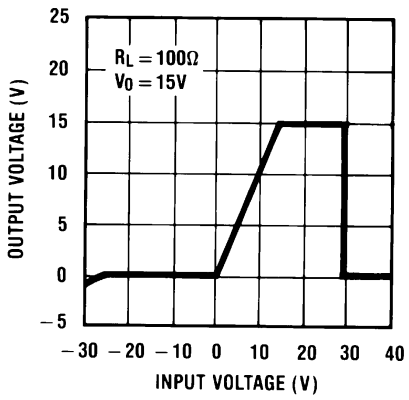


Figure 15. Output at Voltage Extremes

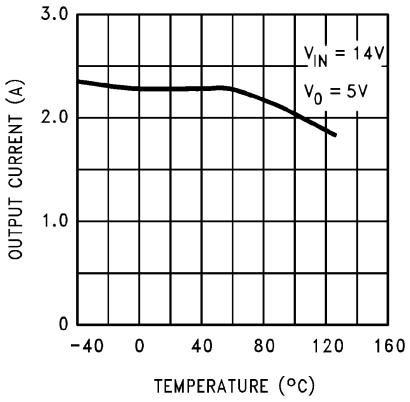


Figure 16. Peak Output Current

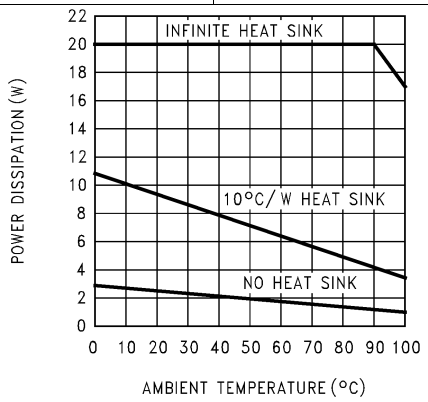


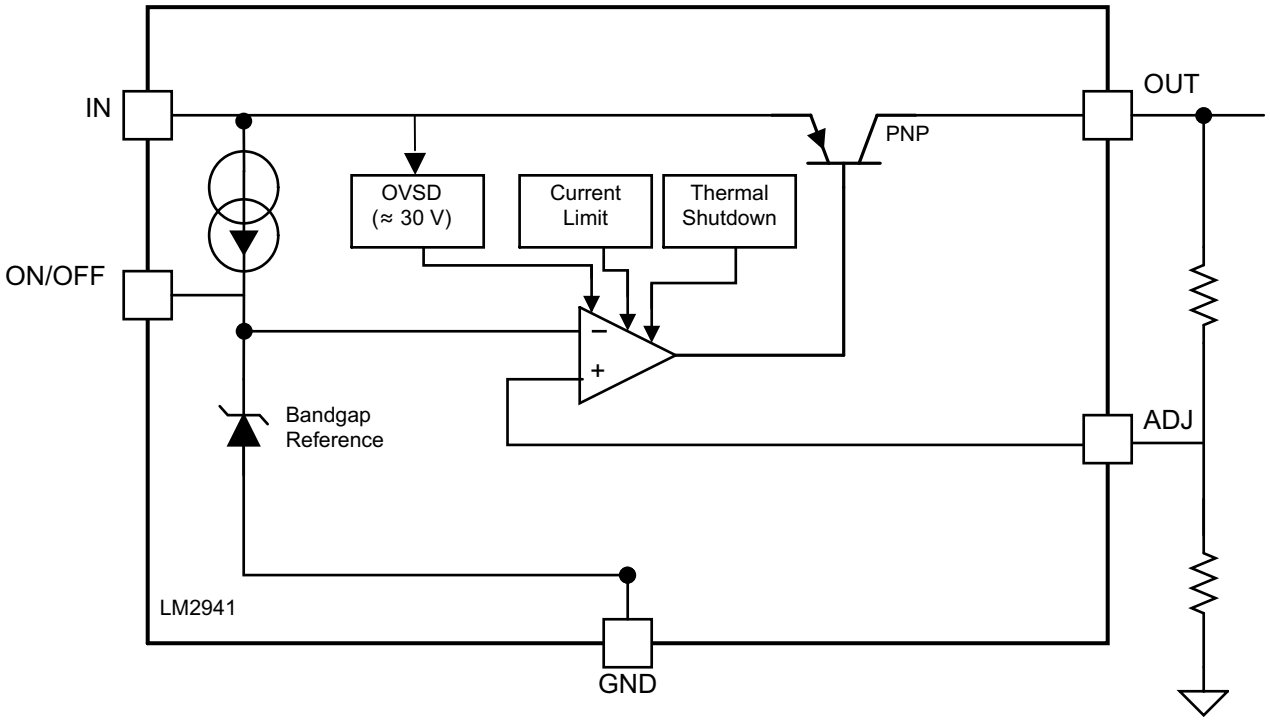
Figure 17. Maximum Power Dissipation (TO-220)

7 Detailed Description

7.1 Overview

The LM2941 positive voltage regulator features the ability to source 1 A of output current with a dropout voltage of typically 0.5 V and a maximum of 1 V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3 V. The quiescent current with 1 A of output current and an input-output differential of 5 V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} – V_{OUT} \leq 3$ V).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Short-Circuit Current Limit

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting a thermal shutdown of the output.

7.3.2 Overvoltage Shutdown (OVSD)

Input voltage greater than typically 30 V will cause the LM2941 output to be disabled. When operating with the input voltage greater than the maximum recommended input voltage of 26 V, the device performance is not ensured. Continuous operation with the input voltage greater than the maximum recommended input voltage is discouraged.

Feature Description (continued)

7.3.3 Thermal Shutdown (TSD)

The LM2941 contains the thermal shutdown circuitry to turn off the output when excessive heat is dissipated in the LDO. The internal protection circuitry of the LM2941 is designed to protect against thermal overload conditions. The TSD circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability as the junction temperature will be exceeding the absolute maximum junction temperature rating.

7.3.4 Thermal Overload Protection

The LM2941 incorporates a linear form of thermal protection that limits the junction temperature (T_J) to typically 155°C.

Should the LM2941 see a fault condition that results in excessive power dissipation and the junction temperature approaches 155°C, the device will respond by reducing the output current (which reduces the power dissipation) to hold the junction temperature at 155°C.

Thermal Overload protection is not an ensured operating condition. Operating at, or near to, the thermal overload condition for any extended period of time is not encouraged, or recommended, as this may shorten the lifetime of the device.

7.4 Device Functional Modes

7.4.1 Operation With ON/OFF Control

The ON/OFF pin has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated externally, either actively or passively. The ON/OFF pin requires a low level to enable the output, and a high level to disable the output. To ensure reliable operation, the ON/OFF pin voltage must rise above the maximum ON/OFF(OFF) voltage threshold (2 V) to disable the output, and must fall below the minimum ON/OFF(ON) voltage threshold (0.8 V) to enable the output. If the ON/OFF function is not needed this pin can be connected directly to Ground. If the ON/OFF pin is being pulled to a high state through a series resistor, an allowance must be made for the ON/OFF pin current that will cause a voltage drop across the pull-up resistor

8 Application and Implementation

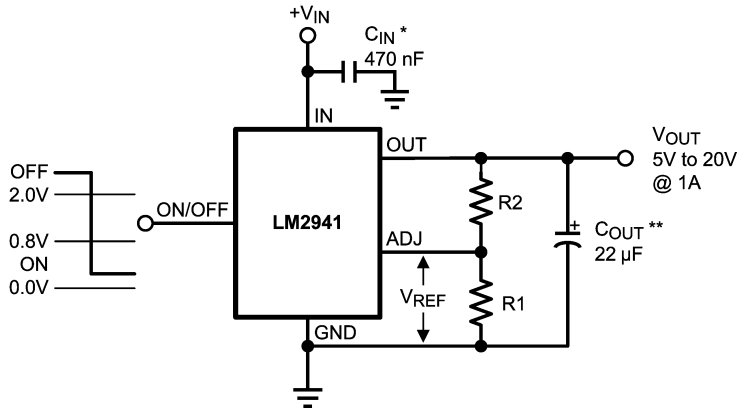
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 18 shows the typical application circuit for the LM2941. The output capacitor, C_{OUT}, must have a capacitance value of at least 22 µF with an equivalent series resistance (ESR) of at least 100 mΩ, but no more than 1 Ω. The minimum capacitance value and the ESR requirements apply across the entire expected operating ambient temperature range.

8.2 Typical Application



$$V_{OUT} = \text{Reference voltage} \times \frac{R1 + R2}{R1} \text{ where } V_{REF} = 1.275 \text{ typical}$$

$$\text{Solving for R2: } R2 = R1 \left(\frac{V_O}{V_{REF}} - 1 \right)$$

Note: Using 1 kΩ for R1 will ensure that the bias current error from the adjust pin will be negligible. Do not bypass R1 or R2. This will lead to instabilities.

***** Required if regulator is located far from power supply filter.

****** C_{OUT} must be at least 22 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical.

Figure 18. 5-V to 20-V Adjustable Regulator

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10 V to 26 V
Output voltage	15 V
Output current range	5 mA to 1 A
Input capacitor value	0.47 µF
Output capacitor value	22 µF minimum
Output capacitor ESR range	100 mΩ to 1 Ω

8.2.2 Detailed Design Procedure

8.2.2.1 Output Capacitor

A tantalum capacitor with a minimum capacitance value of 22 µF, and ESR in the range of 0.01 Ω to 5 Ω, is required at the output pin for loop stability. It must be located less than 1 cm from the device. There is no limitation on any additional capacitance.

Alternately, a high quality X5R/X7R 22 µF ceramic capacitor may be used for the output capacitor only if an appropriate value of series resistance is added to simulate the ESR requirement. The ceramic capacitor selection must include an appropriate voltage de-rating of the capacitance value due to the applied output voltage. The series resistor (for ESR simulation) should be in the range of 0.1 Ω to 1 Ω.

8.2.2.2 Setting the Output Voltage

The output voltage range is 5 V to 20 V and is set by the two external resistors, R1 and R2. See the Figure 18. The output voltage is given by the formula:

$$V_{OUT} = V_{REF} \times ((R1 + R2) / R1)$$

where

- V_{REF} is typically 1.275 V (1)

Using 1 kΩ for R1 will ensure that the bias current error of the adjust pin will be negligible. Using a R1 value higher than 10 kΩ may cause the output voltage to shift across temperature due to variations in the adjust pin bias current.

Calculating the upper resistor (R2) value of the pair when the lower resistor (R1) value is known is accomplished with the following formula:

$$R2 = R1 \times ((V_{OUT} / V_{REF}) - 1) \quad (2)$$

The resistors used for R1 and R2 should be high quality, tight tolerance, and with matching temperature coefficients. It is important to remember that, although the value of V_{REF} is ensured, the final value of V_{OUT} is not. The use of low quality resistors for R1 and R2 can easily produce a V_{OUT} value that is unacceptable.

8.2.3 Application Curves

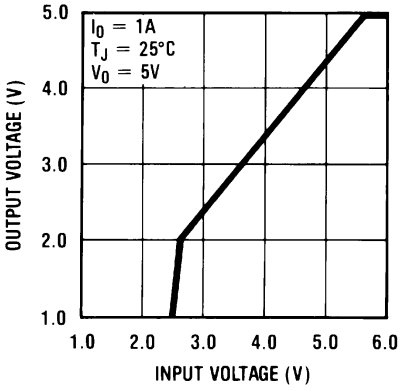


Figure 19. Low Voltage Behavior

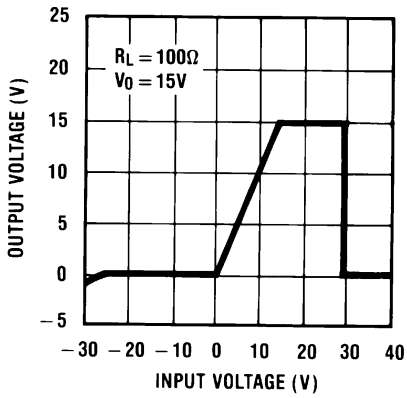


Figure 20. Output at Voltage Extremes

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between V_{OUT} + 1 V up to a maximum of 26 V. This input supply must be well regulated and free of spurious noise. To ensure that the LM2941 output voltage is well regulated, the input supply should be at least V_{OUT} + 2 V.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LM2941 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LM2941. Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LM2941, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LM2941 ground pin using as wide and short of a copper trace as is practical.

10.2 Layout Example

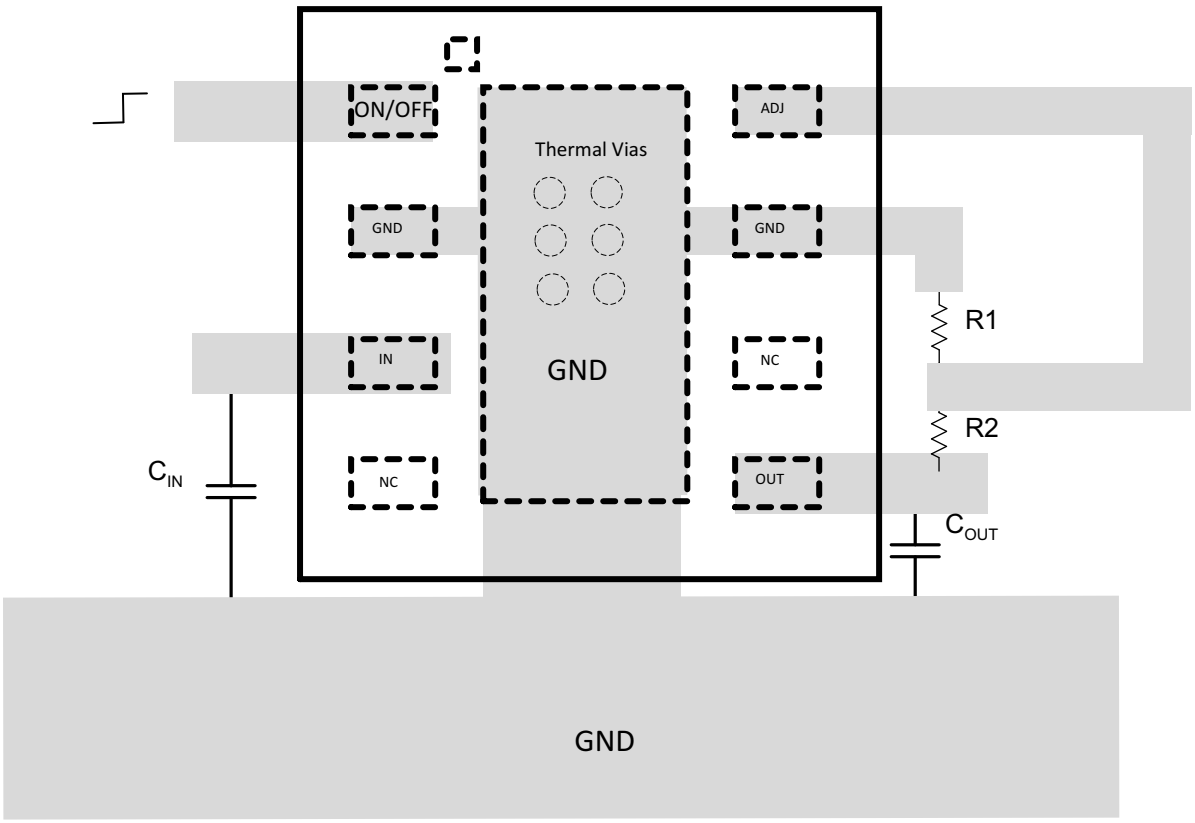


Figure 21. LM2941 WSON Package Typical Layout

Layout Example (continued)

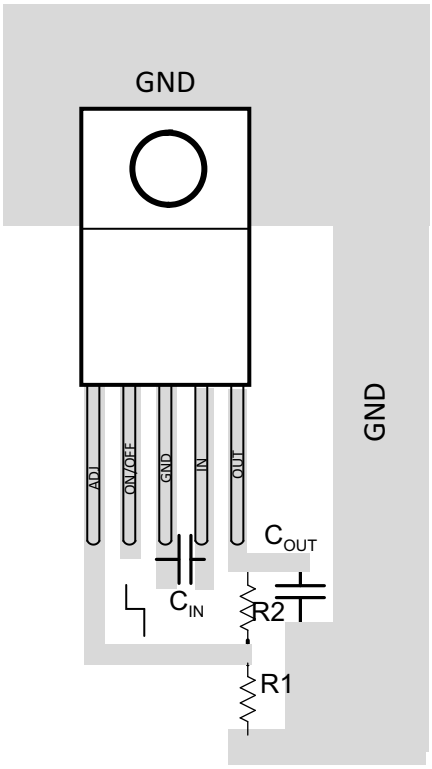


Figure 22. LM2941 TO-220 Package Typical Layout

Layout Example (continued)

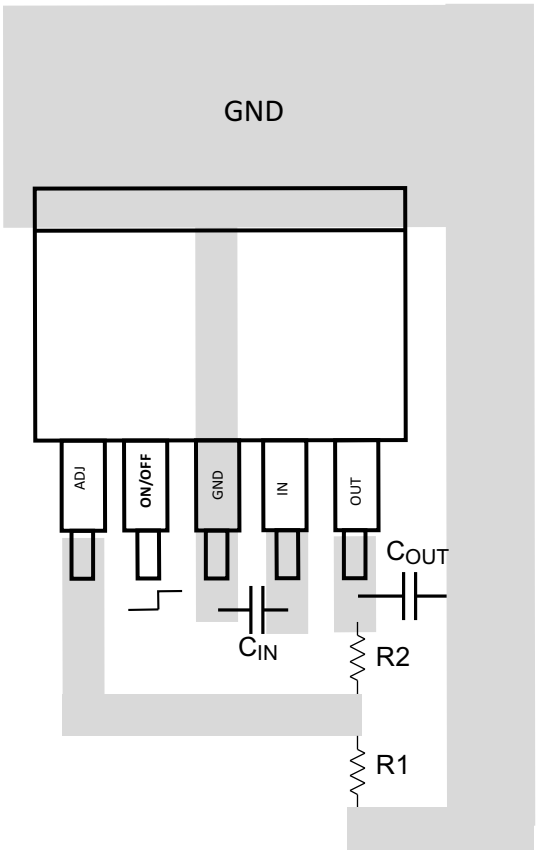


Figure 23. LM2941 TO-263 Package Typical Layout

10.3 Power Dissipation

Consideration should be given to the maximum power dissipation ($P_{D(MAX)}$) which is limited by the maximum operating junction temperature ($T_{J(MAX)}$) of 125°C, the maximum operating ambient temperature ($T_{A(MAX}$)) of the application, and the thermal resistance ($R_{\theta JA}$) of the package. Under all possible conditions, the junction temperature (T_J) must be within the range specified in the Operating Ratings. The total power dissipation of the device is given by:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + (V_{IN} \times I_{GND}) \quad (3)$$

where I_{GND} is the operating ground pin current of the device (specified under *Electrical Characteristics: LM2941T, LM2941S, LM2941LD* and *Electrical Characteristics: LM2941CT, LM2941CS*).

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum expected ambient temperature ($T_{A(MAX)}$) of the application, and the maximum allowable junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (4)$$

The maximum allowable value for junction to ambient Thermal Resistance, $R_{\theta JA}$, required to keep the junction temperature, T_J, from exceeding maximum allowed can be calculated using the formula:

$$R_{\theta JA} = \Delta T_J / P_{D(MAX)} \quad (5)$$

The maximum allowable power dissipation, $P_{D(MAX)}$, required allowed for a specific ambient temperature can be calculated using the formula:

$$P_{D(MAX)} = \Delta T_J / R_{\theta JA} \quad (6)$$

Additional information for thermal performance of surface mount packages can be found in *AN-1520: A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* (SNVA183), *AN-1187: Leadless Leadframe Package (LLP)* (SNOA401), and *AN-2020: Thermal Design By Insight, Not Hindsight* (SNVA419).

10.4 Thermal Considerations

10.4.1 TO-263 Mounting

The thermal dissipation of the TO-263 package is directly related to the printed circuit board construction and the amount of additional copper area connected to the TAB.

The TAB on the bottom of the TO-263 package is connected to the die substrate via a conductive die attach adhesive, and to device pin 3. As such, it is strongly recommend that the TAB area be connected to copper area directly under the TAB that is extended into the ground plane via multiple thermal vias. Alternately, but not recommended, the TAB may be left floating (i.e. no direct electrical connection). The TAB must not be connected to any potential other than ground.

10.4.2 WSON Mounting

The NGN (Pullback) 8-Lead WSON package requires specific mounting techniques which are detailed in Application Note 1187*: Leadless Leadframe Package (LLP)* (SNOA401). Referring to the section PCB Design Recommendations in AN-1187, it should be noted that the pad style which should be used with the WSON package is the NSMD (non-solder mask defined) type.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the WSON package is connected to the die substrate via a conductive die attach adhesive, and to device pin 2 and pin 7. As such, it is strongly recommend that the DAP area be connected copper area directly under the DAP that is extended into the ground plane via multiple thermal vias. Alternately, but not recommended, the DAP area may be left floating (i.e. no direct electrical connection). The DAP area must not be connected to any potential other than ground.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Definition of Terms

Dropout Voltage The input-voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at (V_{OUT} + 5 V) input, dropout voltage is dependent upon load current and junction temperature.

Input-Output Differential The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Input Voltage The DC voltage applied to the input terminals with respect to ground.

Line Regulation The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_{OUT} The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

11.2 Documentation Support

11.2.1 Related Documentation

- *AN-1520: A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* (SNVA183)
- *AN-1187: Leadless Leadframe Package (LLP)* (SNOA401)
- *AN-2020: Thermal Design By Insight, Not Hindsight* (SNVA419)

11.3 Related Links

Table 1 below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2941	Click here	Click here	Click here	Click here	Click here
LM2941C	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2941CS	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	0 to 125	LM2941CS P+	
LM2941CS/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	0 to 125	LM2941CS P+	Samples
LM2941CSX/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	0 to 125	LM2941CS P+	Samples
LM2941CT	NRND	TO-220	KC	5	45	TBD	Call TI	Call TI	0 to 125	LM2941CT P+	
LM2941CT/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM		LM2941CT P+	Samples
LM2941CT/LF04	ACTIVE	TO-220	NEB	5	45	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM		LM2941CT P+	Samples
LM2941CT/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	0 to 125	LM2941CT P+	Samples
LM2941LD	NRND	WSON	NGN	8	1000	TBD	Call TI	Call TI	-40 to 125	L2941LD	
LM2941LD/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L2941LD	Samples
LM2941LDX/NOPB	ACTIVE	WSON	NGN	8	4500	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L2941LD	Samples
LM2941S	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LM2941S P+	
LM2941S/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LM2941S P+	Samples
LM2941SX	NRND	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LM2941S P+	
LM2941SX/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LM2941S P+	Samples
LM2941T	NRND	TO-220	KC	5	45	TBD	Call TI	Call TI	-40 to 125	LM2941T P+	
LM2941T/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM		LM2941T P+	Samples
LM2941T/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 125	LM2941T P+	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

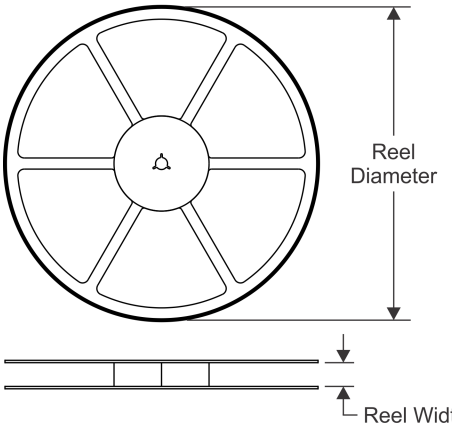
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

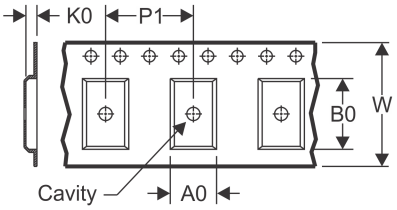
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

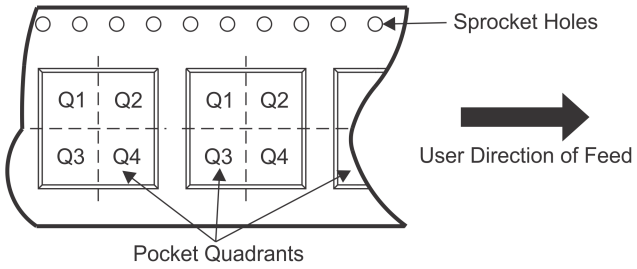


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

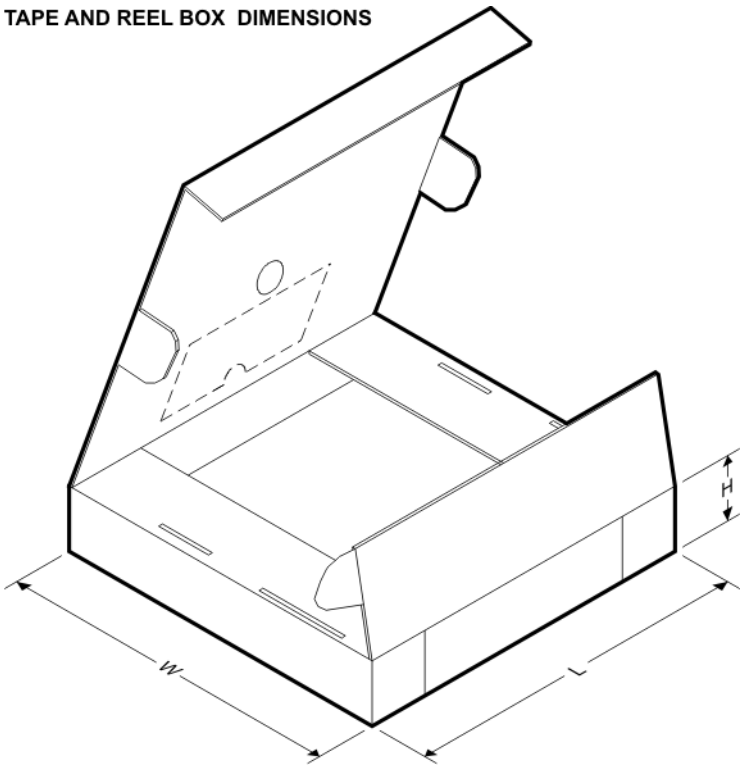
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2941CSX/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2941LD	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM2941LD/NOPB	WSON	NGN	8	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM2941LDX/NOPB	WSON	NGN	8	4500	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM2941SX	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2941SX/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

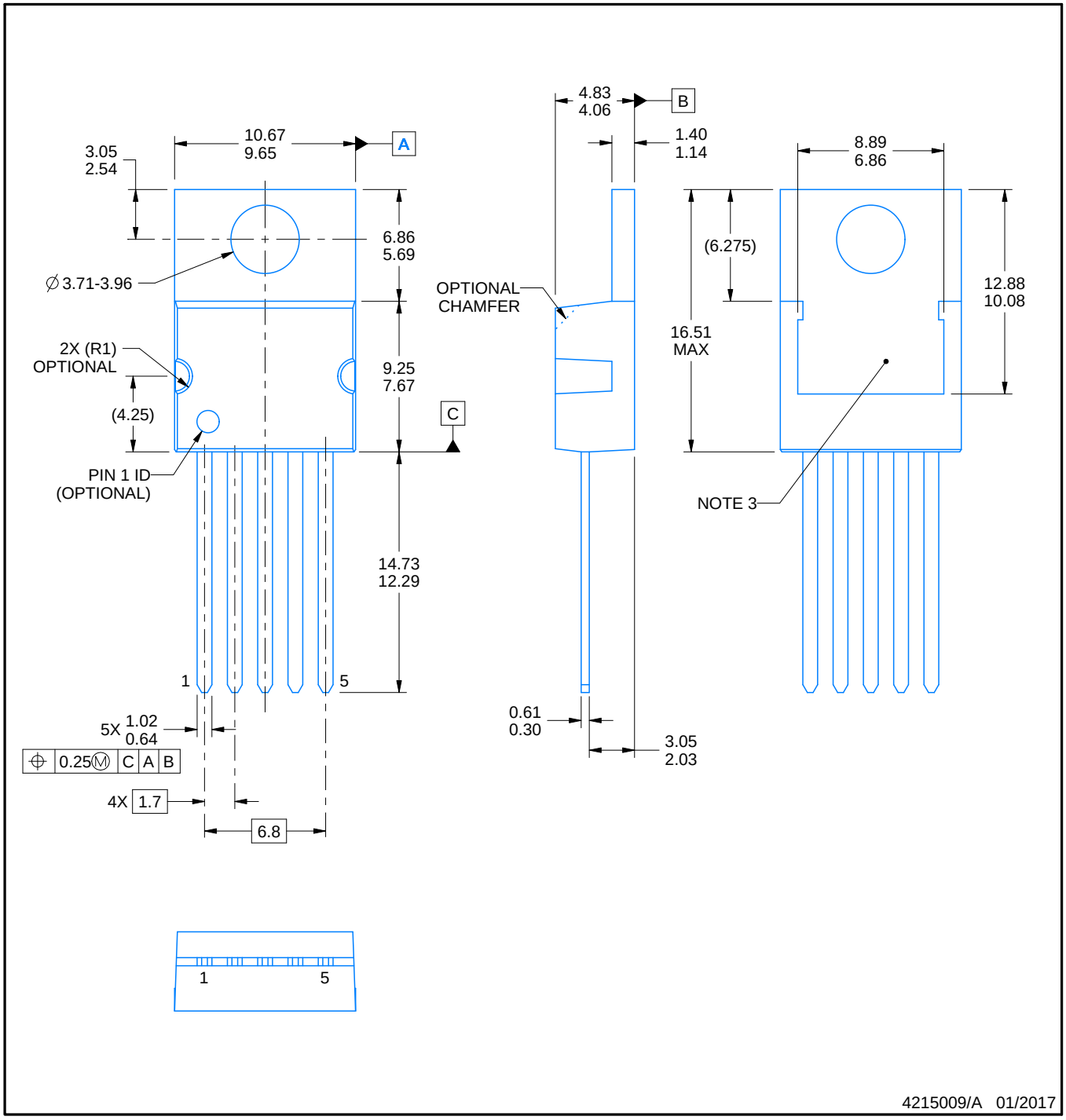
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2941CSX/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2941LD	WSON	NGN	8	1000	210.0	185.0	35.0
LM2941LD/NOPB	WSON	NGN	8	1000	195.0	200.0	45.0
LM2941LDX/NOPB	WSON	NGN	8	4500	370.0	355.0	55.0
LM2941SX	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2941SX/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

KC0005A

PACKAGE OUTLINE

TO-220 - 16.51 mm max height

TO-220



NOTES:

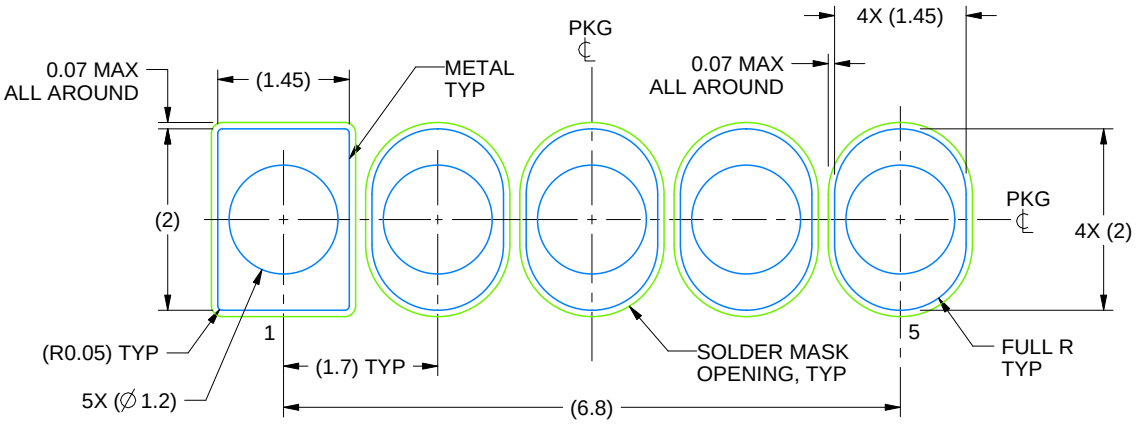
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.

EXAMPLE BOARD LAYOUT

KC0005A

TO-220 - 16.51 mm max height

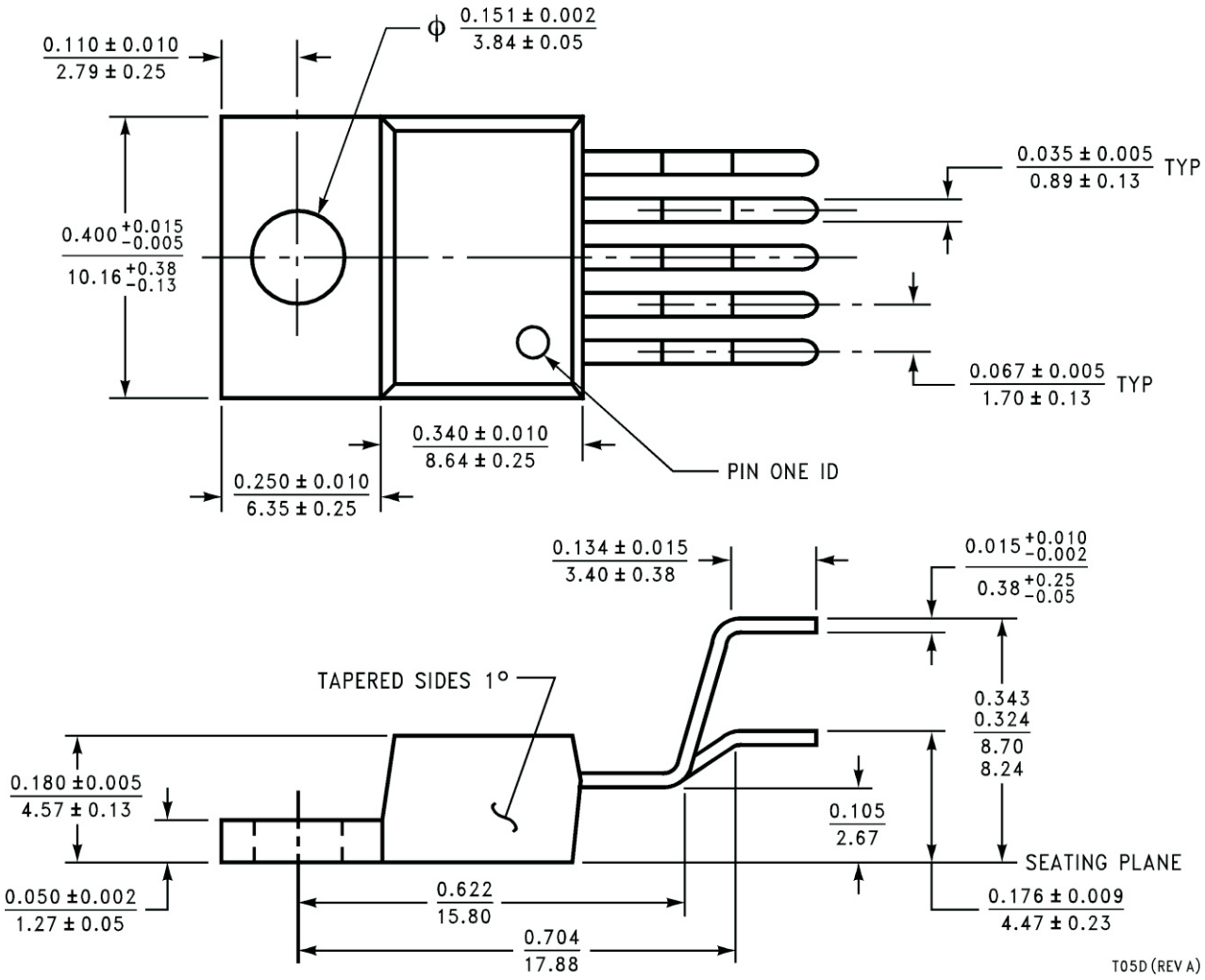
TO-220



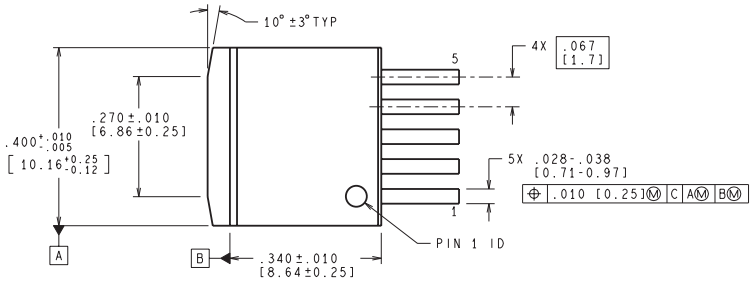
LAND PATTERN
NON-SOLDER MASK DEFINED
SCALE:12X

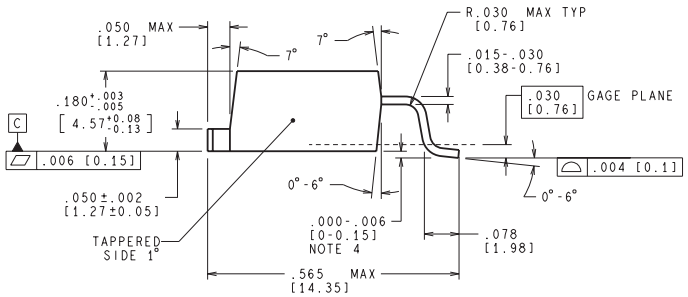
4215009/A 01/2017

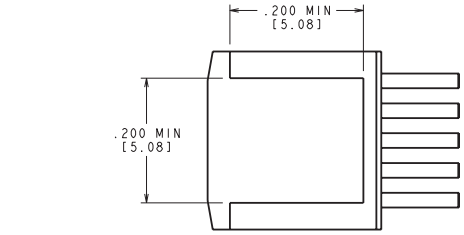
NDH0005D


0.110 ± 0.010
2.79 ± 0.25
ϕ 0.151 ± 0.002
3.84 ± 0.05
0.035 ± 0.005
0.89 ± 0.13
TYP
0.400 +0.015 −0.005
10.16 +0.38 −0.13
0.067 ± 0.005
1.70 ± 0.13
TYP
0.340 ± 0.010
8.64 ± 0.25
PIN ONE ID
0.250 ± 0.010
6.35 ± 0.25
0.134 ± 0.015
3.40 ± 0.38
0.015 +0.010 −0.002
0.38 +0.25 −0.05
TAPERED SIDES 1°
0.343
0.324
8.70
8.24
0.180 ±0.005
4.57 ± 0.13
0.105
2.67
SEATING PLANE
0.050 ±0.002
1.27 ± 0.05
0.622
15.80
0.176 ± 0.009
4.47 ± 0.23
0.704
17.88
T05D (REV A)

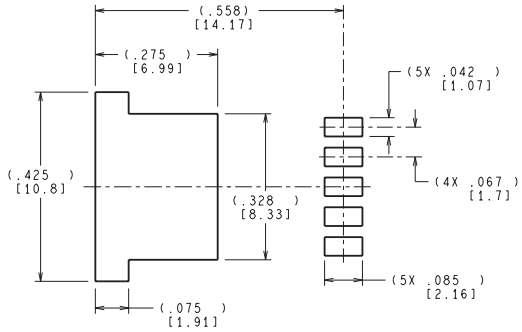
KTT0005B







BOTTOM SIDE OF PACKAGE

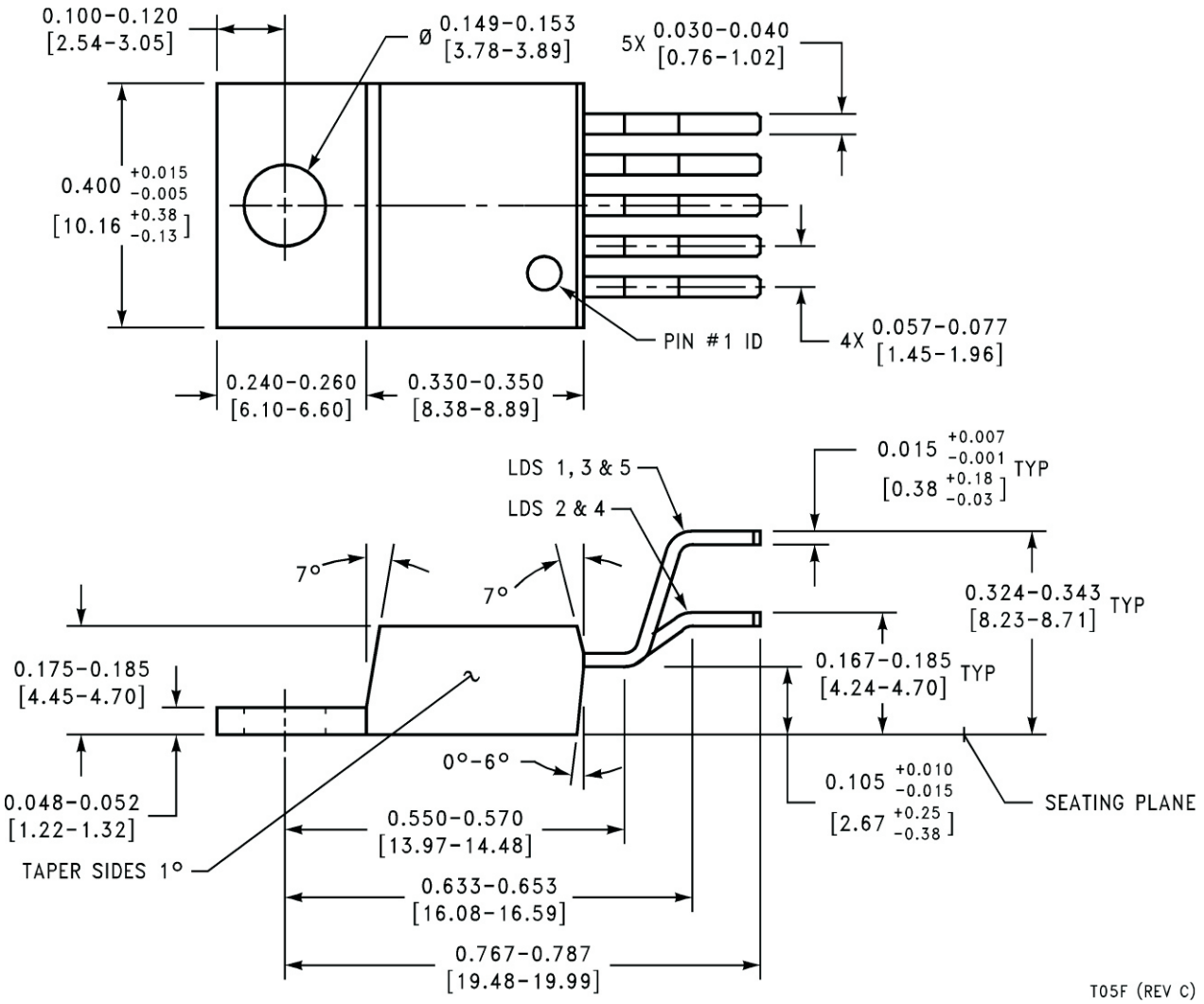


LAND PATTERN RECOMMENDATION

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

TS5B (Rev D)

NEB0005F

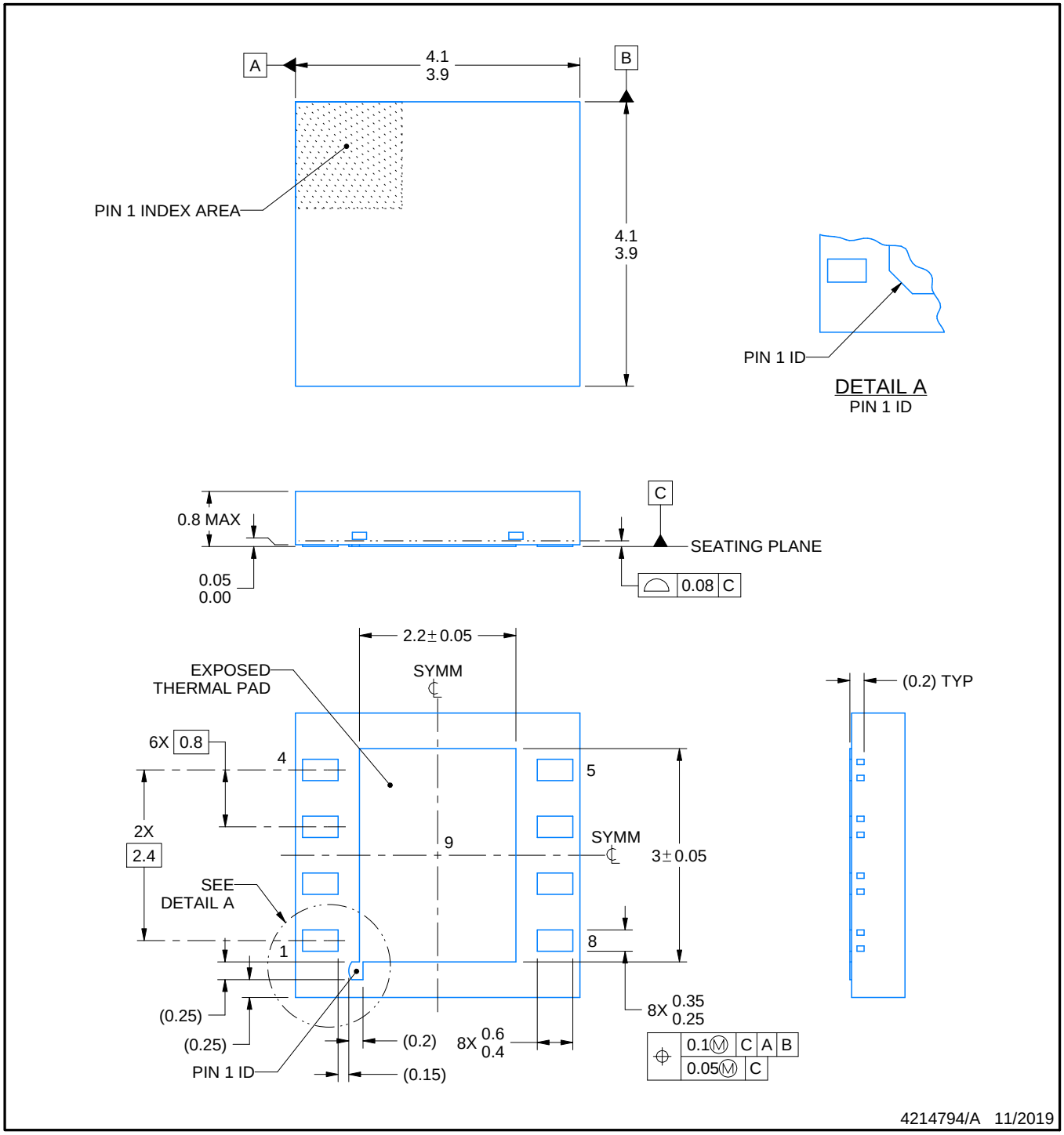

0.100-0.120
[2.54-3.05]
Ø 0.149-0.153
[3.78-3.89]
5X 0.030-0.040
[0.76-1.02]
0.400 +0.015 -0.005
[10.16 +0.38 -0.13]
PIN #1 ID
4X 0.057-0.077
[1.45-1.96]
0.240-0.260
[6.10-6.60]
0.330-0.350
[8.38-8.89]
LDS 1, 3 & 5
LDS 2 & 4
0.015 +0.007 -0.001 TYP
[0.38 +0.18 -0.03]
7°
7°
0.324-0.343 TYP
[8.23-8.71]
0.175-0.185
[4.45-4.70]
0.167-0.185 TYP
[4.24-4.70]
0°-6°
0.105 +0.010 -0.015
[2.67 +0.25 -0.38]
SEATING PLANE
0.048-0.052
[1.22-1.32]
0.550-0.570
[13.97-14.48]
TAPER SIDES 1°
0.633-0.653
[16.08-16.59]
0.767-0.787
[19.48-19.99]
T05F (REV C)

PACKAGE OUTLINE

NGN0008A

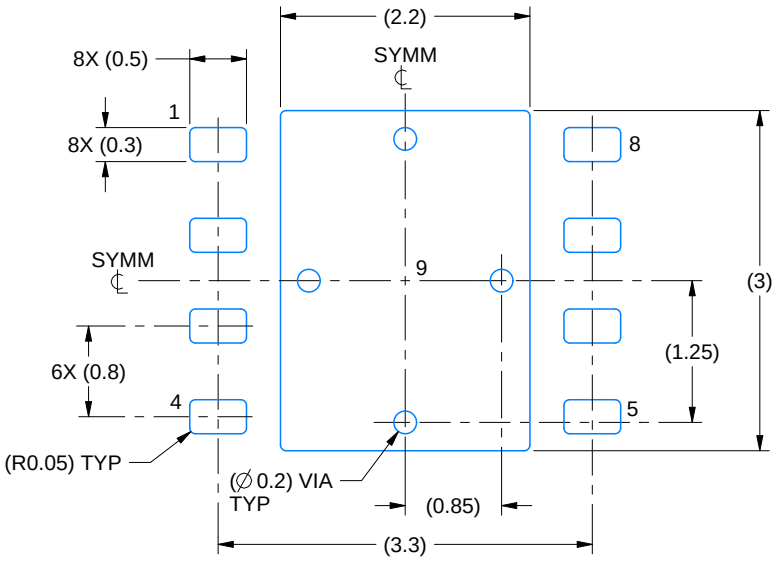
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

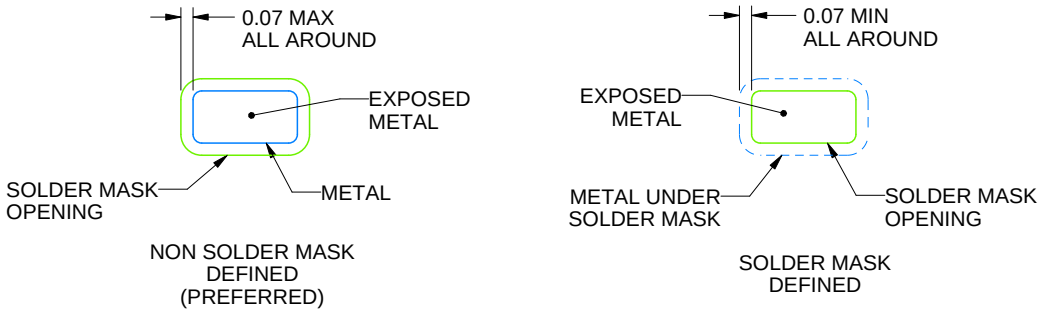


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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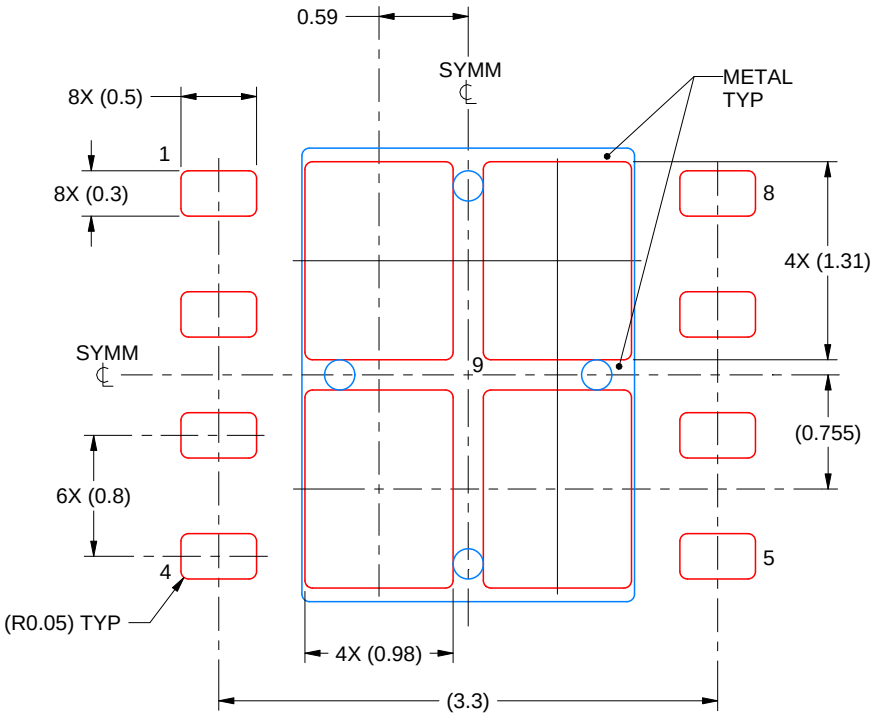
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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