

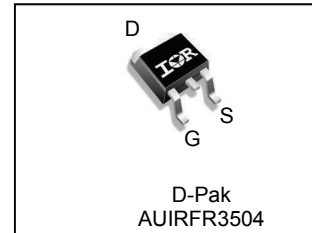
Features

- Advanced Planar Technology
- Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *

HEXFET® Power MOSFET



| | | |
|-------------------------|-------------|------------------------|
| V_{DSS} | | 40V |
| $R_{DS(on)}$ | typ. | 7.8mΩ |
| | max. | 9.2mΩ |
| I_D (Silicon Limited) | | 87A[Ⓢ] |
| I_D (Package Limited) | | 56A |



| | | |
|----------|----------|----------|
| G | D | S |
| Gate | Drain | Source |

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|------------------|--------------|--------------------|----------|-----------------------|
| | | Form | Quantity | |
| AUIRFR3504 | D-Pak | Tube | 75 | AUIRFR3504 |
| | | Tape and Reel Left | 3000 | AUIRFR3504TRL |

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

| Symbol | Parameter | Max. | Units |
|---------------------------|--|-------------------------|-------|
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited) | 87 [Ⓢ] | A |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited) | 61 [Ⓢ] | |
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited) | 56 | |
| I_{DM} | Pulsed Drain Current ^① | 350 | |
| $P_D @ T_C = 25^\circ C$ | Maximum Power Dissipation | 140 | W |
| | Linear Derating Factor | 0.92 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy (Thermally Limited) ^② | 240 | mJ |
| E_{AS} (Tested) | Single Pulse Avalanche Energy Tested Value ^{⑥⑦} | 480 | |
| I_{AR} | Avalanche Current ^① | See Fig.15,16, 12a, 12b | A |
| E_{AR} | Repetitive Avalanche Energy ^⑤ | | mJ |
| T_J | Operating Junction and | -55 to + 175 | °C |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |

Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|-----------------|---|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case [Ⓢ] | — | 1.09 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) [Ⓢ] | — | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 110 | |

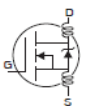
HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

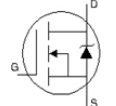
Static @ T_J = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--|--------------------------------------|------|-------|------|-------|---|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 40 | — | — | V | V _{GS} = 0V, I _D = 250μA |
| ΔV _{(BR)DSS} /ΔT _J | Breakdown Voltage Temp. Coefficient | — | 0.041 | — | V/°C | Reference to 25°C, I _D = 1mA |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | 7.8 | 9.2 | mΩ | V _{GS} = 10V, I _D = 30A ④** |
| V _{GS(th)} | Gate Threshold Voltage | 2.0 | — | 4.0 | V | V _{DS} = V _{GS} , I _D = 250μA |
| g _{fs} | Forward Trans conductance | 40 | — | — | S | V _{DS} = 10V, I _D = 30A ④** |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | 20 | μA | V _{DS} = 40V, V _{GS} = 0V |
| | | — | — | 250 | | V _{DS} = 40V, V _{GS} = 0V, T _J = 125°C |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | 200 | nA | V _{GS} = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -200 | | V _{GS} = -20V |

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

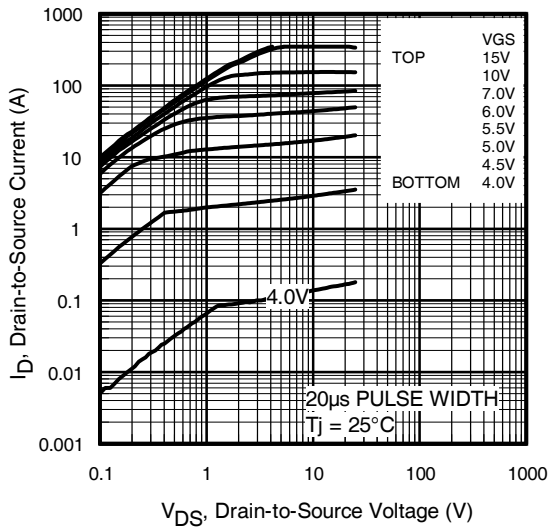
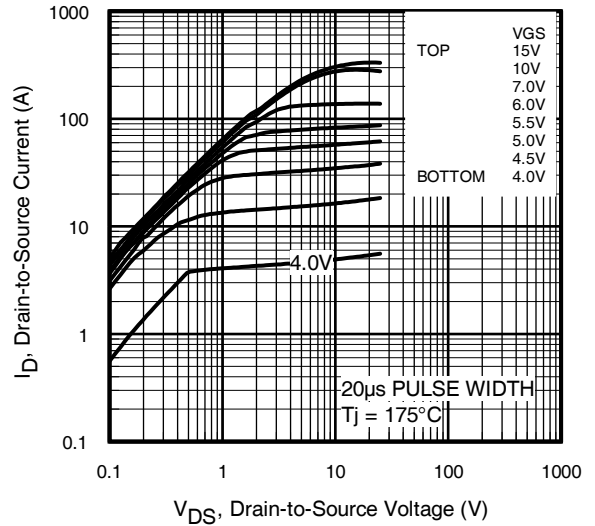
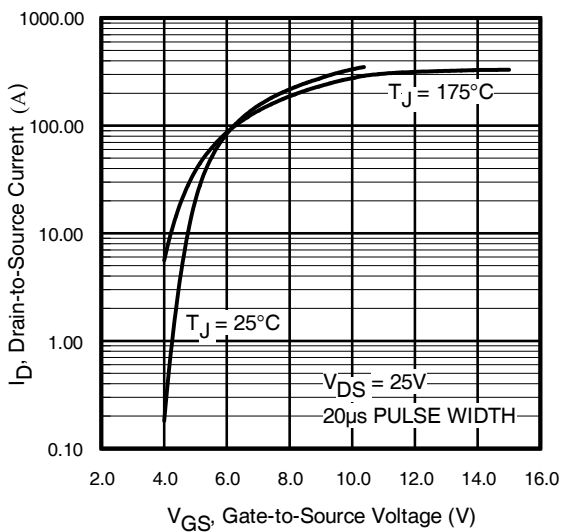
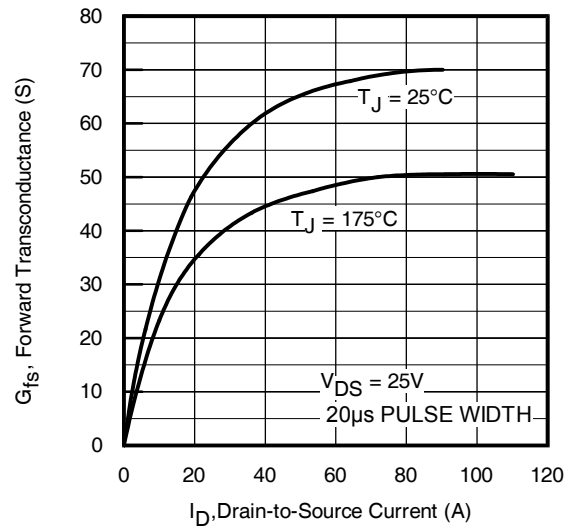
| | | | | | | |
|-----------------------|------------------------------|---|------|----|----|--|
| Q _g | Total Gate Charge | — | 48 | 71 | nC | I _D = 30A** V _{DS} = 32V V _{GS} = 10V④ |
| Q _{gs} | Gate-to-Source Charge | — | 12 | 18 | | |
| Q _{gd} | Gate-to-Drain Charge | — | 13 | 20 | | |
| t _{d(on)} | Turn-On Delay Time | — | 11 | — | ns | V _{DD} = 20V I _D = 30A** R _G = 6.8Ω V _{GS} = 10V④ |
| t _r | Rise Time | — | 53 | — | | |
| t _{d(off)} | Turn-Off Delay Time | — | 36 | — | | |
| t _f | Fall Time | — | 22 | — | | |
| L _D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact  |
| L _S | Internal Source Inductance | — | 7.5 | — | | |
| C _{iss} | Input Capacitance | — | 2150 | — | pF | V _{GS} = 0V V _{DS} = 25V f = 1.0MHz, See Fig.5 V _{GS} = 0V, V _{DS} = 1.0V f = 1.0MHz V _{GS} = 0V, V _{DS} = 32V f = 1.0MHz V _{GS} = 0V, V _{DS} = 0V to 32V |
| C _{oss} | Output Capacitance | — | 580 | — | | |
| C _{rss} | Reverse Transfer Capacitance | — | 46 | — | | |
| C _{oss} | Output Capacitance | — | 2830 | — | | |
| C _{oss} | Output Capacitance | — | 510 | — | | |
| C _{oss eff.} | Effective Output Capacitance | — | 870 | — | | |

Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|-----------------|--|--|------|-----------------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | 87 ^⑧ | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode) ① | — | — | 350 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.3 | V | T _J = 25°C, I _S = 30A**, V _{GS} = 0V ④ |
| t _{rr} | Reverse Recovery Time | — | 53 | 80 | ns | T _J = 25°C, I _F = 30A**, V _{DD} = 20V |
| Q _{rr} | Reverse Recovery Charge | — | 86 | 130 | nC | di/dt = 100A/μs④ |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D) | | | | |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
 - ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.52mH, R_G = 25Ω, I_{AS} = 30A, V_{GS} = 10V. Part not recommended for use above this value.
 - ③ I_{SD} ≤ 30A, di/dt ≤ 170A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
 - ④ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
 - ⑤ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
 - ⑥ Limited by T_{Jmax}, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
 - ⑦ This value determined from sample failure population. 100% tested to this value in production.
 - ⑧ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 56A.
 - ⑨ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
 - ⑩ R_θ is measured at T_J approximately 90°C.
- ** All AC and DC test conditions based on former package limited current of 30A.


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Typical Forward Trans conductance Vs. Drain Current

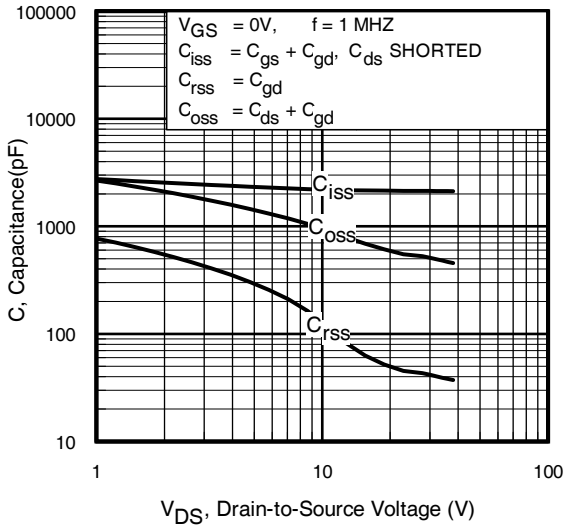


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

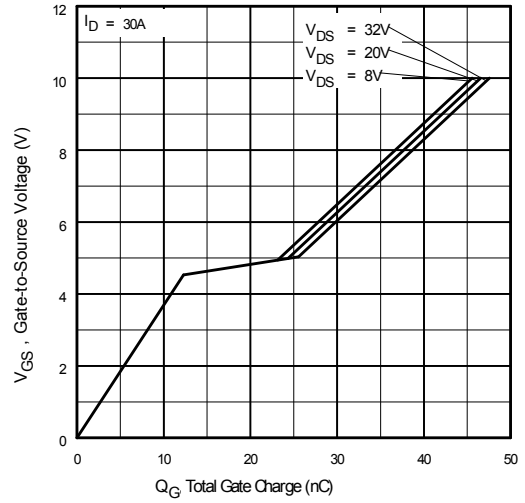


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

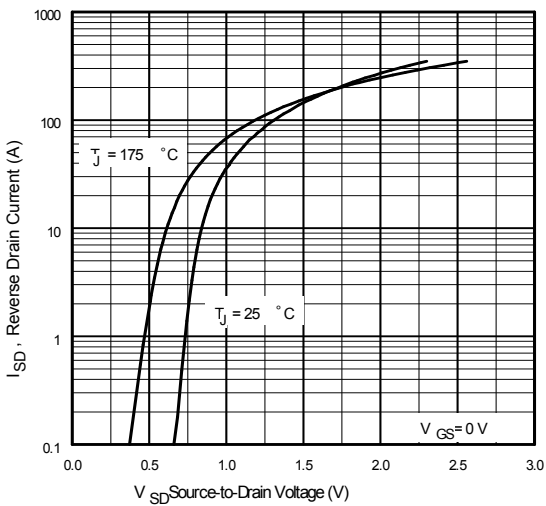


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

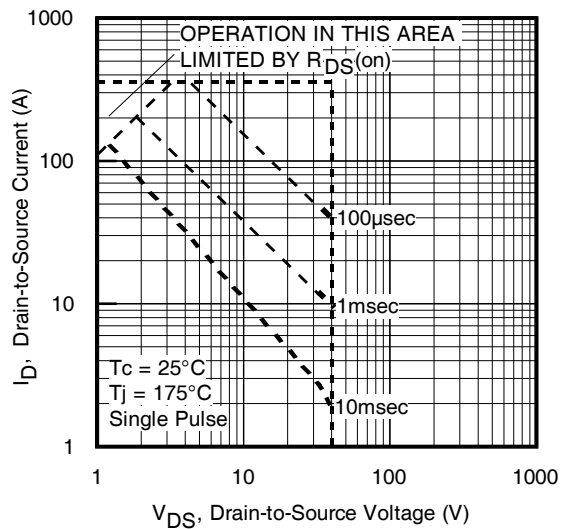


Fig 8. Maximum Safe Operating Area

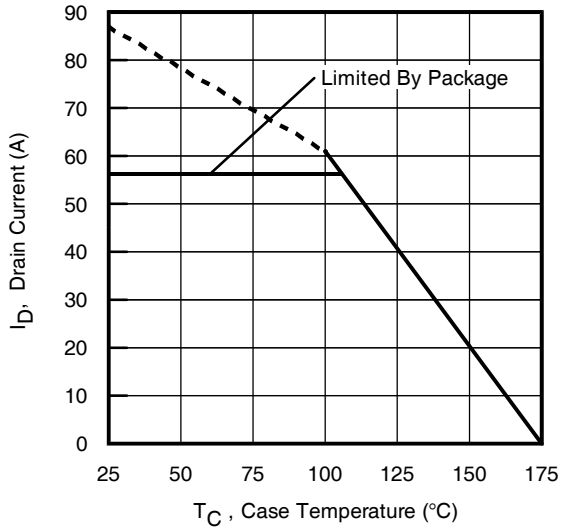


Fig 9. Maximum Drain Current Vs. Case Temperature

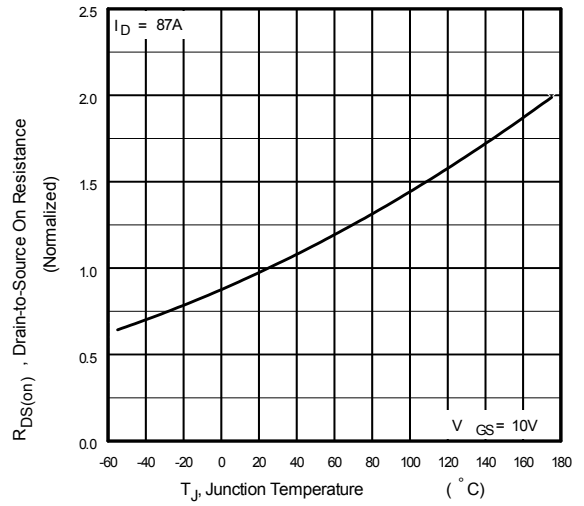


Fig 10. Normalized On-Resistance Vs. Temperature

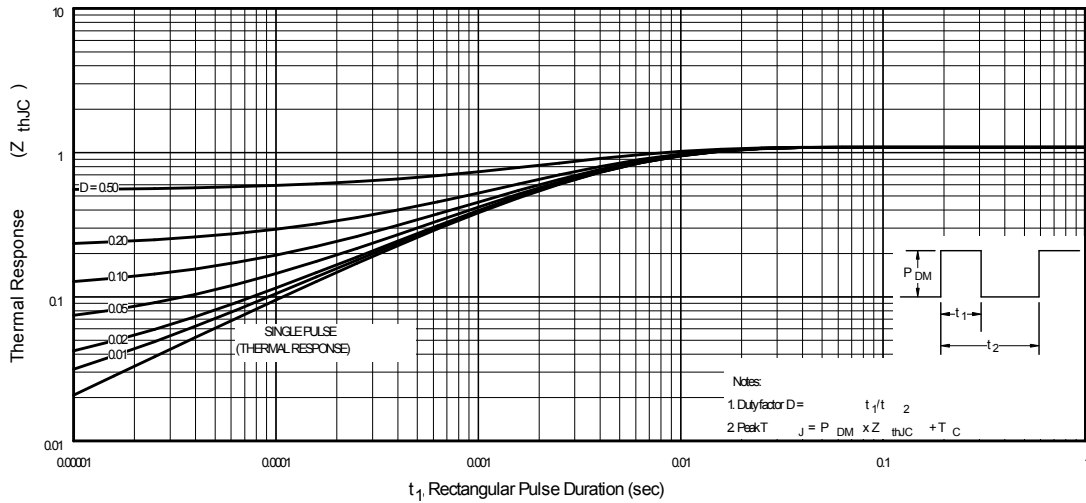


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

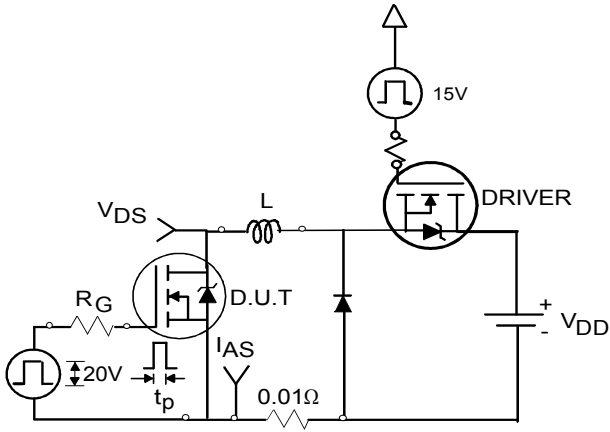
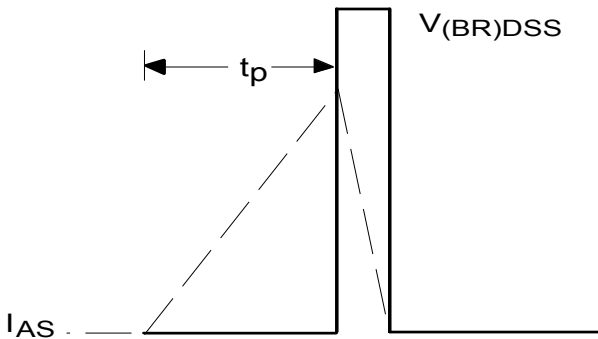
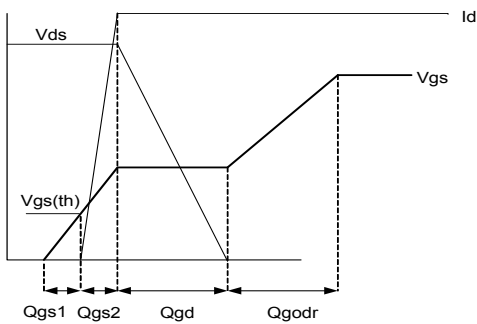
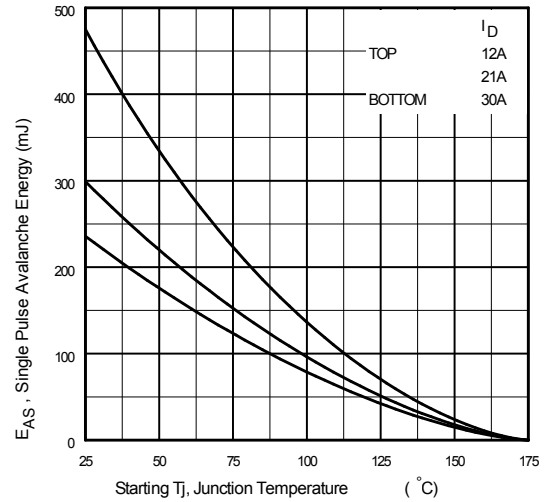
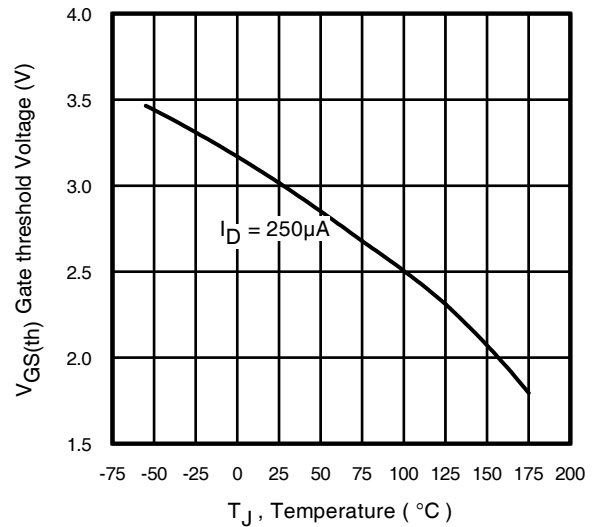
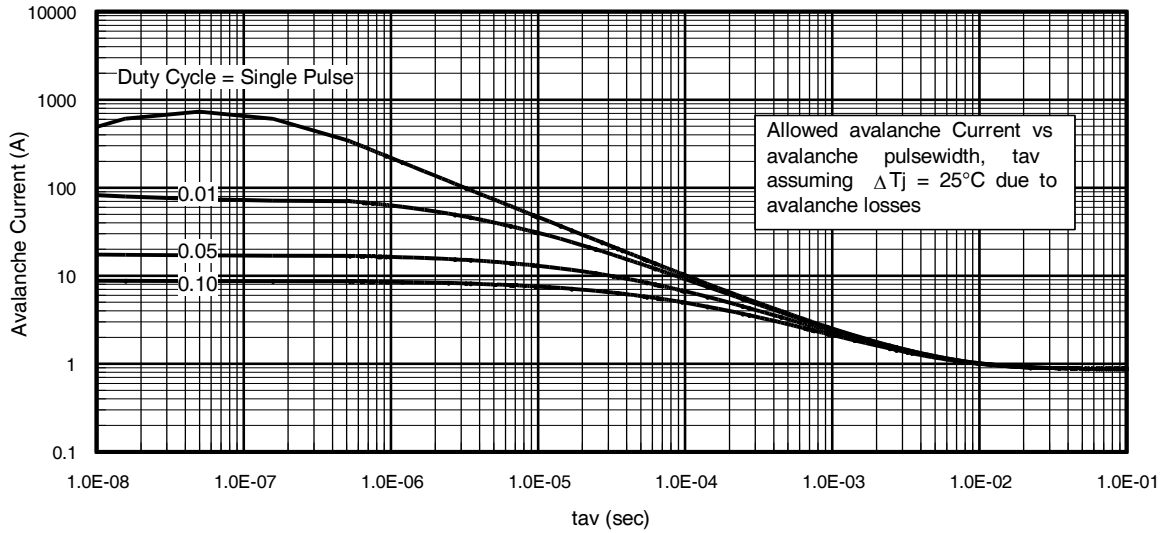
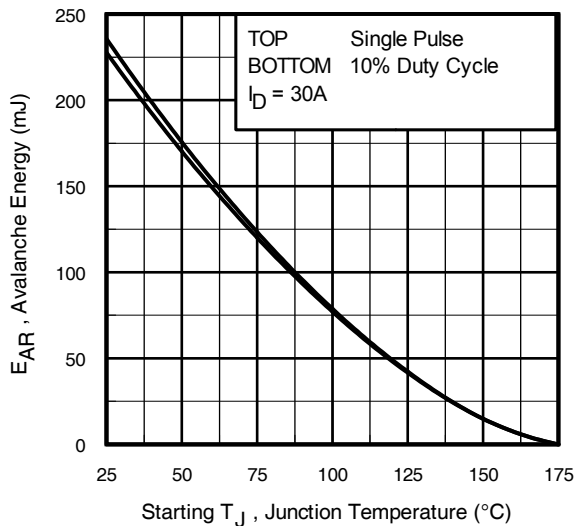

Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 14. Threshold Voltage Vs. Temperature


Fig 15. Typical Avalanche Current Vs. Pulse width

Fig 16. Maximum Avalanche Energy Vs. Temperature
Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

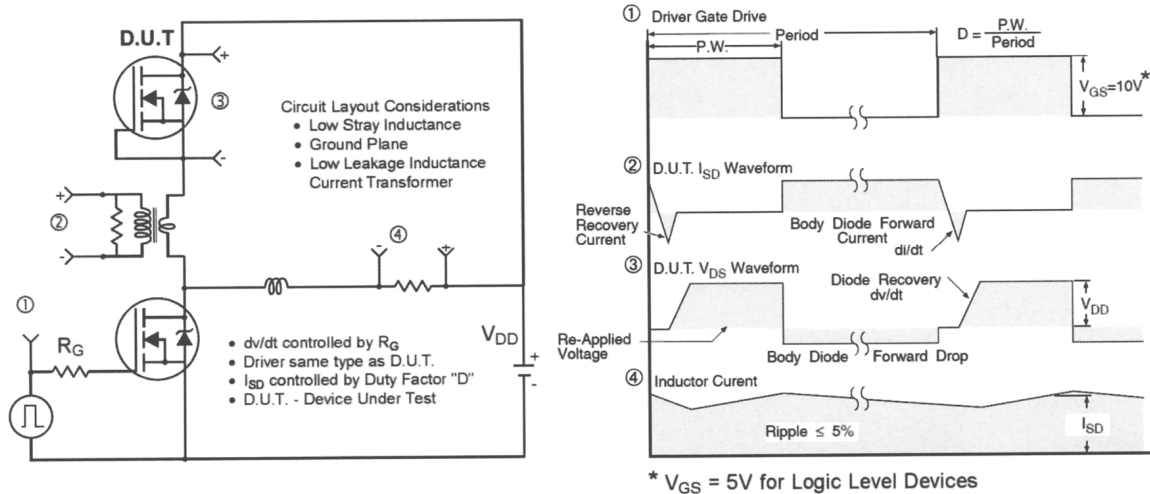


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



Fig 18a. Switching Time Test Circuit



Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

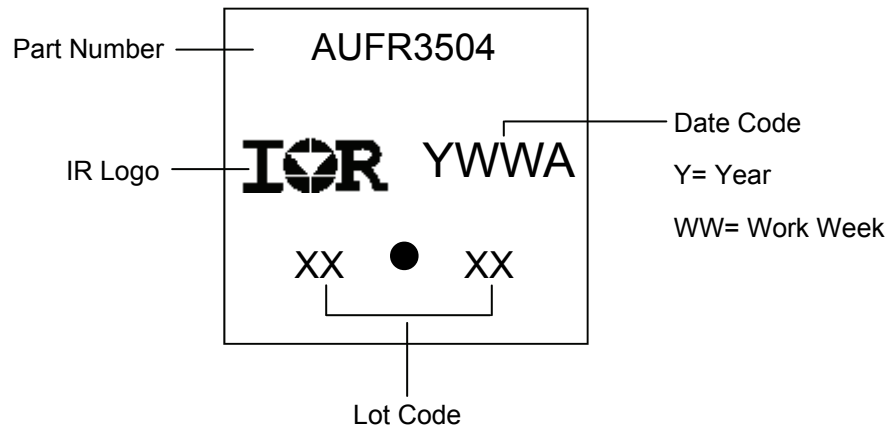
| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|-----------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | |
| A1 | - | 0.13 | - | .005 | |
| b | 0.64 | 0.89 | .025 | .035 | |
| b1 | 0.65 | 0.79 | .025 | .031 | 7 |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 4.95 | 5.46 | .195 | .215 | 4 |
| c | 0.46 | 0.61 | .018 | .024 | |
| c1 | 0.41 | 0.56 | .016 | .022 | 7 |
| c2 | 0.46 | 0.89 | .018 | .035 | |
| D | 5.97 | 6.22 | .235 | .245 | 6 |
| D1 | 5.21 | - | .205 | - | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 6 |
| E1 | 4.32 | - | .170 | - | 4 |
| e | 2.29 BSC | | .090 BSC | | |
| H | 9.40 | 10.41 | .370 | .410 | |
| L | 1.40 | 1.78 | .055 | .070 | |
| L1 | 2.74 BSC | | .108 REF. | | |
| L2 | 0.51 BSC | | .020 BSC | | |
| L3 | 0.89 | 1.27 | .035 | .050 | 4 |
| L4 | - | 1.02 | - | .040 | |
| L5 | 1.14 | 1.52 | .045 | .060 | 3 |
| φ | 0" | 10" | 0" | 10" | |
| φ1 | 0" | 15" | 0" | 15" | |
| φ2 | 25" | 35" | 25" | 35" | |

LEAD ASSIGNMENTS
HEXFET

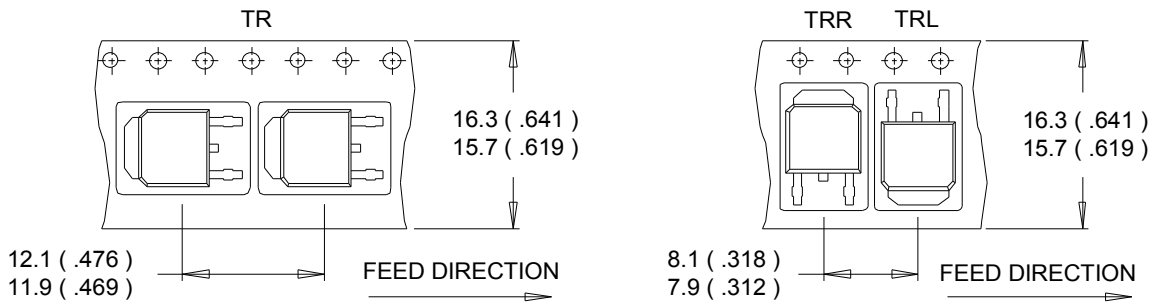
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- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

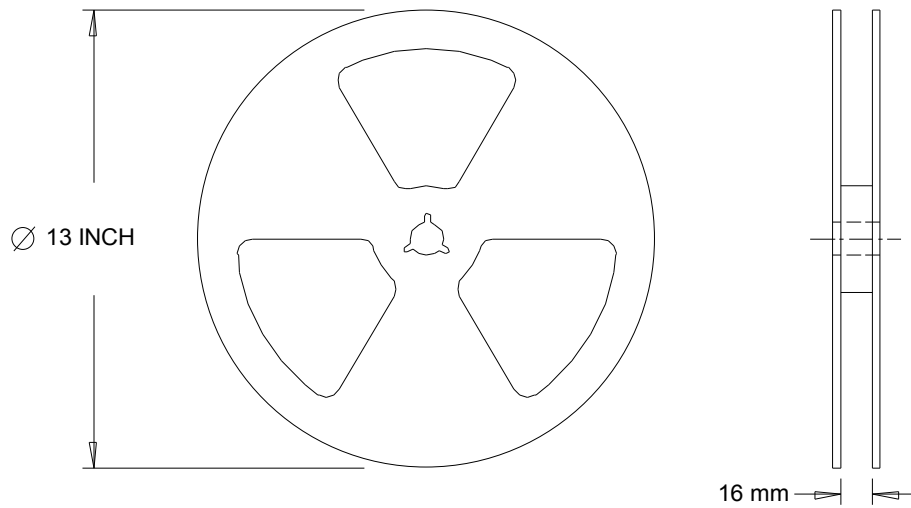
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))

NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information

| | | | |
|-----------------------------------|----------------------|---|------|
| Qualification Level | | Automotive (per AEC-Q101) | |
| | | Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| Moisture Sensitivity Level | | D-Pak | MSL1 |
| ESD | Machine Model | Class M4 (+/- 500V) [†] AEC-Q101-002 | |
| | Human Body Model | Class H1C (+/- 1500V) [†] AEC-Q101-001 | |
| | Charged Device Model | Class C5 (+/- 2000V) [†] AEC-Q101-005 | |
| RoHS Compliant | | Yes | |

† Highest passing voltage.

Revision History

| Date | Comments |
|------------|--|
| 11/23/2015 | <ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1. |

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[IRLR3915TRPBF](#) [IRLU3915PBF](#)