LM3262 6-MHz, 800-mA Miniature, Adjustable, Step-Down DC-DC Converter With Auto Bypass for RF Power Amplifiers

1 Features

- Operates from a Single Li-Ion Cell (2.5 V to 5.5 V)
- 6-MHz (Typical) PWM Switching Frequency
- Adjustable Output Voltage (0.4 V to 3.6 V)
- 800-mA Maximum Load Capability (up to 1 A in Bypass Mode)
- High Efficiency (93% Typical at 3.8 V_{IN}, 3.4 V_{OUT} at 500 mA)
- Automatic ECO/PWM/BP Mode Change
- Current and Thermal Overload Protection
- Multi-Function VCON Pin (Eliminates Need for Separate BPEN Control)
- Soft-Start Function
- Small Chip Inductor in 0805 (2012) Case Size
- 25-µA (Typical) I_Q in Sleep Mode
- 5-µs (Typical) Rise Time and Fall Time for 2-V Step
- 9-Pin DSBGA Package

2 Applications

- HSUPA, LTE Cellular Phones
- TD-SCDMA and TD-LTE
- Hand-Held Radios
- RF PC Cards
- Battery-Powered RF Devices
- USB-Powered Portable Applications

3 Description

The LM3262 is a DC-DC converter optimized for powering RF power amplifiers (PAs) from a single lithium-ion cell; however, it may be used in many other applications such as USB-powered portable applications. The device 2.5-V to 5.5-V input voltage can be stepped down to an adjustable output voltage range from 0.4 V to 3.6 V. Output voltage is set using a VCON analog input which enables improved RF-stage PA efficiencies.

The LM3262 offers five modes of operation. In pulse width modulation (PWM) mode the device operates at a fixed frequency of 6 MHz (typical), which minimizes RF interference at medium-to-low loads. At light load, the device enters into ECO mode automatically and operates with reduced switching frequency. In ECO mode, the quiescent current is reduced and extends the battery life. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typical). At low-battery condition, bypass mode reduces the voltage dropout to less than 50 mV (typical). The device also features a sleep mode.

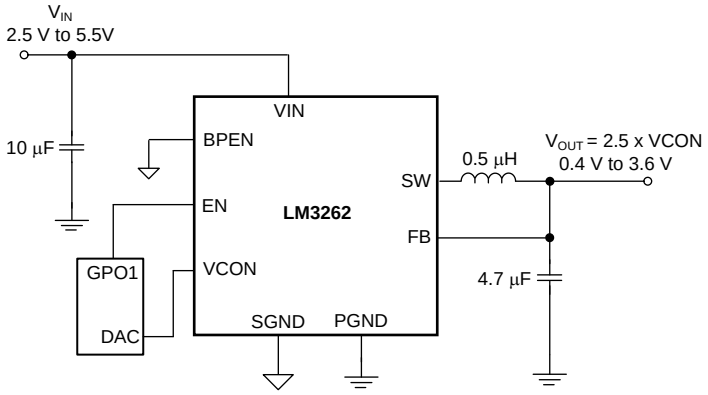
The LM3262 is available in a 9-pin, lead-free DSBGA package. A high-switching frequency (6 MHz) allows use of only three tiny surface-mount components: one inductor and two ceramic capacitors.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3262	DSGBA (9)	1.51 mm × 1.385 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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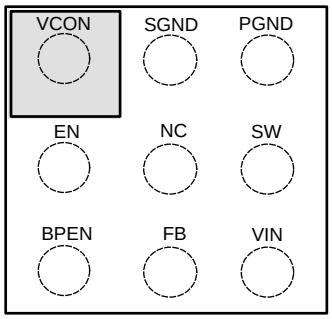
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

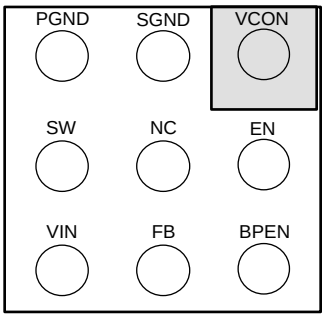
Changes from Revision N (March 2013) to Revision O	Page
• Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1

5 Pin Configuration and Functions

YFQ Package
9-Pin DSBGA
Top View



YFQ Package
9-Pin DSBGA
Bottom View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	VCON	Analog	Voltage control analog input. VCON controls V_{OUT} in PWM and ECO modes. VCON may also be used to force the device into sleep mode by setting VCON < 80 mV or into bypass condition by setting VCON > 1.5 V.
A2	SGND	Ground	Signal ground for analog and control circuitry.
A3	PGND	Ground	Power ground for the Power MOSFETs and gate drive circuitry
B1	EN	Digital/Input	Enable Input. Set this digital input high for normal operation. For shutdown, set low. Do not leave EN pin floating.
B2	NC	—	Do not connect to PGND directly — Internally connected to SGND.
B3	SW	Analog	Switching node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum switch peak current limit specification of the LM3262.
C1	BPEN	Input	Bypass enable input. Set this digital input high to force bypass operation. For normal operation with automatic bypass, set low or connect to ground. Do not leave this pin floating.
C2	FB	Analog	Feedback analog input and bypass FET output. Connect to the output at the output filter capacitor.
C3	VIN	Input	Voltage supply input for SMPS converter.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VIN to SGND	−0.2	6	V
PGND to SGND	−0.2	0.2	V
EN, VCON, BPEN	(SGND − 0.2)	(V_{IN} + 0.2)	V
FB, SW	(PGND − 0.2)	(V_{IN} + 0.2)	V
Continuous power dissipation(3)	Internally limited		
Junction temperature, T_{J-MAX}		150	°C
Maximum lead temperature (soldering, 10 sec)		260	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 130°C (typical).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage, V_{IN}		2.5	5.5	V
Recommended load current	PWM mode	0	800	mA
	Bypass mode	0	1000	mA
Junction temperature, T_J		–30	125	°C
Ambient temperature, T_A(2)		−30	90	°C

(1) All voltages are with respect to the potential at the GND pins
(2) In applications where high-power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LM3262 YFQ (DSBGA) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, all specifications apply to the *Typical Application Circuit* with: V_{IN} = EN = 3.6 V and BPEN = NC = 0 V. All typical (TYP) limits apply for $T_A = T_J$ = 25°C, and all minimum (MIN) and maximum (MAX) apply over the full operating ambient temperature range (−30°C ≤ $T_A = T_J$ ≤ +90°C), unless otherwise specified.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FB,\ MIN}$	Feedback voltage at minimum setting	PWM mode, VCON = 0.16 V(4)	0.38	0.4	0.42	V
$V_{FB,\ MAX}$	Feedback voltage at maximum setting	PWM mode, VCON = 1.44 V, V_{IN} = 4 V	3.55	3.6	3.65	V
I_{SHDN}	Shutdown supply current	EN = SW = VCON = FB = BPEN = NC =0 V(5)		0.1	1	µA
I_{Q_PWM}	PWM mode quiescent current	PWM mode, No switching VCON = 0.13 V, FB = 1 V(6)		650	795	µA
I_{Q_SLEEP}	Low-power sleep mode	EN = VIN, BPEN = NC = 0V, SW = tri state VCON < 0.8 V, FB = 2.05 V(7)		25		µA
I_{Q_ECO}	ECO mode quiescent current	ECO mode, No switching VCON = 0.8 V, FB = 2.05 V(6)		60		µA
$I_{LIM,P}$	PFET switch peak current limit	See(8)	1300	1450	1600	mA
$I_{LIM,\ BP}$	BPFET switch peak current limit	$V_{FB} = V_{IN} – 1$ V	310	400		mA
f_{OSC}	Internal oscillator frequency		5.7	6	6.3	MHz
V_{IH}	EN, BPEN logic high input threshold		1.2			V
V_{IL}	EN, BPEN logic low input threshold				0.4	V
Gain	VCON to V_{OUT} gain	0.16 V ≤ VCON ≤ 1.44 V(9)		2.5		V/V
I_{VCON}	VCON pin leakage current	VCON = 1 V	–1		1	µA
$V_{BP,\ NEG}$	Auto bypass detection negative threshold	VCON = 1.2 V ($V_{OUT\text{-}SET}$ = 3 V) V_{IN} = 3.2 V, R_L = 6 Ω (I_{OUT} = 500 mA)(10)	165	200	235	mV
$V_{BP,\ NEG}$	Auto bypass detection positive threshold	VCON = 1.2 V ($V_{OUT\text{-}SET}$ = 3 V) V_{IN} = 3.25 V, R_L = 6 Ω (I_{OUT} = 500 mA)(11)	215	250	285	mV
$I_{BP,\ SLEW}$		BPEN = High, Forced bypass		1600		mA

(1) All voltages are with respect to the potential at the GND pins.
(2) Minimum and maximum limits are specified by design, test, or statistical analysis.
(3) The parameters in the electrical characteristics table are tested under open loop conditions at V_{IN} = 3.6 V unless otherwise specified. For performance over the input voltage range and closed-loop results, refer to *Typical Characteristics*.
(4) All 0.4-V V_{OUT} specifications are at steady-state only.
(5) Shutdown current includes leakage current of PFET.
(6) I_q specified here is when the device is not switching. For operating input current at no load, refer to *Typical Characteristics*.
(7) FB has 200 kΩ to SGND.
(8) Current limit is built-in, fixed, and not adjustable.
(9) Care should be taken to keep the VCON pin voltage less than the VIN pin voltage as this can place the device into a manufacturing test mode.
(10) Entering bypass mode, V_{IN} is compared to the programmed output voltage (2.5 × VCON). When V_{IN} − (2.5 × VCON) falls below $V_{BP,NEG}$ longer than $T_{BP,NEG}$, the bypass FET turns on, and the switching FET turns on.
(11) Bypass mode is exited when V_{IN} − (2.5 × VCON) exceeds $V_{BP,POS}$ longer than $T_{BP,POS}$, and PWM mode resumes. The hysteresis for the bypass detection threshold $V_{BP,POS}$ − $V_{BP,NEG}$ is always positive and is approximately 50 mV.

6.6 System Characteristics

The following parameters are specified by design and verifications providing the component values in the *Typical Application Circuit* are used. *These parameters are not verified by production testing.* Minimum (MIN) and maximum (MAX) values are specified over the ambient temperature range T_A = −30°C ≤ T_A ≤ +90°C and over the V_{IN} range = 2.5 V to 5.5 V, unless otherwise specified; L = 0.5 µH, DCR = 50 mΩ, C_{IN} = 10 µF, 6.3 V, 0402 (1005), C_{OUT} = 4.7 µF, 6.3 V, 0402 (1005). For bench evaluation, see (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D	Maximum duty cycle	MODE = LOW	100%			
I_{OUT}	Maximum output current capability	2.5 V ≤ V_{IN} ≤ 5.5 V 2.5 × VCON ≤ V_{IN} – 285 mV	800			mA
		2.5 V ≤ V_{IN} ≤ 5.5 V 2.5 × VCON ≤ V_{IN} – 165 mV, bypass mode	1000			
V_{OUT} linearity	VCON = 0.16 V to 1.44 V	0 mA ≤ I_{OUT} ≤ 800 mA (2)	–3%		3%	
			–50		50	mV
η	Efficiency	V_{IN} = 3.8 V, V_{OUT} = 0.8 V I_{OUT} = 10 mA, ECO mode		71%		
		V_{IN} = 3.8 V, V_{OUT} = 2.5 V I_{OUT} = 200 mA, PWM mode		92%		
		V_{IN} = 3.8 V, V_{OUT} = 3.4 V I_{OUT} = 500 mA, PWM mode		93%		
LINE_tr	Line transient response	V_{IN} = 3.6 V to 4.2 V, T_R = T_F = 10 µs, I_{OUT} = 100 mA, V_{OUT} = 0.8 V		50		mVpk
LOAD_tr	Load transient response	V_{IN} = 3.1/3.6/4.5 V, V_{OUT} = 0.8 V I_{OUT} = 50 mA to 150 mA T_R = T_F = 10 µs,		50		mVpk

(1) When the LM3262 device is being evaluated apart from a normal system design or on a PCB other than the TI LM3262 evaluation module, user should ensure that a 50-µF to 100-µF ceramic input capacitor is added to the PCB to keep input voltage from sagging during rapid load transitions.
(2) Linearity limits are ±3% or ±50 mV, whichever is larger. V_{OUT} is monotonic in nature with respect to VCON input.

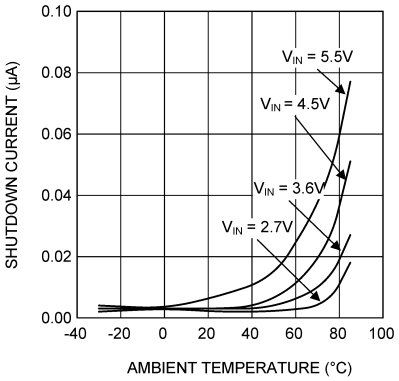
6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
T_{VCON_TR}	V_{OUT} rise time VCON change to 90%; V_{IN} = 3.7 V, V_{OUT} = 1.4 V to 3.4 V 0.1 µs < VCON_T_R < 1 µs, RL = 12 Ω		5		µs
	V_{OUT} fall time VCON change to 10%; V_{IN} = 3.7 V, V_{OUT} = 3.4 V to 1.4 V 0.1 µs < VCON_T_R < 1 µs, RL = 12 Ω		5		µs
T_{ON}	Turnon time (time for output to reach 95% final value after Enable low-to-high transition) EN = low-to-high, V_{IN} = 4.2 V , V_{OUT} = 3.4 V I_{OUT} ≤ 1 mA, COUT = 4.7 µF			50	µs
$T_{BP, NEG}$	Auto bypass detect negative threshold delay time (1)		10		µs
$T_{BP, POS}$	Auto bypass detect positive threshold delay time (2)		0.1		µs

(1) Entering bypass mode, V_{IN} is compared to the programmed output voltage (2.5 × VCON). When V_{IN} − (2.5 × VCON) falls below $V_{BP, NEG}$ longer than $T_{BP, NEG}$, the bypass FET turns on, and the switching FET turns on.
(2) Bypass mode is exited when V_{IN} − (2.5 × VCON) exceeds $V_{BP, POS}$ longer than $T_{BP, POS}$, and PWM mode resumes. The hysteresis for the bypass detection threshold $V_{BP, POS}$ − $V_{BP, NEG}$ is always positive and will be approximately 50 mV.

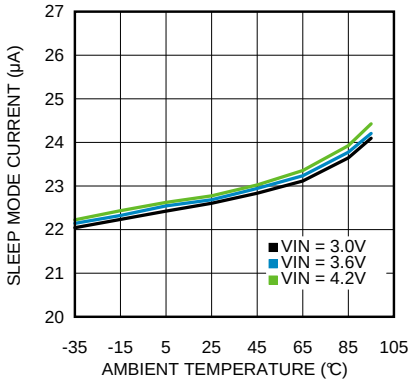
6.8 Typical Characteristics

V_{IN} = EN = 3.6 V, L = 0.5 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF and T_A = 25°C, unless otherwise noted.



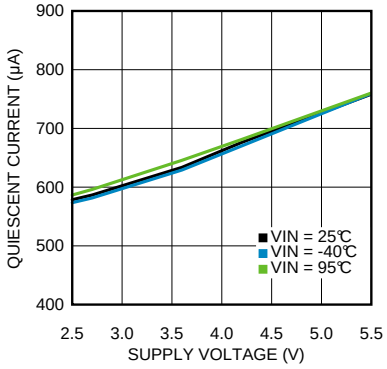
SW = VCON = EN = BPEN = 0V

Figure 1. Shutdown Current vs Temperature



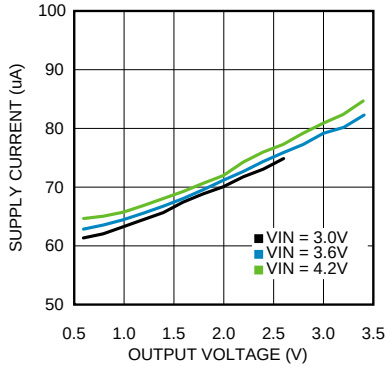
VCON < 80 mV EN = V_{IN} BPEN = 0

Figure 2. Sleep Mode Current vs Temperature



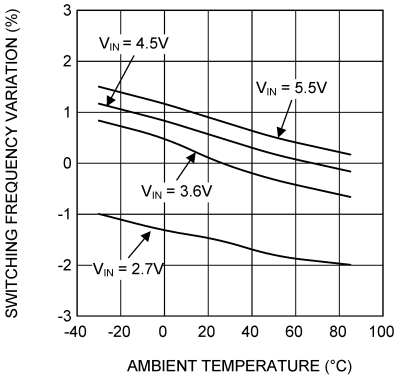
No Switching FB = 1 V VCON = 0.13 V

Figure 3. Quiescent Current vs Supply Voltage



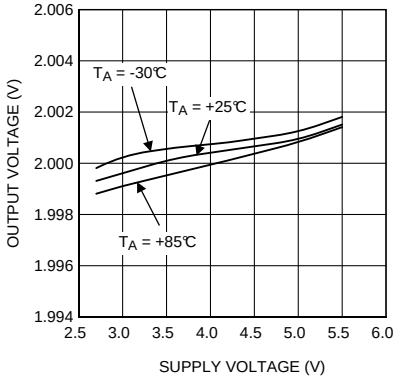
Closed Loop Switching No load

Figure 4. ECO Mode Supply Current vs Output Voltage



V_{OUT} = 2 V I_{OUT} = 200 mA

Figure 5. Switching Frequency vs Temperature

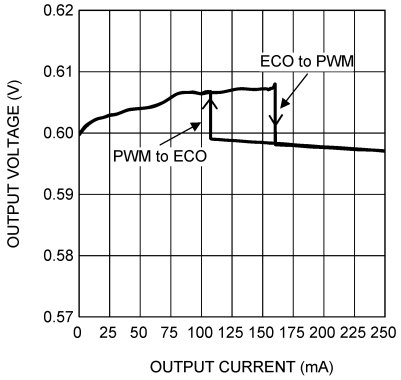


V_{OUT} = 2 V R_{LOAD} = 10 Ω

Figure 6. Output Voltage vs Supply Voltage

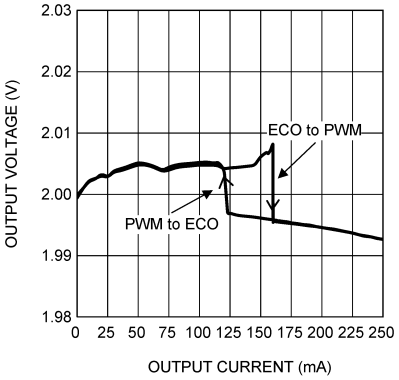
Typical Characteristics (continued)

V_{IN} = EN = 3.6 V, L = 0.5 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF and T_A = 25°C, unless otherwise noted.



V_{IN} = 3.8 V V_{OUT} = 0.6 V

Figure 7. Output Voltage vs Output Current



V_{IN} = 3.8 V V_{OUT} = 2 V

Figure 8. Output Voltage vs Output Current

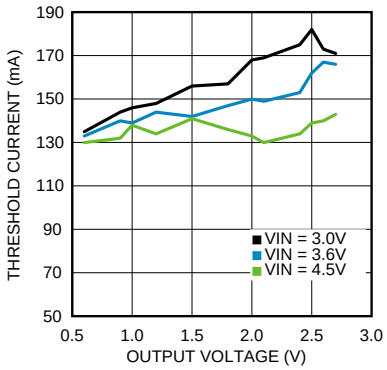


Figure 9. ECO-PWM Mode Threshold Current vs Output Voltage

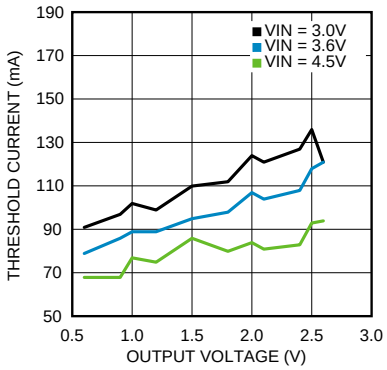


Figure 10. PWM-ECO Mode Threshold Current vs Output Voltage

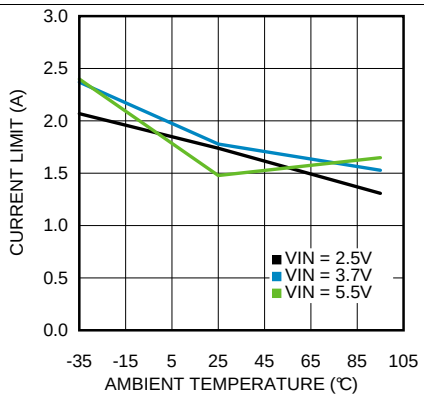


Figure 11. Closed-Loop Current Limit vs Temperature

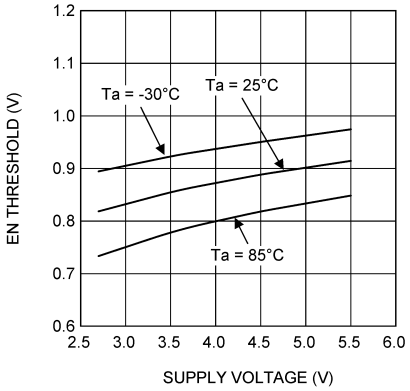
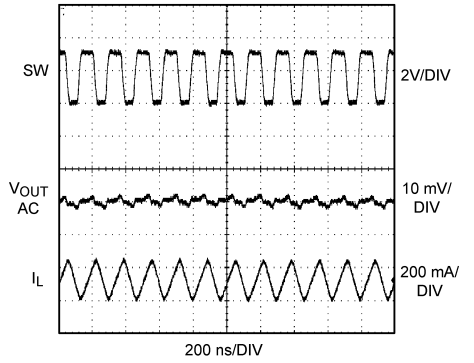


Figure 12. EN High Threshold vs Supply Voltage

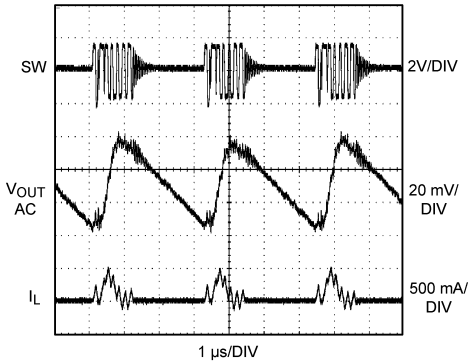
Typical Characteristics (continued)

V_{IN} = EN = 3.6 V, L = 0.5 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF and T_A = 25°C, unless otherwise noted.



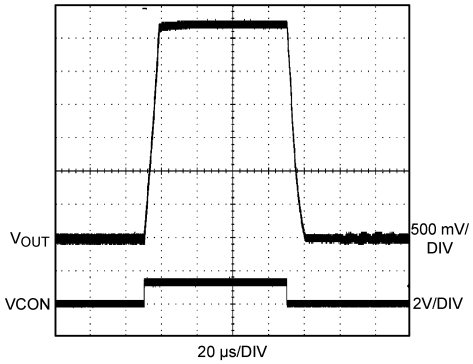
V_{IN} = 3.6 V V_{OUT} = 2 V I_{OUT} = 200 mA

Figure 13. Output Voltage Ripple in PWM Mode



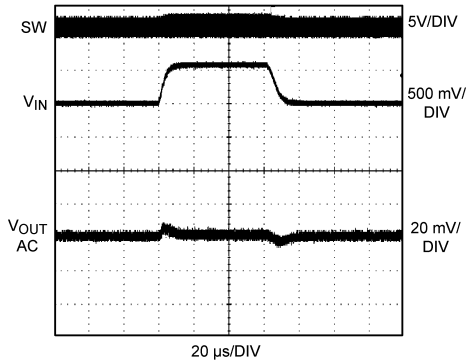
V_{OUT} = 2 V I_{OUT} = 50 mA

Figure 14. Output Voltage Ripple in ECO Mode



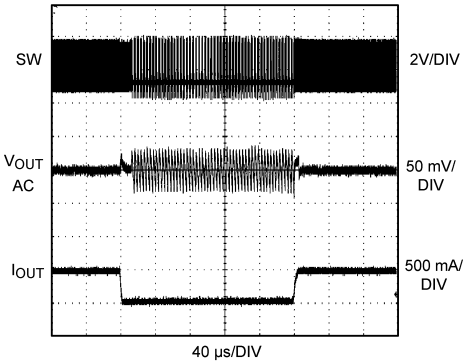
V_{IN} = 4 V V_{OUT} = 0.4 V to 3.6 V R_{LOAD} = 10 Ω

Figure 15. VCON Transient Response



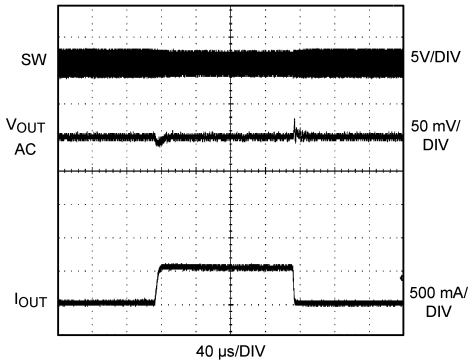
V_{IN} = 3.6 V to 4.2 V V_{OUT} = 0.6 V I_{OUT} = 750 mA

Figure 16. Line Transient Response



V_{IN} = 3.6 V V_{OUT} = 0.5 V I_{OUT} = 500 mA to 60 mA

Figure 17. Load Transient Response

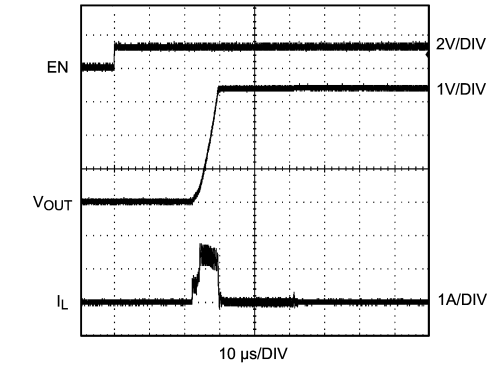


V_{IN} = 4.2 V V_{OUT} = 3.1 V I_{OUT} = 200 mA to 750 mA

Figure 18. Load Transient Response

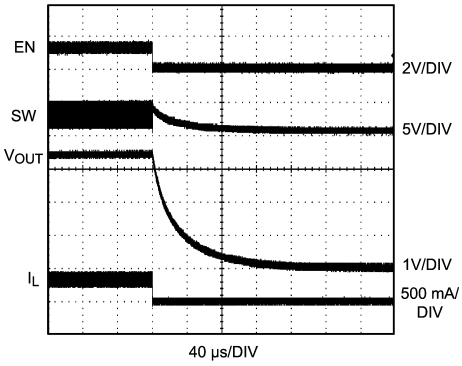
Typical Characteristics (continued)

V_{IN} = EN = 3.6 V, L = 0.5 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF and T_A = 25°C, unless otherwise noted.



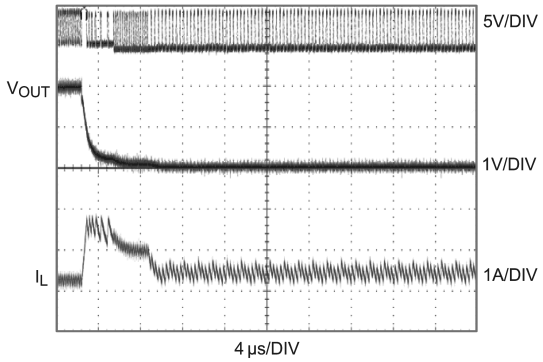
V_{IN} = 4.2 V V_{OUT} = 3.4 V R_{LOAD} = 3.6 kΩ

Figure 19. Start-Up



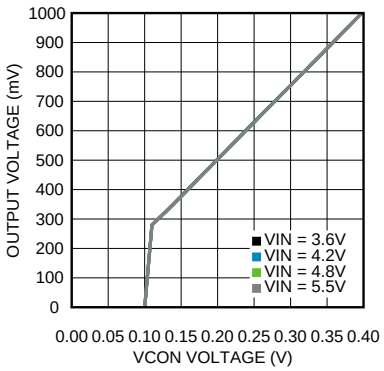
V_{IN} = 4.2 V V_{OUT} = 3.4 V R_{LOAD} = 10 Ω

Figure 20. Shutdown



V_{OUT} = 2 V R_{LOAD} = 10 Ω→ 0 Ω

Figure 21. Timed Current Limit



R_{LOAD} = 10 Ω

Figure 22. Low VCON Voltage vs Output Voltage

7 Detailed Description

7.1 Overview

The LM3262 is a simple, step-down DC-DC converter optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single li-ion battery cell. The device is based on a voltage-mode buck architecture, with synchronous rectification for high efficiency. It is designed for a maximum load capability of 800 mA in PWM mode. Maximum load range may vary from this depending on input voltage, output voltage, and the inductor chosen.

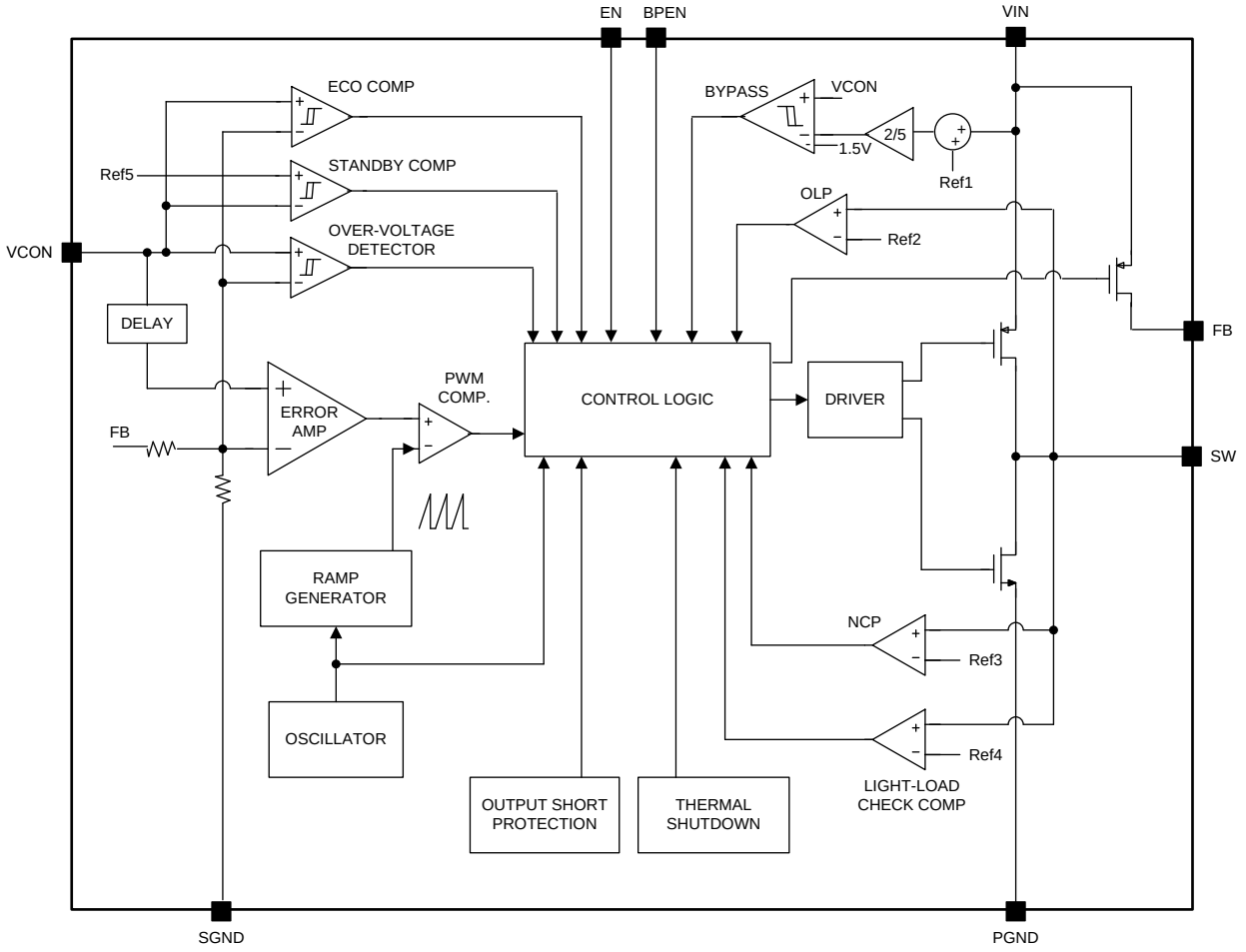
There are five modes of operation depending on the current required: pulse width modulation (PWM), ECOnomy (ECO), bypass (BP), sleep, and shutdown. (See Table 1.) The LM3262 operates in PWM mode at higher load current conditions. Lighter loads cause the device to automatically switch into ECO mode. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typical).

DC PWM mode output voltage precision is ±2% for 3.6 V_{OUT}. Efficiency is approximately 93% (typical) for a 500-mA load with 3.4-V output, 3.8-V input. The output voltage is dynamically programmable from 0.4 V to 3.6 V by adjusting the voltage on the control pin (VCON) without the need for external feedback resistors. This ensures longer battery life by being able to change the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection and thermal overload shutdown.

The LM3262 is constructed using a chip-scale, 9-pin DSBGA package. This package offers the smallest possible size for space-critical applications, such as cell phones, where board area is an important design consideration. Use of a high switching frequency (6 MHz, typical) reduces the size of external components. As shown in the *Typical Application Circuit*, only three external power components are required for implementation. Use of a DSBGA package requires special design considerations for implementation. (See *DSBGA Assembly and Use*.) The fine bump-pitch of the DSBGA package requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller must set EN low during power-up and other low supply voltage conditions. (See *Shutdown Mode*.)

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Circuit Operation

Referring to the *Functional Block Diagram*, the LM3262 operates as follows. During the first part of each switching cycle, the control block in the LM3262 turns on the internal top-side PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around (V_{IN} – V_{OUT}) / L, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the bottom-side NFET synchronous rectifier on. In response, the magnetic field of the inductor collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is high and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

Feature Description (continued)

7.3.2 Internal Synchronous Rectification

While in PWM mode, the LM3262 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

With medium and heavy loads, the NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

7.3.3 Current Limiting

The current limit feature allows the LM3262 to protect itself and external components during overload conditions. In PWM mode, the cycle-by-cycle current limit is a 1450 mA (typical). If an excessive load pulls the output voltage down to less than 0.3 V (typical), the NFET synchronous rectifier is disabled, and the current limit is reduced to 530 mA (typical). Moreover, when the output voltage becomes less than 0.15 V (typical), the switching frequency will decrease to 3 MHz, thereby preventing excess current and thermal stress.

7.3.4 Dynamically Adjustable Output Voltage

The LM3262 features dynamically adjustable output voltage to eliminate the need for external feedback resistors by controlling this voltage using the analog VCON pin. The input impedance of this pin can be approximated by a series 50-KΩ resistor and 10-pF capacitor. The output can be set from 0.4 V to 3.6 V by changing the voltage on the analog VCON pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. See *Setting The Output Voltage* for further details. The LM3262 moves into pulse-skipping mode when duty cycle is over approximately 92% or less than approximately 15%, and the output voltage ripple increases slightly.

7.3.5 Thermal Overload Protection

The LM3262 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

7.3.6 Soft Start

The LM3262 has a soft-start circuit that limits in-rush current during start-up. During start-up, the switch current limit is increased in steps. Soft start is activated if EN goes from low to high after V_{IN} reaches 2.5 V.

7.4 Device Functional Modes

7.4.1 PWM Mode Operation

While in PWM mode operation, the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced. While in PWM mode, the output voltage is regulated by switching at a constant frequency, then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current-limit comparator can also turn off the switch if the current limit of the PFET is exceeded — in this case, the NFET switch is turned on, and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

7.4.2 Bypass Mode Operation

The LM3262 contains an internal BPFET switch for bypassing the PWM DC-DC converter during bypass mode. In bypass mode, this BPFET is turned on to power the PA directly from the battery for maximum RF output power. When the device operates in the bypass mode, the output voltage is the input voltage less the voltage drop across the resistance of the BPFET in parallel with the PFET plus switch inductor. Bypass mode is more efficient than operating in PWM mode at 100% duty cycle because the combined resistance is significantly less than the series resistance of the PWM PFET and inductor. This translates into higher voltage available on the output in bypass mode, for a given battery voltage. The device can be forced into bypass mode by setting the BPEN pin high or by driving the VCON control pin voltage higher than 1.5 V. This is called forced bypass mode, and it remains in bypass mode until the BPEN pin goes low or VCON pin drops below 1.5 V. Alternatively, the device can go into bypass mode automatically. This is called auto-bypass mode or automatic bypass mode. The bypass switch turns on when the difference between the input voltage and programmed output voltage is less than 200 mV (typical) for longer than 10 µs (typical). The bypass switch turns off when the input voltage is higher than the programmed output voltage by 250 mV (typical) for longer than 0.1 µs (typical). This method is very system resource friendly in that the bypass PFET is turned on automatically when the input voltage gets close to the output voltage, a typical scenario of a discharging battery. It is also turned off automatically when the input voltage rises, a typical scenario when connecting a charger. When the device is in SLEEP mode (VCON < 80 mV), BPEN is *don't care*.

7.4.3 ECO Mode Operation

At very light loads (50 mA to 100 mA), the LM3262 enters ECO mode operation with reduced switching frequency and supply current to maintain high efficiency. During ECO mode operation, the LM3262 positions the output voltage slightly higher (7 mV typical) than the normal output voltage during PWM mode operation, allowing additional headroom for voltage drop during a load transient from light-to-heavy load.

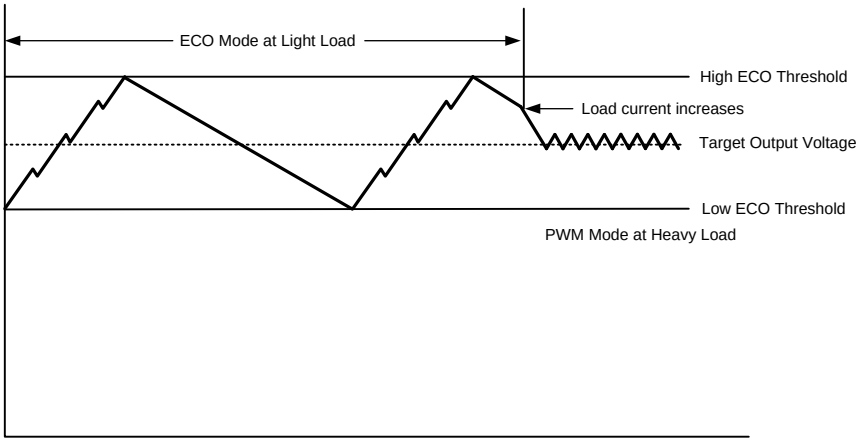


Figure 23. Operation in ECO Mode and Transfer to PWM Mode

Device Functional Modes (continued)

7.4.4 Sleep Mode Operation

When VCON is less than 80 mV in 7 µs, the LM3262 goes into sleep mode — the SW pin is in tri-state (floating), which operates like ECO mode with no switching. The LM3262 device returns to normal operation immediately when VCON ≥ 130 mV in PWM mode or ECO mode, depending on load detection.

7.4.5 Shutdown Mode

Setting the EN digital pin low (< 0.4 V) places the LM3262 in shutdown mode (0.1 µA typical). During shutdown, the PFET switch, the NFET synchronous rectifier, reference voltage source, control, and bias circuitry of the LM3262 are turned off. Setting EN high (> 1.2 V) enables normal operation. EN must be set low to turn off the LM3262 during power-up and undervoltage conditions when the power supply is less than the 2.5-V minimum operating voltage. The LM3262 has an undervoltage lockout (UVLO) comparator to turn the power device off in the case the input voltage or battery voltage is too low. The typical UVLO threshold is approximately 2 V for lock and 2.1 V for release.

Table 1. Description Of Modes(1)

MODE	EN	BPEN	VCON	I_{OUT} (APPROX.)	FB RES
Shutdown	0	X	X	X	Open
Sleep	1	X	< 80 mV	X	Open
PWM	1	0	> 130 mV < (V_{IN} − 0.2)/2.5	> 180 mA	Closed
ECO	1	0		< 140 mA	Closed
Auto bypass	1	0	> (V_{IN} − 0.2)/2.5	X	Closed
Forced bypass	1	1	> 130 mV	X	Closed
	1	0	> 1.5 V	X	Closed

(1) X = Don't care.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3262 DC-DC converter steps down an input voltage from 2.5 V to 5.5 V to a dynamically adjustable output voltage of 0.4 V to 3.6 V.

8.2 Typical Application

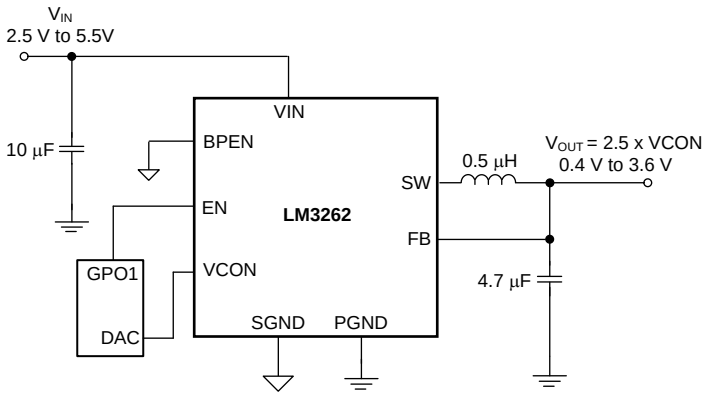


Figure 24. LM3262 Typical Application

8.2.1 Design Requirements

For the typical LM3262 buck regulator, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 5.5 V
Output voltage	0.4 V to 3.6 V
Output current	800 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

There are two main considerations when choosing an inductor: the inductor must not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings over the ambient temperature of application should be requested from manufacturer.

The minimum value of inductance to ensure good performance is 0.3 µH at bias current (I_{LIM} (typical)) over the ambient temperature range. Shielded inductors radiate less noise and are preferred. There are two methods to choose the inductor saturation current rating.

8.2.2.1.1 Method 1

The saturation current must be greater than the sum of the maximum load current and the worst-case average-to-peak inductor current. This is shown in Equation 1 :

$$I_{SAT} > I_{OUT\_MAX} + I_{RIPPLE}$$

where

$$I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right)$$

where

- I_{RIPPLE}: average-to-peak inductor current
- I_{OUT_MAX}: maximum load current (800 mA)
- V_{IN}: maximum input voltage in application
- L: minimum inductor value including worst-case tolerances (30% drop can be considered for Method 1)
- F: minimum switching frequency (5.7 MHz)
- V_{OUT}: output voltage (1)

8.2.2.1.2 Method 2

A more conservative and recommended approach is to choose an inductor than can handle the maximum current limit of 1600 mA.

The resistance of the inductor must be less than 0.1 Ω for good efficiency. Table 3 lists suggested inductors and suppliers.

Table 3. Suggested Inductors

MODEL	SIZE (W × L × H) (mm)	VENDOR
LQM21PNR50XGHL11	2 × 1.25 × 1	Murata
MIPSZ2012D0R5	2 × 1.2 × 1	FDK
LQM21PNR54MG0	2 × 1.25 × 0.9	Murata
LQM2MPNR47NG0	2 × 1.6 × 0.9	Murata
CIG21LR47M	2 × 1.25 × 1	Samsung
CKP2012NR47M	2 × 1.25 × 1	Taiyo Yuden

8.2.2.2 Capacitor Selection

The LM3262 is designed for use with ceramic capacitors for its input and output filters. Use a 10-µF ceramic capacitor for input and a sum total of 4.7-µF ceramic capacitance for the output. They should maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitors types such as X5R, X7R, and B are recommended for both filters. These provide an optimal balance between small size, cost, reliability, and performance for cell phones and similar applications. Table 4 lists some suggested part numbers and suppliers. DC-bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. If it is necessary to choose a 0603 (1608) size capacitor for V_{IN} and 0402 (1005) size capacitor for V_{OUT}, the operation of the LM3262 must be carefully evaluated on the system board. Use of a 2.2-µF capacitor in conjunction with multiple 0.47-µF or 1-µF capacitors in parallel may also be considered when connecting to power amplifier devices that require local decoupling.

Table 4. Suggested Capacitors And Their Suppliers

CAPACITANCE	MODEL	SIZE (W × L) (mm)	VENDOR
2.2 µF	GRM155R60J225M	1 × 0.5	Murata
2.2 µF	C1005X5R0J225M	1 × 0.5	TDK
2.2 µF	CL05A225MQ5NSNC	1 × 0.5	Samsung
4.7 µF	C1608JB0J475M	1.6 × 0.8	TDK
4.7 µF	C1005X5R0J475M	1 × 0.5	TDK
4.7 µF	CL05A475MQ5NRNC	1 × 0.5	Samsung
10 µF	C1608X5R0J106M	1.6 × 0.8	TDK
10 µF	GRM155r60J106M	1 × 0.5	Murata
10 µF	CL05A106MQ5NUNC	1 × 0.5	Samsung

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3262 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions. The equivalent series resistance (ESR) of the filter capacitors is generally a major factor in voltage ripple.

8.2.2.3 Setting The Output Voltage

The LM3262 features a pin-controlled adjustable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.4 V to 3.6 V by setting the voltage on the VCON pin, as in Equation 2:

$$V_{OUT} = 2.5 \times VCON \quad (2)$$

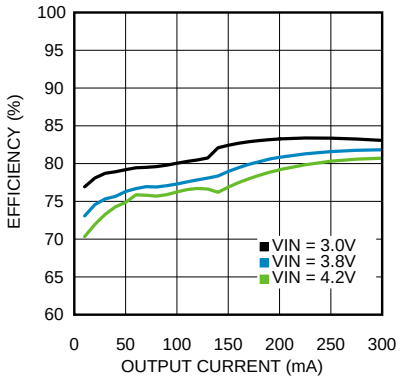
When VCON is between 0.16 V and 1.44 V, the output voltage follows proportionally by 2.5 × VCON.

If VCON is less than 0.16 V (V_{OUT} = 0.4 V), the output voltage may not be well regulated. Refer to Figure 22 for details. This curve exhibits the characteristics of a typical part, and the performance cannot be ensured as there may be a part-to-part variation for output voltages less than 0.4 V. For V_{OUT} lower than 0.4 V, the converter may suffer from larger output ripple voltage and higher current limit operation.

8.2.2.4 FB

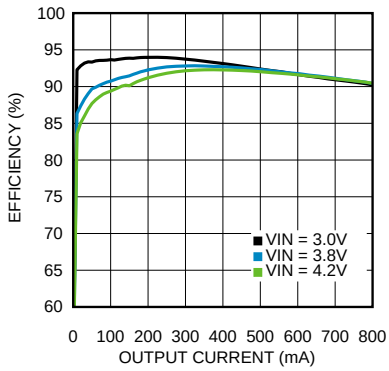
Typically the FB pin is connected to VOUT for regulating the output voltage maximum of 3.6 V. In any application case, the voltage on FB pin should not exceed 4.5 V.

8.2.3 Application Curves



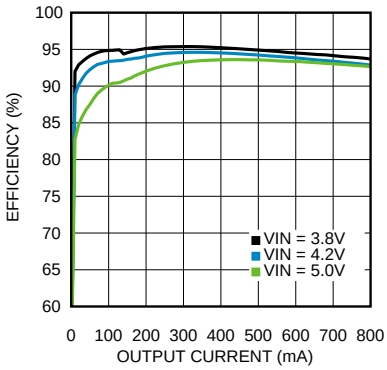
V_{OUT} = 0.8 V

Figure 25. Efficiency vs Output Current



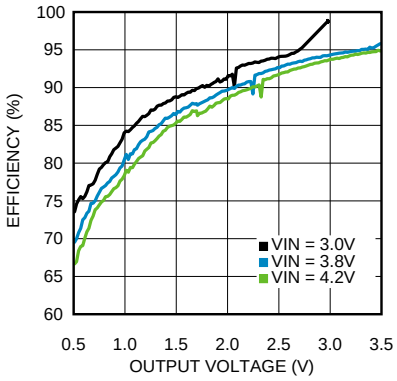
V_{OUT} = 2.5 V

Figure 26. Efficiency vs Output Current



V_{OUT} = 3.4 V

Figure 27. Efficiency vs Output Current



R_L =10 Ω

Figure 28. Efficiency vs Output Voltage

9 Power Supply Recommendations

The LM3262 device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. This input supply should be well-regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition.

10 Layout

10.1 Layout Guidelines

PC board layout is critical to successfully designing a DC-DC converter into a product. As much as a 20-dB improvement in RX noise floor can be achieved by carefully following recommended layout practices. A properly planned board layout optimizes the performance of a DC-DC converter and minimizes effects on surrounding circuitry while also addressing manufacturing issues that can have adverse impacts on board quality and final product yield.

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. Erroneous signals could be sent to the DC-DC converter device, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance of the converter.

10.1.1 Energy Efficiency

Minimize resistive losses by using wide traces between the power components and doubling up traces on multiple layers when possible.

10.1.2 EMI

By its very nature, any switching converter generates electrical noise, and the design challenge is to minimize, contain, or attenuate such switcher-generated noise. A high-frequency switching converter, such as the LM3262, switches Ampere level currents within nanoseconds, and the traces interconnecting the associated components can act as radiating antennas. The following guidelines are offered to help to ensure that EMI is maintained within tolerable levels.

To minimize radiated noise:

- Place the LM3262 switcher, input capacitor, output filter inductor, and output filter capacitor close together, making the interconnecting traces as short as possible.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the internal PFET of the LM3262 and the inductor, to the output filter capacitor, then back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the internal synchronous NFET of the LM3262 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- Make the current loop area(s) as small as possible.

To minimize ground-plane noise:

- Reduce the amount of switching current that circulates through the ground plane — connect the ground bumps of the LM3262 and its input filter capacitor together using generous component-side copper fill as a pseudo-ground plane. Then connect this copper fill to the system ground-plane (if one is used) with multiple vias. These multiple vias help to minimize ground bounce at the LM3262 by giving it a low-impedance ground connection.

To minimize coupling to the voltage feedback trace of the DC-DC converter:

- Route noise sensitive traces, such as the voltage feedback path, as directly as possible from the switcher FB pad to the VOUT pad of the output capacitor, but keep it away from noisy traces between the power components.

To decouple common power supply lines, series impedances may be used to strategically isolate circuits:

- Take advantage of the inherent inductance of circuit traces to reduce coupling among function blocks, by way of the power supply traces.
- Use star connection for separately routing VBATT to PVIN and VBATT_PA.
- Inserting a single ferrite bead in-line with a power supply trace may offer a favorable tradeoff in terms of board area by allowing the use of fewer bypass capacitors.

Layout Guidelines (continued)

10.1.3 Manufacturing Considerations

The LM3262 package employs a 9-pin, 3-mm × 3-mm array of 250 micron solder balls, with a 0.4-mm pad pitch. The following simple design rules go a long way to ensuring a good layout:

- The pad size must be 0.225 ± 0.02 mm, and the solder mask opening must be 0.325 ± 0.02 mm.
- As a thermal relief, connect to each pad with 7-mil wide, 7-mil long traces, incrementally increasing each trace to its optimal width. Symmetry is important to ensure the solder bumps re-flow evenly (refer to *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009)).

10.2 Layout Examples

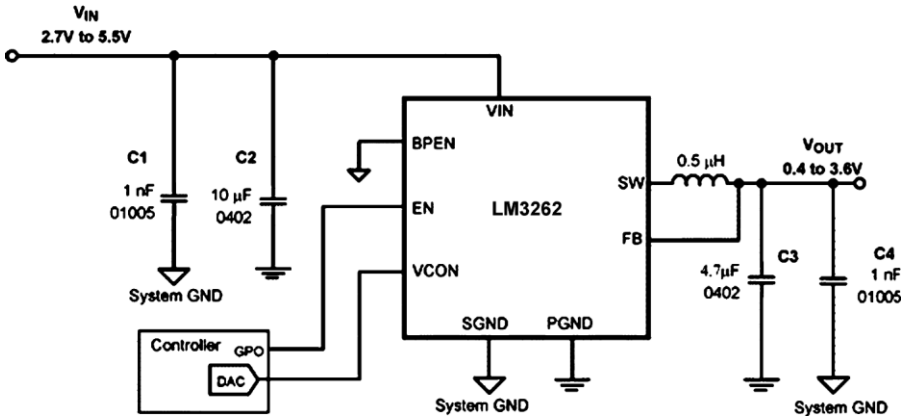


Figure 29. Simplified LM3262 RF Evaluation Board Schematic

1. Bulk Input Capacitor C2 must be placed closer to LM3262 than C1.
2. Add a 1-nF (C1) on input of LM3262 for high frequency filtering.
3. Bulk Output Capacitor C3 must be placed closer to LM3262 than C4.
4. Add a 1-nF (C4) on output of LM3262 for high frequency filtering.
5. Connect both GND terminals of C1 and C4 directly to system GND layer of phone board.
6. Connect bumps SGND (A2), NC (B2), BPEN (C1) directly to System GND.
7. Use 0402 caps for both C2 and C3 due to better high frequency filtering characteristics over 0603 capacitors.
8. TI has seen some improvement in high-frequency filtering for small bypass caps (C1 and C4) when they are connected to System GND instead of same ground as PGND. These capacitors should be 01005 case size for minimum footprint and best high frequency characteristics.

Layout Examples (continued)

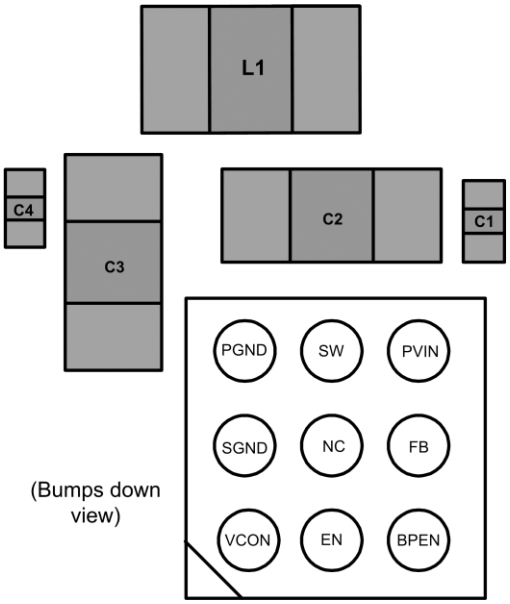


Figure 30. LM3262 Recommended Parts Placement (Top View)

10.2.1 Component Placement

- PVIN
  1. Use a star connection from PVIN to LM3262 and PVIN to PA VBATT connection (V_{CC1}). Do not daisy-chain PVIN connection to LM3262 circuit and then to PA device PVIN connection.
- TOP LAYER
  1. Place a via in LM3262 SGND(A2), BPEN(C1) pads to drop and connect directly to System GND Layer 4.
  2. Place two vias at LM3262 SW solder bump to drop VSW trace to Layer 3.
  3. Connect C2 and C3 capacitor GND pads to PGND bump on LM3262 using a star connection. Place vias in C2 and C3 GND pads that connect directly to System GND Layer 4.
  4. Add 01005/0201 capacitor footprints (C1, C4) to input/output of LM3262 for improved high frequency filtering. C1 and C4 GND pads connect directly to System GND Layer 4.
  5. Place three vias at L1 inductor pad to bring up VSW trace from Layer 3 to Top Layer.
- LAYER 2
  1. Make FB trace at least 10 mils (0.254 mm) wide.
  2. Isolate FB trace away from noisy nodes and connect directly to C3 output capacitor. Place a via in LM3262 SGND (A2), BPEN (C1) pads to drop and connect directly to System GND Layer 4.
- LAYER 3
  1. Make VSW trace at least 15 mils (0.381 mm) wide.
- LAYER 4 (System GND)
  1. Connect C2 and C3 PGND vias to this layer.
  2. Connect C1 and C4 GND vias to this layer.
  3. Connect LM3262 SGND (A2), BPEN (C1), and NC (B2) pad vias to this layer.

Layout Examples (continued)

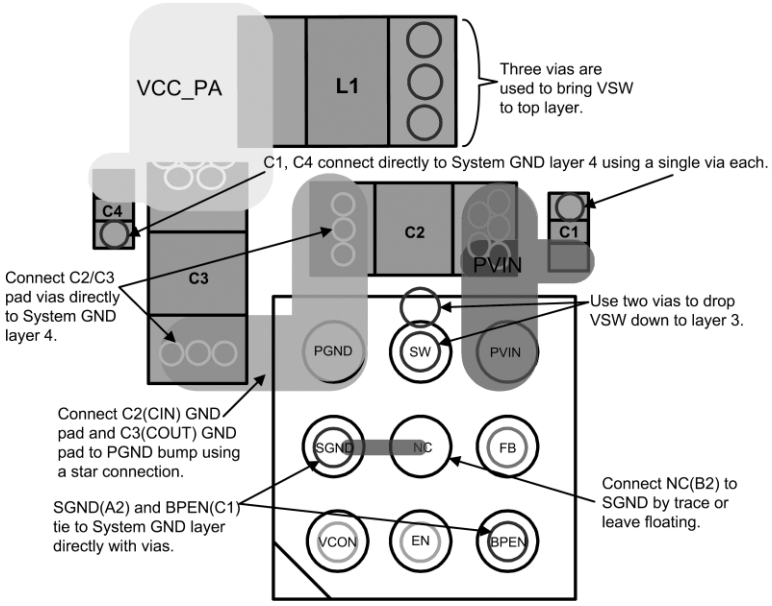


Figure 31. Board Layer 1 — PVIN and PGND Routing

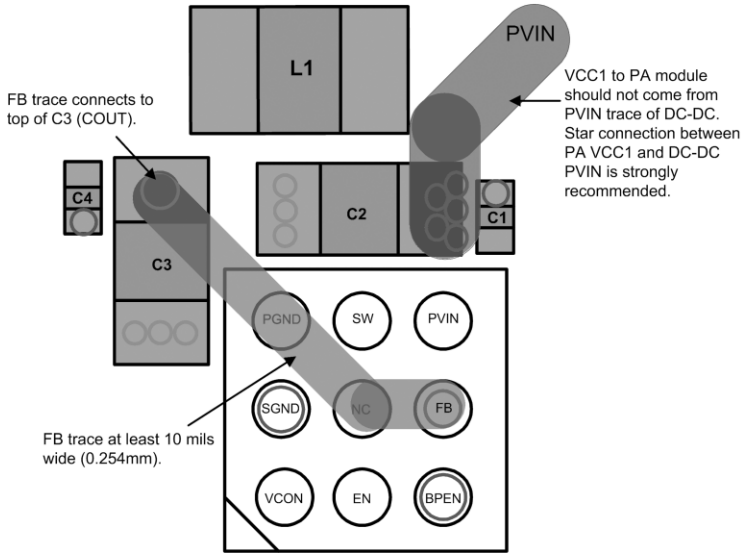


Figure 32. Board Layer 2 — FB and PVIN Routing

Layout Examples (continued)

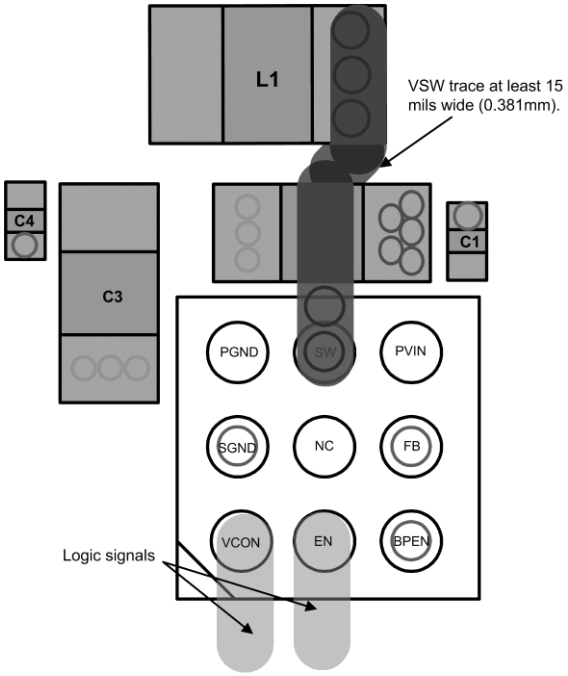


Figure 33. Board Layer 3 — SW, VCON and EN Routing

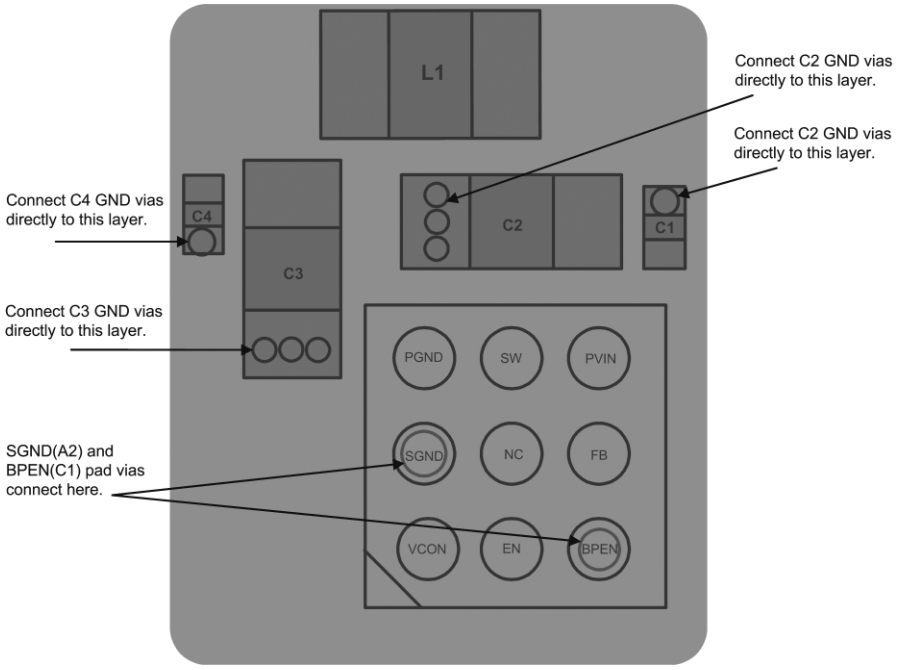


Figure 34. Board Layer 4 — System GND Plane

10.3 DSBGA Assembly and Use

Use of the DSBGA package requires specialized board layout, precision mounting, and careful re-flow techniques, as detailed in *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009). Refer to the section regarding surface mount technology assembly. For best results in assembly, alignment ordinals on the PC board must be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap from holding the device off the surface of the board and interfering with mounting. See SNVA009 for specific instructions on how to do this.

The 9-pin package used for the LM3262 has 250 micron solder balls and requires 0.225-mm pads for mounting on the circuit board. The trace to each pad must enter the pad with a 90° angle to prevent debris from being caught in deep corners. Initially, as a thermal relief, the trace to each pad must be a width of 7 mil for a section approximately 7 mil long. Each trace must neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3262 re-flow evenly, and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A3 and C3. Because VIN and PGND are typically connected to large copper planes, inadequate thermal reliefs can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on exposed die edges of the package.

TI recommends using a 10-nF capacitor between VCON and ground for non-standard ESD events or environments and manufacturing processes to prevent unexpected output voltage drift.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

AN-1112 DSBGA Wafer Level Chip Scale Package (SNVA009)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3262TME/NOPB	ACTIVE	DSBGA	YFQ	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S6	Samples
LM3262TMX/NOPB	ACTIVE	DSBGA	YFQ	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S6	Samples

(1) The marketing status values are defined as follows:
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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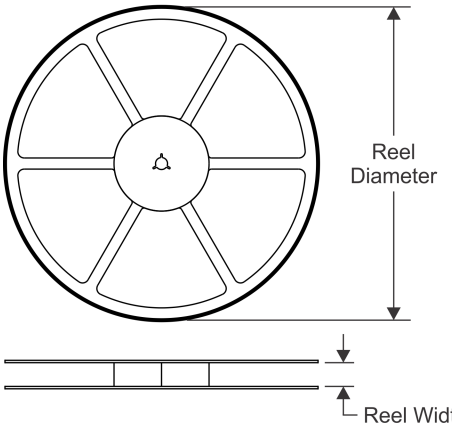
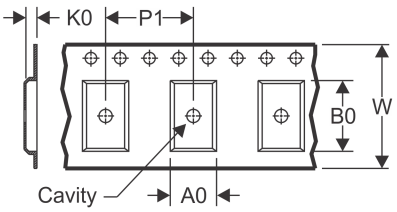
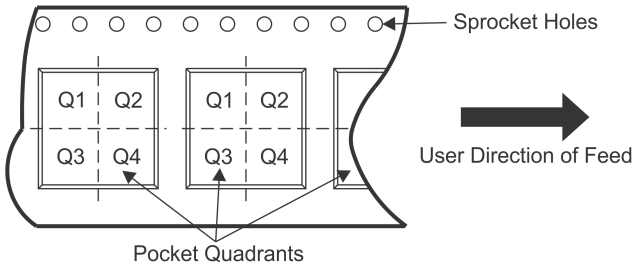


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

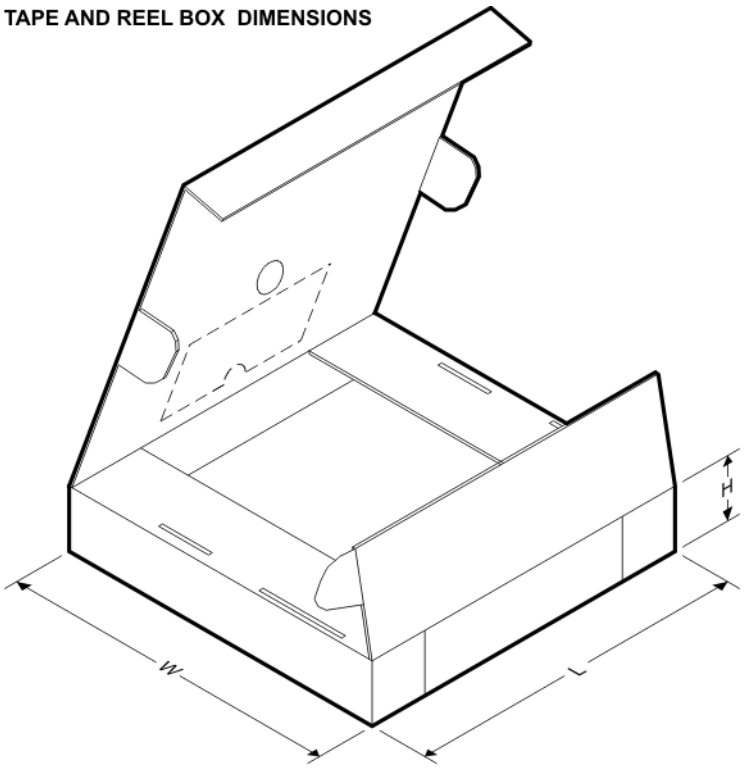
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3262TME/NOPB	DSBGA	YFQ	9	250	178.0	8.4	1.57	1.57	0.76	4.0	8.0	Q1
LM3262TMX/NOPB	DSBGA	YFQ	9	3000	178.0	8.4	1.57	1.57	0.76	4.0	8.0	Q1

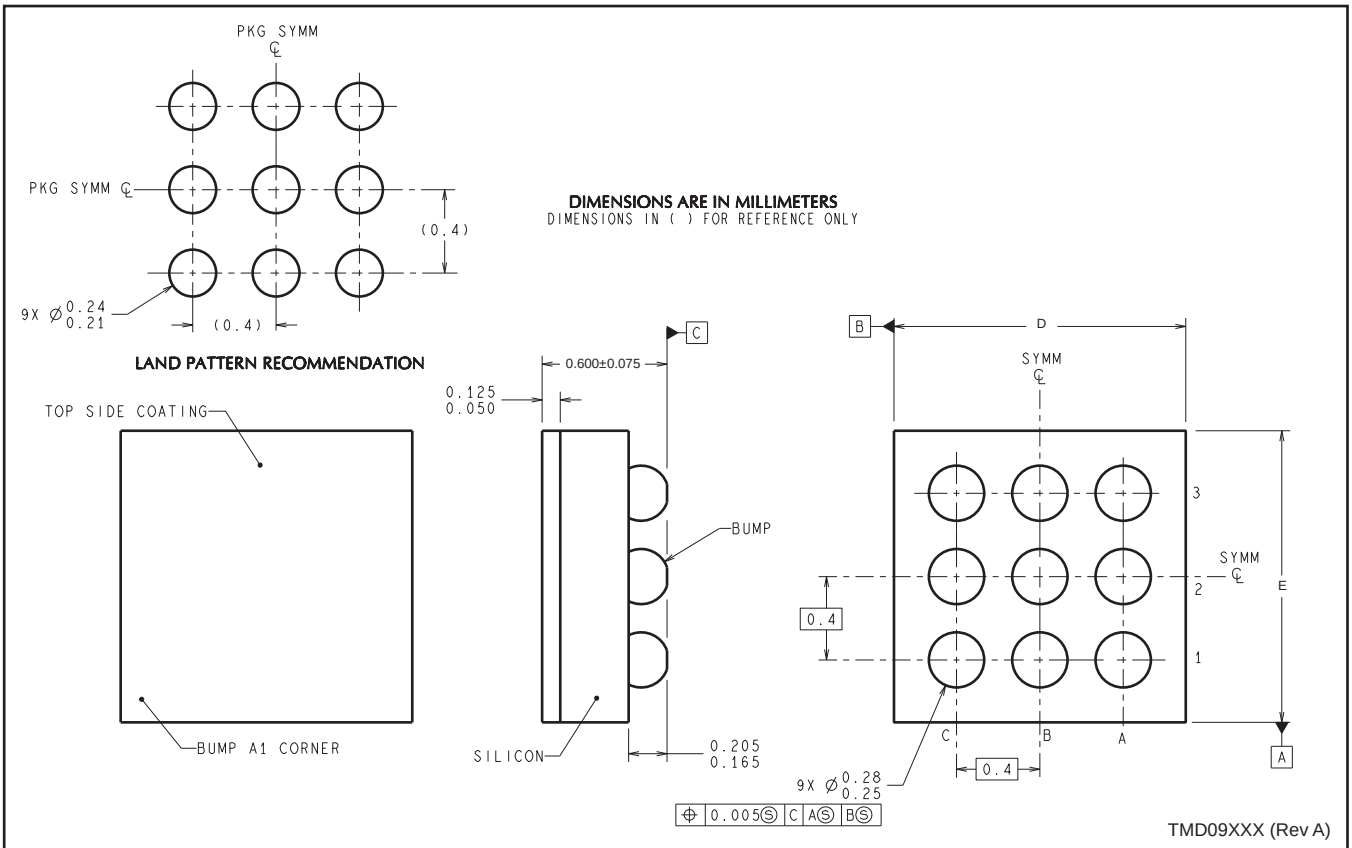
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3262TME/NOPB	DSBGA	YFQ	9	250	210.0	185.0	35.0
LM3262TMX/NOPB	DSBGA	YFQ	9	3000	210.0	185.0	35.0

YFQ0009



D: Max = 1.51 mm, Min = 1.45 mm

E: Max = 1.385 mm, Min =1.325 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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LM3262TMX/NOPB	ACTIVE	DSBGA	YFQ	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S6	Samples

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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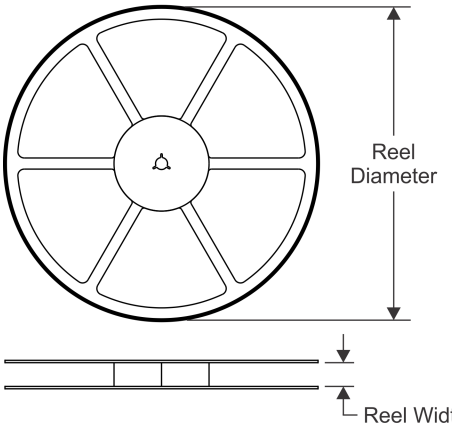
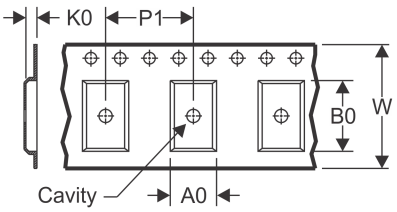


TAPE DIMENSIONS



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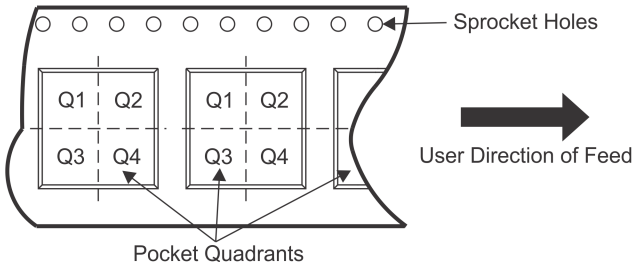

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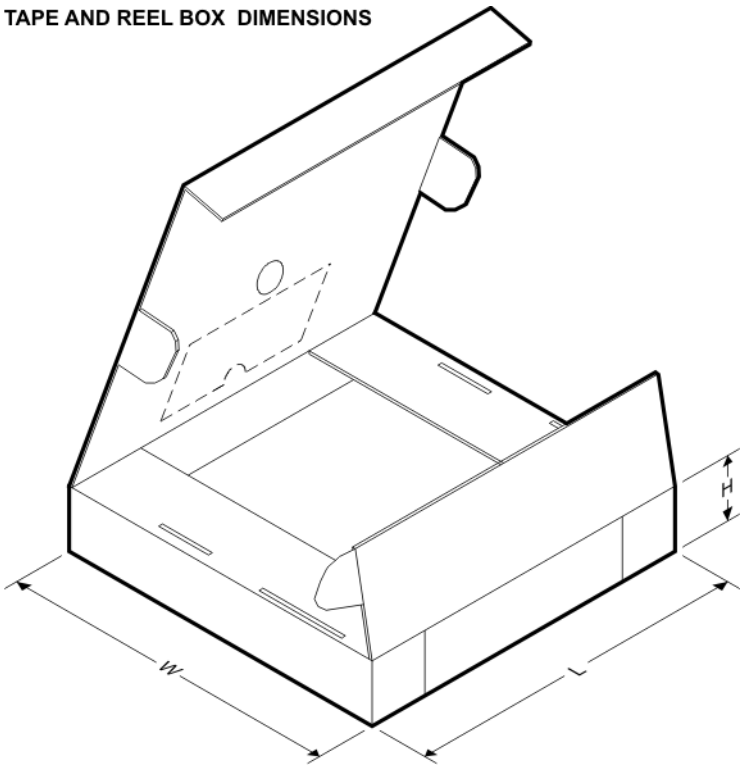
TAPE AND REEL BOX DIMENSIONS



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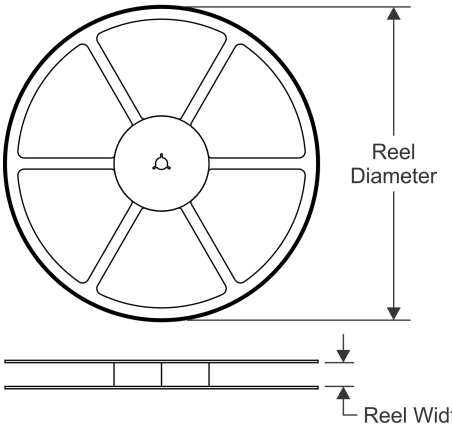
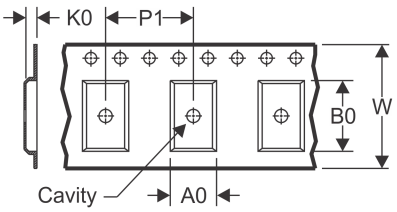


TAPE DIMENSIONS



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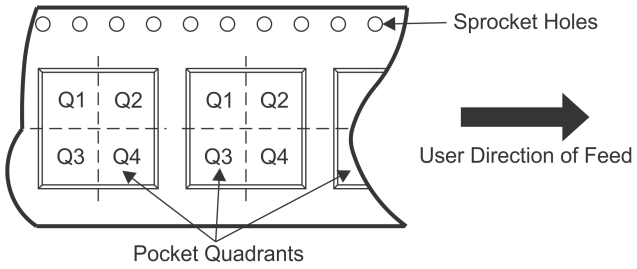

*All dimensions are nominal

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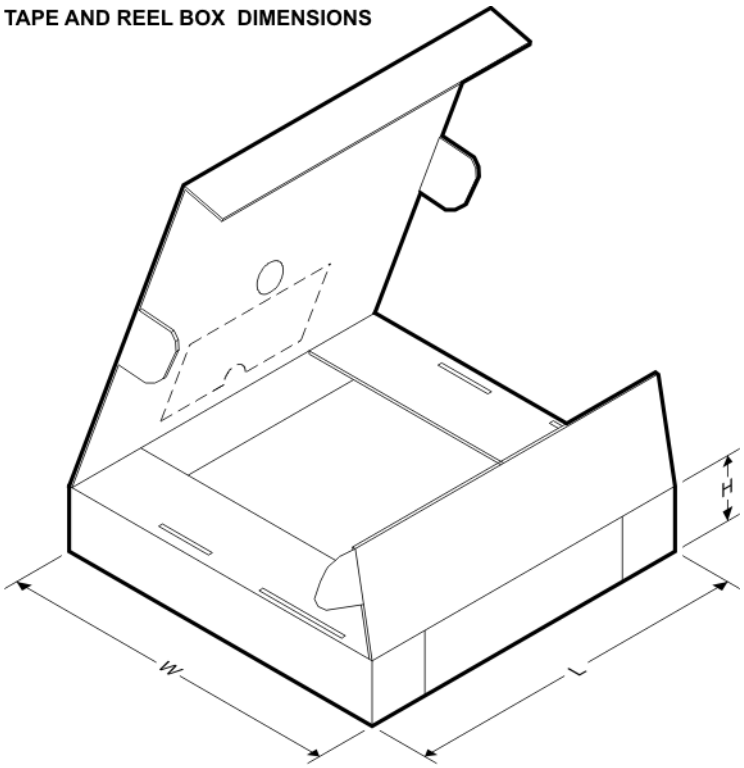
LM3262TMX/NOPB	DSBGA	YFQ	9	3000	178.0	8.4	1.57	1.57	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
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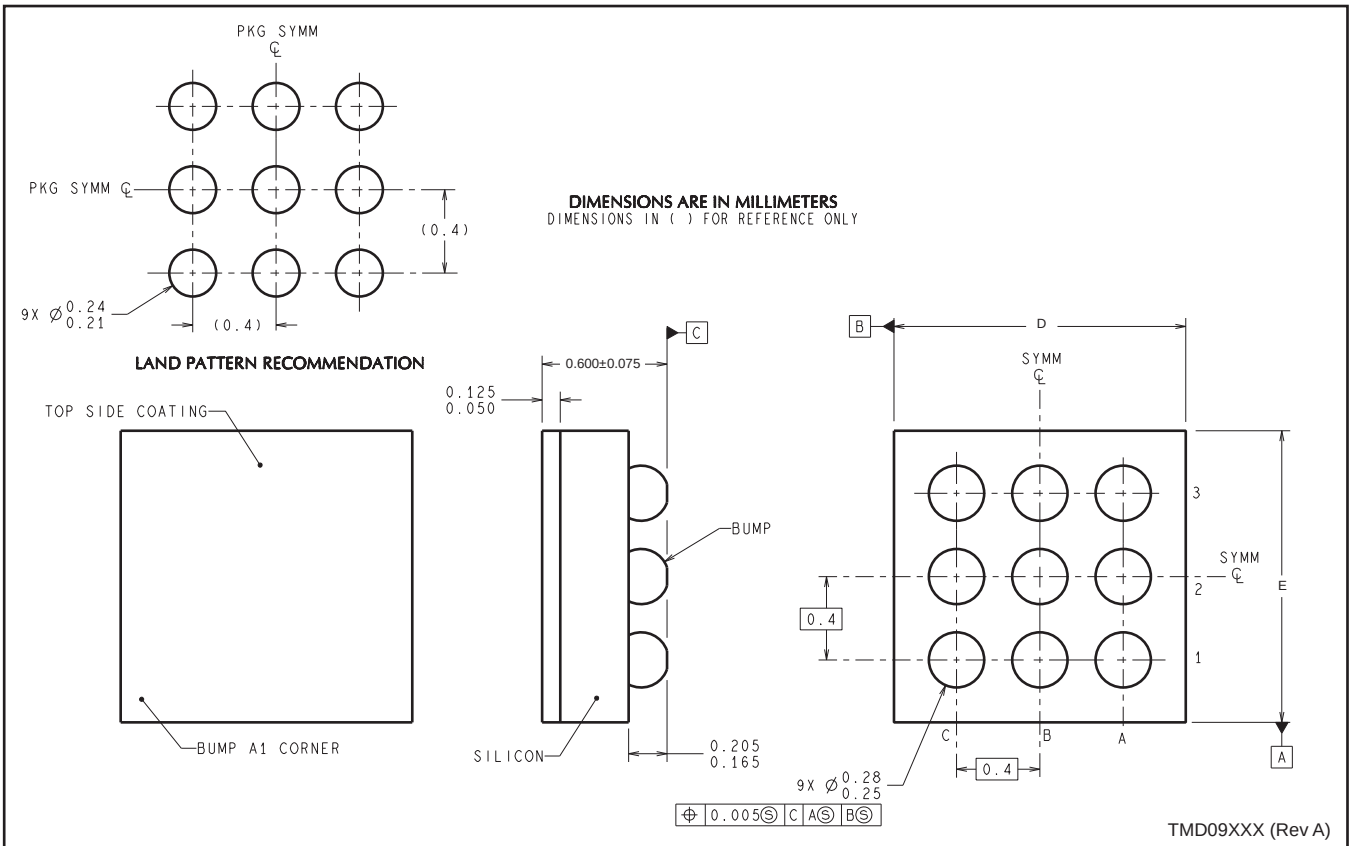
LM3262TMX/NOPB	DSBGA	YFQ	9	3000	210.0	185.0	35.0

YFQ0009



D: Max = 1.51 mm, Min = 1.45 mm

E: Max = 1.385 mm, Min =1.325 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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