

## N-channel 100 V, 0.0036 $\Omega$ typ., 65 A, STripFET™ F7 Power MOSFET in a TO-220FP package

Datasheet – production data

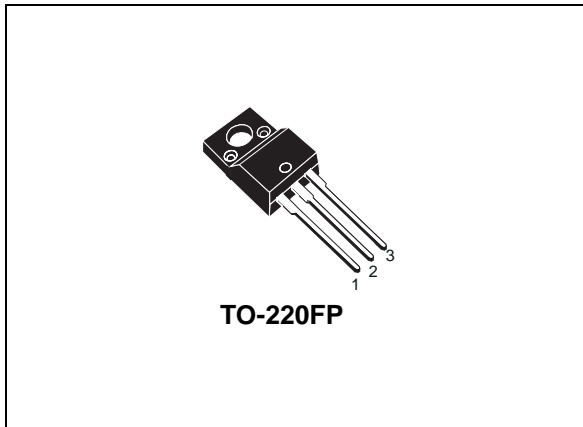
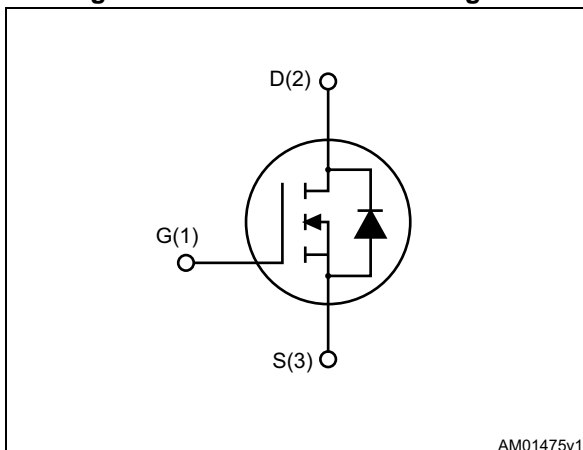


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)max</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STF150N10F7	100 V	0.0042 $\Omega$	65 A	35 W

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
STF150N10F7	150N10F7	TO-220FP	Tube

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate- source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	65	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	45	A
$I_{DM}^{(1)}$	Drain current (pulsed) $T_C = 25\text{ }^\circ\text{C}$	260	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	35	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	495	mJ
$T_J$	Operating junction temperature	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature		$^\circ\text{C}$

1. Pulse width is limited by safe operating area

2. Starting  $T_j=25\text{ }^\circ\text{C}$ ,  $I_D=30\text{ A}$ ,  $V_{DD}=50\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	4.29	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C/W}$

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\ \mu A$	100			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 100\ V$			1	$\mu A$
		$V_{GS} = 0, V_{DS} = 100\ V, T_C = 125\text{ °C}$			100	$\mu A$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = +20\ V$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ V, I_D = 55\ A$		0.0036	0.0042	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\ V, f = 1\ MHz, V_{GS} = 0$	-	8115	-	pF
$C_{oss}$	Output capacitance		-	1510	-	pF
$C_{riss}$	Reverse transfer capacitance		-	67	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\ V, I_D = 65\ A, V_{GS} = 10\ V$ (see <a href="#">Figure 14</a> )	-	117	-	nC
$Q_{gs}$	Gate-source charge		-	47	-	nC
$Q_{gd}$	Gate-drain charge		-	26	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ V, I_D = 55\ A, R_G = 4.7\ \Omega, V_{GS} = 10\ V$ (see <a href="#">Figure 13</a> )	-	33	-	ns
$t_r$	Rise time		-	57	-	ns
$t_{d(off)}$	Turn-off delay time		-	72	-	ns
$t_f$	Fall time		-	33	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		65	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		260	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 65 \text{ A}, V_{GS} = 0$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 65 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 80 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	70		ns
$Q_{rr}$	Reverse recovery charge		-	165		nC
$I_{RRM}$	Reverse recovery current		-	4.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

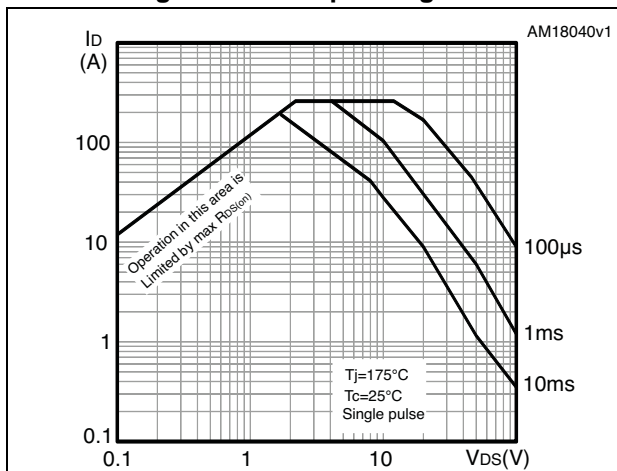


Figure 3. Thermal impedance

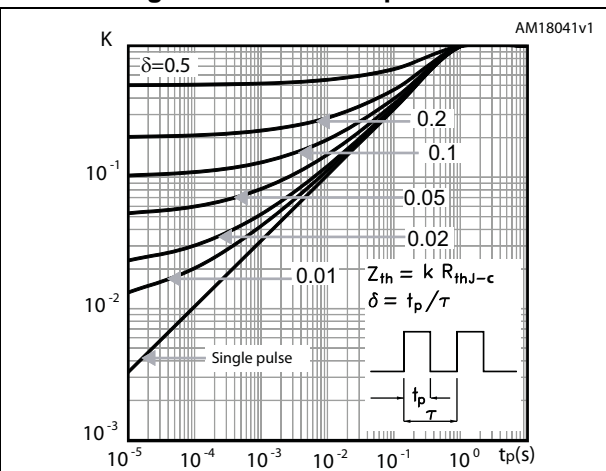


Figure 4. Output characteristics

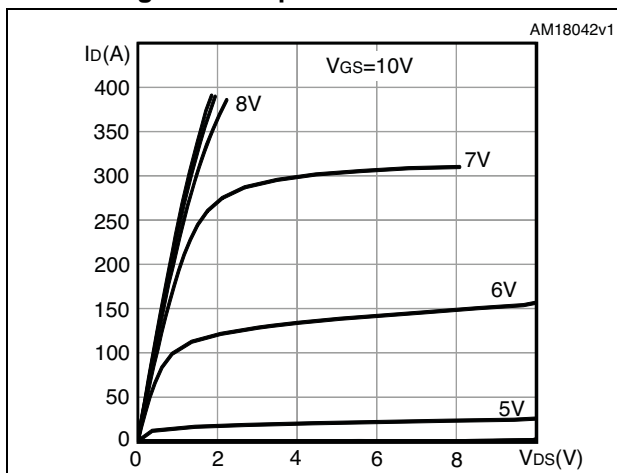


Figure 5. Transfer characteristics

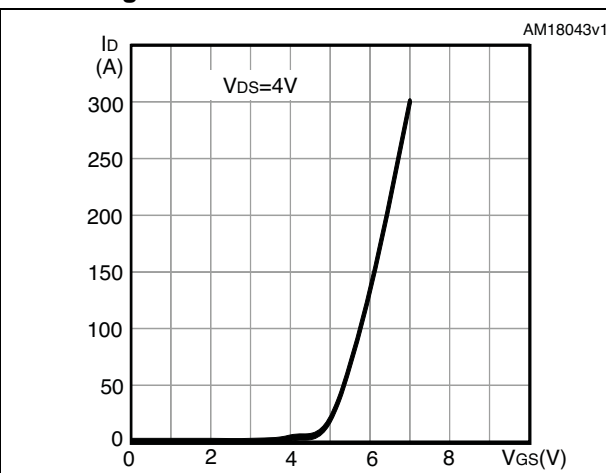


Figure 6. Gate charge vs gate-source voltage

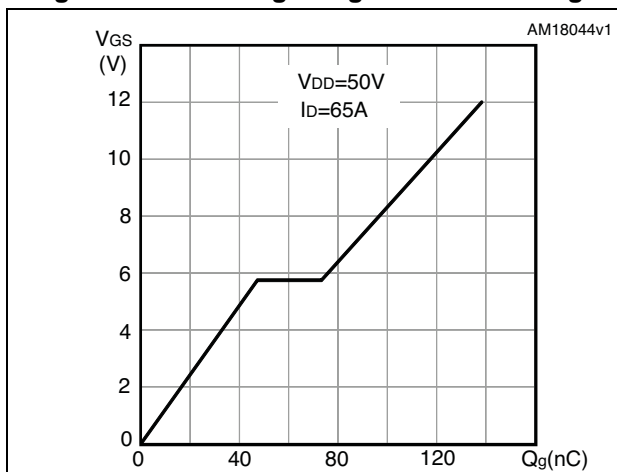


Figure 7. Static drain-source on-resistance

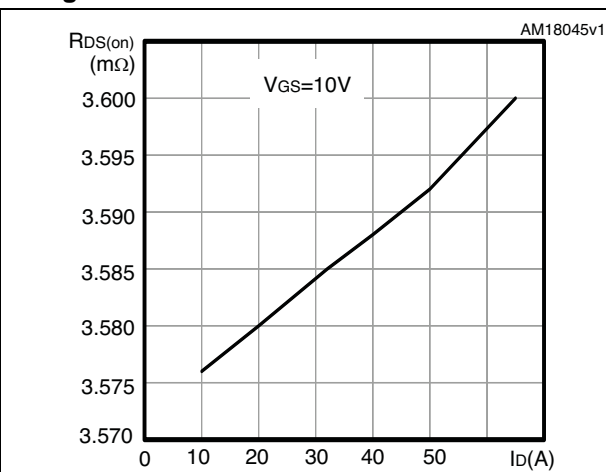


Figure 8. Capacitance variations

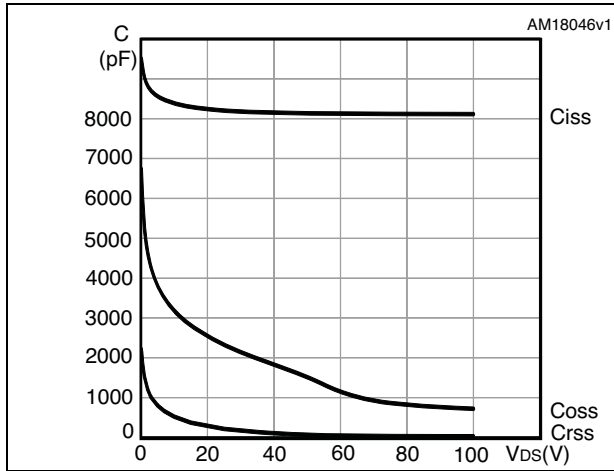


Figure 9. Normalized gate threshold voltage vs temperature

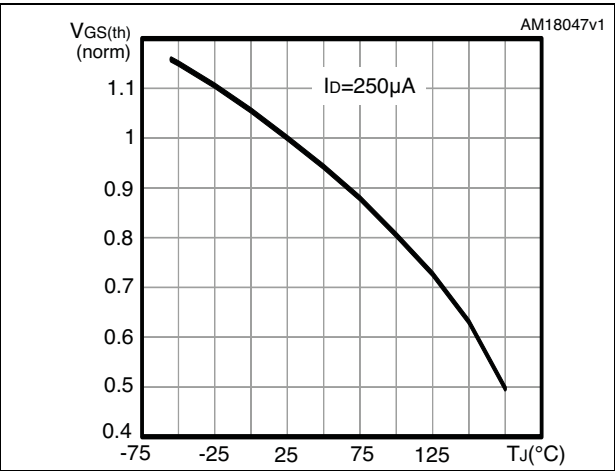


Figure 10. Normalized on-resistance vs temperature

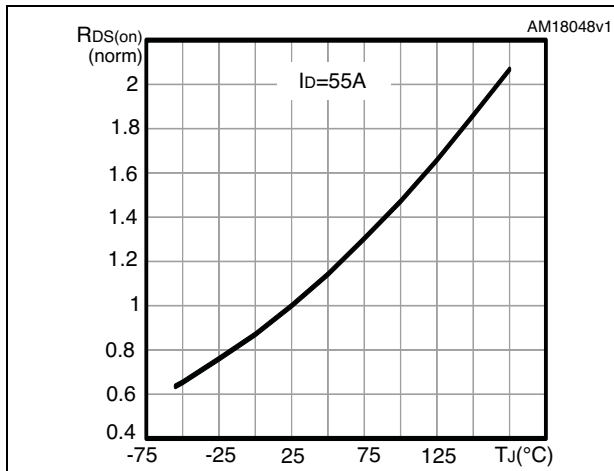


Figure 11. Normalized V<sub>DS</sub> vs temperature

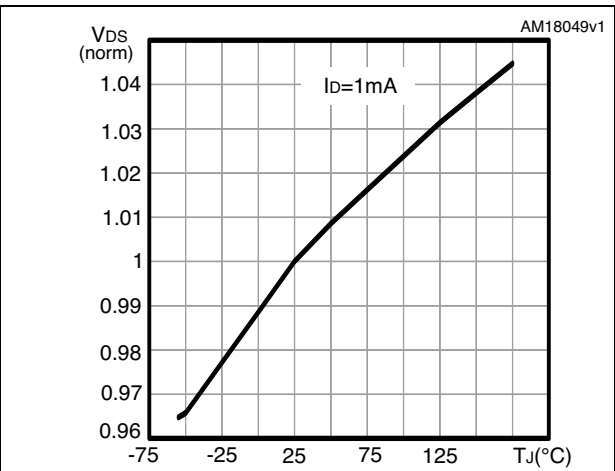
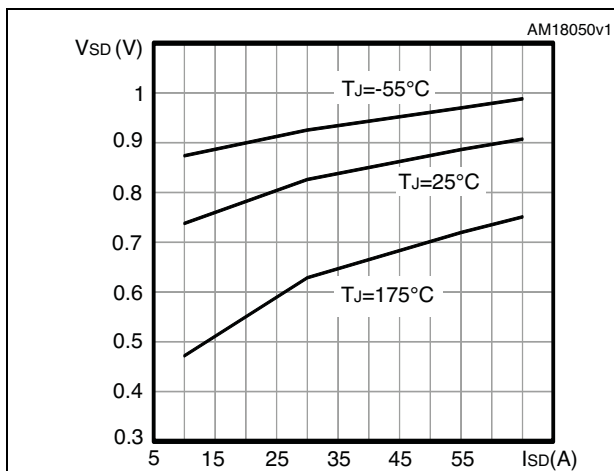


Figure 12. Source-drain diode forward characteristics



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load



Figure 14. Gate charge test circuit

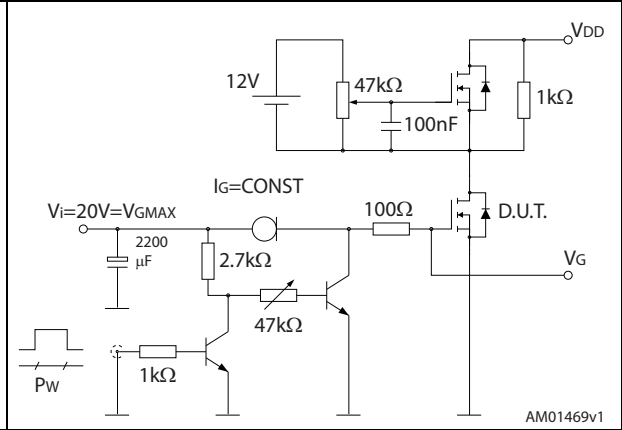


Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped inductive load test circuit



Figure 17. Unclamped inductive waveform



Figure 18. Switching time waveform

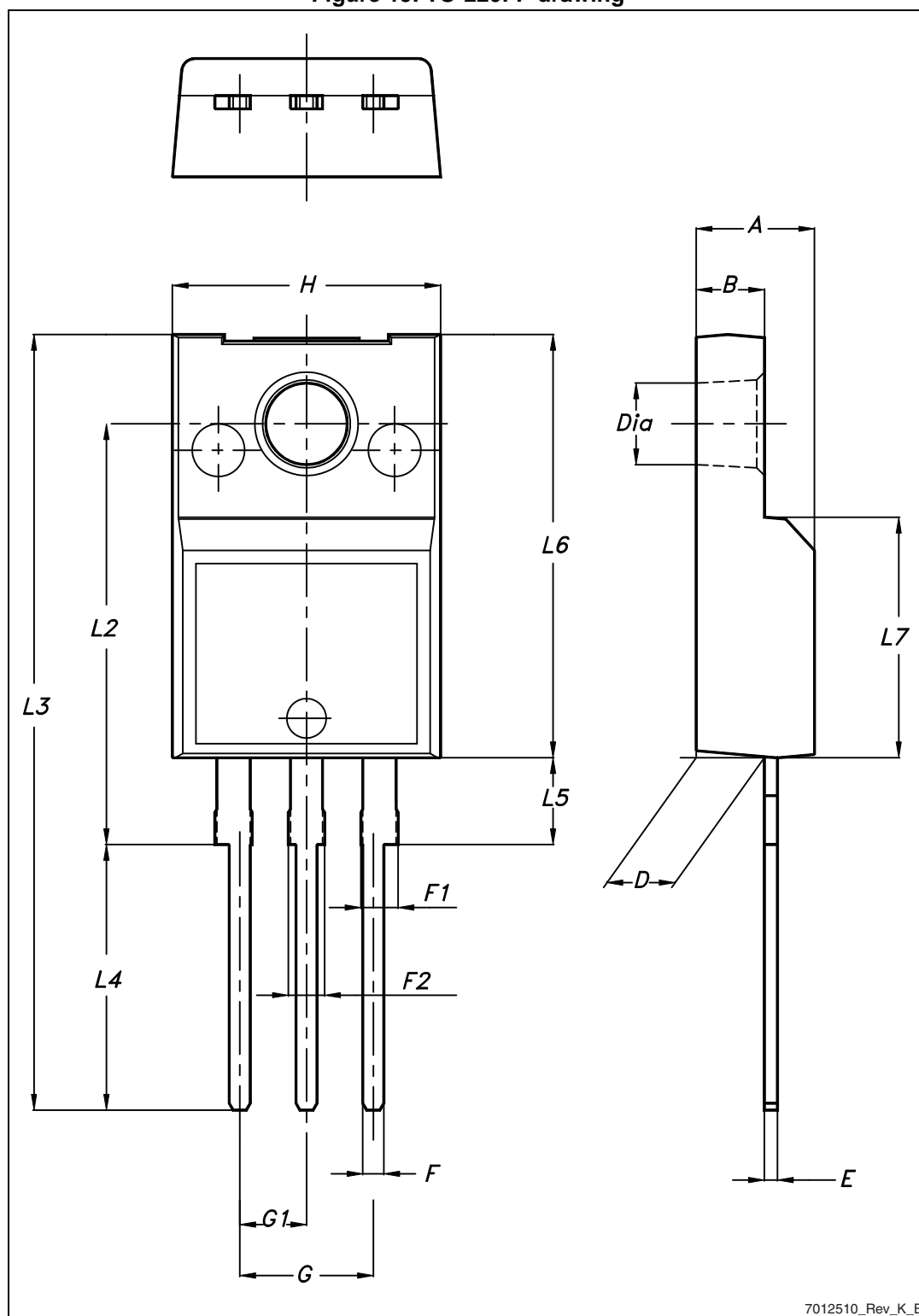




## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 19. TO-220FP drawing



7012510\_Rev\_K\_B

Table 8. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

## 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
22-Jan-2014	1	First release.
22-Aug-2014	2	Updated title, features and description in cover page. Updated <a href="#">Figure 3: Thermal impedance</a> .

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