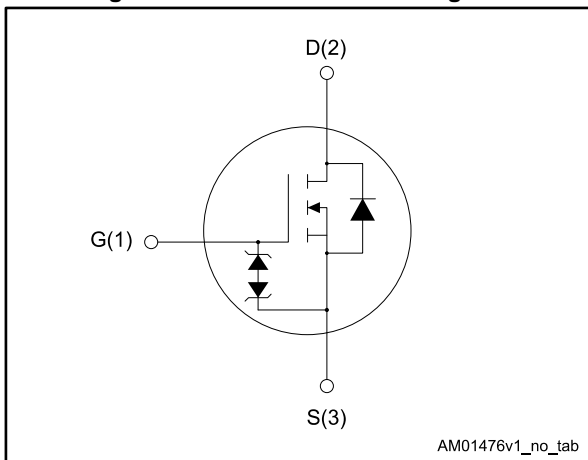


N-channel 600 V, 0.175 Ω typ., 18 A MDmesh™ DM2 Power MOSFET in a TO-220FP package

Datasheet - production data



Figure 1: Internal schematic diagram



Features

Order code	V _{DS} @ T _{Jmax}	R _{DS(on)} max.	I _D
STF24N60DM2	650 V	0.200 Ω	18 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STF24N60DM2	24N60DM2	TO-220FP	Tube

Contents

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	18	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11	
$I_{DM}^{(2)(1)}$	Drain current (pulsed)	72	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	30	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	40	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$)	2500	V
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature range		

Notes:

(1) Limited by package.

(2) Pulse width is limited by safe operating area.

(3) $I_{SD} \leq 18\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{S}$, $V_{DS(\text{peak})} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

(4) $V_{DS} \leq 480\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max.	4.2	$^\circ\text{C}/\text{W}$
$R_{thj\text{-amb}}$	Thermal resistance junction-ambient max.	62.5	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{Jmax})	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	180	mJ

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$			1.5	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$, $T_{\text{C}} = 125\text{ °C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 10	μA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 9\text{ A}$		0.175	0.200	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	1055	-	pF
C_{oss}	Output capacitance		-	56	-	pF
C_{rss}	Reverse transfer capacitance		-	2.4	-	pF
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	259	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	7	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 480\text{ V}$, $I_{\text{D}} = 18\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	29	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

Notes:

⁽¹⁾ $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 9\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	15	-	ns
t_r	Rise time		-	8.7	-	ns
$t_{d(off)}$	Turn-off-delay time		-	60	-	ns
t_f	Fall time		-	15	-	ns

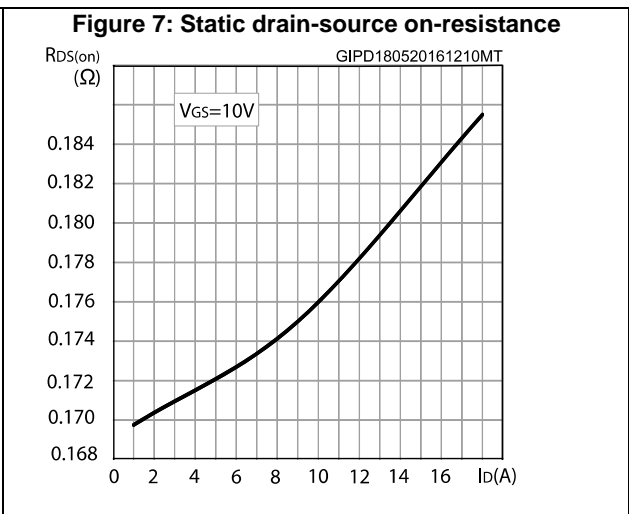
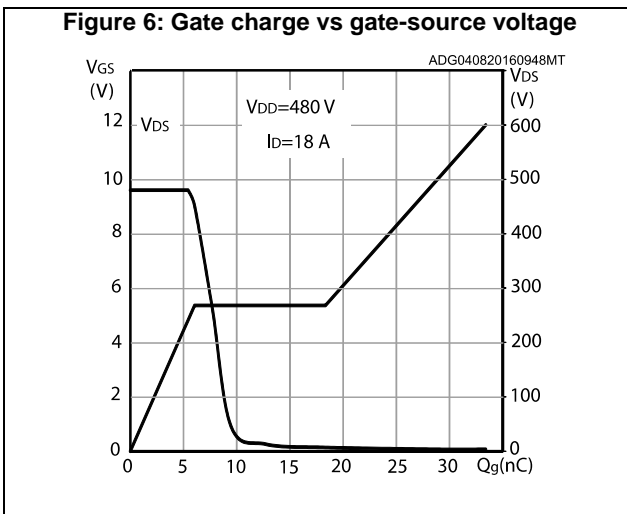
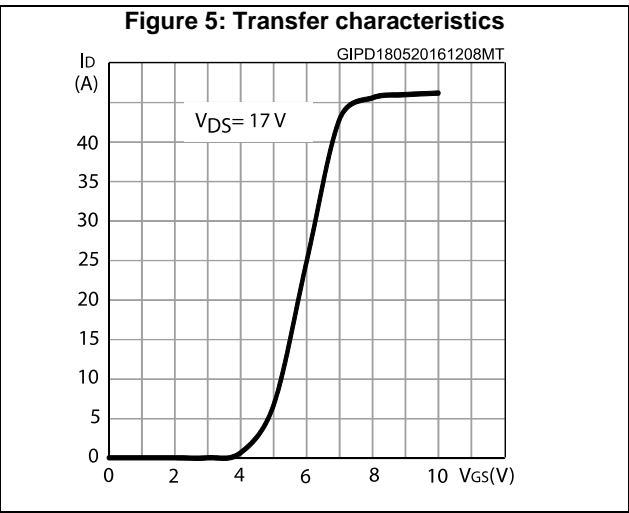
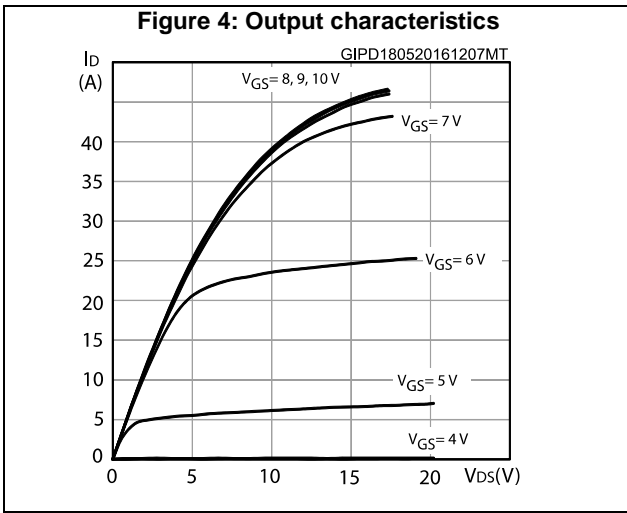
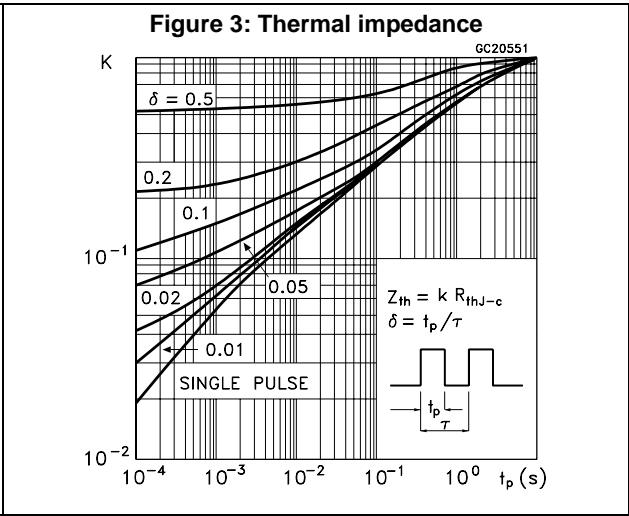
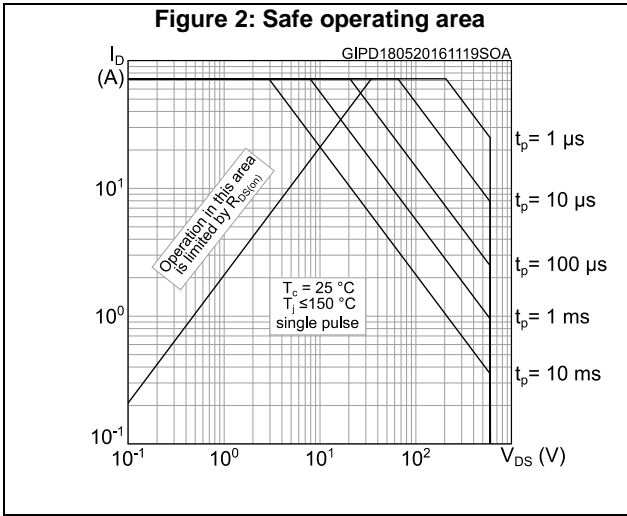
Table 8: Source-drain diode

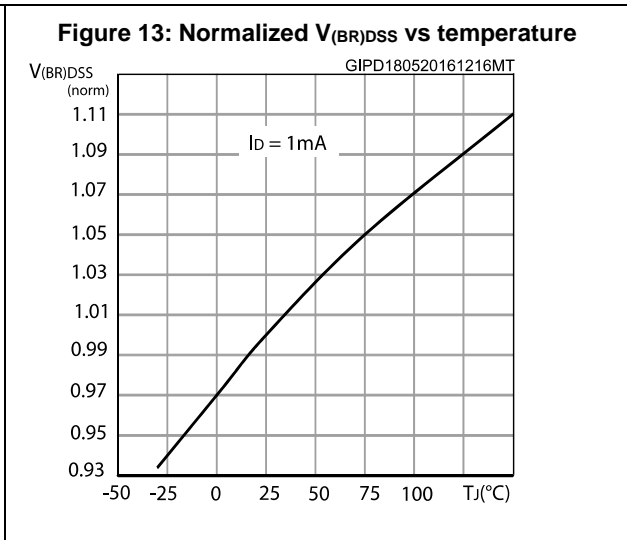
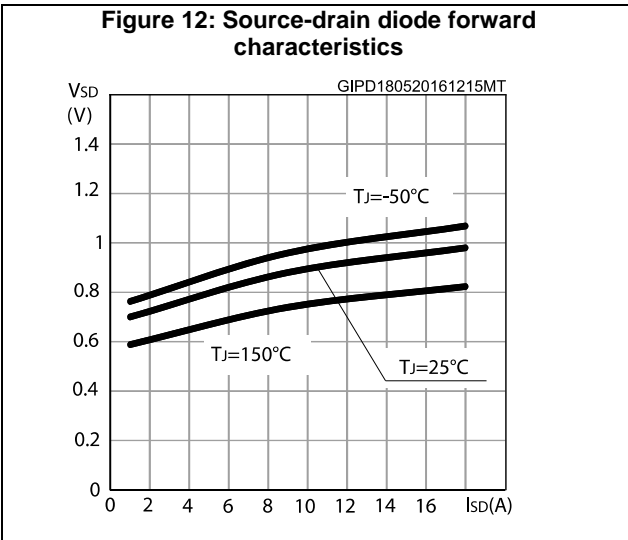
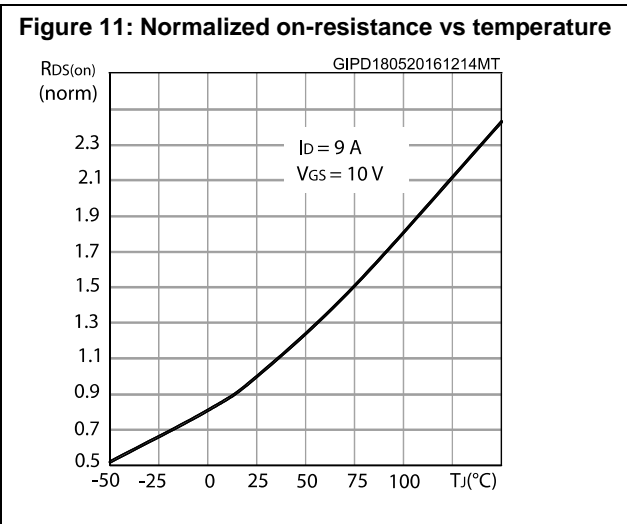
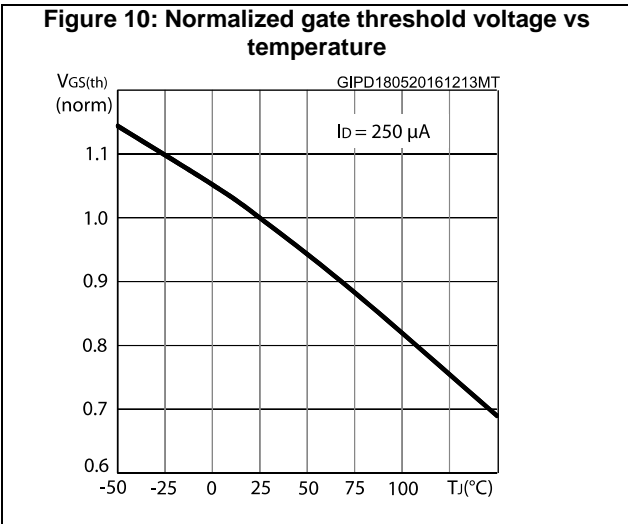
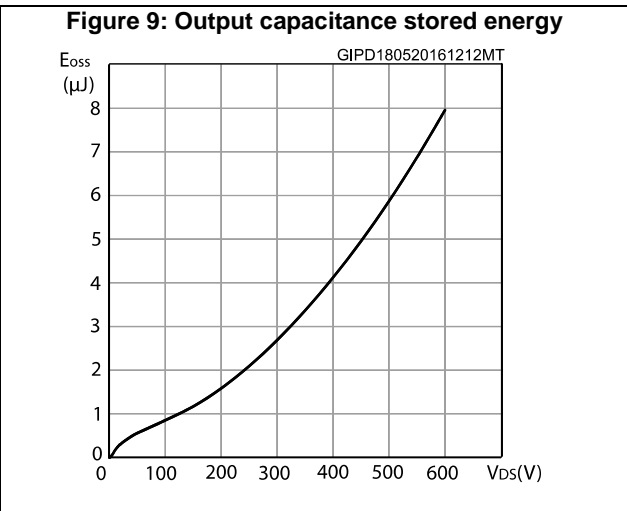
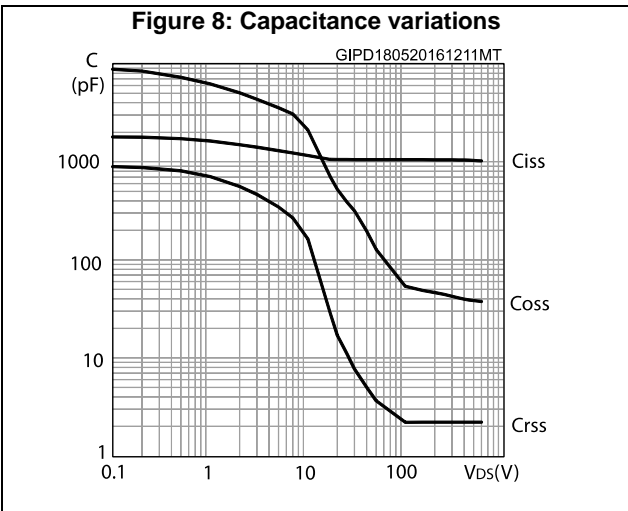
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		72	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 18\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	155		ns
Q_{rr}	Reverse recovery charge		-	956		nC
I_{RRM}	Reverse recovery current		-	12.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	200		ns
Q_{rr}	Reverse recovery charge		-	1450		nC
I_{RRM}	Reverse recovery current		-	13		A

Notes:

- (1) Pulse width is limited by safe operating area.
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 14: Test circuit for resistive load switching times



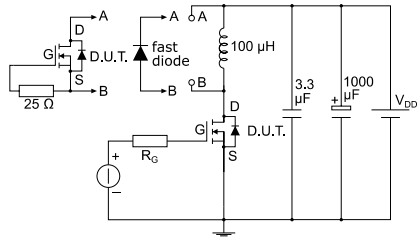
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Figure 15: Test circuit for gate charge behavior



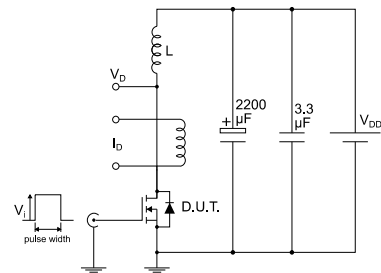
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Figure 16: Test circuit for inductive load switching and diode recovery times



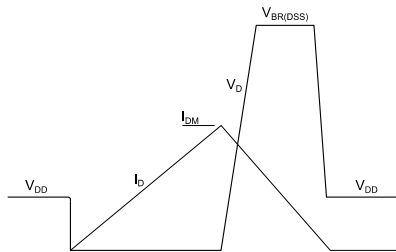
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Figure 17: Unclamped inductive load test circuit



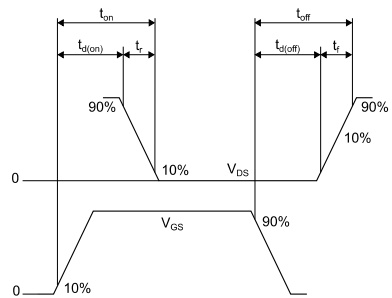
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



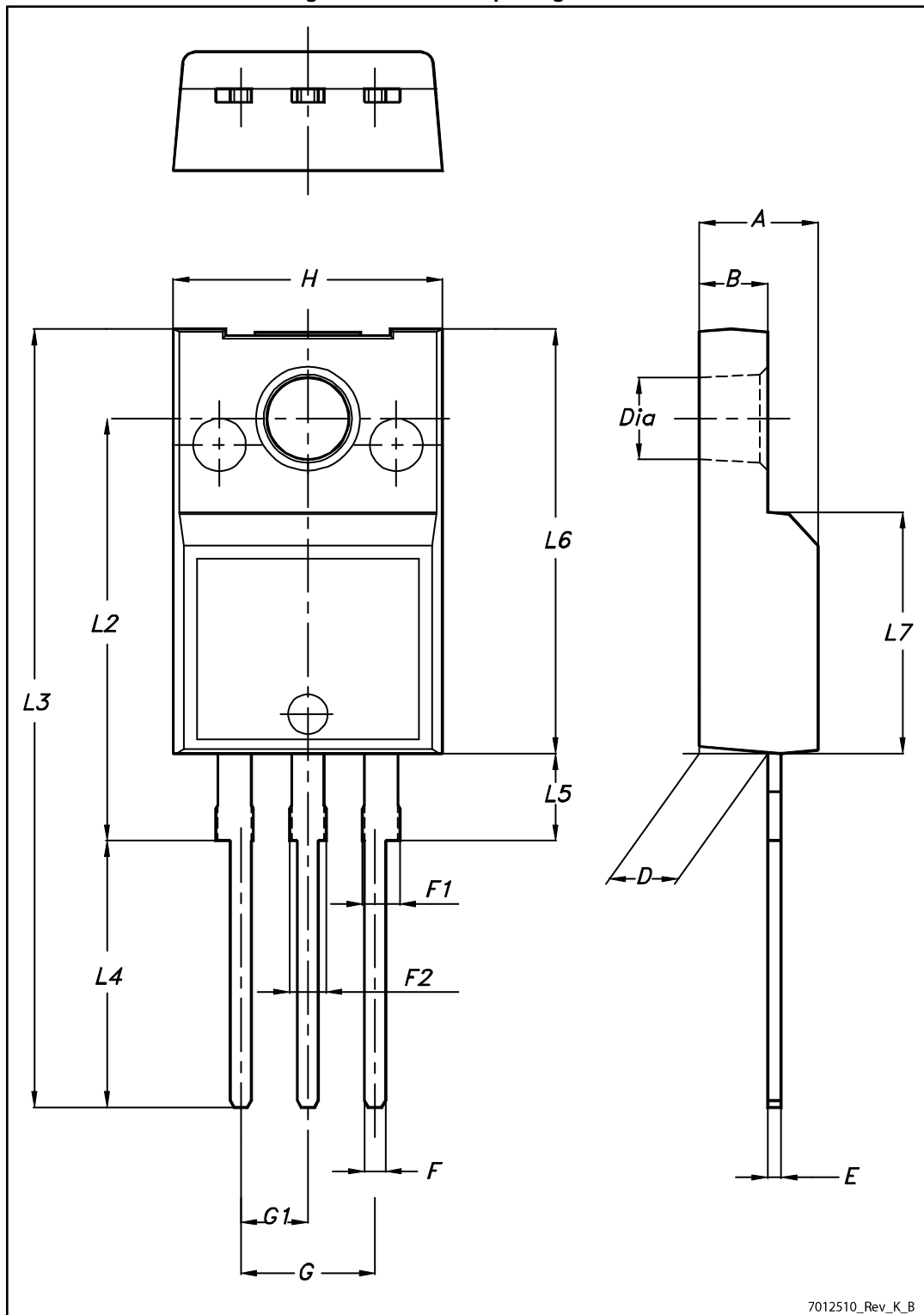
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 20: TO-220FP package outline



7012510_Rev_K_B

Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
12-Nov-2013	1	First release.
21-Jan-2014	2	<ul style="list-style-type: none"> – Modified: dv/dt value in Table 2 – Modified: I_{AR} value in Table 4 – Modified: I_{DSS} and $V_{GS(th)}$ in Table 5 – Minor text changes
03-Mar-2014	3	<ul style="list-style-type: none"> – Modified: Figure 1 – Modified: P_{TOT} value and note 1 in Table 2 – Modified: $R_{thj-case}$ value in Table 3 – Modified: I_{AR} value in Table 4 – Minor text changes
05-Mar-2015	4	<ul style="list-style-type: none"> – Document status promoted from preliminary to production data. – Updated title, features and description in cover page.
20-Sep-2016	5	<ul style="list-style-type: none"> Updated Figure 2: "Safe operating area". Minor text changes

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