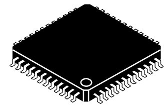


16-BIT, 1.25-MSPS, UNIPOLAR PSEUDO-DIFFERENTIAL INPUT, MICROPOWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE

FEATURES

- **Unipolar Pseudo-Differential Input, 0 V to V_{ref}**
- **16-Bit NMC at 1.25 MSPS**
- **±2 LSB INL Max, -1/+1.5 LSB DNL**
- **86 dB SNR, -90 dB THD at 100 kHz Input**
- **Zero Latency**
- **Internal 4.096-V Reference**
- **High-Speed Parallel Interface**
- **Single 5-V Analog Supply**
- **Wide I/O Supply: 2.7 V to 5.25 V**
- **Low Power: 155 mW at 1.25 MHz Typ**
- **Pin Compatible With ADS8411/8401**
- **48-Pin TQFP Package**

APPLICATIONS

- **DWDM**
- **Instrumentation**
- **High-Speed, High-Resolution, Zero Latency Data Acquisition Systems**
- **Transducer Interface**
- **Medical Instruments**
- **Communications**

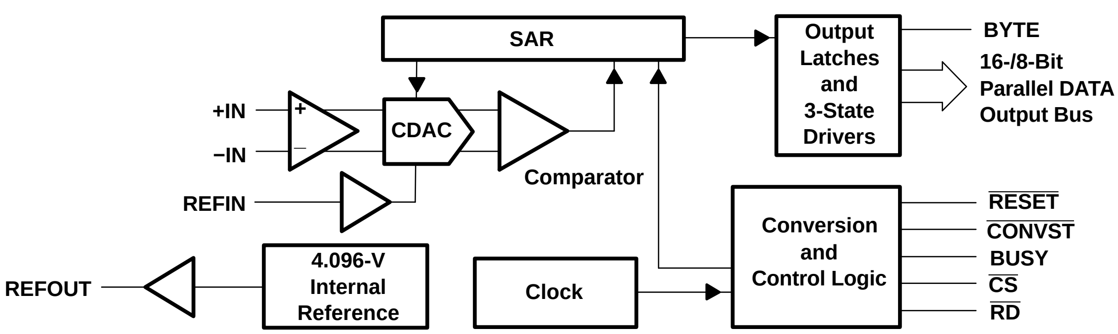
DESCRIPTION

The ADS8405 is a 16-bit, 1.25-MHz A/D converter with an internal 4.096-V reference. The device includes a 16-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8405 offers a full 16-bit interface and an 8-bit option where data is read using two 8-bit read cycles if necessary.

The ADS8405 has a unipolar pseudo-differential input. It is available in a 48-lead TQFP package and is characterized over the industrial -40°C to 85°C temperature range.

High Speed SAR Converter Family

Type/Speed	500 kHz	~600 kHz	750 kHz	1 MHz	1.25 MHz	2 MHz	3 MHz	4 MHz
18-Bit Pseudo-Diff	ADS8383	ADS8381						
		ADS8380 (S)						
18-Bit Pseudo-Bipolar, Fully Diff		ADS8382 (S)						
16-Bit Pseudo-Diff			ADS8371		ADS8401/05	ADS8411		
16-Bit Pseudo-Bipolar, Fully Diff					ADS8402/06	ADS8412		
14-Bit Pseudo-Diff					ADS7890 (S)		ADS7891	
12-Bit Pseudo-Diff				ADS7886				ADS7881



ORDERING INFORMATION[1]

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS8405I	–4 to +4	–2 to +2	15	48 Pin TQFP	PFB	–40°C to 85°C	ADS8405IPFBT	Tape and reel 250
							ADS8405IPFBR	Tape and reel 1000
ADS8405IB	–2 to +2	–1 to +1.5	16	48 Pin TQFP	PFB	–40°C to 85°C	ADS8405IBPFBT	Tape and reel 250
							ADS8405IBPFBR	Tape and reel 1000

(1) For the most current specifications and package information, refer to our website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

			UNIT
	Voltage	+IN to AGND	–0.4 V to +VA + 0.1 V
		–IN to AGND	–0.4 V to 0.5 V
		+VA to AGND	–0.3 V to 7 V
		+VBD to BDGND	–0.3 V to 7 V
		+VA to +VBD	–0.3 V to 2.55 V
	Digital input voltage to BDGND		–0.3 V to +VBD + 0.3 V
	Digital output voltage to BDGND		–0.3 V to +VBD + 0.3 V
T_A	Operating free-air temperature range		–40°C to 85°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Junction temperature (T_J max)		150°C
	TQFP package	Power dissipation	$(T_J Max – T_A)/\theta_{JA}$
		θ_{JA} thermal impedance	86°C/W
	Lead temperature, soldering	Vapor phase (60 sec)	215°C
		Infrared (15 sec)	220°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

T_A = –40°C to 85°C, +VA = 5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 1.25 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Full-scale input voltage [(1)]		+IN – (–IN)	0		V_{ref}	V
	Absolute input voltage		+IN	–0.2		V_{ref} + 0.2	V
			–IN	–0.2		0.2	
	Input capacitance				25		pF
	Input leakage current				0.5		nA
SYSTEM PERFORMANCE							
	Resolution				16		Bits
	No missing codes	ADS8405I		15			Bits
		ADS8405IB		16			
INL	Integral linearity [(2)(3)]	ADS8405I		–4	±2	4	LSB
		ADS8405IB		–2	±1	2	
DNL	Differential linearity	ADS8405I		–2	±1	2	LSB
		ADS8405IB		–1	±0.75	1.5	
E_O	Offset error [(4)]	ADS8405I		–3	±1	3	mV
		ADS8405IB		–1.5	±0.5	1.5	mV
E_G	Gain error [(4)(5)]	ADS8405I		–0.15		0.15	%FS
		ADS8405IB		–0.098		0.98	
	Noise				60		µV RMS
	DC Power supply rejection ratio		At FFFFh output code, +VA = 4.75 V to 5.25 V, V_{ref} = 4.096 V [(4)]		2		LSB
SAMPLING DYNAMICS							
	Conversion time			500		650	ns
	Acquisition time			150			ns
	Throughput rate					1.25	MHz
	Aperture delay				2		ns
	Aperture jitter				25		ps
	Step response				100		ns
	Overvoltage recovery				100		ns
DYNAMIC CHARACTERISTICS							
THD	Total harmonic distortion [(6)]		VIN = 4 V_{p-p} at 100 kHz		–90		dB
			VIN = 4 V_{p-p} at 500 kHz		–88.5		dB
SNR	Signal-to-noise ratio		VIN = 4 V_{p-p} at 100 kHz		86		dB
SINAD	Signal-to-noise + distortion		VIN = 4 V_{p-p} at 100 kHz		85		dB
SFDR	Spurious free dynamic range		VIN = 4 V_{p-p} at 100 kHz		90		dB
			VIN = 4 V_{p-p} at 500 kHz		88		dB
	-3dB Small signal bandwidth				5		MHz
EXTERNAL VOLTAGE REFERENCE INPUT							
	Reference voltage at REFIN, V_{ref}			2.5	4.096	4.2	V
	Reference resistance [(7)]				500		kΩ

(1) Ideal input span, does not include gain or offset error.
(2) LSB means least significant bit
(3) This is endpoint INL, not best fit.
(4) Measured relative to an ideal full-scale input (+IN – (–IN)) of 4.096 V.
(5) This specification does not include the internal reference voltage error and drift.
(6) Calculated on the first nine harmonics of the input frequency.
(7) Can vary ±20%

SPECIFICATIONS (continued)

T_A = –40°C to 85°C, +VA = 5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 1.25 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE OUTPUT							
	Internal reference start-up time		From 95% (+VA), with 1-µF storage capacitor			120	ms
	V_{ref} range		IOUT = 0	4.065	4.096	4.13	V
	Source current		Static load			10	µA
	Line regulation		+VA = 4.75 V to 5.25 V		0.6		mV
	Drift		IOUT = 0		36		PPM/C
DIGITAL INPUT/OUTPUT							
	Logic family - CMOS						
V_{IH}	High-level input voltage		I_{IH} = 5 µA	+VBD – 1		+VBD + 0.3	V
V_{IL}	Low-level input voltage		I_{IL} = 5 µA	–0.3		0.8	V
V_{OH}	High-level output voltage		I_{OH} = 2 TTL loads	+VBD – 0.6		+VBD	V
V_{OL}	Low-level output voltage		I_{OL} = 2 TTL loads	0		0.4	V
	Data format - straight binary						
POWER SUPPLY REQUIREMENTS							
	Power supply voltage	+VBD		2.7	3	5.25	V
	Power supply voltage	+VA		4.75	5	5.25	V
	+VA Supply current [8]		f_s = 1.25 MHz		31	34	mA
	Power dissipation[8]		f_s = 1.25 MHz		155	170	mW
TEMPERATURE RANGE							
	Operating free-air			–40		85	°C

(8) This includes only VA+ current. +VBD current is typically 1 mA with 5-pF load capacitance on output pins.

TIMING CHARACTERISTICS

All specifications typical at –40°C to 85°C, +VA = +VBD = 5 V (1)(2)(3)

PARAMETER		MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time	500		650	ns
t_{ACQ}	Acquisition time	150			ns
t_{pd1}	$\overline{\text{CONVST}}$ low to BUSY high		40		ns
t_{pd2}	Propagation delay time, end of conversion to BUSY low		5		ns
t_{w1}	Pulse duration, $\overline{\text{CONVST}}$ low	20			ns
t_{su1}	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	0			ns
t_{w2}	Pulse duration, $\overline{\text{CONVST}}$ high	20			ns
	$\overline{\text{CONVST}}$ falling edge jitter			10	ps
t_{w3}	Pulse duration, BUSY signal low	Min(t_{ACQ})			ns
t_{w4}	Pulse duration, BUSY signal high		610		ns
t_{h1}	Hold time, first data bus data transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE input changes) after $\overline{\text{CONVST}}$ low	40			ns
t_{d1}	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low (or BUSY low to $\overline{\text{RD}}$ low when $\overline{\text{CS}}$ = 0)	0			ns
t_{su2}	Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t_{w5}	Pulse duration, $\overline{\text{RD}}$ low	50			ns
t_{en}	Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid			20	ns
t_{d2}	Delay time, data hold from $\overline{\text{RD}}$ high	0			ns
t_{d3}	Delay time, BYTE rising edge or falling edge to data valid	2		20	ns
t_{w6}	Pulse duration, $\overline{\text{RD}}$ high	20			ns
t_{w7}	Pulse duration, $\overline{\text{CS}}$ high	20			ns
t_{h2}	Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	50			ns
t_{su3}	Setup time, BYTE transition to $\overline{\text{RD}}$ falling edge	0			ns
t_{h3}	Hold time, BYTE transition to $\overline{\text{RD}}$ falling edge	0			ns
t_{dis}	Disable time, $\overline{\text{RD}}$ high ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus			20	ns
t_{d5}	Delay time, end of conversion to MSB data valid			10	ns
t_{su4}	Byte transition setup time, from BYTE transition to next BYTE transition	50			ns
t_{d6}	Delay time, $\overline{\text{CS}}$ rising edge to BUSY falling edge	50			ns
t_{d7}	Delay time, BUSY falling edge to $\overline{\text{CS}}$ rising edge	50			ns
$t_{su(AB)}$	Setup time, from the falling edge of $\overline{\text{CONVST}}$ (used to start the valid conversion) to the next falling edge of $\overline{\text{CONVST}}$ (when $\overline{\text{CS}}$ = 0 and $\overline{\text{CONVST}}$ used to abort) or to the next falling edge of $\overline{\text{CS}}$ (when $\overline{\text{CS}}$ is used to abort)	60		500	ns
t_{su5}	Setup time, falling edge of $\overline{\text{CONVST}}$ to read valid data (MSB) from current conversion	MAX(t_{CONV}) + MAX(t_{d5})			ns
t_{h4}	Hold time, data (MSB) from previous conversion hold valid from falling edge of $\overline{\text{CONVST}}$			MIN(t_{CONV})	ns

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.
(3) All timings are measured with 20-pF equivalent loads on all data bits and BUSY pins.

TIMING CHARACTERISTICS

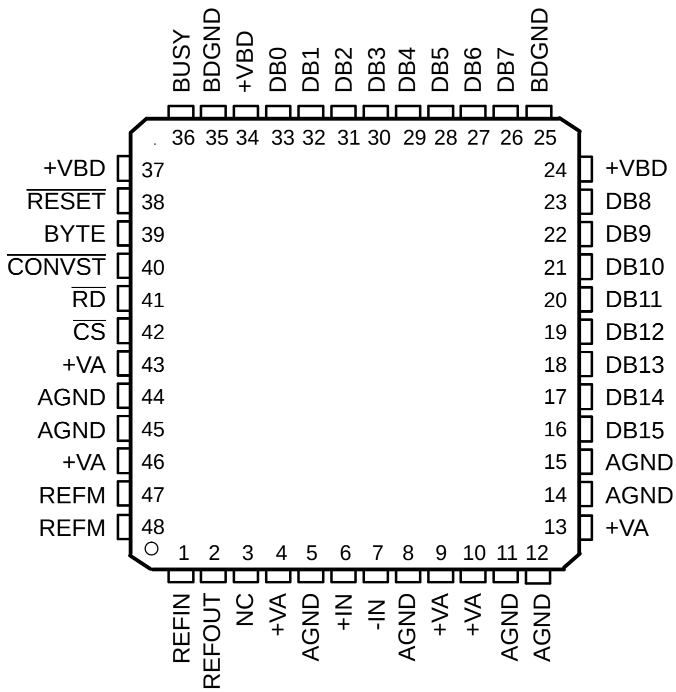
All specifications typical at –40°C to 85°C, +VA = 5 V, +VBD = 3 V(1)(2)(3)

PARAMETER		MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time	500		650	ns
t_{ACQ}	Acquisition time	150			ns
t_{pd1}	$\overline{\text{CONVST}}$ low to BUSY high		50		ns
t_{pd2}	Propagation delay time, end of conversion to BUSY low		10		ns
t_{w1}	Pulse duration, $\overline{\text{CONVST}}$ low	20			ns
t_{su1}	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	0			ns
t_{w2}	Pulse duration, $\overline{\text{CONVST}}$ high	20			ns
	$\overline{\text{CONVST}}$ falling edge jitter			10	ps
t_{w3}	Pulse duration, BUSY signal low	Min(t_{ACQ})			ns
t_{w4}	Pulse duration, BUSY signal high		610		ns
t_{h1}	Hold time, first data bus transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE input changes) after $\overline{\text{CONVST}}$ low	40			ns
t_{d1}	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low (or BUSY low to $\overline{\text{RD}}$ low when $\overline{\text{CS}}$ = 0)	0			ns
t_{su2}	Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t_{w5}	Pulse duration, $\overline{\text{RD}}$ low	50			ns
t_{en}	Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid			30	ns
t_{d2}	Delay time, data hold from $\overline{\text{RD}}$ high	0			ns
t_{d3}	Delay time, BYTE rising edge or falling edge to data valid	2		30	ns
t_{w6}	Pulse duration, $\overline{\text{RD}}$ high	20			ns
t_{w7}	Pulse duration, $\overline{\text{CS}}$ high	20			ns
t_{h2}	Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	50			ns
t_{su3}	Setup time, BYTE transition to $\overline{\text{RD}}$ falling edge	0			ns
t_{h3}	Hold time, BYTE transition to $\overline{\text{RD}}$ falling edge	0			ns
t_{dis}	Disable time, $\overline{\text{RD}}$ high ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus			30	ns
t_{d5}	Delay time, end of conversion to MSB data valid			20	ns
t_{su4}	Byte transition setup time, from BYTE transition to next BYTE transition	50			ns
t_{d6}	Delay time, $\overline{\text{CS}}$ rising edge to BUSY falling edge	50			ns
t_{d7}	Delay time, BUSY falling edge to $\overline{\text{CS}}$ rising edge	50			ns
$t_{su(AB)}$	Setup time, from the falling edge of $\overline{\text{CONVST}}$ (used to start the valid conversion) to the next falling edge of $\overline{\text{CONVST}}$ (when $\overline{\text{CS}}$ = 0 and $\overline{\text{CONVST}}$ used to abort) or to the next falling edge of $\overline{\text{CS}}$ (when $\overline{\text{CS}}$ is used to abort)	70		500	ns
t_{su5}	Setup time, falling edge of $\overline{\text{CONVST}}$ to read valid data (MSB) from current conversion	MAX(t_{CONV}) + MAX(t_{d5})			ns
t_{h4}	Hold time, data (MSB) from previous conversion hold valid from falling edge of $\overline{\text{CONVST}}$			MIN(t_{CONV})	ns

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.
(3) All timings are measured with 10-pF equivalent loads on all data bits and BUSY pins.

PIN ASSIGNMENTS

PFB PACKAGE
(TOP VIEW)



NC - No connection

Texas Instruments
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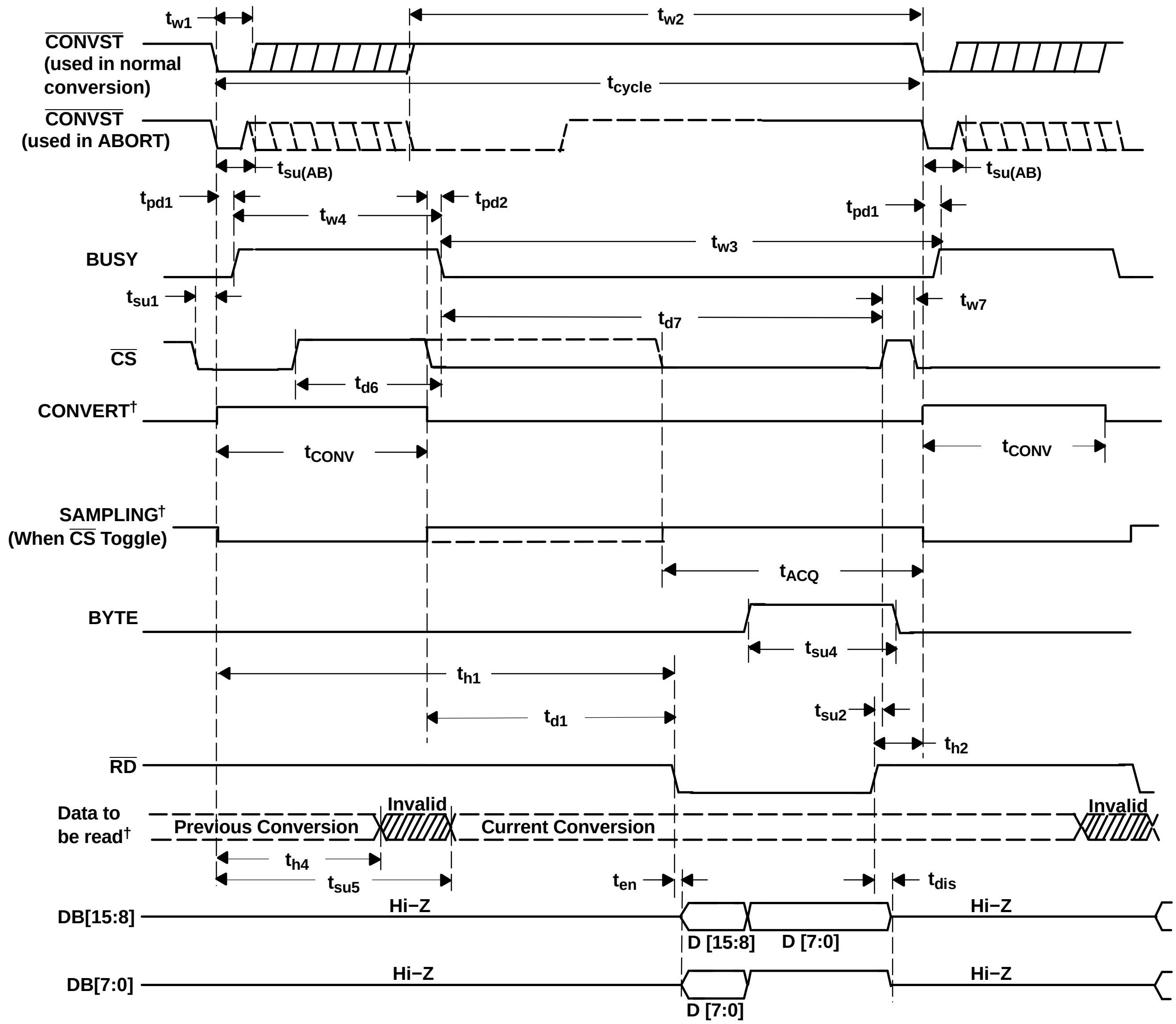
Terminal Functions

NAME	NO.	I/O	DESCRIPTION		
AGND	5, 8, 11, 12, 14, 15, 44, 45	–	Analog ground		
BDGND	25, 35	–	Digital ground for bus interface digital supply		
BUSY	36	O	Status output. High when a conversion is in progress.		
BYTE	39	I	Byte select input. Used for 8-bit bus reading. 0: No fold back 1: Low byte D[7:0] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[15:8].		
$\overline{\text{CONVST}}$	40	I	Convert start. The falling edge of this input ends the acquisition period and starts the hold period.		
$\overline{\text{CS}}$	42	I	Chip select. The falling edge of this input starts the acquisition period.		
Data Bus			**8-Bit Bus**		**16-Bit Bus**
			BYTE = 0	**BYTE = 1**	**BYTE = 0**
DB15	16	O	D15 (MSB)	D7	D15 (MSB)
DB14	17	O	D14	D6	D14
DB13	18	O	D13	D5	D13
DB12	19	O	D12	D4	D12
DB11	20	O	D11	D3	D11
DB10	21	O	D10	D2	D10
DB9	22	O	D9	D1	D9
DB8	23	O	D8	D0 (LSB)	D8
DB7	26	O	D7	All ones	D7
DB6	27	O	D6	All ones	D6
DB5	28	O	D5	All ones	D5
DB4	29	O	D4	All ones	D4
DB3	30	O	D3	All ones	D3
DB2	31	O	D2	All ones	D2
DB1	32	O	D1	All ones	D1
DB0	33	O	D0 (LSB)	All ones	D0 (LSB)
–IN	7	I	Inverting input channel		
+IN	6	I	Noninverting input channel		
NC	3	–	No connection		
REFIN	1	I	Reference input		
REFM	47, 48	I	Reference ground		
REFOUT	2	O	Reference output. Add 1-μF capacitor between the REFOUT pin and REFM pin when the internal reference is used.		
$\overline{\text{RESET}}$	38	I	Current conversion is aborted and output latches are cleared (set to zeros) when this pin is asserted low. $\overline{\text{RESET}}$ works independantly of $\overline{\text{CS}}$.		
$\overline{\text{RD}}$	41	I	Synchronization pulse for the parallel output. When $\overline{\text{CS}}$ is low, this serves as the output enable and puts the previous conversion result on the bus.		
+VA	4, 9, 10, 13, 43, 46	–	Analog power supplies, 5-V dc		
+VBD	24, 34, 37	–	Digital power supply for bus		

TIMING DIAGRAMS



†Signal internal to device

Figure 1. Timing for Conversion and Acquisition Cycles With CS and RD Toggling

TIMING DIAGRAMS (continued)

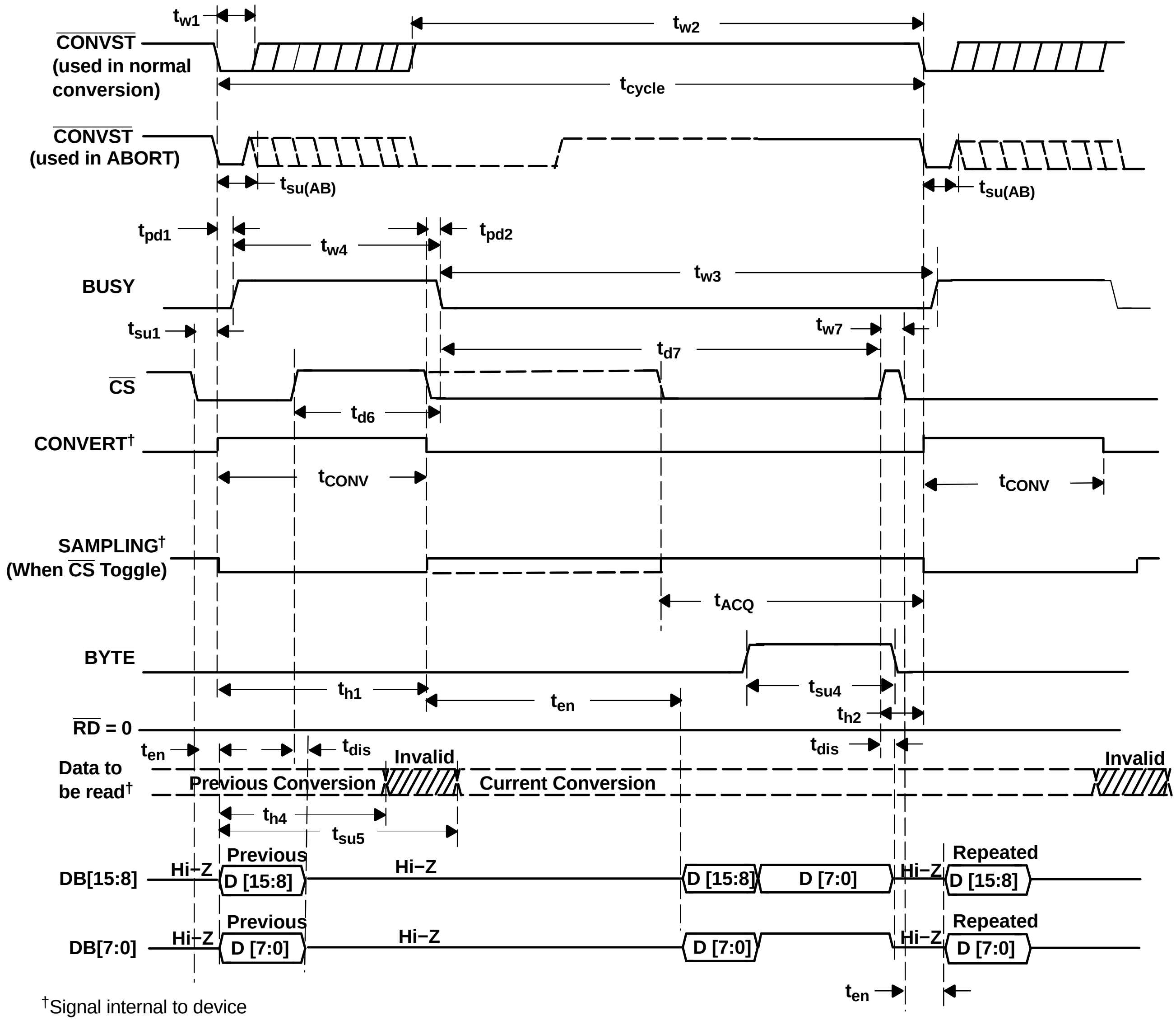


Figure 2. Timing for Conversion and Acquisition Cycles With CS Toggling, RD Tied to BDGND

TIMING DIAGRAMS (continued)

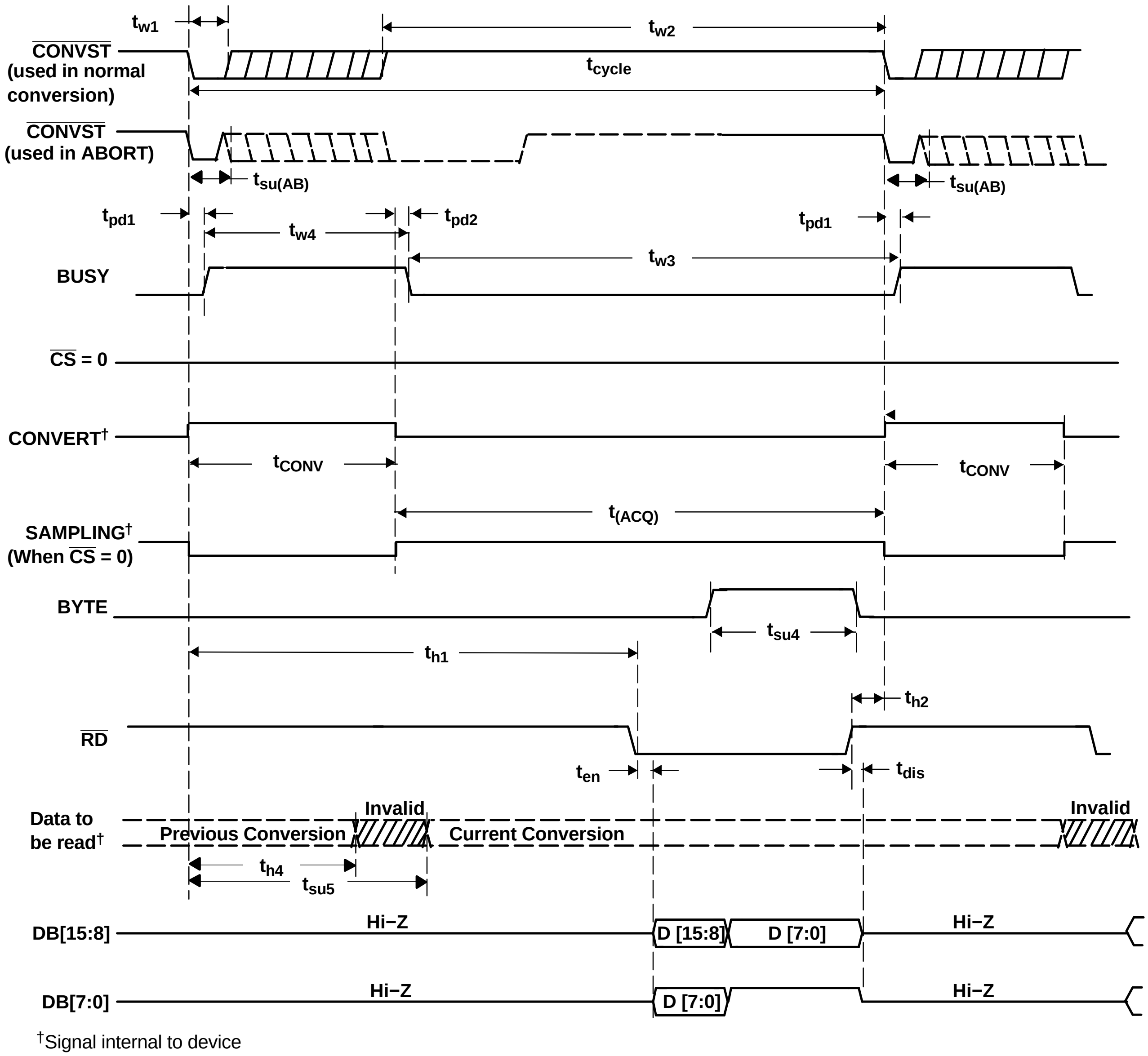
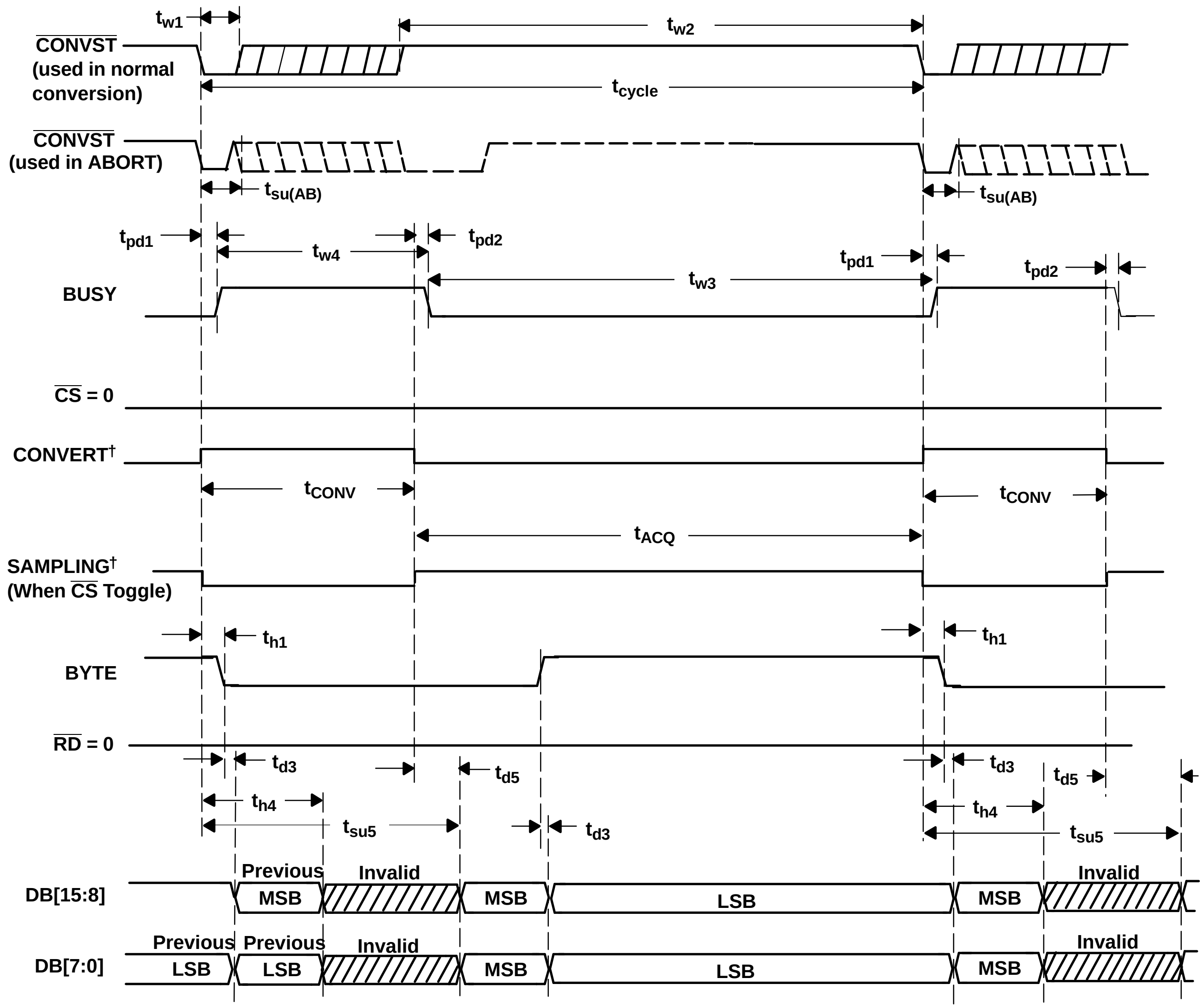


Figure 3. Timing for Conversion and Acquisition Cycles With CS Tied to BDGND, RD Toggling

TIMING DIAGRAMS (continued)



†Signal internal to device

Figure 4. Timing for Conversion and Acquisition Cycles With CS and RD Tied to BDGND—Auto Read

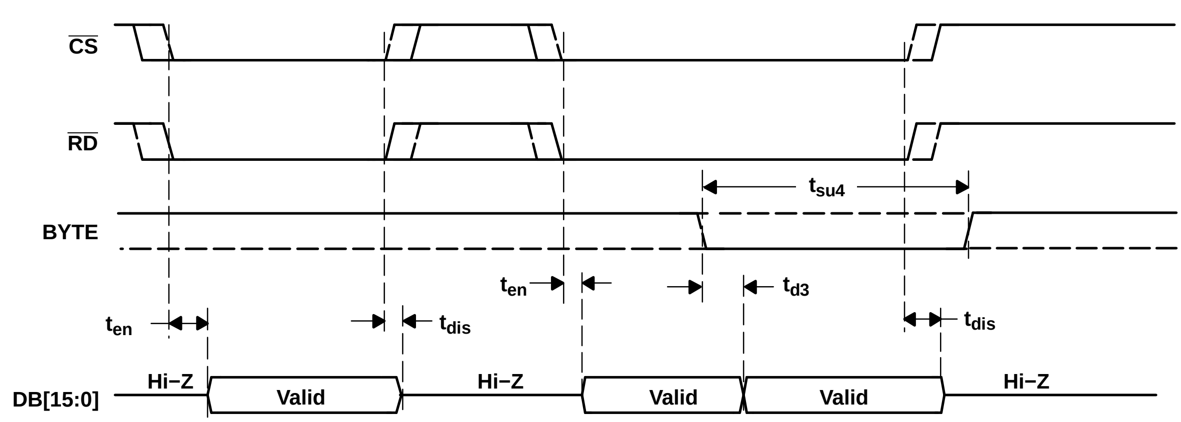


Figure 5. Detailed Timing for Read Cycles

TYPICAL CHARACTERISTICS

At –40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V (internal reference used) and f_{sample} = 1.25 MHz (unless otherwise noted)

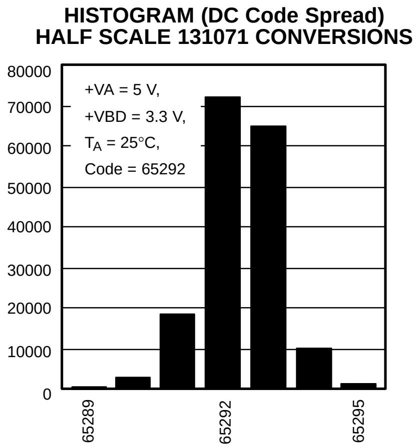


Figure 6.

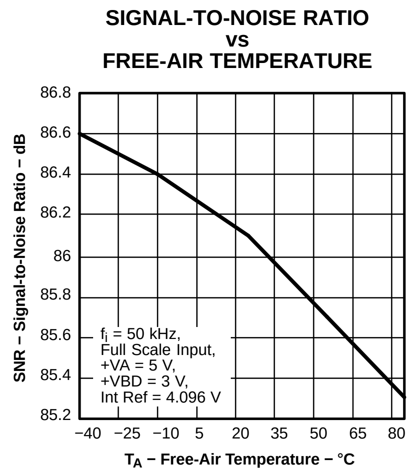


Figure 7.

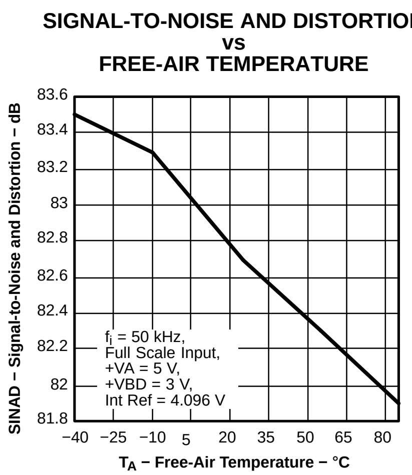


Figure 8.

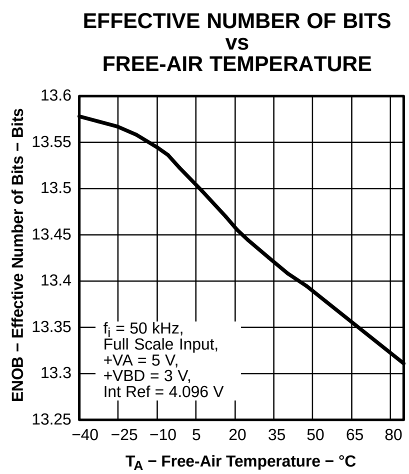


Figure 9.

TYPICAL CHARACTERISTICS (continued)

SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

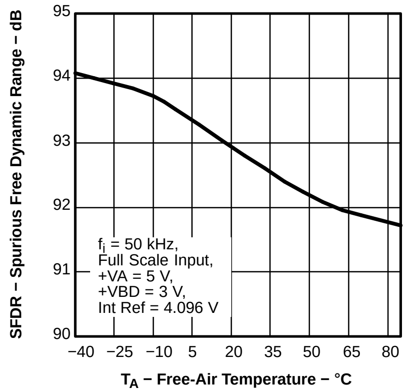


Figure 10.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

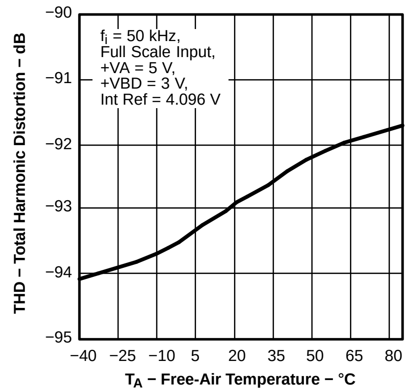


Figure 11.

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

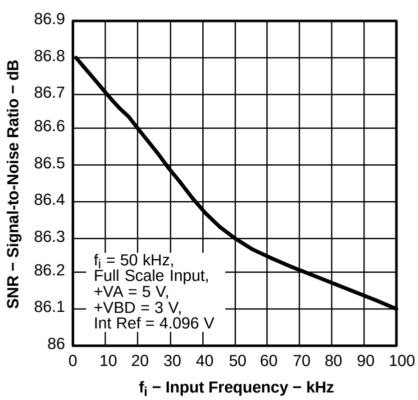


Figure 12.

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

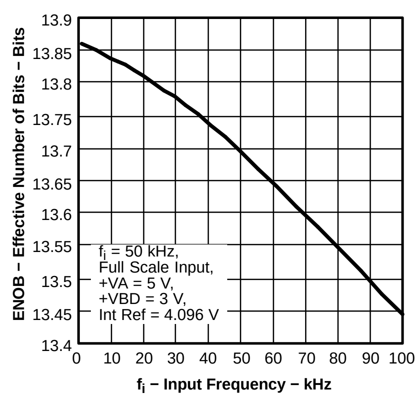


Figure 13.

SIGNAL-TO-NOISE AND DISTORTION vs INPUT FREQUENCY

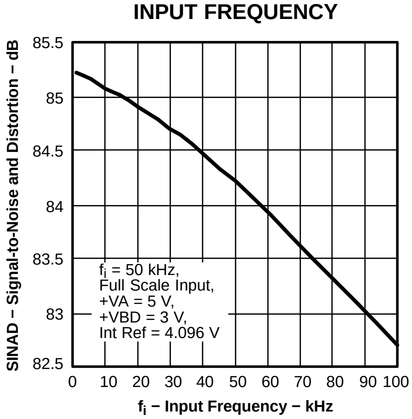


Figure 14.

SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY

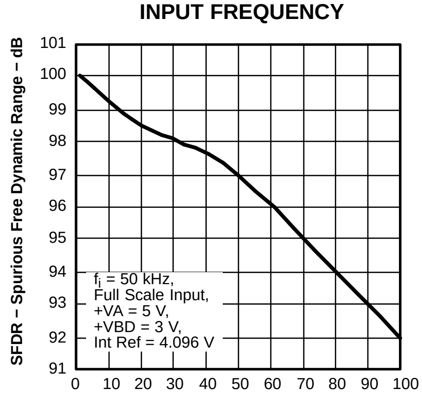


Figure 15.

TYPICAL CHARACTERISTICS (continued)

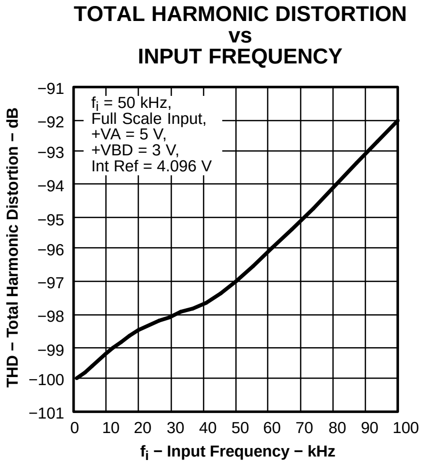


Figure 16.

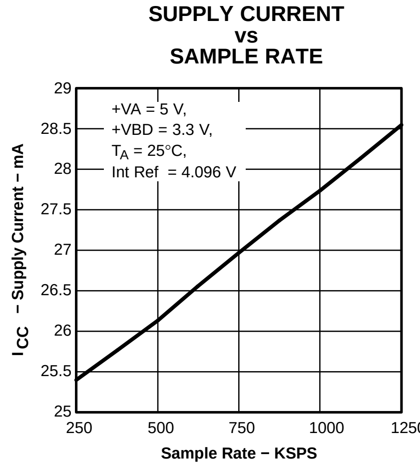


Figure 17.

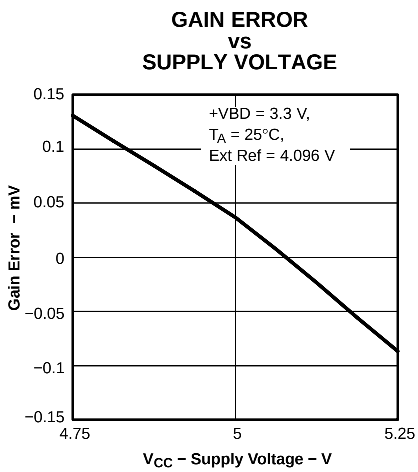


Figure 18.

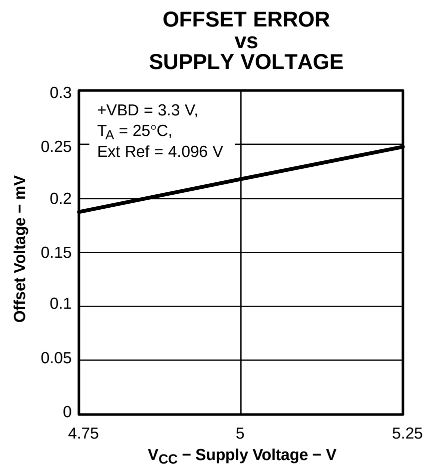


Figure 19.

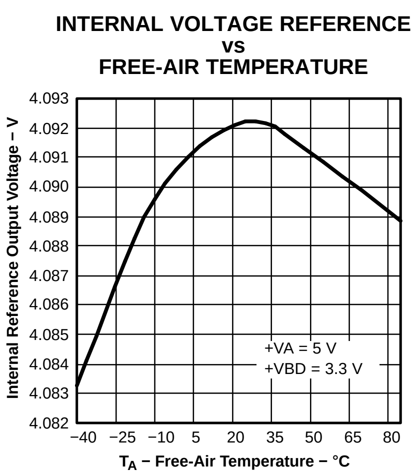


Figure 20.

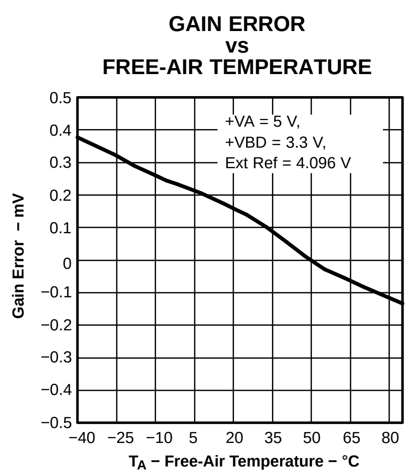


Figure 21.

TYPICAL CHARACTERISTICS (continued)

OFFSET ERROR vs FREE-AIR TEMPERATURE

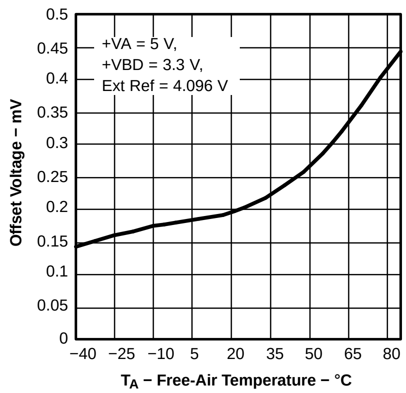


Figure 22.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

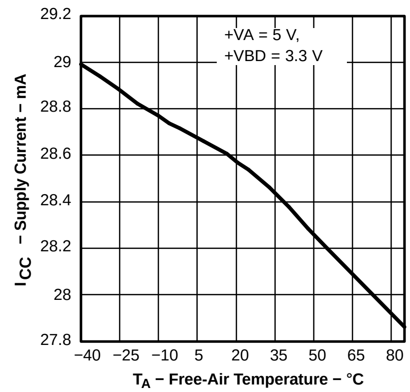


Figure 23.

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

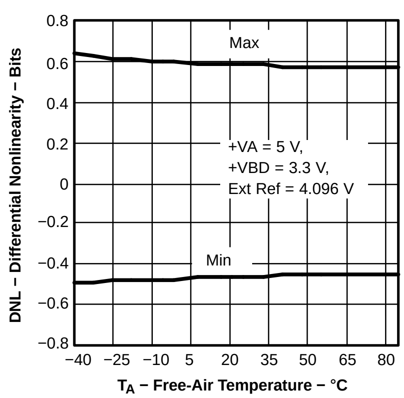


Figure 24.

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

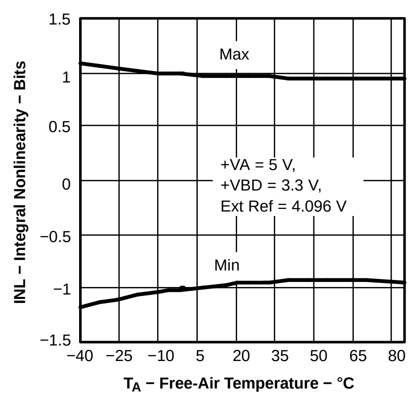


Figure 25.

DIFFERENTIAL NONLINEARITY vs REFERENCE VOLTAGE

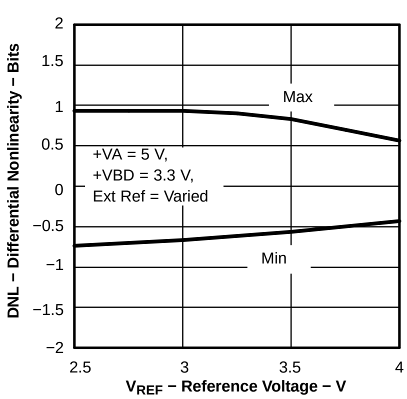


Figure 26.

INTEGRAL NONLINEARITY vs REFERENCE VOLTAGE

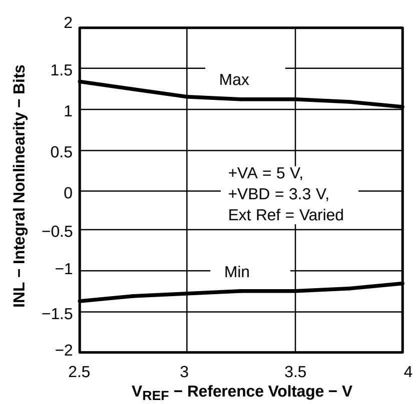


Figure 27.

TYPICAL CHARACTERISTICS (continued)

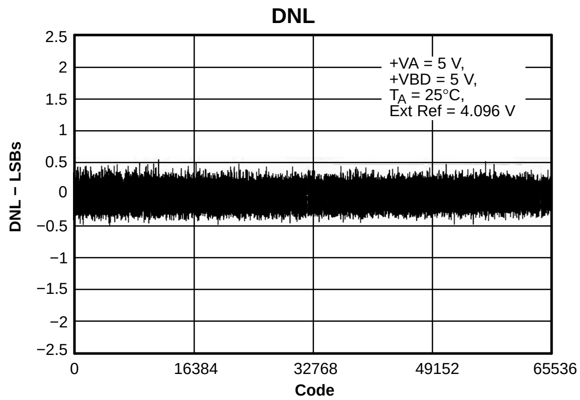


Figure 28.

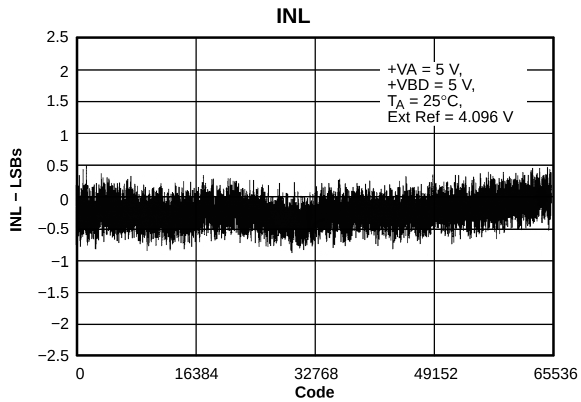


Figure 29.

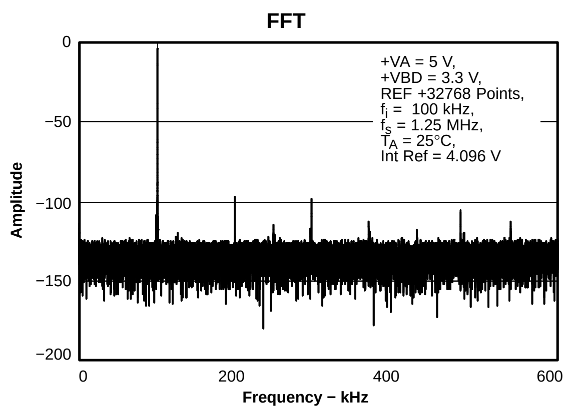


Figure 30.

APPLICATION INFORMATION

MICROCONTROLLER INTERFACING

ADS8405 to 8-Bit Microcontroller Interface

Figure 31 shows a parallel interface between the ADS8405 and a typical microcontroller using the 8-bit data bus. The BUSY signal is used as a falling-edge interrupt to the microcontroller.

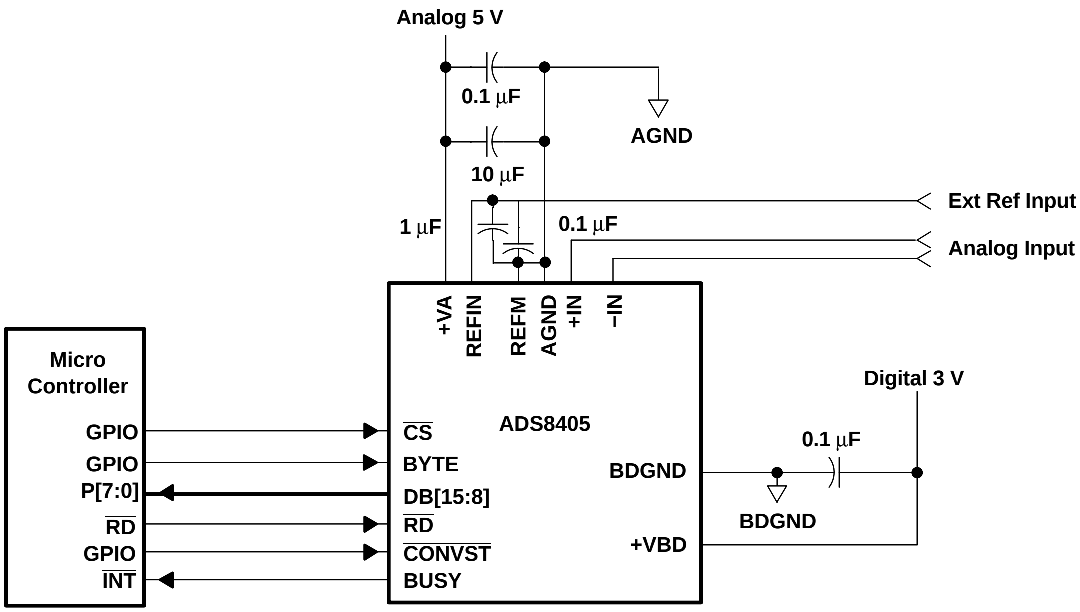


Figure 31. ADS8405 Application Circuitry (Using an External Reference)

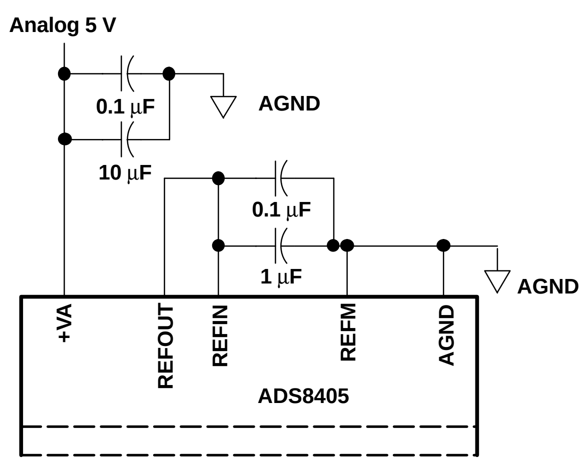


Figure 32. Using the Internal Reference

PRINCIPLES OF OPERATION

The ADS8405 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution, which inherently includes a sample/hold function. See Figure 31 for the application circuit for the ADS8405.

The conversion clock is generated internally. The conversion time of 650 ns is capable of sustaining a 1.25-MHz throughput.

PRINCIPLES OF OPERATION (continued)

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8405 can operate with an external reference with a range from 2.5 V to 4.2 V. A 4.096-V internal reference is included. When an internal reference is used, pin 2 (REFOUT) should be connected to pin 1 (REFIN) with a 0.1-µF decoupling capacitor and a 1-µF storage capacitor between pin 2 (REFOUT) and pins 47 and 48 (REFM) (see Figure 32). The internal reference of the converter is double buffered. If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of the CDAC during conversion. Pin 2 (REFOUT) can be left unconnected (floating) if an external reference is used.

ANALOG INPUT

When the converter enters hold mode, the voltage difference between the +IN and -IN inputs is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.2 V and 0.2 V, allowing the input to reject small signals which are common to both the +IN and –IN inputs. The +IN input has a range of –0.2 V to V_{ref} + 0.2 V. The input span (+IN – (–IN)) is limited to 0 V to V_{ref}.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8405 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25 pF) to an 16-bit settling level within the acquisition time (150 ns) of the device. When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN and –IN inputs and the span (+IN – (–IN)) should be within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used.

Care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this is not observed, the two inputs could have different setting times. This may result in offset error, gain error, and linearity error which varies with temperature and input voltage. A typical input circuit using TI's THS4031 is shown in Figure 33.

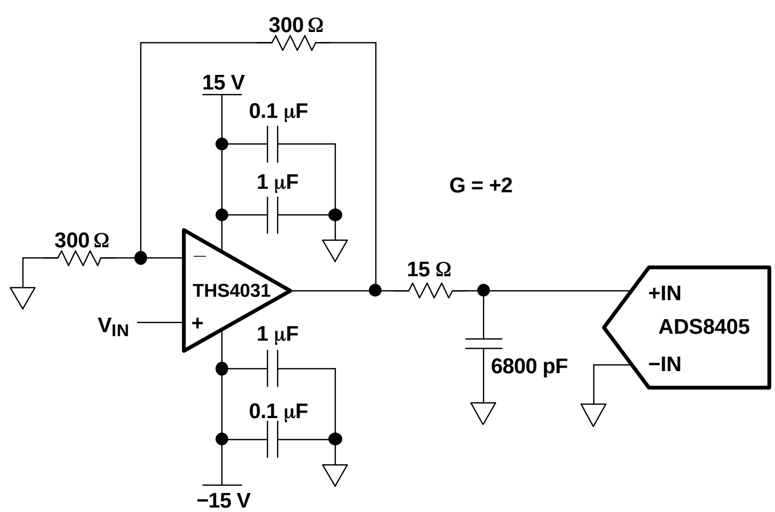


Figure 33. Using the THS4031 with the ADS8405

PRINCIPLES OF OPERATION (continued)

DIGITAL INTERFACE

Timing And Control

See the timing diagrams in the specifications section for detailed information on timing signals and their requirements.

The ADS8405 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 20 ns (after the 20 ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high) while $\overline{\text{CS}}$ is low. The ADS8405 switches from the sample to the hold mode on the falling edge of the $\overline{\text{CONVST}}$ command. A clean and low jitter falling edge of this signal is important to the performance of the converter. The BUSY output is brought high after $\overline{\text{CONVST}}$ goes low. BUSY stays high throughout the conversion process and returns low when the conversion has ended.

Sampling starts as soon as the conversion is over when $\overline{\text{CS}}$ is tied low or starts with the falling edge of $\overline{\text{CS}}$ when BUSY is low.

Both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ can be high during and before a conversion with one exception ($\overline{\text{CS}}$ must be low when $\overline{\text{CONVST}}$ goes low to initiate a conversion). Both the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins are brought low in order to enable the parallel output bus with the conversion.

Reading Data

The ADS8405 outputs full parallel data in straight binary format as shown in Table 1. The parallel output is active when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low. There is a minimal quiet zone requirement around the falling edge of $\overline{\text{CONVST}}$. This is 50 ns prior to the falling edge of $\overline{\text{CONVST}}$ and 40 ns after the falling edge. No data read should be attempted within this zone. Any other combination of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ sets the parallel output to 3-state. BYTE is used for multiword read operations. BYTE is used whenever lower bits of the converter result are output on the higher byte of the bus. Refer to Table 1 for ideal output codes.

Table 1. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
Full scale range	$+V_{ref}$		
Least significant bit (LSB)	$(+V_{ref})/65536$	**BINARY CODE**	**HEX CODE**
Full scale	$(+V_{ref})$ – 1 LSB	1111 1111 1111 1111	FFFF
Midscale	$(+V_{ref})/2$	1000 0000 0000 0000	8000
Midscale – 1 LSB	$(+V_{ref})/2$ – 1 LSB	0111 1111 1111 1111	7FFF
Zero	0 V	0000 0000 0000 0000	0000

The output data is a full 16-bit word (D15 – D0) on the DB15 – DB0 pins (MSB-LSB) if BYTE is low.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB15 – DB8. In this case two reads are necessary: the first as before, leaving BYTE low and reading the 8 most significant bits on pins DB15 – DB8, then bringing BYTE high. When BYTE is high, the low bits (D7 – D0) appear on pins DB15 – D8.

These multiword read operations can be done with multiple active $\overline{\text{RD}}$ (toggling) or with $\overline{\text{RD}}$ tied low for simplicity.

Conversion Data Readout

BYTE	DATA READ OUT	
	DB15–DB8 Pins	**DB7–DB0 Pins**
High	D7–D0	All one's
Low	D15–D8	D7-D0

$\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is an asynchronous active low input signal (that works independently of $\overline{\text{CS}}$). Minimum $\overline{\text{RESET}}$ low time is 25 ns. The current conversion is aborted no later than 50 ns after the converter is in reset mode. In addition, all output latches are cleared (set to zero's) after $\overline{\text{RESET}}$. The converter goes back to normal operation mode no later than 20 ns after the $\overline{\text{RESET}}$ input is brought high.

The converter starts the first sampling period 20 ns after the rising edge of $\overline{\text{RESET}}$. Any sampling period except for the one immediately after a $\overline{\text{RESET}}$ is started with the falling edge of the previous BUSY signal or the falling edge of CS, whichever is later.

Another way to reset the device is through the use of the combination of $\overline{\text{CS}}$ and $\overline{\text{CONVST}}$. This is useful when the dedicated $\overline{\text{RESET}}$ pin is tied to the system reset but there is a need to abort only the conversion in a specific converter. Since the BUSY signal is held high during the conversion, either one of these conditions triggers an internal self-clear reset to the converter just the same as a reset via the dedicated $\overline{\text{RESET}}$ pin. The reset does not have to be cleared as for the dedicated $\overline{\text{RESET}}$ pin. A reset can be started with either of the two following steps.

- Issue a $\overline{\text{CONVST}}$ when $\overline{\text{CS}}$ is low and a conversion is in progress. The falling edge of $\overline{\text{CONVST}}$ must satisfy the timing as specified by the timing parameter $t_{su(AB)}$ specified in the timing characteristics table to ensure a reset. The falling edge of $\overline{\text{CONVST}}$ starts a reset. The timing is the same as a reset using the dedicated $\overline{\text{RESET}}$ pin except the instance of the falling edge is replaced by the falling edge of $\overline{\text{CONVST}}$.
- Issue a $\overline{\text{CS}}$ while a conversion is in progress. The falling edge of $\overline{\text{CS}}$ must satisfy the timing as specified by the timing parameter $t_{su(AB)}$ specified in the timing characteristics table to ensure a reset. The falling edge of $\overline{\text{CS}}$ causes a reset. The timing is the same as a reset using the dedicated $\overline{\text{RESET}}$ pin except the instance of the falling edge is replaced by the falling edge of $\overline{\text{CS}}$.

POWER-ON INITIALIZATION

RESET is not required after power on. An internal power-on reset circuit generates the reset. To ensure that all of the registers are cleared, the three conversion cycles must be given to the converter after power on.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8405 circuitry.

As the ADS8405 offers single-supply operation, it is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are at least n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8405 draws very little current from an external reference, as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1-µF bypass capacitor and a 1-µF storage capacitor are recommended from pin 1 (REFIN) directly to pin 48 (REFM). REFM and AGND should be shorted on the same ground plane under the device.

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8405 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. See Table 2 for the placement of the capacitor. In addition, a 1-µF to 10-µF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

Table 2. Power Supply Decoupling Capacitor Placement

POWER SUPPLY PLANE SUPPLY PINS	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE
Pin pairs that require shortest path to decoupling capacitors	(4,5), (8,9), (10,11), (13,15), (43,44), (45,46)	(24,25), (34, 35)
Pins that require no decoupling	12, 14	37

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8405IBPFBR	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8405I B	Samples
ADS8405IBPFBT	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8405I B	Samples
ADS8405IBPFBTG4	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8405I B	Samples
ADS8405IPFBR	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8405I	Samples
ADS8405IPFBT	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8405I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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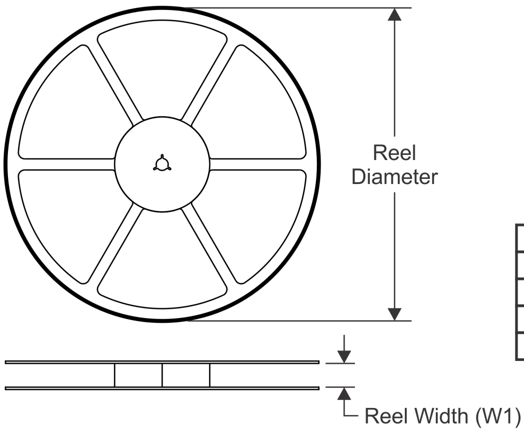
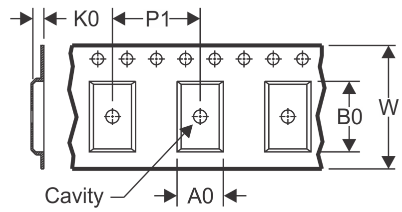
TAPE AND REEL INFORMATION

REEL DIMENSIONS

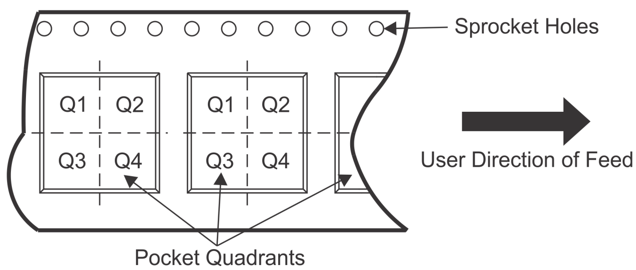


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

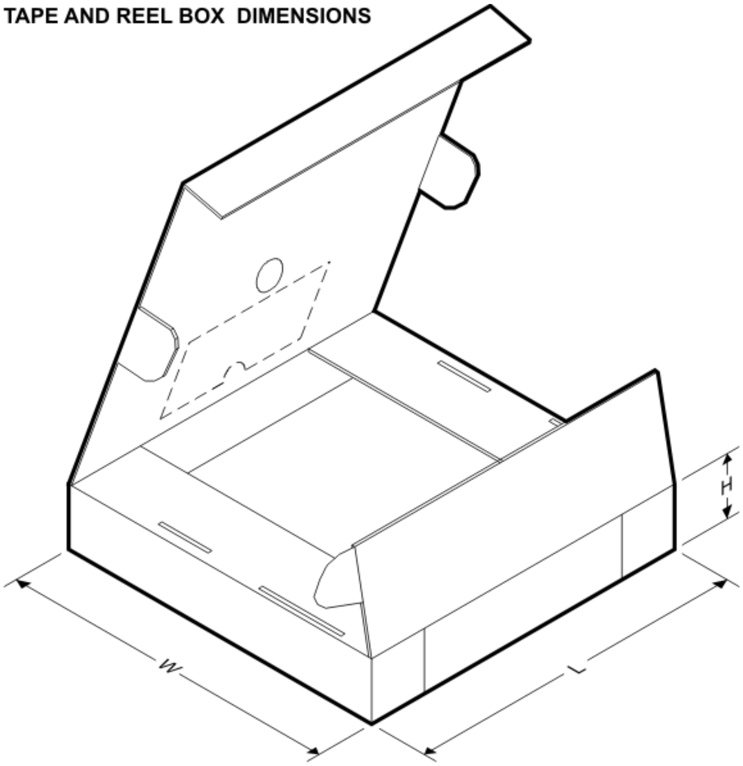
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8405IBPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS8405IBPFBT	TQFP	PFB	48	250	180.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS8405IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS8405IPFBT	TQFP	PFB	48	250	180.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

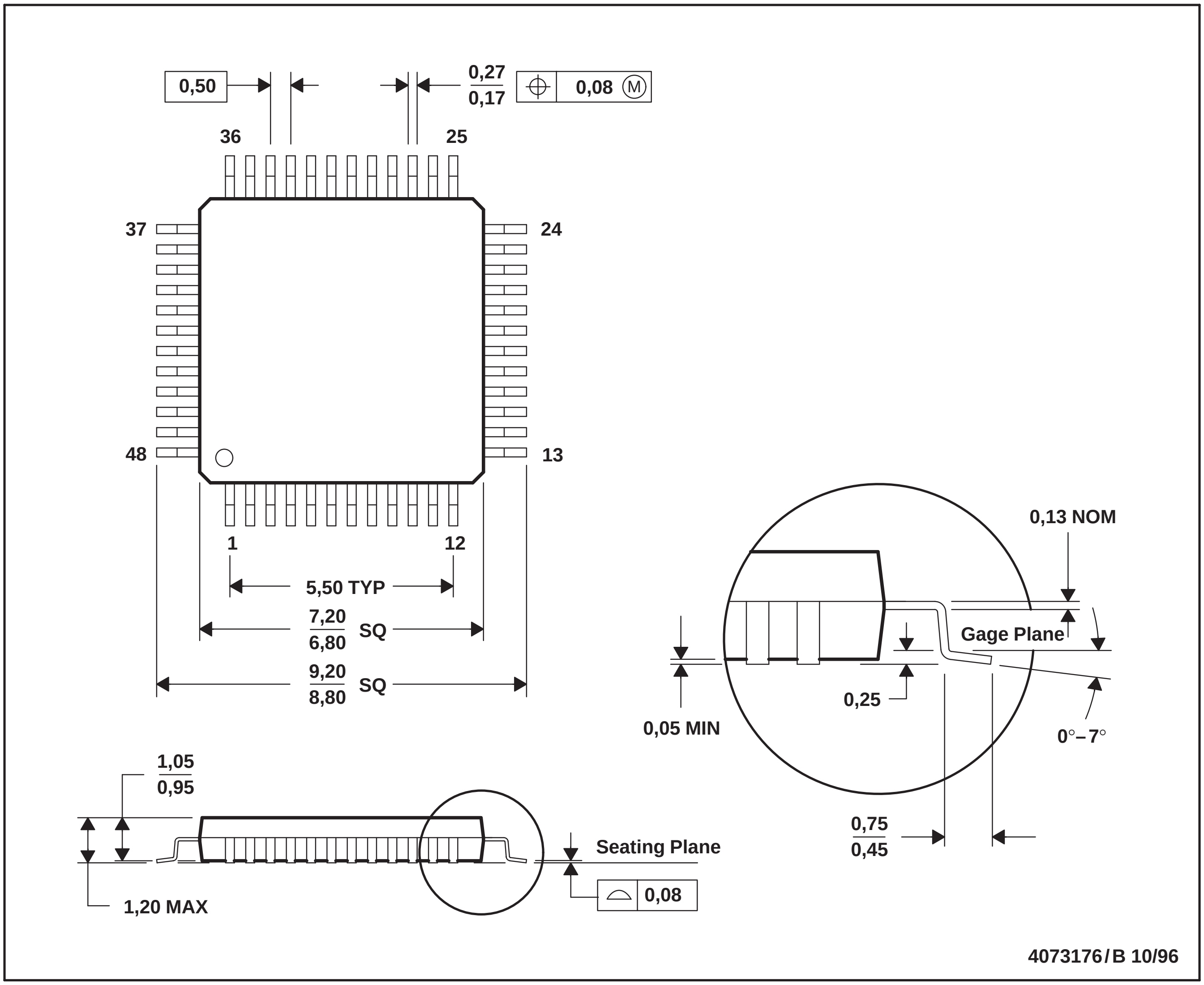
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

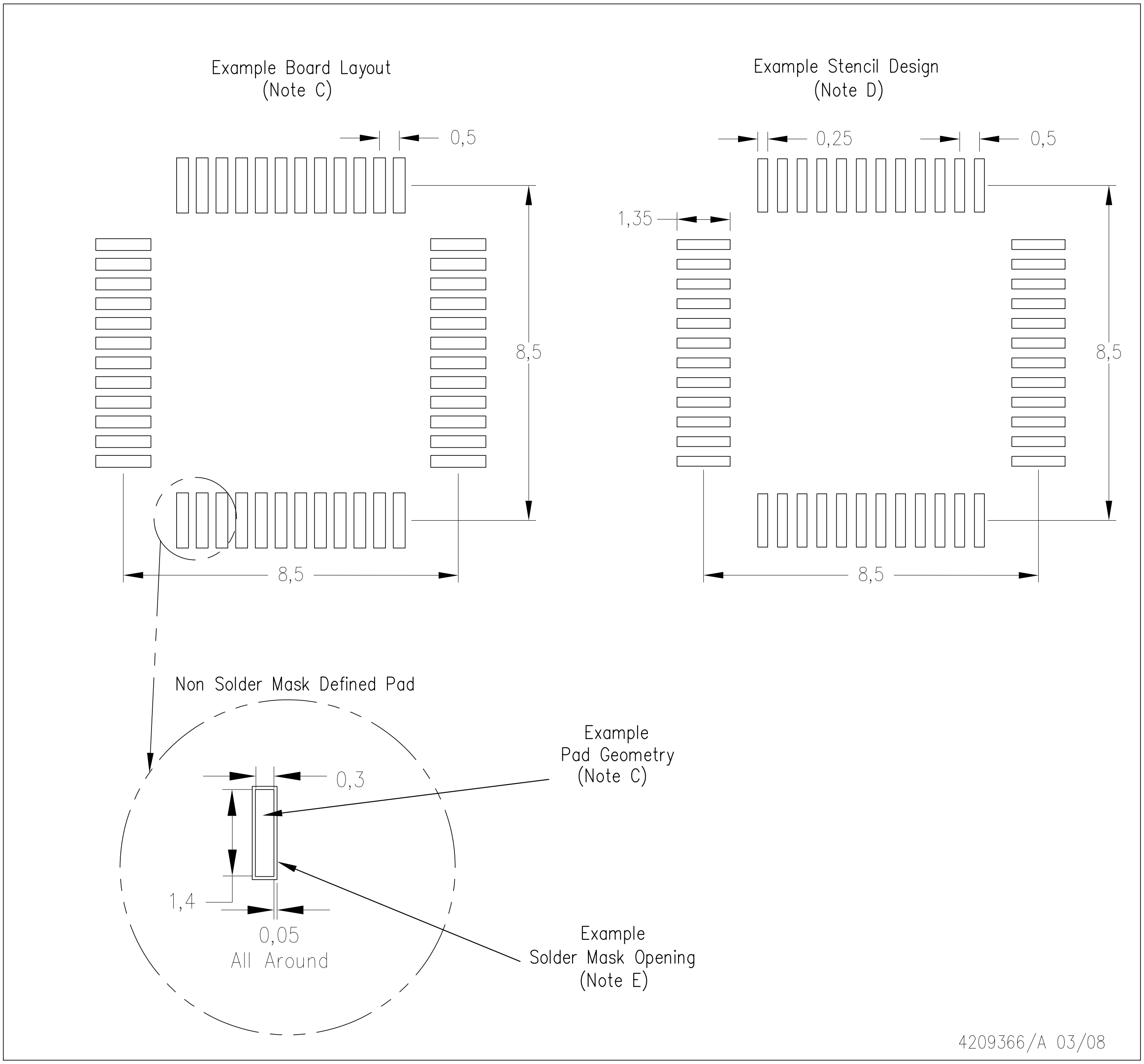
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8405IBPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
ADS8405IBPFBT	TQFP	PFB	48	250	213.0	191.0	55.0
ADS8405IPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
ADS8405IPFBT	TQFP	PFB	48	250	213.0	191.0	55.0

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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