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FDS6961A

Dual N-Channel Logic Level PowerTrench™ MOSFET

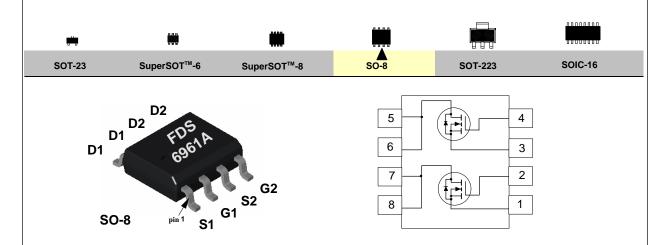
General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- Fast switching speed.
- Low gate charge (2.1nC typical).
- High performance trench technology for extremely low R_{DS/ONI}.
- High power and current handling capability.



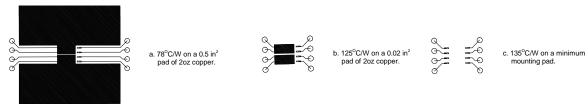
Absolute Maximum Ratings T_A = 25°C unless other wise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	±20	V
l _D	Drain Current - Continuous (Note 1a)	3.5	A
	- Pulsed	14	
P_{D}	Power Dissipation for Single Operation (Note 1)	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
Γ_{J} , T_{STG}	Operating and Storage Temperature Range	-55 to 150	℃
THERMA	L CHARACTERISTICS		
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R _{euc}	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHAR	ACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	$I_D = 250 \mu\text{A}$, Referenced to	25 °C		25		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, \ V_{GS} = 0 \text{ V}$				1	μΑ
			$T_J = 55^{\circ}C$			10	μA
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	l.			100	nA
GSSR	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
	CTERISTICS (Note 2)				II.		
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1	1.8	3	V
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C			-5		mV/°C
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 3.5 \text{ A}$			0.076	0.09	Ω
-(-)			T _. =125°C		0.11	0.155	
		$V_{GS} = 4.5 \text{ V}, I_D = 2.8 \text{ A}$	<u> </u>		0.107	0.14	
I _{D(ON)}	On-State Drain Current	$V_{GS} = 10 \text{ V}, \ V_{DS} = 5 \text{ V}$		14			Α
g _{FS}	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_{D} = 3.5 \text{ A}$			6		S
DYNAMIC C	HARACTERISTICS	•				•	•
C _{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz			220		pF
Coss	Output Capacitance				50		pF
C _{rss}	Reverse Transfer Capacitance				20		pF
SWITCHING	CHARACTERISTICS (Note 2)	T-					
t _{D(on)}	Turn - On Delay Time	$V_{DS} = 15 \text{ V}, I_{D} = 1 \text{ A}$			3	6	ns
t _r	Turn - On Rise Time	$V_{GS} = 10 \text{ V}$, $R_{GEN} = 6 \Omega$			11	22	ns
t _{D(off)}	Turn - Off Delay Time				7	14	ns
t _f	Turn - Off Fall Time				3	6	ns
Q_g	Total Gate Charge	$V_{DS} = 15 \text{ V}, I_{D} = 3.5 \text{ A},$			2.1	4	nC
Q_{gs}	Gate-Source Charge	V _{GS} =5 V			0.8		nC
Q_{gd}	Gate-Drain Charge				0.7		nC
DRAIN-SOUI	RCE DIODE CHARACTERISTICS AND MAXIM	UM RATINGS					
l _s	Maximum Continuous Drain-Source Diode Fo	orward Current				1.3	Α
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 1.3 \text{ A} \text{ (Note 2)}$			0.73	1.2	V

Notes:

^{1.} R_{QLA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{QLC} is guaranteed by design while R_{QCA} is determined by the user's board design.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics

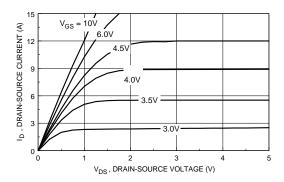


Figure 1. On-Region Characteristics.

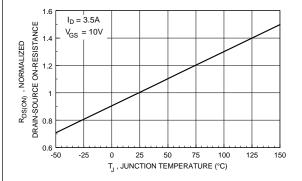


Figure 3. On-Resistance Variation with Temperature.

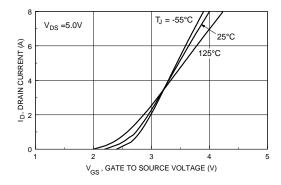


Figure 5. Transfer Characteristics.

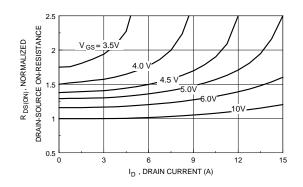


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

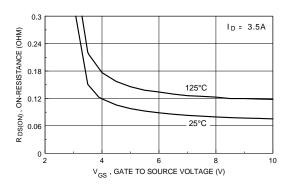


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

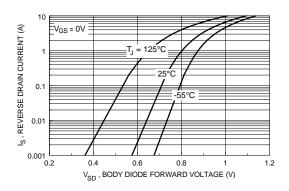
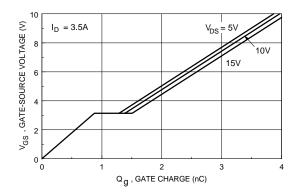


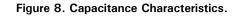
Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

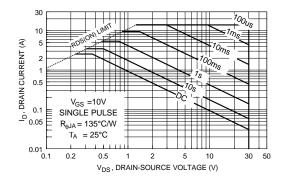
Typical Electrical Characteristics



500 200 200 100 50 20 Tell MHz V_{GS} = 0 V 10,1 0.2 0.5 1 2 5 10 30 V_{DS}, DRAIN TO SOURCE VOLTAGE (V)

Figure 7. Gate Charge Characteristics.





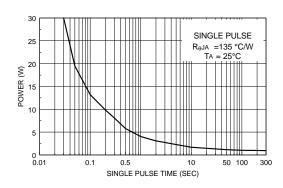


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

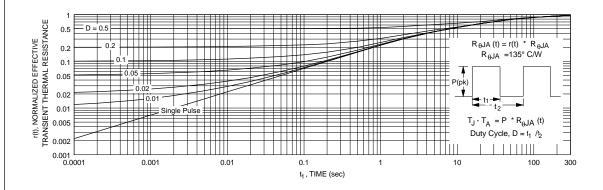


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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 E^2CMOS^{TM} PowerTrenchTM

FACT™ QFET™ FACT Quiet Series™ QS™

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