- **Load Clocks and Unload Clocks Can Be Asynchronous or Coincident**
- **2048 Words by 9 Bits**
- **Low-Power Advanced CMOS Technology**
- **Fast Access Times of 15 ns With a 50-pF Load**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Expansion Logic for Depth Cascading**
- **Empty, Full, and Half-Full Flags**
- **Fall-Through Time of 20 ns Typical**
- **Data Rates up to 50 MHz**
- **3-State Outputs**
- **Package Options Include 44-Pin Plastic Leaded Chip Carrier (FN), 64-Pin Thin Quad Flat (PM), and Reduced-Height 64-Pin Quad Flat (PAG) Packages**

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7808 is a 2048-word by 9-bit FIFO designed for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load-clock (LDCK) input and is read out on a low-to-high transition at the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 2048. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 1024 or more words and is low when it contains 1023 or fewer words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset can be used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{\text{PEN}}$) is low. The AF/AE flag is high when the FIFO contains X or fewer words or (2048 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (2047 – Y) words.

A low level on the reset ($\overline{\text{RESET}}$) input resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, AF/AE high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level.

The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable (OE) input is low. OE does not affect the output flags.

Cascading is easily accomplished in the word-width and word-depth directions. When not using the FIFO in depth expansion, cascade enable ($\overline{\text{CASEN}}$) must be tied high.

The FIFO must be reset upon power up.

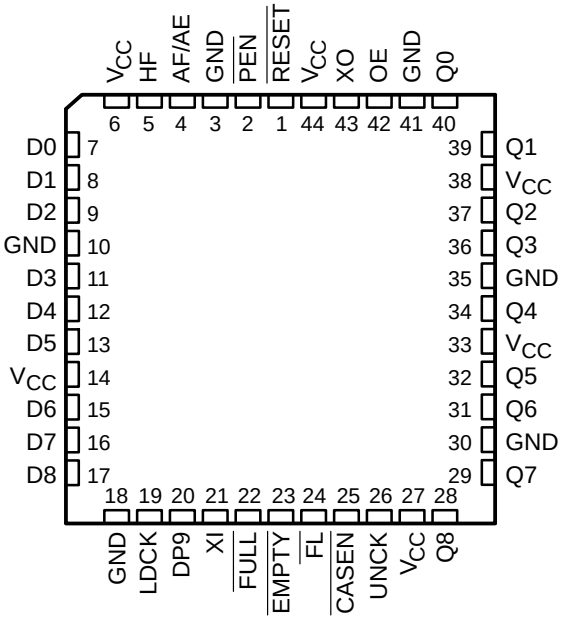
The SN74ACT7808 is characterized for operation from 0°C to 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

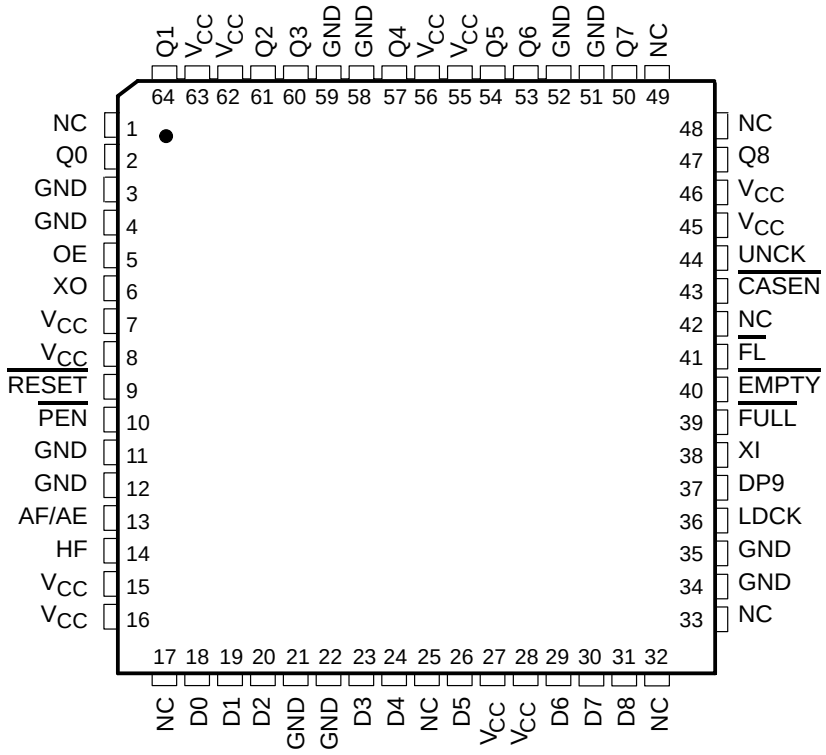
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2001, Texas Instruments Incorporated

FN PACKAGE
(TOP VIEW)

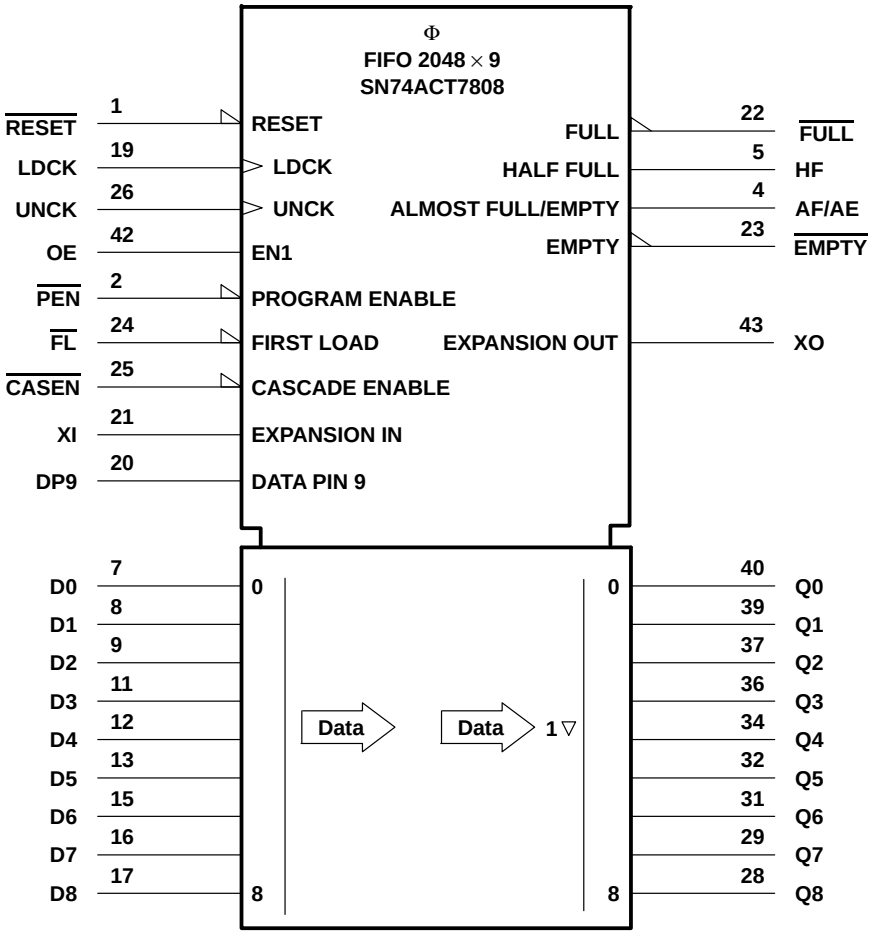


PAG OR PM PACKAGE
(TOP VIEW)



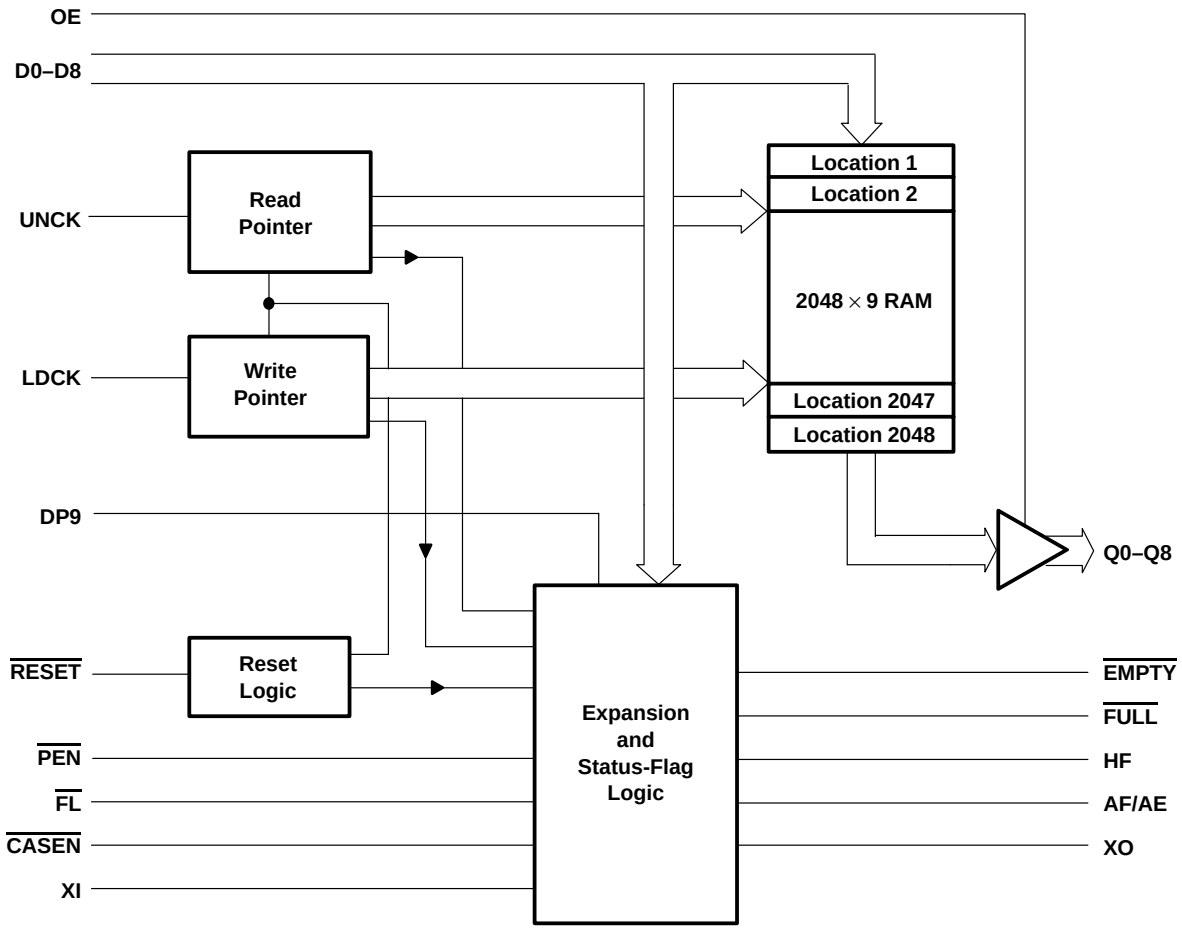
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
AF/AE	O	Almost-full/almost-empty flag. Depth-offset values can be programmed for AF/AE or the default value of 256 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or fewer words or (2048 – Y) or more words. AF/AE is high after reset.
$\overline{\text{CASEN}}$†	I	Cascade enable. When multiple SN74ACT7808 devices are depth cascaded, every device must have $\overline{\text{CASEN}}$ tied low. $\overline{\text{CASEN}}$ must be tied high when a device is not used in depth expansion.
D0–D8	I	Nine-bit data input port
DP9	I	DP9 is used as the most significant bit when programming the AF/AE offset values.
$\overline{\text{EMPTY}}$	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO memory is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FL}}$†	I	First load. When multiple SN74ACT7808 devices are depth cascaded, the first device in the chain must have its $\overline{\text{FL}}$ input tied low and all other devices must have their $\overline{\text{FL}}$ inputs tied high.
$\overline{\text{FULL}}$	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	O	Half-full flag. HF is high when the FIFO memory contains 1024 or more words. HF is low after reset.
LDCK	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
OE	I	Output enable. When OE is low, D0–D8 are in the high-impedance state.
$\overline{\text{PEN}}$	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D8 and DP9 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and LDCK is high.
Q0–Q8	O	Nine-bit data output port
$\overline{\text{RESET}}$	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives $\overline{\text{FULL}}$ and AF/AE high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.
XI†	I	Expansion input (XI) and expansion output (XO). When multiple SN74ACT7808 devices are depth cascaded, the XO of one device must be connected to the XI of the next device in the chain. The XO of the last device in the chain is connected to the XI of the first device in the chain.
XO†	O	

† See Figures 6 and 7 for application information on FIFO word-width and word-depth expansions, respectively.

offset values for AF/AE

The AF/AE flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 256 are used. The AF/AE flag is high when the FIFO contains X or fewer words or (2048 – Y) or more words.

To program the offset values, program enable ($\overline{PEN}$) can be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D8 and DP9 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D8 and DP9 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 1023 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 256, $\overline{PEN}$ must be held high.

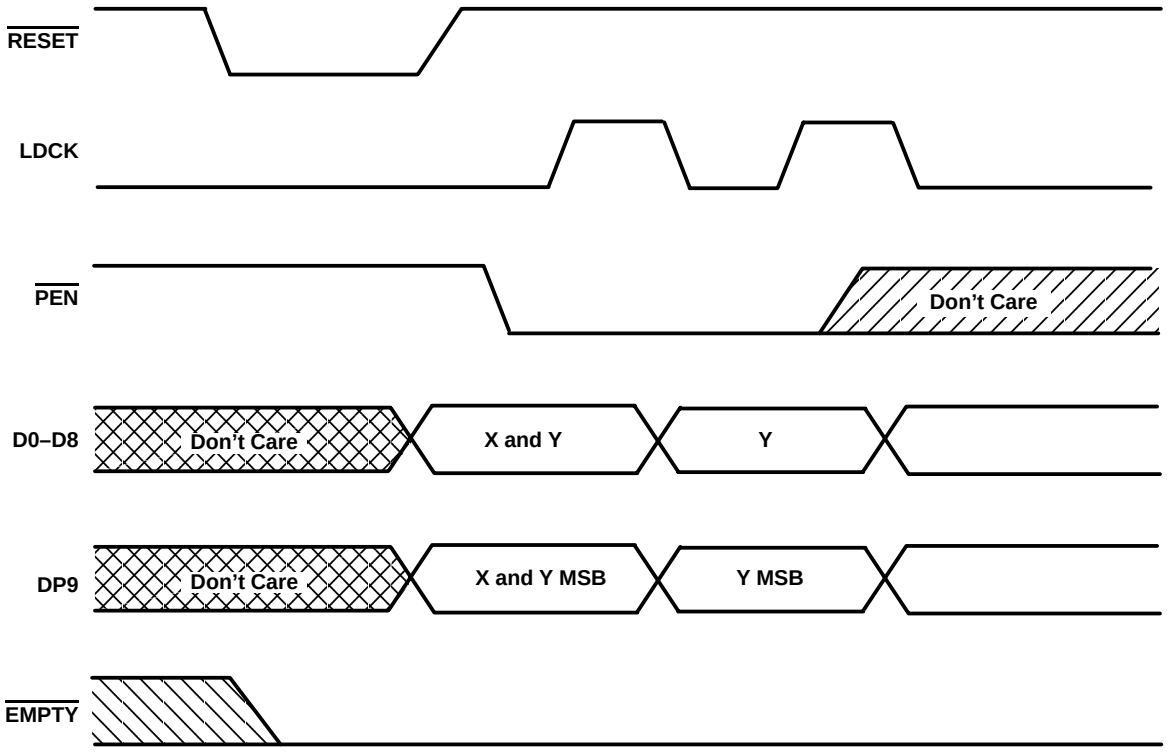


Figure 1. Programming X and Y Separately

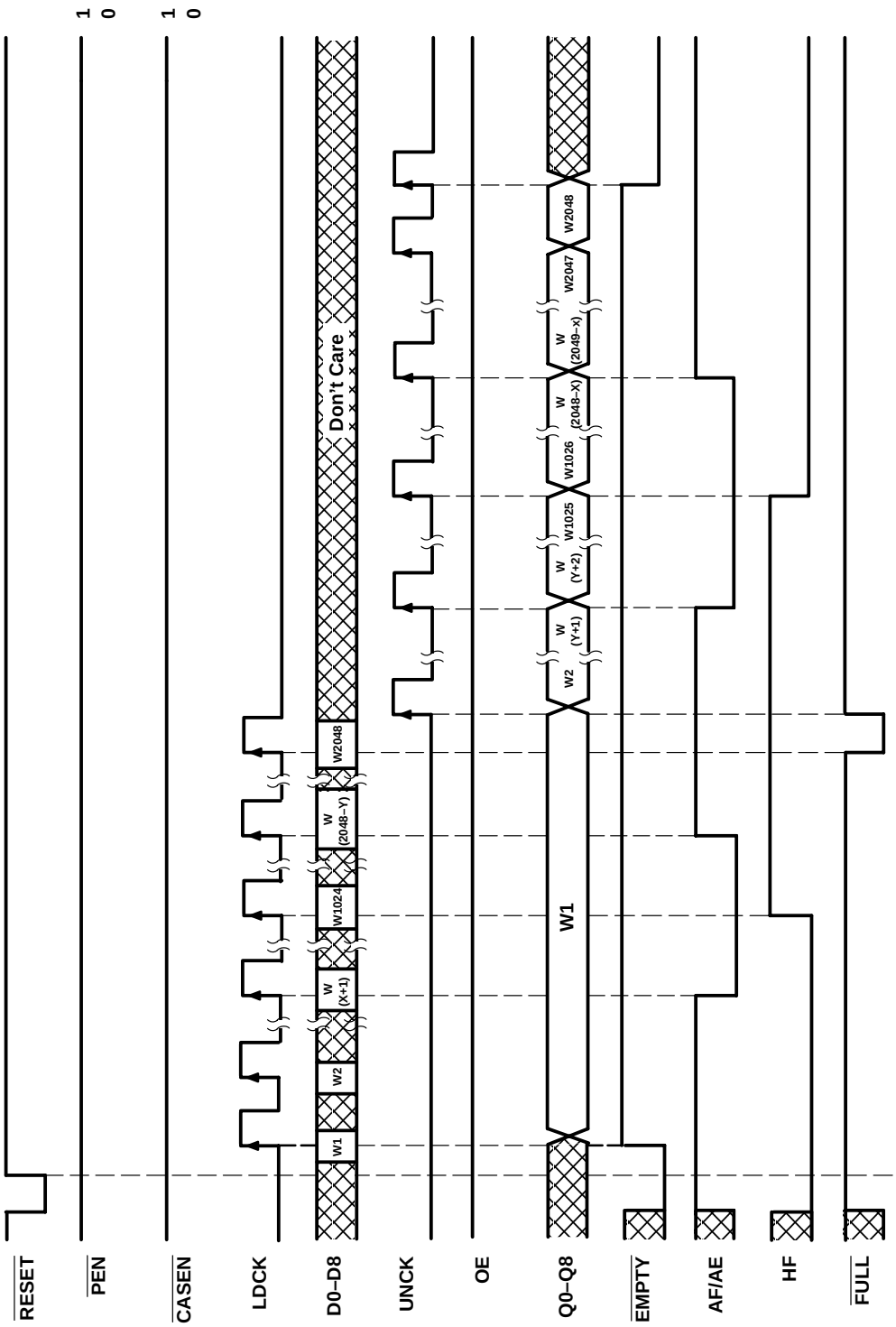


Figure 2. Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Voltage range applied to a disabled 3-state output . . . . . –0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): FN package . . . . . 46°C/W
PAG package . . . . . 58°C/W
PM package . . . . . 67°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			’ACT7808-20		’ACT7808-25		’ACT7808-30		’ACT7808-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	XI	3.85		3.85		3.85		3.85		V
		Other inputs	2		2		2		2		
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current			–8		–8		–8		–8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –8 mA	2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0			±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0			±5	µA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0			400	µA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V, Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz		4		pF
C_o		V_O = 0,	f = 1 MHz		8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the increase in supply current for each input, excluding XI, that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.

timing requirements over recommended operating conditions (unless otherwise noted) (see Figures 1 through 3)

			’ACT7808-20		’ACT7808-25		’ACT7808-30		’ACT7808-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			50		40		33.3		25	MHz
t_w	Pulse duration	LDCK high or low	8		9		11		13		ns
		UNCK high or low	8		9		11		13		
		$\overline{PEN}$ low	9		9		11		13		
		$\overline{RESET}$ low	10		13		16		19		
t_{su}	Setup time	D0–D8, DP9 before LDCK↑	5		5		5		5		ns
		LDCK inactive before $\overline{RESET}$ high	5		5		5		5		
		$\overline{PEN}$ before LDCK↑	5		5		5		5		
t_h	Hold time	D0–D8, DP9 after LDCK↑	0		0		0		0		ns
		LDCK inactive after $\overline{RESET}$ high	5		5		5		5		
		$\overline{PEN}$ low after LDCK↑	4		4		4		4		
		$\overline{PEN}$ high after LDCK low	0		0		0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 3)

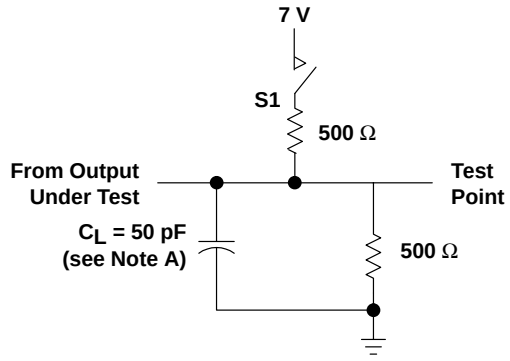
PARAMETER	FROM (INPUT)	TO (OUTPUT)	’ACT7808-20			’ACT7808-25		’ACT7808-30		’ACT7808-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		50			40		33.3		25		MHz
t_{pd}	LDCK↑	Any Q	5		20	5	22	5	25	5	28	ns
	UNCK↑		4.5	11	15	4.5	18	4.5	20	4.5	22	
t_{pd}‡	UNCK↑	Any Q		10								ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$	4		15	4	17	4	19	4	21	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$	2		15	2	17	2	19	2	21	ns
	$\overline{RESET}$ low		2		16	2	18	2	20	2	22	
	LDCK↑	$\overline{FULL}$	4		15	4	17	4	19	4	21	
t_{PLH}	UNCK↑	$\overline{FULL}$	4		14	4	16	4	18	4	20	ns
	$\overline{RESET}$ low		2		18	2	20	2	22	2	24	
t_{pd}	LDCK↑	AF/AE	2		16	2	18	2	20	2	22	ns
	UNCK↑		2		16	2	18	2	20	2	22	
t_{PLH}	$\overline{RESET}$ low	AF/AE	0		10	0	12	0	14	0	16	ns
	LDCK↑	HF	2		19	2	21	2	23	2	25	
t_{PHL}	UNCK↑	HF	2		16	2	18	2	20	2	22	ns
	$\overline{RESET}$ low		2		12	2	14	2	16	2	18	
t_{PLH}	UNCK↑	XO	2		11	2	13	2	15	2	17	ns
t_{PHL}	LDCK↑	XO	2		11	2	13	2	15	2	17	ns
t_{en}	OE	Any Q	1		10	1	12	1	14	1	16	ns
t_{dis}	OE	Any Q	1		9	1	11	1	13	1	15	ns
t_{en}	XI high	Any Q	3		13	3	15	3	17	3	19	ns
t_{dis}	XO high	Any Q			4		4		4		4	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is measured with C_L = 30 pF (see Figure 4).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

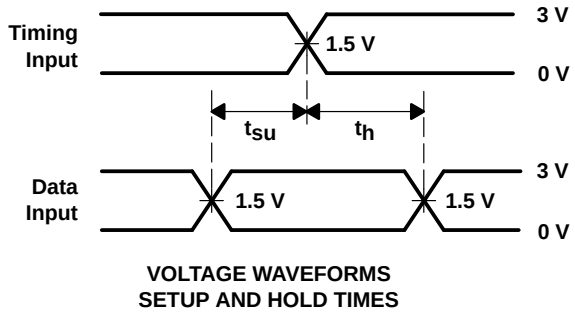
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF,	f = 5 MHz	91	pF

PARAMETER MEASUREMENT INFORMATION

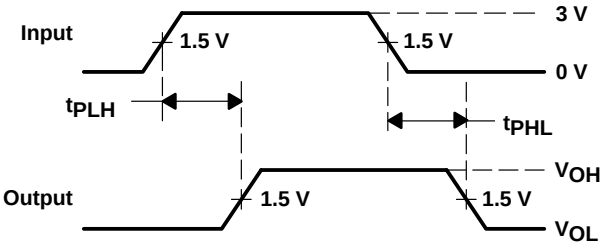


LOAD CIRCUIT

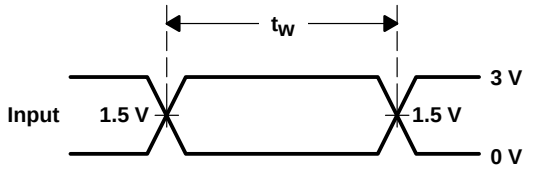
PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open



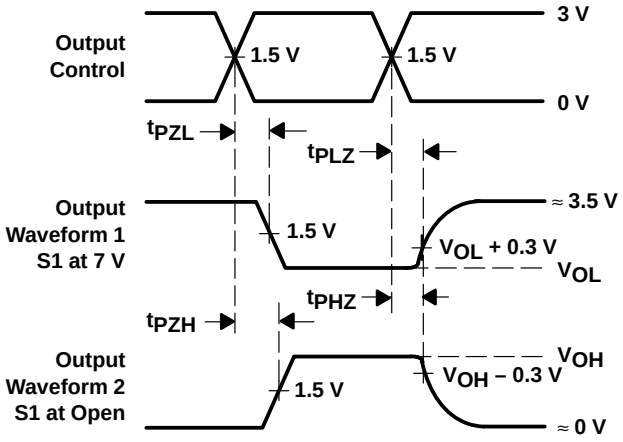
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

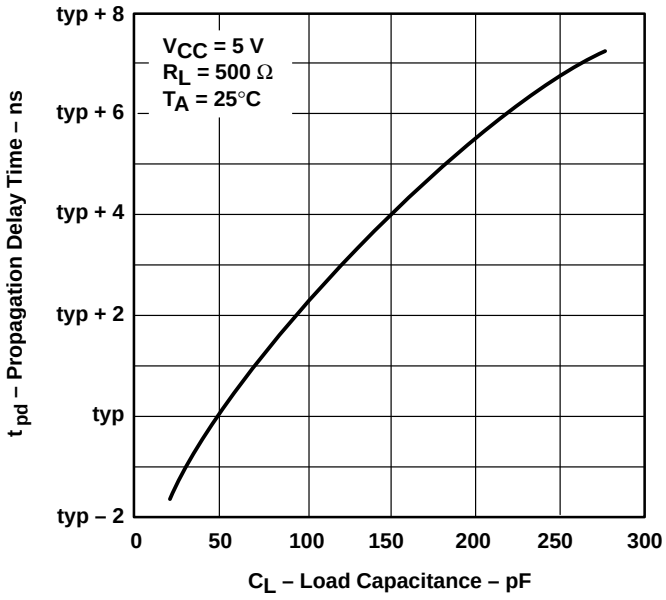


Figure 4

SUPPLY CURRENT vs CLOCK FREQUENCY

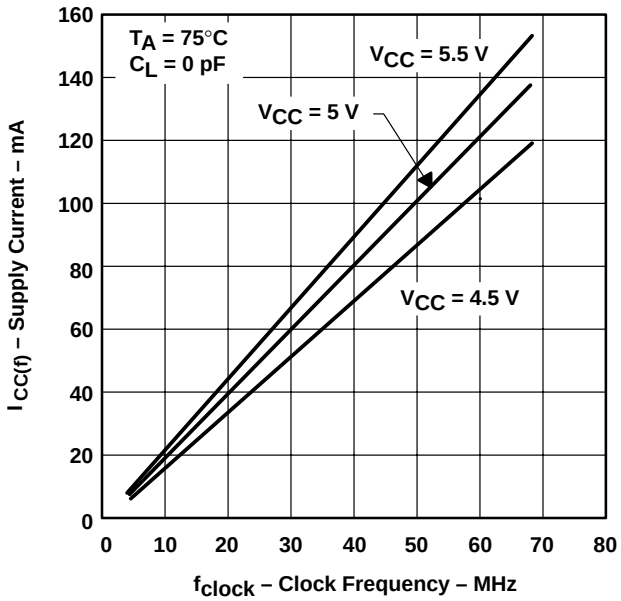


Figure 5

APPLICATION INFORMATION

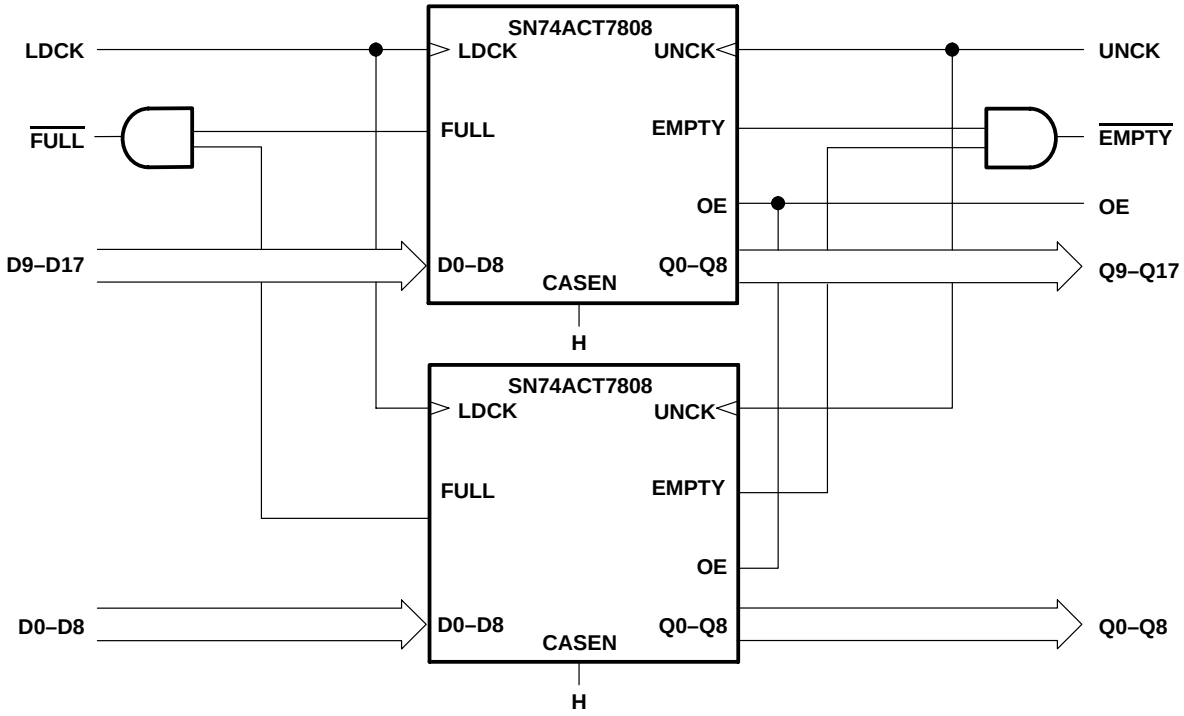


Figure 6. Word-Width Expansion: 2048 × 18 Bits

APPLICATION INFORMATION

depth cascading (see Figure 7)

The SN74ACT7808 provides expansion logic necessary for cascading an unlimited number of the FIFOs in depth. $\overline{\text{CASEN}}$ must be low on all FIFOs used in depth expansion. $\overline{\text{FL}}$ must be tied low on the first FIFO in the chain; all others must have $\overline{\text{FL}}$ tied high. The expansion-out (XO) output of a FIFO must be tied to the expansion-in (XI) input of the next FIFO in the chain. The XO output of the last FIFO is tied to the XI input of the first FIFO to complete the loop. Data buses are common to each FIFO in the chain. A composite $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ signal must be generated to indicate boundary conditions.

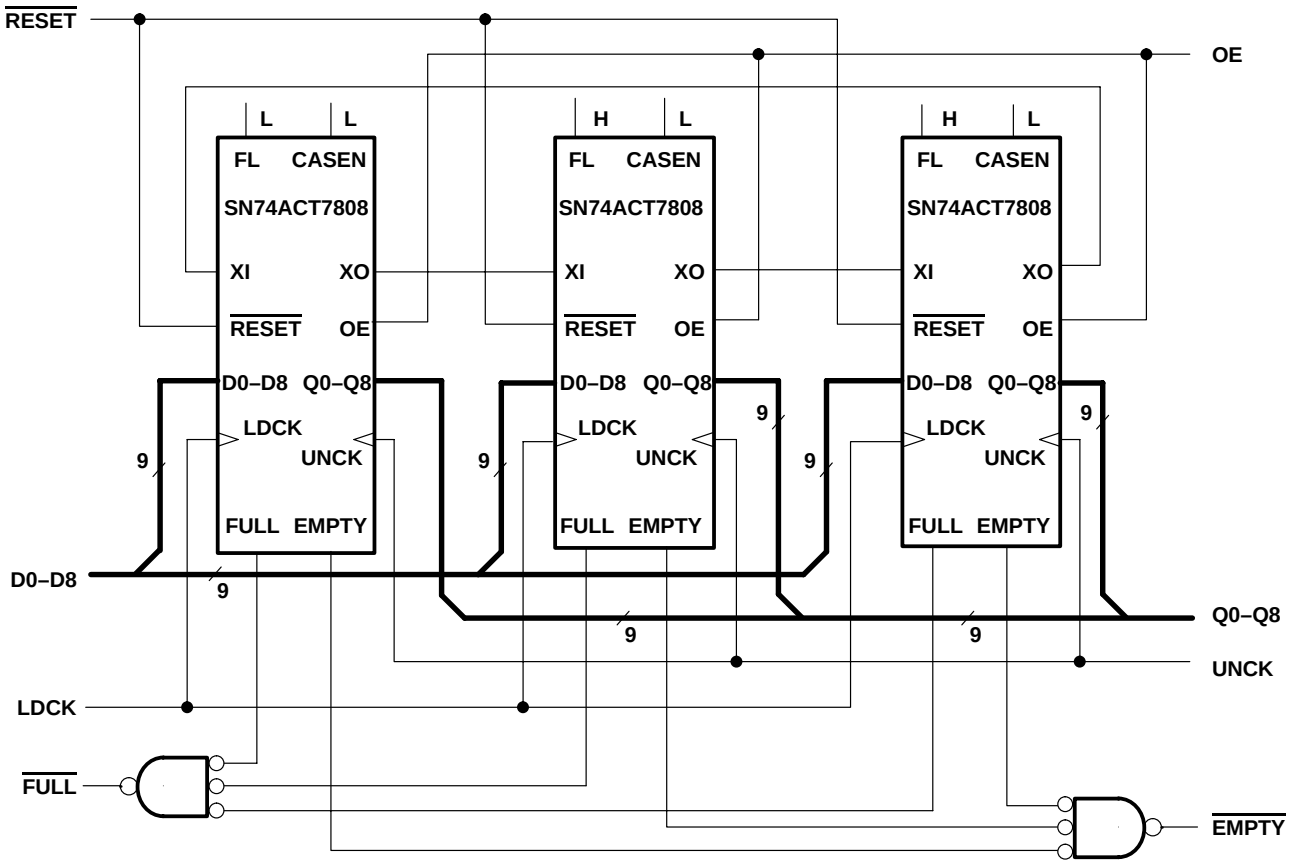


Figure 7. Depth Cascading to Form a 6K × 9 FIFO

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2001, Texas Instruments Incorporated