LM2936 Ultra-Low Quiescent Current LDO Voltage Regulator

1 Features

- LM2936 Operating V_{IN} range of 5.5 V to 40 V
- LM2936HV Operating V_{IN} range of 5.5 V to 60 V
- Ultra Low Quiescent Current (I_Q ≤ 15 µA for I_{OUT} = 100 µA)
- Fixed 3-V, 3.3-V or 5-V with 50-mA Output
- ±2% Initial Output Tolerance
- ±3% Output Tolerance Over Line, Load, and Temperature
- Dropout Voltage Typically 200 mV at I_{OUT} = 50 mA
- –24-V Input Voltage Protection
- –50-V Input Transient Protection
- Internal Short Circuit Current Limit
- Internal Thermal Shutdown Protection
- Shutdown Pin Available with LM2936BM Package

2 Applications

- Automotive
- Industrial Controls
- Point of Load

3 Description

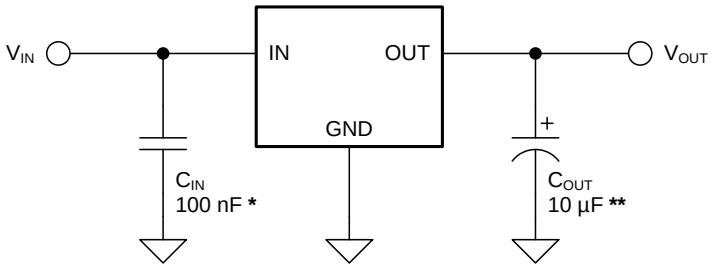
The LM2936 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 15-µA quiescent current at a 100-µA load, the LM2936 is ideally suited for automotive and other battery operated systems. The LM2936 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM2936 has a 40-V maximum operating voltage limit, a −40°C to 125°C operating temperature range, and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range. The LM2936 is available in a TO-92 through-hole package, as well as SOIC-8, VSSOP, SOT–223, and TO-252 surface mount packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2936	SOIC (8)	4.90 mm x 3.91 mm
	TO-252 (3)	6.10 mm x 6.58 mm
	VSSOP (8)	3.00 mm x 3.00 mm
	SOT-223 (4)	6.50 mm x 3.50 mm
	TO-92 (3)	4.30 mm x 4.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



* Required if regulator is located more than 2″ from power supply filter capacitor.
** Required for stability. See *Electrical Characteristics for 3-V LM2936* for required values. Must be rated over intended operating temperature range. Effective series resistance (ESR) is critical, see *Typical Characteristics*. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (March 2013) to Revision O — **Page**

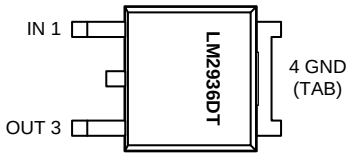
- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision M (March 2013) to Revision N — **Page**

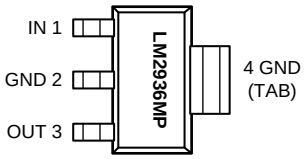
- Changed layout of National Data Sheet to TI format ... 13

5 Pin Configuration and Functions

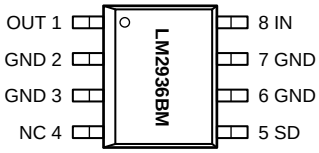
LM2936DT TO-252 (NDP) Package
3-Pins
Top View



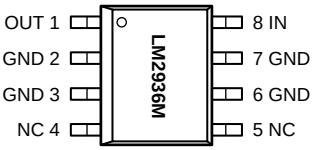
LM2936MP SOT-223 (DCY) Package
4-Pins
Top View



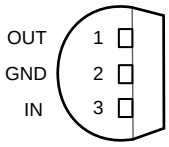
LM2936BM SOIC (D) Package
8-Pins
Top View



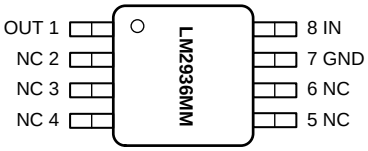
LM2936M SOIC (D) Package
8-Pins
Top View



LM2936Z TO-92 (LP) Package
3-Pins
Bottom View



LM2936MM VSSOP (DGK) Package
8-Pins
Top View



Pin Functions

PIN							I/O	DESCRIPTION
NAME	D (LM2936BM)	D (LM2936M)	NDP	DGK	DCY	LP		
IN	8	8	1	8	1	3	I	Unregulated input voltage.
GND	2, 3, 6, 7	2, 3, 6, 7	4	7	2, 4	2	—	Ground.
OUT	1	1	3	1	3	1	O	Regulated output voltage. Requires a minimum output capacitance, with specific ESR, on this pin to maintain stability.
SD	5	—	—	—	—	—	I	Shutdown. LM2936BM only. Pull this pin HIGH (> 2 V) to turn the output OFF. If this pin is left open, pull ed low (< 0.6 V), or connected to GND, the output will be ON by default. Avoid having any voltage between 0.6 V and 2 V on this pin as the output status may not be predicable across the operating range.
NC	4	4, 5	—	2, 3, 4, 5, 6	—	—	—	No internal connection, Connect to GND, or leave open.

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)

	MIN	MAX	UNIT
Input voltage (survival)	−50	60	V
Power dissipation (3)	Internally limited		
Junction temperature (T_{JMAX})		150	°C
Storage temperature, T_{stg}	−65	150	

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. If this dissipation is exceeded, the die temperature can rise above the $T_{J(MAX)}$ of 150°C, and the LM2936 may go into thermal shutdown.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Temperature, T_J	−40	125	°C
Input voltage, V_{IN} , LM2936	5.5	40	V
Input voltage, V_{IN} , LM2936HV only	5.5	60	V
Shutdown pin voltage, V_{SD}, LM2936BM only	0	40	V

6.4 Thermal Information

THERMAL METRIC (1)		LM2936					UNIT
		SOIC (D)	TO-252 (NDP)	VSSOP (DGK)	SOT-223 (DCY)	TO-92 (LP)	
		8 PINS	3 PINS	8 PINS	4 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.4	50.5	173.4	62.8	156.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	52.6	65.9	44.2	80.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	51.9	29.7	94.9	11.7	n/a	
ψ_{JT}	Junction-to-top characterization parameter	10.9	4.8	9.6	3.6	24.5	
ψ_{JB}	Junction-to-board characterization parameter	51.4	29.3	93.3	11.6	136.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	1.6	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 3-V LM2936

V_{IN} = 14 V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
3-V LM2936HV ONLY					
Output voltage	5.5 V ≤ V_{IN} ≤ 48 V, 100 µA ≤ I_{OUT} ≤ 50 mA,(2) –40°C ≤ T_J ≤ 125°C	2.91	3	3.09	V
Line regulation	6 V ≤ V_{IN} ≤ 60 V, I_{OUT} = 1 mA		10	30	mV
ALL 3-V LM2936					
Output voltage		2.94	3	3.06	V
	4 V ≤ V_{IN} ≤ 26 V, 100 µA ≤ I_{OUT} ≤ 50 mA,(2) –40°C ≤ T_J ≤ 125°C	2.91	3.000	3.09	
Quiescent current	I_{OUT} = 100 µA, 8 V ≤ V_{IN} ≤ 24 V		15	20	µA
	I_{OUT} = 10 mA, 8 V ≤ V_{IN} ≤ 24 V		0.2	0.5	mA
	I_{OUT} = 50 mA, 8 V ≤ V_{IN} ≤ 24 V		1.5	2.5	mA
Line regulation	9 V ≤ V_{IN} ≤ 16 V		5	10	mV
	6 V ≤ V_{IN} ≤ 40 V, I_{OUT} = 1 mA		10	30	
Load regulation	100 µA ≤ I_{OUT} ≤ 5 mA		10	30	mV
	5 mA ≤ I_{OUT} ≤ 50 mA		10	30	
Dropout voltage	I_{OUT} = 100 µA		0.05	0.1	V
	I_{OUT} = 50 mA		0.20	0.40	V
Short-circuit current	V_{OUT} = 0 V	65	120	250	mA
Output impedance	I_{OUT} = 30 mAdc and 10 mArms, f = 1000 Hz		450		mΩ
Output noise voltage	10 Hz–100 kHz		500		µV
Long-term stability			20		mV/1000 Hr
Ripple rejection	V_{ripple} = 1 V_{rms}, f_{ripple} = 120 Hz	−40	−60		dB
Reverse polarity transient input voltage	R_L = 500 Ω, t = 1 ms	−50	−80		V
Output voltage with reverse polarity input	V_{IN} = −15 V, R_L = 500 Ω		0	−0.3	V
Maximum Line Transient	R_L = 500 Ω, V_{OUT} ≤ 3.3 V, T = 40 ms	60			V
Output bypass capacitance (C_{OUT}) ESR	C_{OUT} = 22 µF, 0.1 mA ≤ I_{OUT} ≤ 50 mA	0.3		8	Ω
SHUTDOWN INPUT − 3-V LM2936BM ONLY					
Output voltage, V_{OUT}	Output off, V_{SD} = 2.4 V, R_{LOAD} = 500 Ω		0	0.01	V
Shutdown high threshold voltage, V_{IH}	Output off, R_{LOAD} = 500 Ω	2	1.1		V
Shutdown low threshold voltage, V_{IL}	Output on, R_{LOAD} = 500 Ω		1.1	0.6	V
Shutdown high current, I_{IH}	Output off, V_{SD} = 2.4 V, R_{LOAD} = 500Ω		12		µA
Quiescent current	Output off, V_{SD} = 2.4 V, R_{LOAD} = 500 Ω, includes I_{IH} current		30		µA

(1) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.

6.6 Electrical Characteristics for 3.3-V LM2936

V_{IN} = 14 V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
3.3-V LM2936HV ONLY					
Output voltage	5.5 V ≤ V_{IN} ≤ 48 V, 100 µA ≤ I_{OUT} ≤ 50 mA,(3) –40°C ≤ T_J ≤ 125°C	3.201	3.300	3.399	V
Line regulation	6 V ≤ V_{IN} ≤ 60 V, I_{OUT} = 1 mA		10	30	mV
ALL 3.3-V LM2936					
Output voltage		3.234	3.300	3.366	V
	4 V ≤ V_{IN} ≤ 26 V, 100 µA ≤ I_{OUT} ≤ 50 mA,(3) –40°C ≤ T_J ≤ 125°C	3.201	3.300	3.399	
Quiescent current	I_{OUT} = 100 µA, 8 V ≤ V_{IN} ≤ 24 V		15	20	µA
	I_{OUT} = 10 mA, 8 V ≤ V_{IN} ≤ 24 V		0.2	0.5	mA
	I_{OUT} = 50 mA, 8 V ≤ V_{IN} ≤ 24 V		1.5	2.5	mA
Line regulation	9 V ≤ V_{IN} ≤ 16 V		5	10	mV
	6 V ≤ V_{IN} ≤ 40 V, I_{OUT} = 1 mA		10	30	
Load regulation	100 µA ≤ I_{OUT} ≤ 5 mA		10	30	mV
	5 mA ≤ I_{OUT} ≤ 50 mA		10	30	
Dropout voltage	I_{OUT} = 100 µA		0.05	0.10	V
	I_{OUT} = 50 mA		0.2	0.4	V
Short-circuit current	V_{OUT} = 0 V	65	120	250	mA
Output impedance	I_{OUT} = 30 mAdc and 10 mArms, f = 1000 Hz		450		mΩ
Output noise voltage	10 Hz–100 kHz		500		µV
Long-term stability			20		mV/1000 Hr
Ripple rejection	V_{ripple} = 1 V_{rms}, f_{ripple} = 120 Hz	−40	−60		dB
Reverse polarity transient input voltage	R_L = 500 Ω, T = 1 ms	−50	−80		V
Output voltage with reverse polarity input	V_{IN} = −15 V, R_L = 500 Ω		0	−0.3	V
maximum line transient	R_L = 500 Ω, V_{OUT} ≤ 3.63 V, T = 40 ms	60			V
Output bypass capacitance (C_{OUT}) ESR	C_{OUT} = 22 µF, 0.1 mA ≤ I_{OUT} ≤ 50 mA	0.3		8	Ω
SHUTDOWN INPUT − 3.3-V LM2936BM ONLY					
Output voltage, V_{OUT}	Output off, V_{SD} = 2.4 V, R_{LOAD} = 500 Ω		0	0.01	V
Shutdown high threshold voltage, V_{IH}	Output off, R_{LOAD} = 500 Ω	2	1.1		V
Shutdown low threshold voltage, V_{IL}	Output on, R_{LOAD} = 500 Ω		1.1	0.6	V
Shutdown high current, I_{IH}	Output off, V_{SD} = 2.4V, R_{LOAD} = 500 Ω		12		µA
Quiescent current	Output off, V_{SD} = 2.4V, R_{LOAD} = 500 Ω, includes I_{IH} current		30		µA

(1) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
(3) To ensure constant junction temperature, pulse testing is used.

6.7 Electrical Characteristics for 5-V LM2936

V_{IN} = 14 V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
5-V LM2936HV ONLY					
Output voltage	5.5 V ≤ V_{IN} ≤ 48 V, 100 µA ≤ I_{OUT} ≤ 50 mA,(3) –40°C ≤ T_J ≤ 125°C	4.85	5	5.15	V
Line regulation	6 V ≤ V_{IN} ≤ 60 V, I_{OUT} = 1 mA		15	35	mV
ALL 5-V LM2936					
Output voltage		4.9	5	5.1	V
	5.5 V ≤ V_{IN} ≤ 26 V, 100 µA ≤ I_{OUT} ≤ 50 mA,(3) –40°C ≤ T_J ≤ 125°C	4.85	5	5.15	
Quiescent current	I_{OUT} = 100 µA, 8 V ≤ V_{IN} ≤ 24 V		9	15	µA
	I_{OUT} = 10 mA, 8 V ≤ V_{IN} ≤ 24 V		0.2	0.5	mA
	I_{OUT} = 50 mA, 8 V ≤ V_{IN} ≤ 24 V		1.5	2.5	mA
Line regulation	9 V ≤ V_{IN} ≤ 16 V		5	10	mV
	6 V ≤ V_{IN} ≤ 40 V, I_{OUT} = 1 mA		10	30	
Load regulation	100 µA ≤ I_{OUT} ≤ 5 mA		10	30	mV
	5 mA ≤ I_{OUT} ≤ 50 mA		10	30	
Dropout voltage	I_{OUT} = 100 µA		0.05	0.1	V
	I_{OUT} = 50 mA		0.2	0.4	V
Short-circuit current	V_{OUT} = 0 V	65	120	250	mA
Output impedance	I_{OUT} = 30 mAdc and 10 mArms, f = 1000 Hz		450		mΩ
Output noise voltage	10 Hz–100 kHz		500		µV
Long-term stability			20		mV/1000 Hr
Ripple rejection	V_{ripple} = 1 V_{rms}, f_{ripple} = 120 Hz	−40	−60		dB
Reverse polarity transient input voltage	R_L = 500 Ω, T = 1 ms	−50	−80		V
Output voltage with reverse polarity input	V_{IN} = −15 V, R_L = 500 Ω		0	−0.3	V
Maximum line transient	R_L = 500 Ω, V_{OUT} ≤ 5.5 V, T = 40 ms	60			V
Output bypass capacitance (C_{OUT}) ESR	C_{OUT} = 10 µF, 0.1 mA ≤ I_{OUT} ≤ 50 mA	0.3		8	Ω
SHUTDOWN INPUT − 5-V LM2936BM ONLY					
Output voltage, V_{OUT}	Output off, V_{SD} = 2.4 V, R_{LOAD} = 500 Ω		0	0.01	V
Shutdown high threshold voltage, V_{IH}	Output off, R_{LOAD} = 500 Ω	2	1.1		V
Shutdown low threshold voltage, V_{IL}	Output on, R_{LOAD} = 500 Ω		1.1	0.6	V
Shutdown high current, I_{IH}	Output off, V_{SD} = 2.4 V, R_{LOAD} = 500 Ω		12		µA
Quiescent current	Output off, V_{SD} = 2.4 V, R_{LOAD} = 500Ω, includes I_{IH} current		30		µA

(1) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
(3) To ensure constant junction temperature, pulse testing is used.

6.8 Typical Characteristics

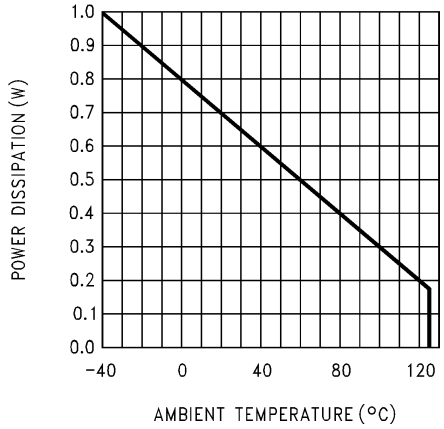


Figure 1. Maximum Power Dissipation (TO-92)

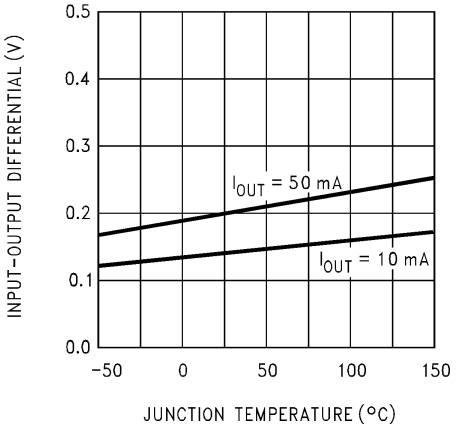


Figure 2. Dropout Voltage

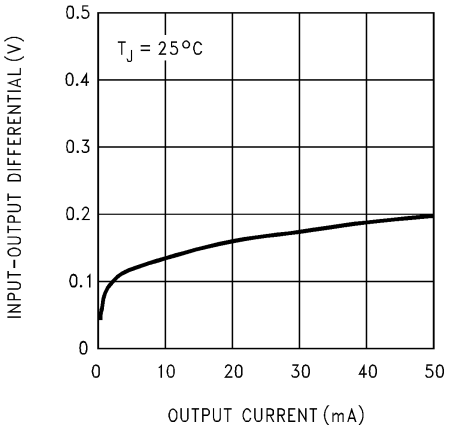


Figure 3. Dropout Voltage

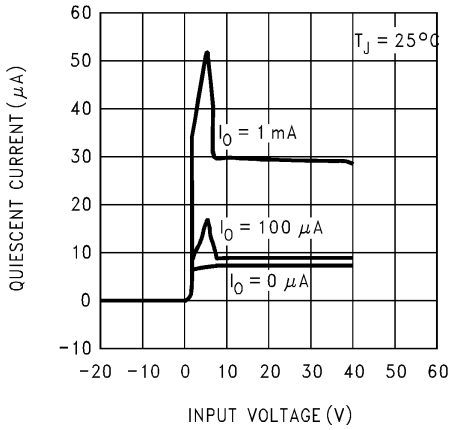


Figure 4. Quiescent Current

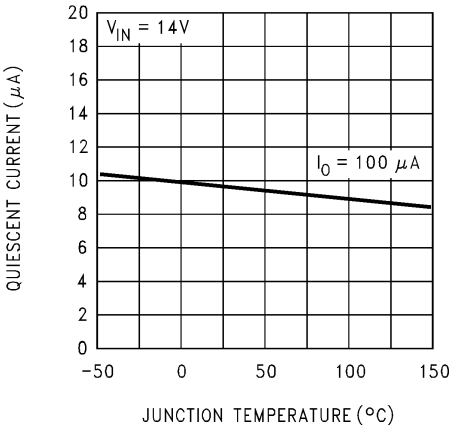


Figure 5. Quiescent Current

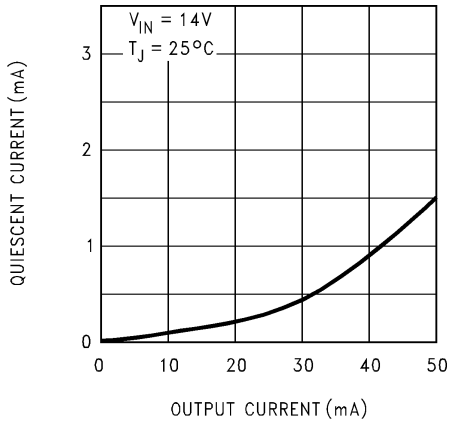


Figure 6. Quiescent Current

Typical Characteristics (continued)

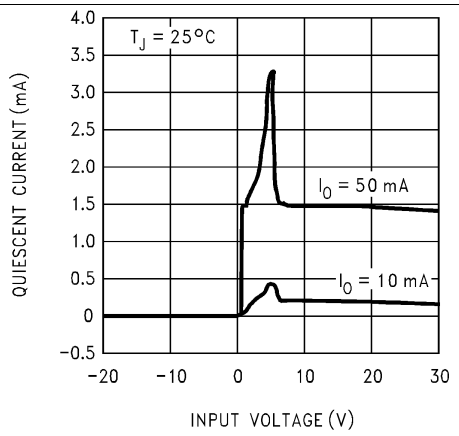


Figure 7. Quiescent Current

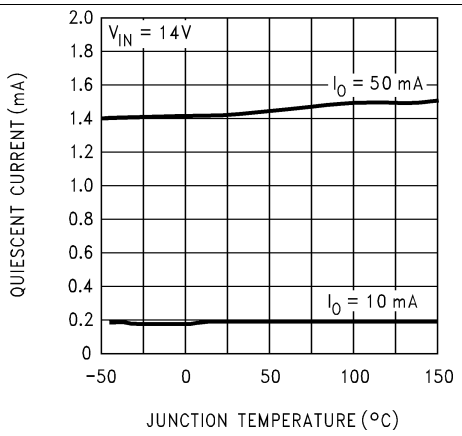


Figure 8. Quiescent Current

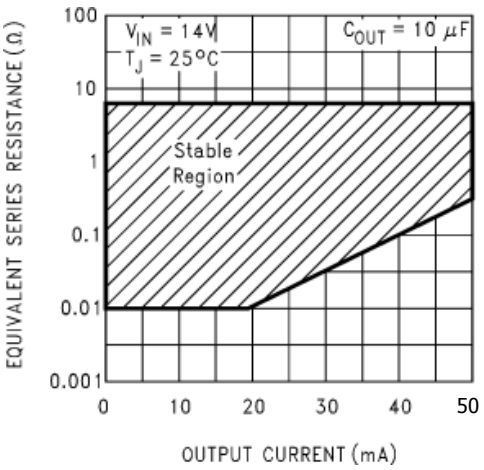


Figure 9. 5-V LM2936 C_{OUT} ESR

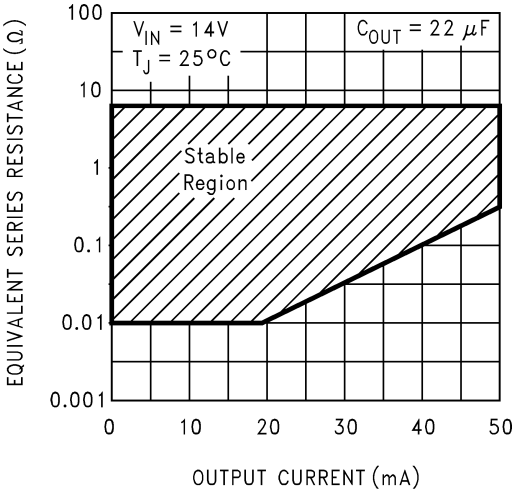


Figure 10. 3-V LM2936 C_{OUT} ESR

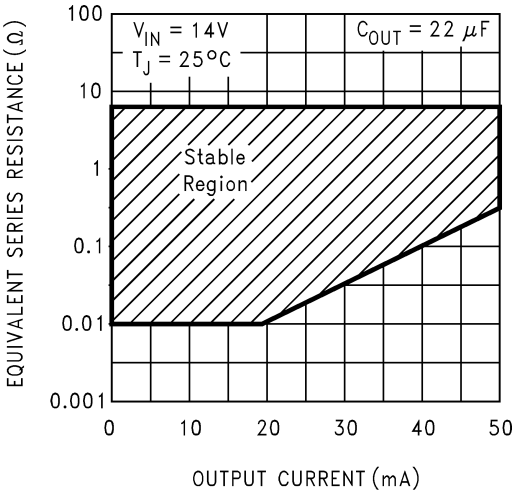


Figure 11. 3.3-V LM2936 C_{OUT} ESR

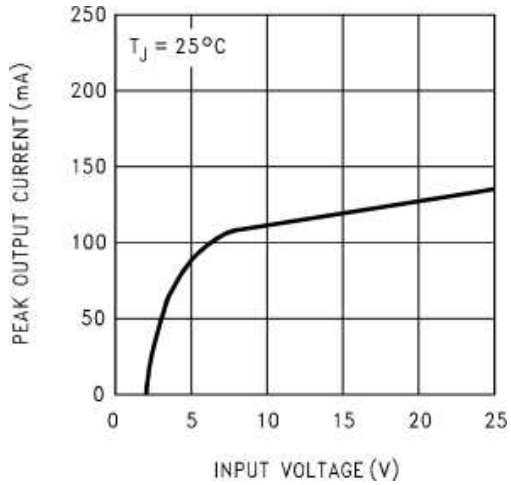


Figure 12. Peak Output Current

Typical Characteristics (continued)

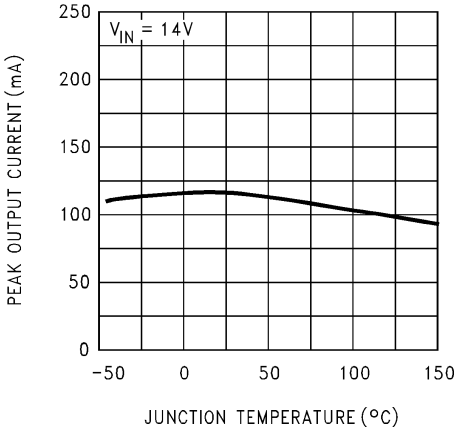


Figure 13. Peak Output Current

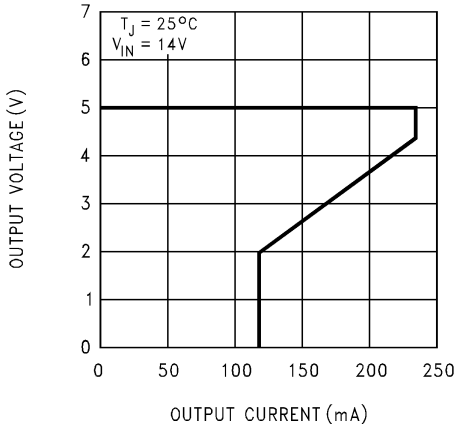


Figure 14. 5-V LM2936 Current Limit

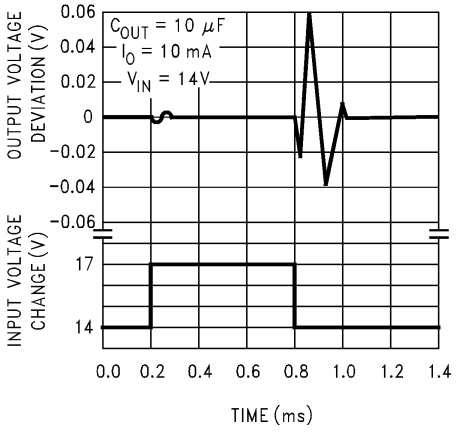


Figure 15. 5-V LM2936 Line Transient Response

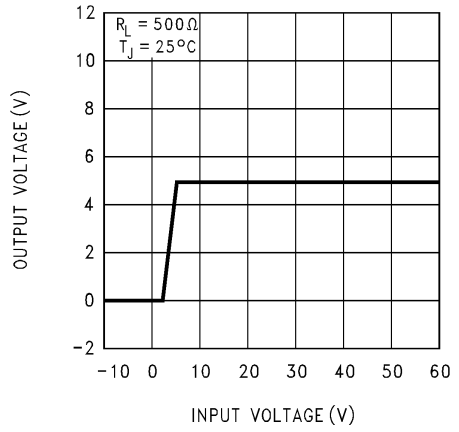


Figure 16. 5-V LM2936 Output at Voltage Extremes

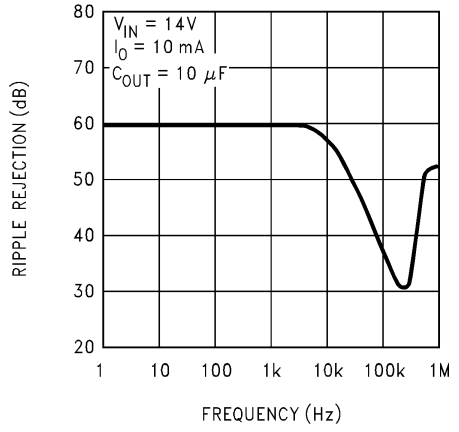


Figure 17. 5-V LM2936 Ripple Rejection

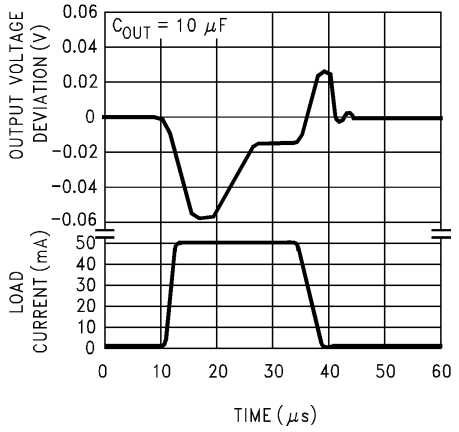


Figure 18. 5-V LM2936 Load Transient Response

Typical Characteristics (continued)

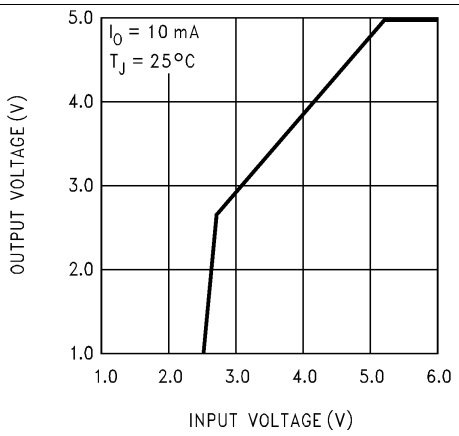


Figure 19. 5-V LM2936 Low Voltage Behavior

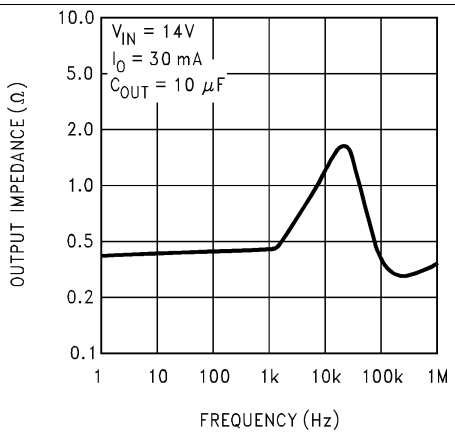


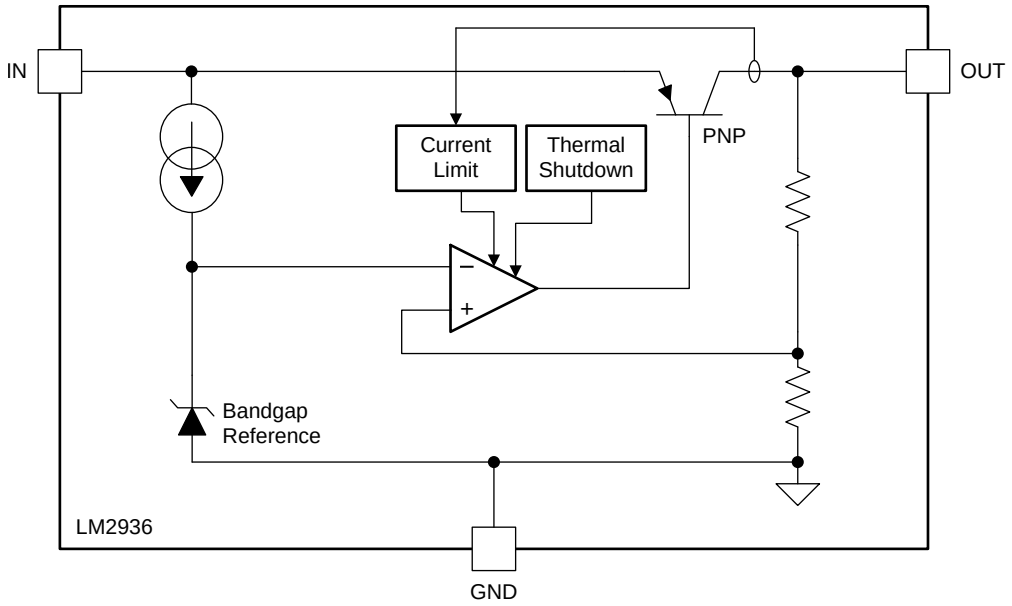
Figure 20. 5-V LM2936 Output Impedance

7 Detailed Description

7.1 Overview

The LM2936 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 15 µA quiescent current at a 100-µA load, the LM2936 is ideally suited for automotive and other battery operated systems. The LM2936 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery input protection, and thermal shutdown. The LM2936 has a 40-V maximum operating voltage limit, a −40°C to 125°C operating temperature range, and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High Input Operating Voltage

Unlike namy other PNP low dropout regulators, the LM2936 remains fully operational with V_{IN} = 40 V, and the LM2936HV remains fully operational with V_{IN} = 60 V . Owing to power dissipation characteristics of the available packages, full output current cannot be ensured for all combinations of ambient temperature and input voltage.

While the LM2936HV maintains regulation to 60 V, it will not withstand a short circuit to ground on the output when V_{IN} is above 40 V because of safe operating area limitations in the internal PNP pass device. Above 60V the LM2936 will break down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage may exceed 40 V, or where transients are likely to exceed 60 V.

7.3.2 Thermal Shutdown (TSD)

The TSD circuitry of the LM2936 has been designed to protect the device against temporary thermal overload conditions. The TSD circuitry is not intended to replace proper heat-sinking. Continuously running the LM2936 device at TSD may degrade device reliability as the junction temperature will be exceeding the absolute maximum junction temperature rating. If the LM2936 goes into TSD mode, the output current will be shut off until the junction temperature falls approximately 10°C, then the output current will automatically be restored. The LM2936 will continuously cycle in and out of TSD until the condition is corrected. The LM2936 TSD junction temperature is typically 160°C.

Feature Description (continued)

7.3.3 Short-Circuit Current Limit

The output current limiting circuitry of the LM2936 has been designed to limit the output current in cases where the load impedance is unusually low. This includes situations where the output may be shorted directly to ground. Continuous operation of the LM2936 at the current limit will typically result in the LM2936 transitioning into TSD mode.

7.3.4 Shutdown (SD) Pin

The LM2936BM has a pin for shutting down the regulator output. Applying a Logic Level High (> 2 V) to the SD pin will cause the output to turn off. Leaving the SD pin open, connecting it to Ground, or applying a Logic Level Low (< 0.6 V) will allow the regulator output to turn on.

7.4 Device Functional Modes

The LM2936 design does not include any undervoltage lockout (UVLO), or overvoltage shutdown (OVSD) functions. Generally, the output voltage will track the input voltage until the input voltage is greater than V_{OUT} + 1 V. When the input voltage is greater than V_{OUT} + 1 V the LM2936 will be in linear operation, and the output voltage will be regulated; however, the device will be sensitive to any small perturbation of the input voltage. Device dynamic performance is improved when the input voltage is at least 2 V greater than the output voltage.

8 Application and Implementation

NOTE

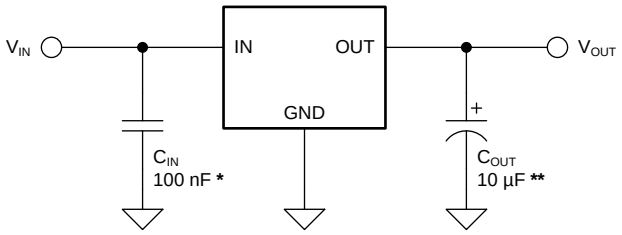
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2936 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. The LM2936 has a 40-V maximum operating voltage limit, a −40°C to 125°C operating temperature range, –24-V input voltage protection and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range This following section presents a simplified discussion of the design process. Also the WEBENCH® software may be used to generate complete designs. When generating a design, WEBENCH utilizes iterative design procedure and accesses comprehensive databases of components. Please go to www.ti.com for more details.

8.2 Typical Application

Figure 21 shows the typical application circuit for the LM2936. For the LM2936 5-V option, the output capacitor, C_{OUT}, must have a capacitance value of at least 10 µF with an equivalent series resistance (ESR) of at least 300 mΩ, but no more than 8 Ω. For the LM2936 3.3-V and 3-V options, the output capacitor, C_{OUT}, must have a capacitance value of at least 22 µF with an ESR of at least 300 mΩ, but no more than 8 Ω. The minimum capacitance value and the ESR requirements apply across the entire expected operating ambient temperature range.



* C_{IN} is required only if the regulator is located more than 3 inches from the power-supply-filter capacitors.

** Required for stability. C_{OUT} must be at least 10 µF for the LM2936 5-V option, and at least 22 µF for the 3.3-V and 3-V options. Capacitance must be maintained over entire expected operating temperature range, and located as close as possible to the regulator. The ESR, of the C_{OUT} capacitor must at least 300 mΩ, but no more than 8 Ω.

Figure 21. LM2936 Typical Application

8.2.1 Design Requirements

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	5 V
Input voltage	10 V to 26 V
Output current requirement	1 mA to 50 mA
Input capacitor	0.1 µF
Output capacitance	10 µF minimum
Output capacitor ESR value	300 mΩ to 8 Ω

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

The output capacitor is critical to maintaining regulator stability, and must meet the required conditions for both ESR and minimum amount of capacitance.

8.2.2.1.1 Minimum Capacitance

The minimum output capacitance required to maintain stability is at least 10 µF for the LM2936 5-V option, and at least 22 µF for the 3.3-V and 3-V options. This value may be increased without limit. Larger values of output capacitance will give improved transient response.

8.2.2.1.2 ESR Limits

The ESR of the output capacitor will cause loop instability if it is too high, or too low. ESR, of the C_{OUT} capacitor must at least 300 mΩ, but no more than 8 Ω.

8.2.2.2 Output Capacitor ESR

It is essential that the output capacitor meet the capacitance and ESR requirements, or oscillations can result. The ESR is used with the output capacitance in

Ceramic capacitors (MLCC) can be used for C_{OUT} only if a series resistor is added to simulate the ESR requirement. The ESR is not optional, it is mandatory. Typically, a 500-mΩ to 1-Ω series resistor is used for this purpose. When using ceramic capacitors, due diligence must be given to initial tolerances, capacitance derating due to applied DC voltage, and capacitance variations due to temperature. Dielectric types X5R and X7R are preferred.

8.2.3 Application Curve

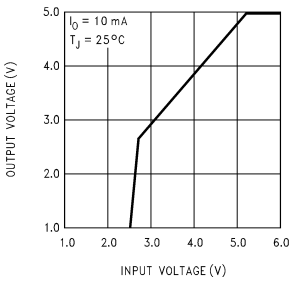


Figure 22. LM2936 V_{OUT} vs. V_{IN}

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage from at least V_{OUT} + 1 V up to a maximum of 40 V. The input supply should be well regulated and free of spurious noise. To ensure that the LM2936 output voltage is well regulated the input supply should be at least V_{OUT} + 2 V. A capacitor at the IN pin may not be specifically required if the bulk input supply filter capacitors are within three inches of the IN pin, but adding one will not be detrimental to operation.

While the LM2936 maintains regulation to V_{IN} = 60 V, it will not withstand a short circuit on the output with V_{IN} above 40 V because of safe operating area limitations in the internal PNP pass device. With V_{IN} above 60 V the LM2936 will break down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage, including transients, is likely to exceed 60 V.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LM2936 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LM2936. Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LM2936, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LM2936 ground pin using as wide, and as short, of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided as these will add parasitic inductances and resistances that will give inferior performance, especially during transient conditions

10.2 Layout Examples

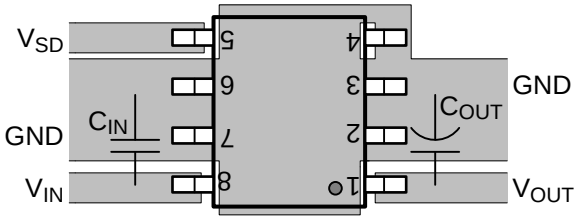


Figure 23. LM2936BM SOIC (D) Layout

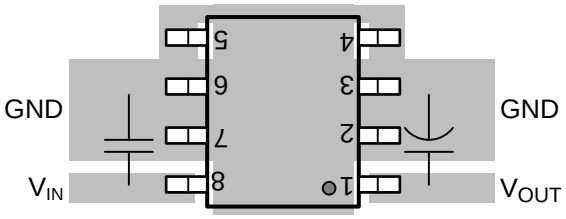


Figure 24. LM2936M SOIC (D) Layout

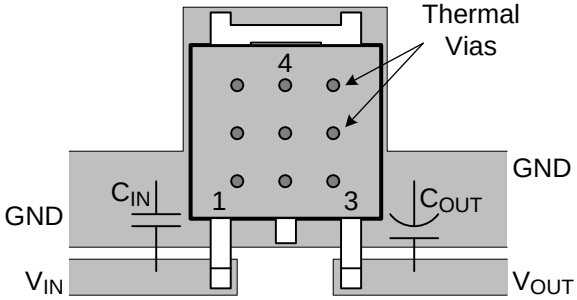


Figure 25. LM2936 TO-252 (NDP) Layout

10.3 Thermal Considerations

Due to the power dissipation characteristics of the available packages ($R_{\theta JA}$), full output current cannot be ensured for all combinations of ambient temperature and input voltage.

Exceeding the maximum allowable power dissipation as defined by the final package $R_{\theta JA}$ will cause excessive die junction temperature, and the regulator may go into thermal shutdown.

Power dissipation, P_D, is calculated from the following formula:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + (V_{IN} \times I_{GND}) \quad (1)$$

Thermal Considerations (continued)

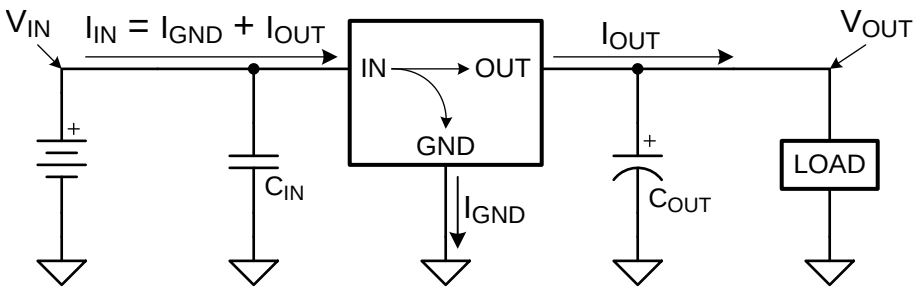


Figure 26. Current Paths for Power Dissipation Calculation

Knowing the power dissipation (P_D), the thermal resistance of the package ($R_{\theta JA}$), and the ambient temperature (T_A), the junction temperature (T_J) can be estimated using the following formula:

$$T_J = (P_D \times R_{\theta JA}) + T_A \quad (2)$$

Knowing the thermal resistance of the package ($R_{\theta JA}$), the ambient temperature (T_A), and the maximum allowed operating junction temperature (T_J) of 125°C, the maximum power dissipation can be estimated using the following formula:

$$P_{D(MAX)} = (125°C - T_A) / R_{\theta JA} \quad (3)$$

Alternately, solving for the required thermal resistance ($R_{\theta JA}$):

$$R_{\theta JA} = (125°C - T_A) / P_{D(MAX)} \quad (4)$$

The maximum allowed P_D information from Equation 3 can be used to estimate the maximum allowed load current (I_{OUT}), or the maximum allowed $_{VIN}$:

$$V_{IN(MAX)} = (P_{D(MAX)} / I_{OUT}) + V_{OUT} \quad (5)$$

$$I_{OUT(MAX)} = (P_{D(MAX)} / (V_{IN} - V_{OUT})) \quad (6)$$

As an example, an application requires : V_{IN} = 14 V, V_{OUT} = 5 V, I_{OUT} = 25 mA, and T_A = 85°C. Find the maximum $R_{\theta JA}$ to keep the junction temperature under 125°C.

$$R_{\theta JA} \le (125°C - T_A) / P_{D(MAX)} \quad (7)$$

$$R_{\theta JA} \le (125°C - 85°C) / ((14\ V - 5\ V) \times 0.025\ A) \quad (8)$$

$$R_{\theta JA} \le 40°C / 0.225W \quad (9)$$

$$R_{\theta JA} \le 177°C/W \quad (10)$$

The EIA/JEDEC standard (JESD51-2) provides methodologies to estimate the junction temperature from external measurements (Ψ_{JB} references the temperature at the PCB, and Ψ_{JT} references the temperature at the top surface of the package) when operating under steady-state power dissipation conditions. These methodologies have been determined to be relatively independent of the copper thermal spreading area that may be attached to the package DAP when compared to the more typical $R_{\theta JA}$. Refer to Texas Instruments Application Report *Semiconductor and IC Package Thermal Metrics* (SPRA953), for specifics.

On the 8-pin SOIC (D) package, the four ground pins are thermally connected to the backside of the die. Adding approximately 0.04 square inches of 2 oz. copper pad area to these four pins will improve the JEDEC $R_{\theta JA}$ rating from 111.4°C/W to approximately 100°C/W. If this extra copper area is placed directly beneath the SOIC package there should not be any impact on board density.

The LM2936 has an internally set thermal shutdown point of typically 160°C. Thermal shutdown is outside the ensured operating temperature range and is intended as a safety feature only. Continuous operation near the thermal shutdown temperature should be avoided as it may have a negative affect on the life of the device.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Texas Instruments Application Report *Semiconductor and IC Package Thermal Metrics* (SPRA953)

11.2 Trademarks

WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2936BM-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6B3.3	Samples
LM2936BM-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6B5.0	Samples
LM2936BMX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6B3.3	Samples
LM2936BMX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6B5.0	Samples
LM2936DT-3.0/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936D T-3.0	Samples
LM2936DT-3.3/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936D T-3.3	Samples
LM2936DT-5.0	NRND	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125	LM2936D T-5.0	
LM2936DT-5.0/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936D T-5.0	Samples
LM2936DTX-3.3/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936D T-3.3	Samples
LM2936DTX-5.0/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936D T-5.0	Samples
LM2936HVBMA-3.3	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2936H BM3.3	
LM2936HVBMA-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	2936H BM3.3	Samples
LM2936HVBMA-5.0	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2936H BM5.0	
LM2936HVBMA-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	2936H BM5.0	Samples
LM2936HVBMAX3.3	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI		2936H BM3.3	
LM2936HVBMAX3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		2936H BM3.3	Samples
LM2936HVBMAX5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		2936H BM5.0	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2936HVMA-5.0	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2936H M-5.0	
LM2936HVMA-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	2936H M-5.0	Samples
LM2936HVMAX-5.0	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	2936H M-5.0	
LM2936HVMAX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	2936H M-5.0	Samples
LM2936M-3.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6M-3	Samples
LM2936M-3.3	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LM293 6-3.3	
LM2936M-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6-3.3	Samples
LM2936M-5.0	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LM293 6M-5	
LM2936M-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6M-5	Samples
LM2936MM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	KBC	Samples
LM2936MM-3.3	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	KBB	
LM2936MM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	KBB	Samples
LM2936MM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	KBA	Samples
LM2936MMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	KBB	Samples
LM2936MMX-5.0	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	KBA	
LM2936MMX-5.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	KBA	Samples
LM2936MP-3.0/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		KACA	Samples
LM2936MP-3.3	NRND	SOT-223	DCY	4	1000	TBD	Call TI	Call TI	-40 to 125	KABA	
LM2936MP-3.3/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	KABA	Samples
LM2936MP-5.0	NRND	SOT-223	DCY	4	1000	TBD	Call TI	Call TI	-40 to 125	KAAA	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2936MP-5.0/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	KAAA	Samples
LM2936MPX-3.0/NOPB	ACTIVE	SOT-223	DCY	4	2000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	KACA	Samples
LM2936MPX-3.3/NOPB	ACTIVE	SOT-223	DCY	4	2000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	KABA	Samples
LM2936MPX-5.0/NOPB	ACTIVE	SOT-223	DCY	4	2000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	KAAA	Samples
LM2936MX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6-3.3	Samples
LM2936MX-5.0	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	LM293 6M-5	
LM2936MX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6M-5	Samples
LM2936Z-3.3/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	SN	N / A for Pkg Type	-40 to 125	LM2936 Z-3.3	Samples
LM2936Z-5.0/LFT1	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN	N / A for Pkg Type		LM293 6Z-5	Samples
LM2936Z-5.0/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN	N / A for Pkg Type		LM293 6Z-5	Samples
LM2936Z-5.0/LFT4	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN	N / A for Pkg Type		LM293 6Z-5	Samples
LM2936Z-5.0/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	SN	N / A for Pkg Type	-40 to 125	LM293 6Z-5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

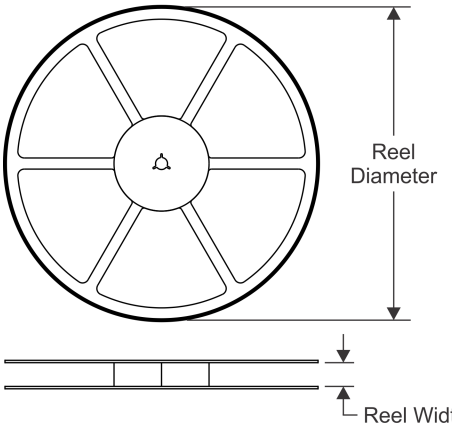
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

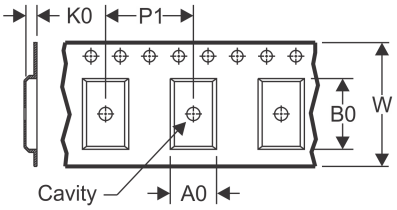
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

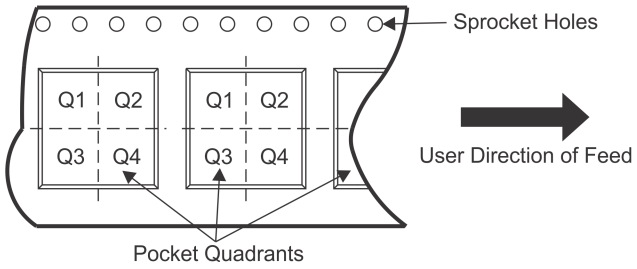


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

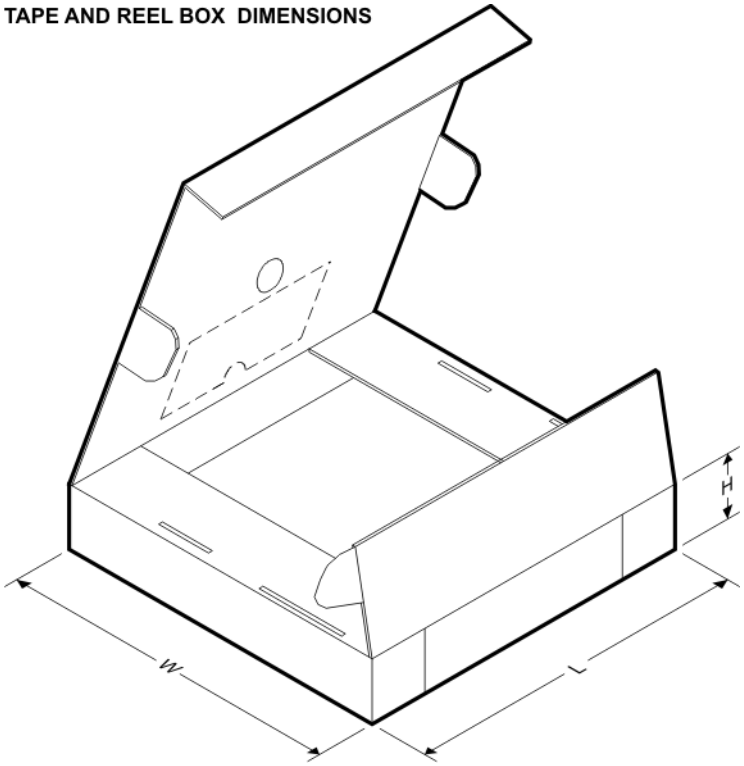


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2936BMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936BMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936DTX-3.3/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LM2936DTX-5.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LM2936HVBMAX3.3	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936HVBMAX3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936HVBMAX5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936HVMAX-5.0	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936HVMAX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936MM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936MM-3.3	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936MM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936MM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936MMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936MMX-5.0	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936MMX-5.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2936MP-3.0/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936MP-3.3	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936MP-3.3/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936MP-5.0	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936MP-5.0/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936MPX-3.0/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936MPX-3.3/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936MPX-5.0/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936MX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936MX-5.0	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936MX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



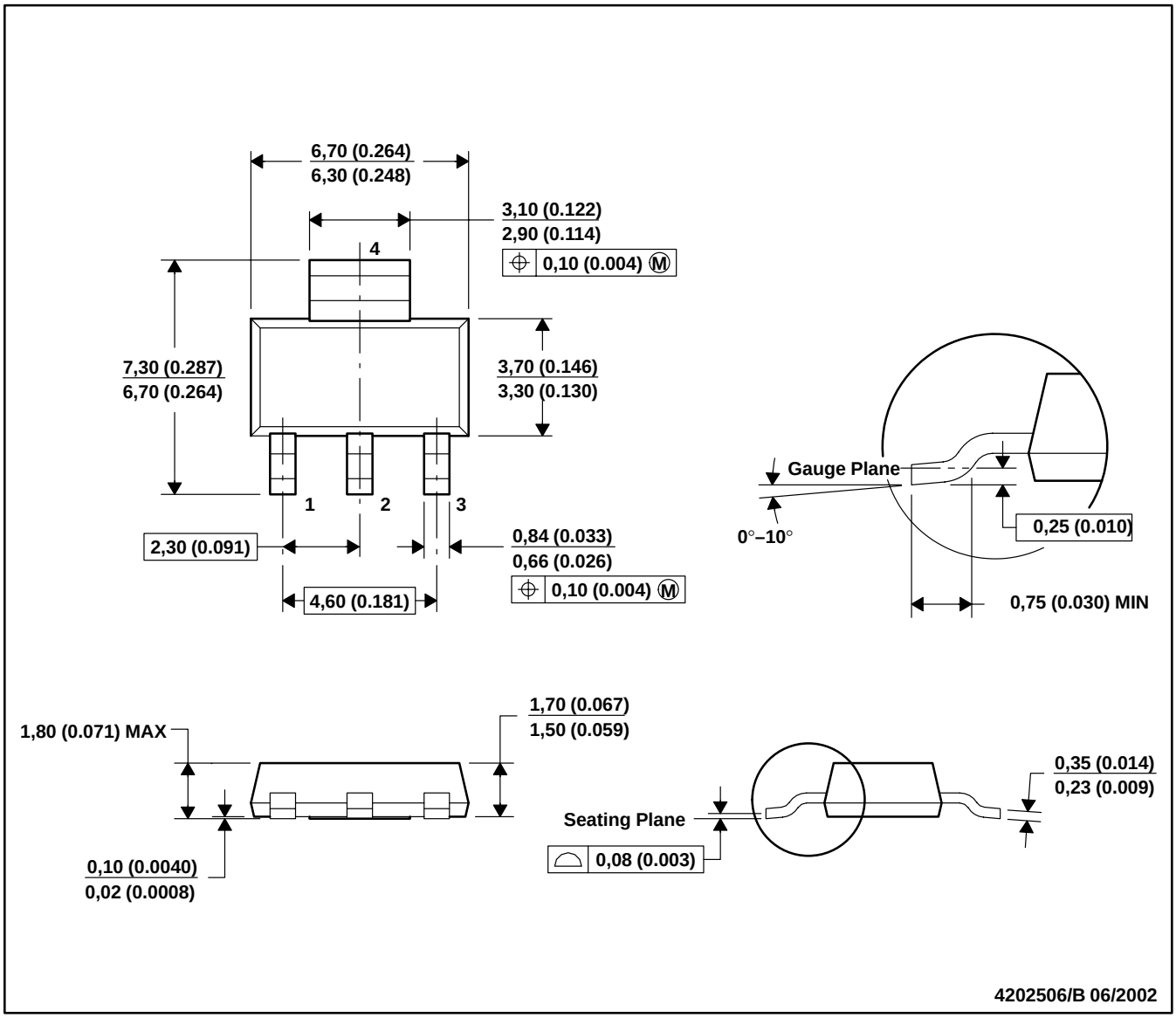
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2936BMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM2936BMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM2936DTX-3.3/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LM2936DTX-5.0/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LM2936HVBMAX3.3	SOIC	D	8	2500	367.0	367.0	35.0
LM2936HVBMAX3.3/NOP	SOIC	D	8	2500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
B							
LM2936HVBMAX5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM2936HVMAX-5.0	SOIC	D	8	2500	367.0	367.0	35.0
LM2936HVMAX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM2936MM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM2936MM-3.3	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM2936MM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM2936MM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM2936MMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM2936MMX-5.0	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM2936MMX-5.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM2936MP-3.0/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2936MP-3.3	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2936MP-3.3/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2936MP-5.0	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2936MP-5.0/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2936MPX-3.0/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM2936MPX-3.3/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM2936MPX-5.0/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM2936MX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM2936MX-5.0	SOIC	D	8	2500	367.0	367.0	35.0
LM2936MX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

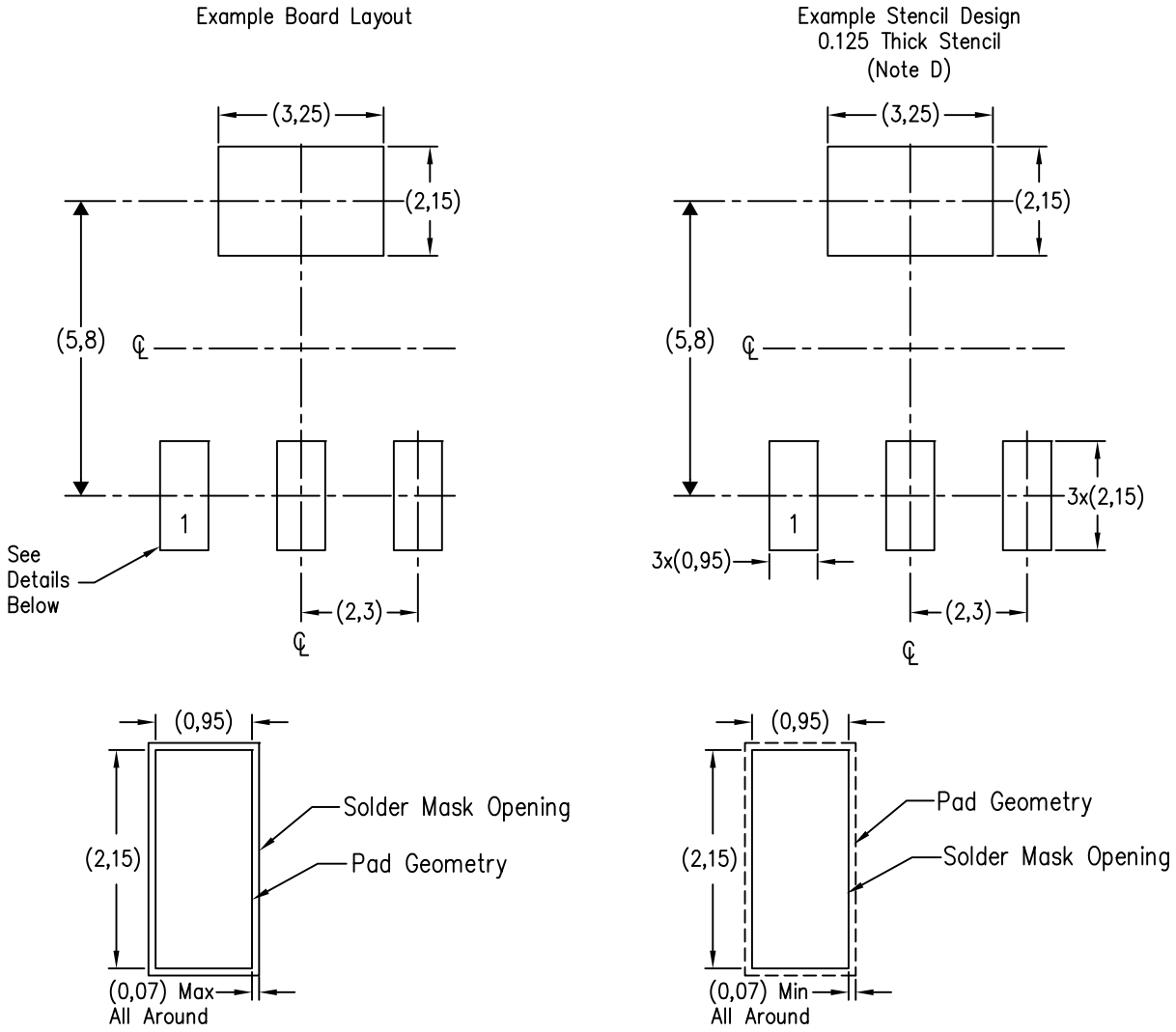
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



NOTES:

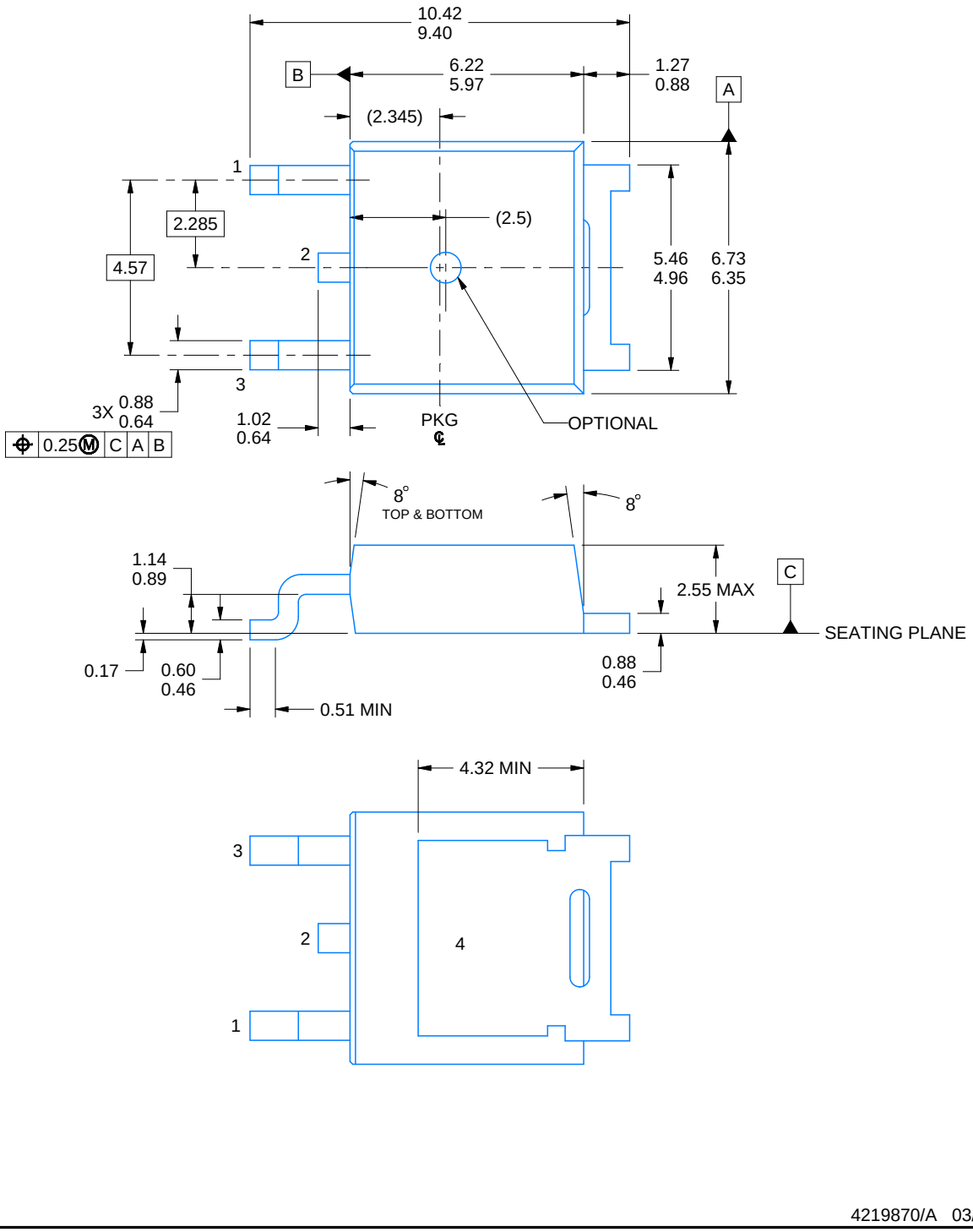
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

NDP0003B

PACKAGE OUTLINE

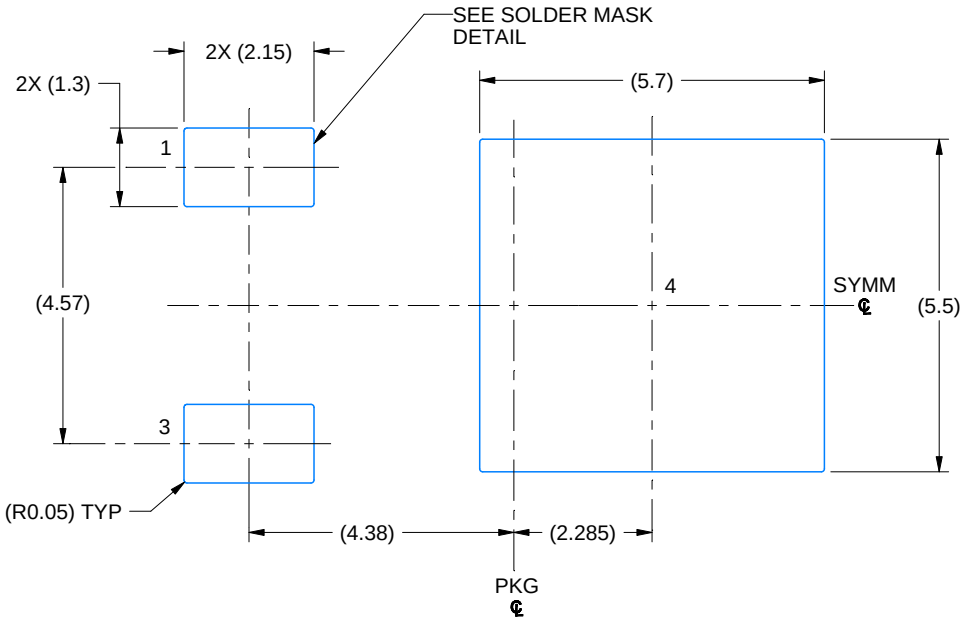
TO-252 - 2.55 mm max height

TRANSISTOR OUTLINE

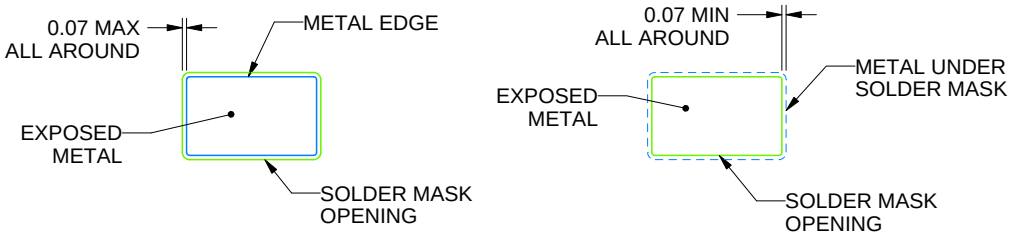


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

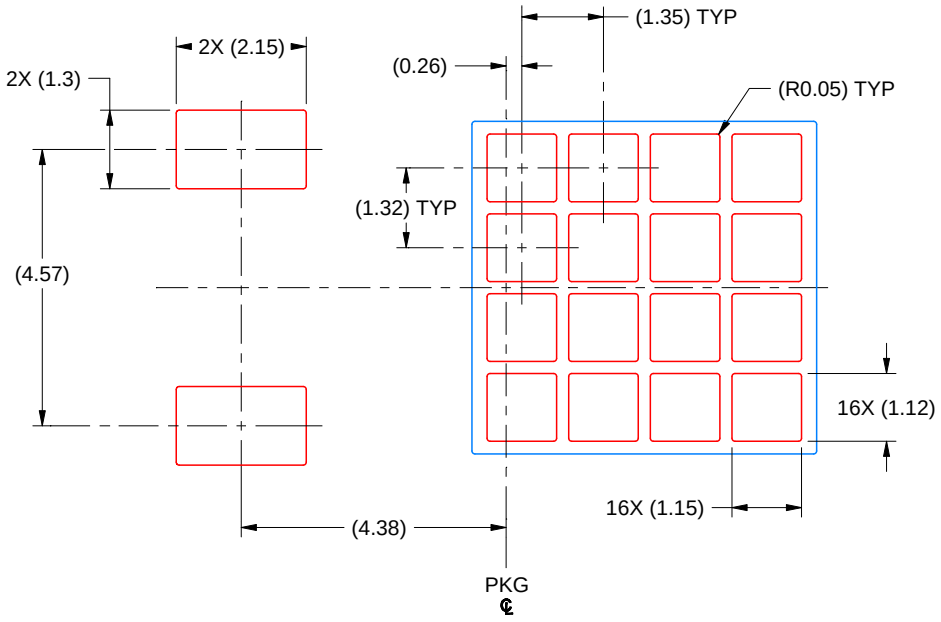


SOLDER MASK DETAIL

4219870/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

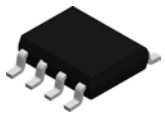


SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

4219870/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

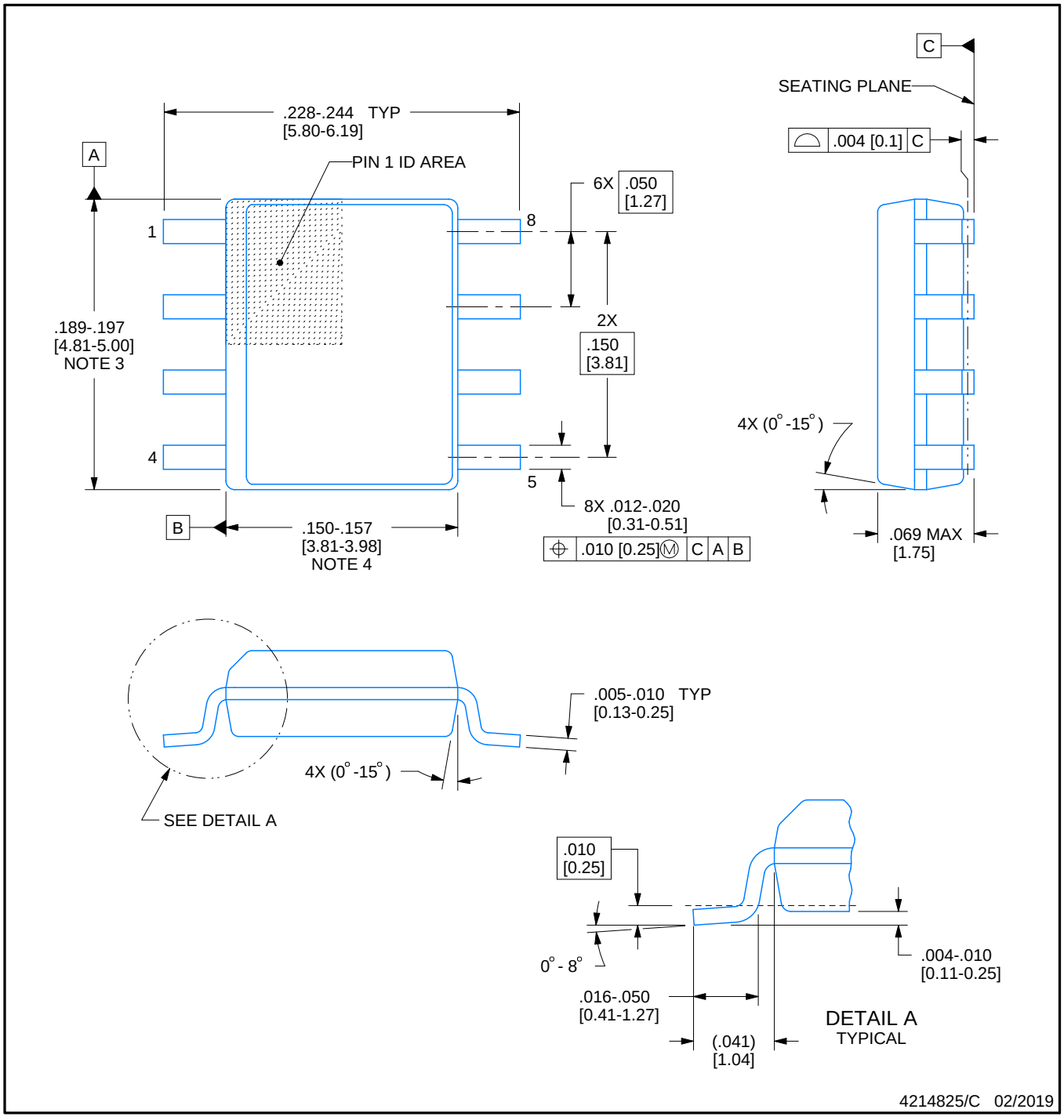


PACKAGE OUTLINE

D0008A

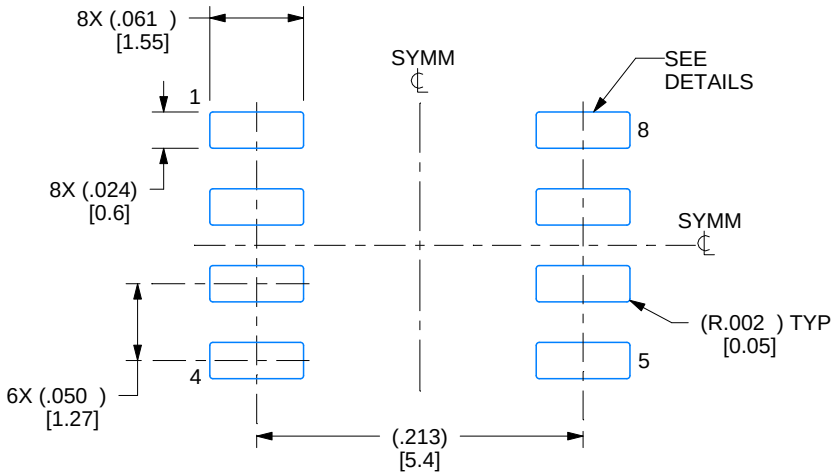
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

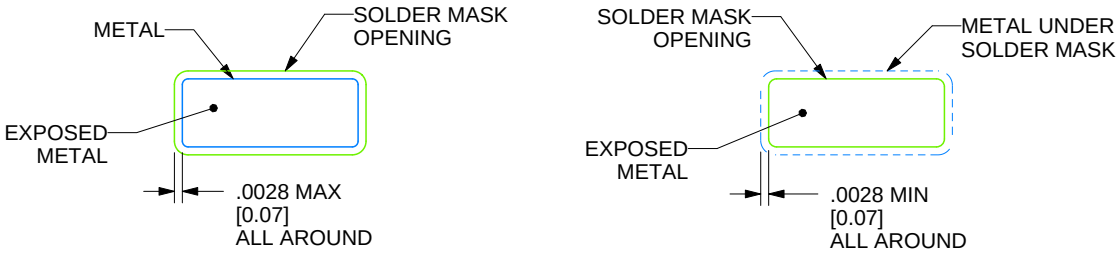


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

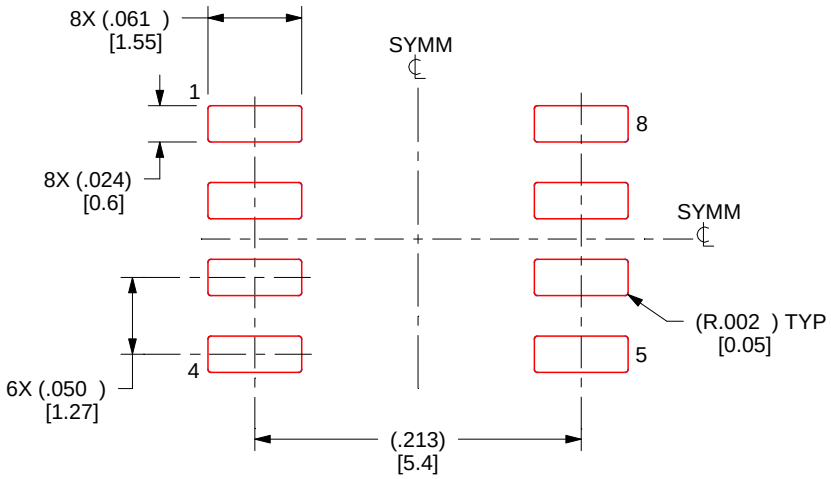
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



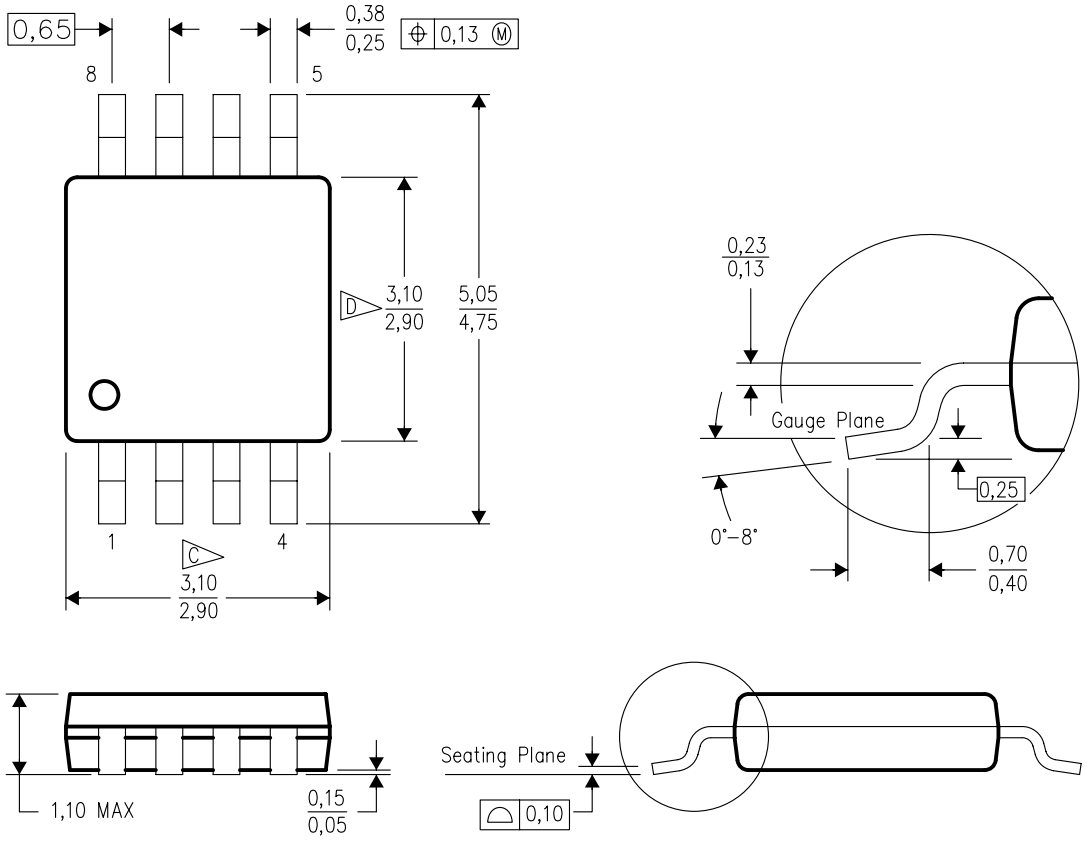
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

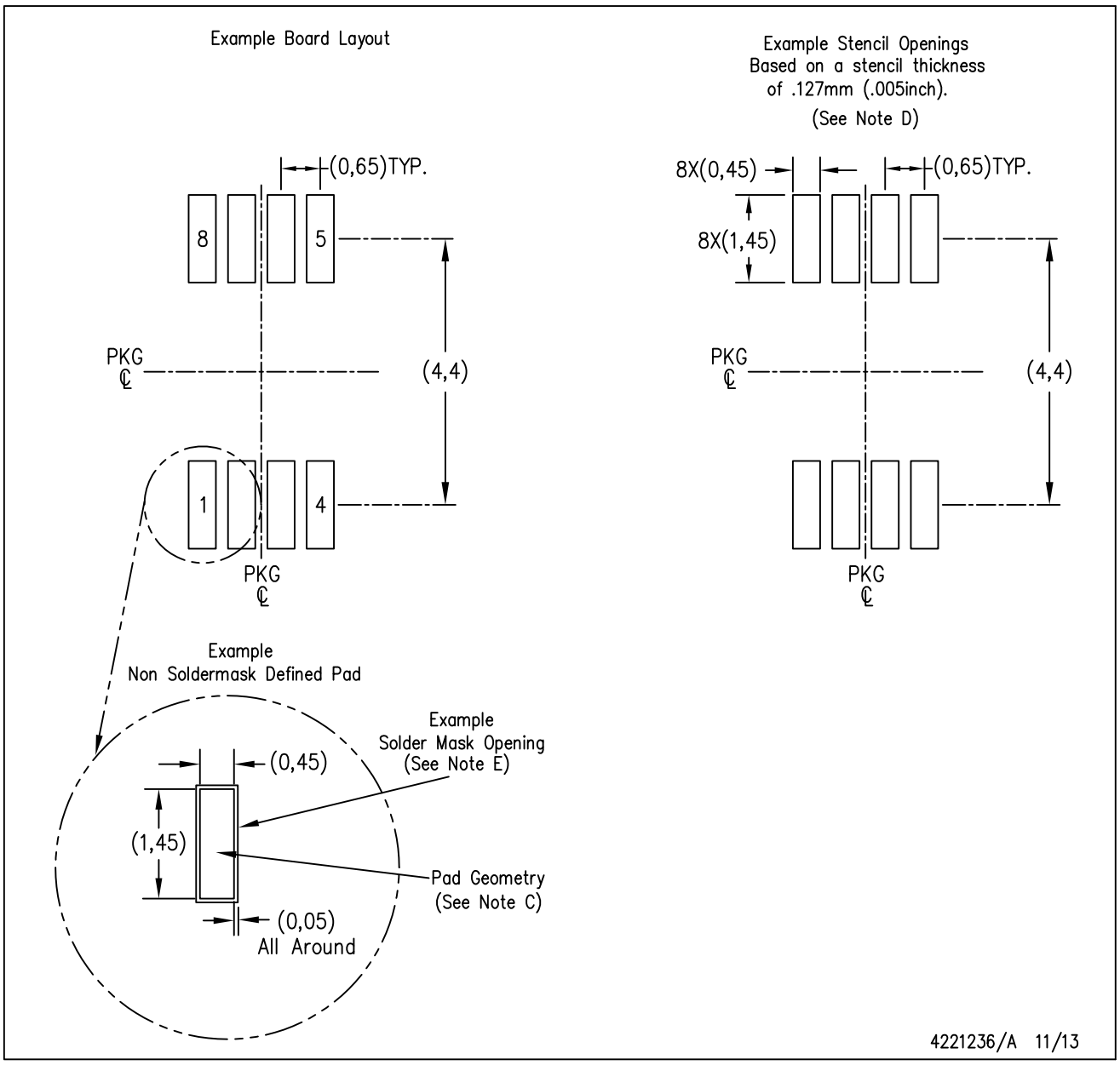
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE

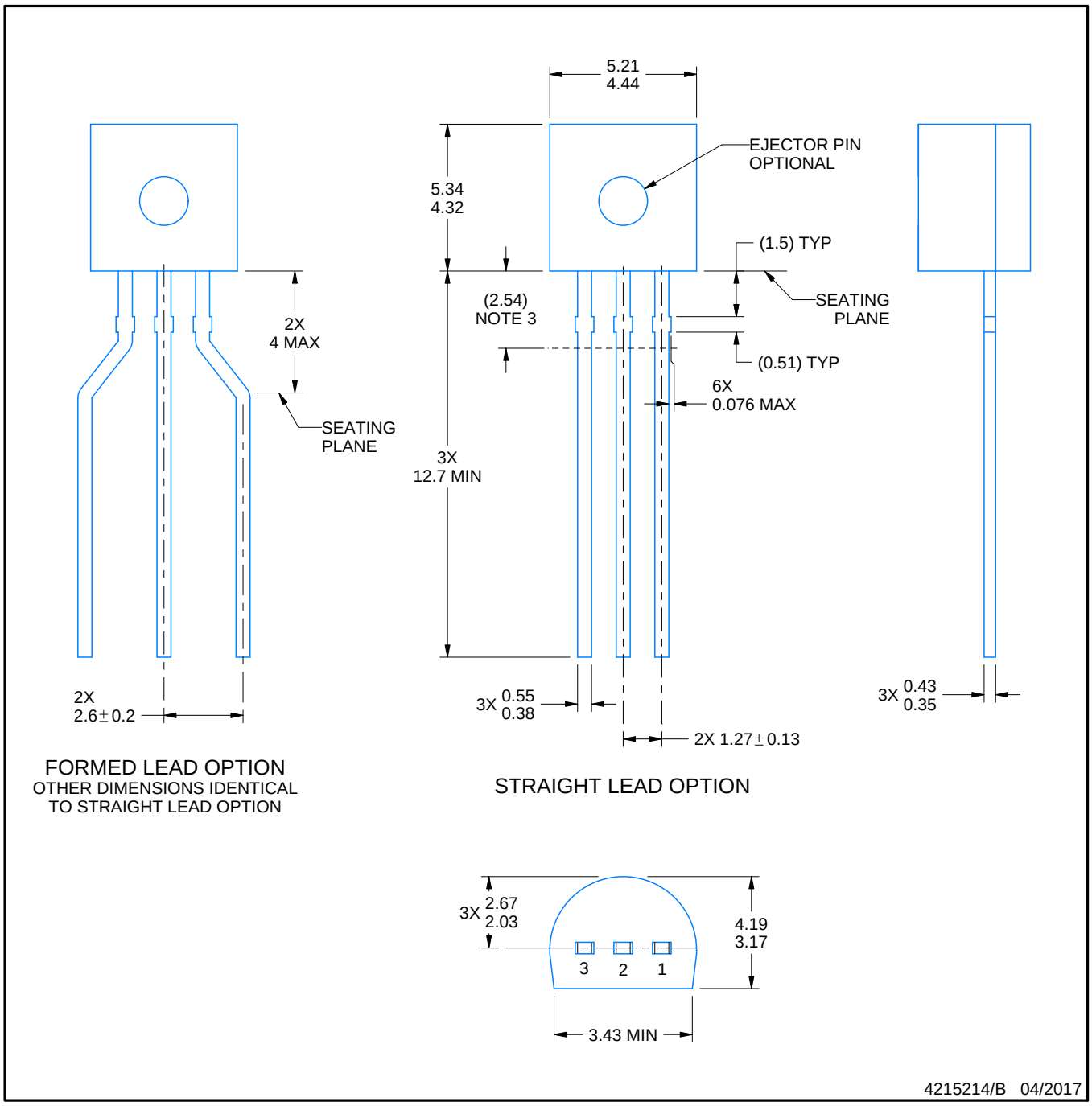
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

PACKAGE OUTLINE

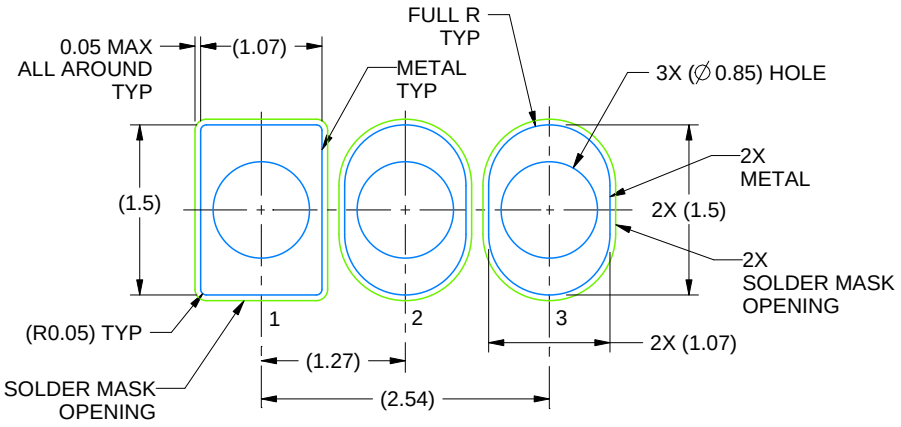
TO-92 - 5.34 mm max height

TO-92

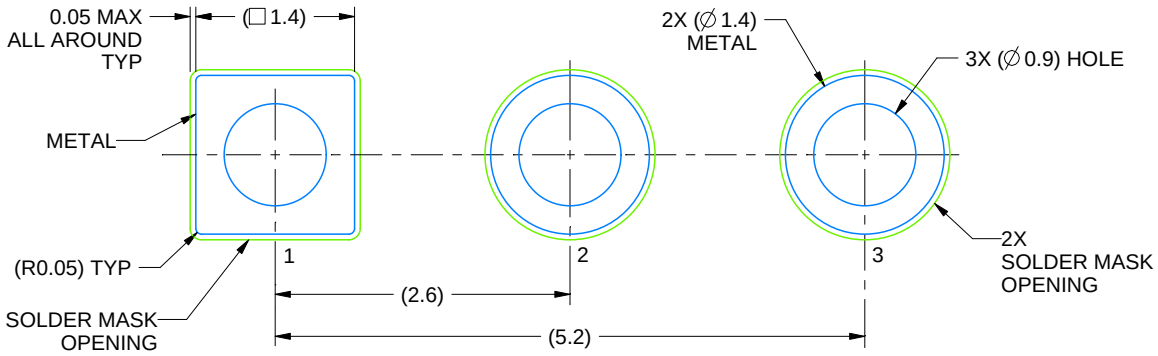


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



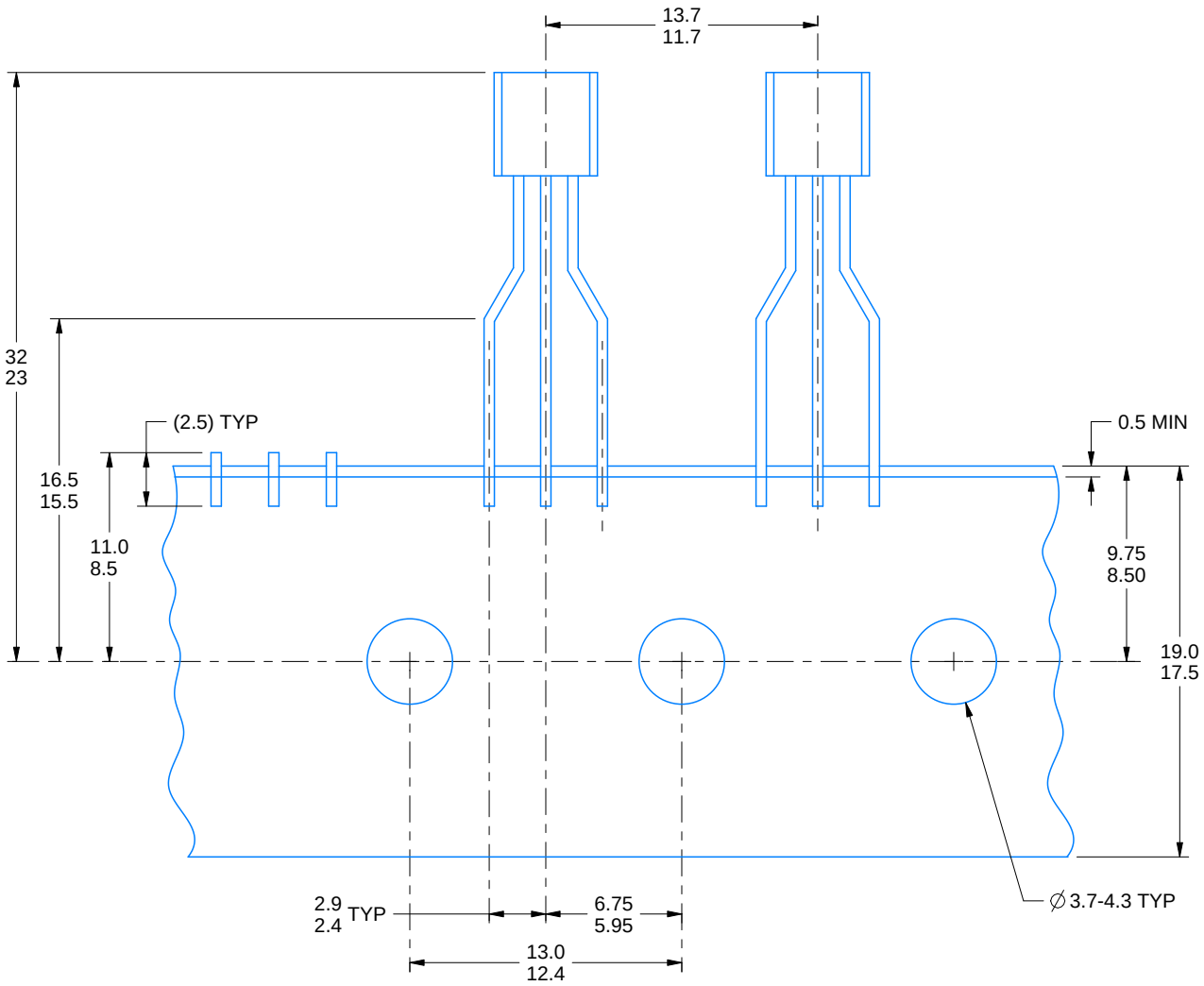
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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