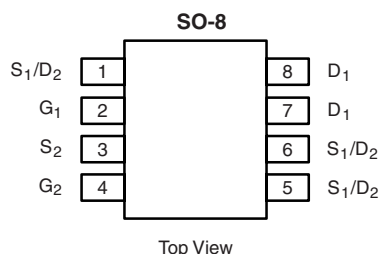


Dual N-Channel 25-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ.)
Channel-1	25	0.023 at V _{GS} = 10 V	8.0	5.5
		0.028 at V _{GS} = 4.5 V	8.0	
Channel-2	25	0.023 at V _{GS} = 10 V	8.0	5.5
		0.028 at V _{GS} = 4.5 V	8.0	

SCHOTTKY PRODUCT SUMMARY		
V _{DS} (V)	V _{SD} (V) Diode Forward Voltage	I _F (A) ^a
25	0.43 V at 1.0 A	2.3



Ordering Information: Si4670DY-T1-E3 (Lead (Pb)-free)
Si4670DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

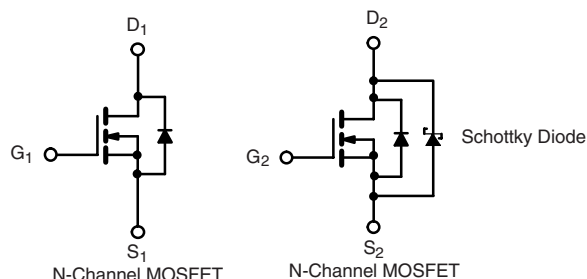
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- PWM Optimized
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Synchronous Buck Converter
- Game Machine
- Notebook



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Channel-1	Channel-2	Unit
Drain-Source Voltage	V _{DS}	25	25	V
Gate-Source Voltage	V _{GS}	± 16	± 16	
Continuous Drain Current (T _J = 150 °C)	I _D	8.0 ^e	8.0 ^e	A
		7	7	
		7 ^{b, c}	7 ^{b, c}	
		5.6 ^{b, c}	5.6 ^{b, c}	
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	30	30	A
Source-Drain Current Diode Current	I _S	2.3	2.3	
		1.5 ^{b, c}	1.5 ^{b, c}	
Maximum Power Dissipation	P _D	2.8	2.8	W
		1.8	1.8	
		1.8 ^{b, c}	1.8 ^{b, c}	
		1.1 ^{b, c}	1.1 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Channel-1		Channel-2		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	57	70	57	70	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	36	44	36	44	

Notes:

a. Based on T_C = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 110 °C/W (Channel-1 and Channel-2).

e. Package limited.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	Ch-1	25		V	
		V _{GS} = 0 V, I _D = 250 μA	Ch-2	25			
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	Ch-1		25	mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	Ch-1		- 4.7		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1		2.2	V
		V _{DS} = V _{GS} , I _D = 250 μA	Ch-2	1		2.2	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 16 V	Ch-1			100	nA
		V _{DS} = 0 V, V _{GS} = ± 16 V	Ch-2			100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25 V, V _{GS} = 0 V	Ch-1			0.001	mA
		V _{DS} = 25 V, V _{GS} = 0 V	Ch-2		0.07	0.5	
		V _{DS} = 25 V, V _{GS} = 0 V, T _J = 100 °C	Ch-1			0.025	
		V _{DS} = 25 V, V _{GS} = 0 V, T _J = 100 °C	Ch-2		5	20	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-1	20		A	
		V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-2	20			
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 7 A	Ch-1		0.019	0.023	Ω
		V _{GS} = 10 V, I _D = 7 A	Ch-2		0.019	0.023	
		V _{GS} = 4.5 V, I _D = 6.3 A	Ch-1		0.023	0.028	
		V _{GS} = 4.5 V, I _D = 6.3 A	Ch-2		0.023	0.028	
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 7 A	Ch-1		23	S	
		V _{DS} = 10 V, I _D = 7 A	Ch-2		23		
Dynamic ^a							
Input Capacitance	C _{iss}	Channel-1 V _{DS} = 13 V, V _{GS} = 0 V, f = 1 MHz	Ch-1		680	pF	
			Ch-2		680		
Output Capacitance	C _{oss}	Channel-2 V _{DS} = 13 V, V _{GS} = 0 V, f = 1 MHz	Ch-1		120		
			Ch-2		180		
Reverse Transfer Capacitance	C _{rss}	Channel-1 V _{DS} = 13 V, V _{GS} = 0 V, f = 1 MHz	Ch-1		55	nC	
			Ch-2		70		
Total Gate Charge	Q _g	V _{DS} = 13 V, V _{GS} = 10 V, I _D = 7 A	Ch-1		12		18
		V _{DS} = 13 V, V _{GS} = 10 V, I _D = 7 A	Ch-2		12		18
Gate-Source Charge	Q _{gs}	Channel-1 V _{DS} = 13 V, V _{GS} = 4.5 V, I _D = 7 A	Ch-1		5.5	8.5	
			Ch-2		5.5	8.5	
Gate-Drain Charge	Q _{gd}	Channel-2 V _{DS} = 13 V, V _{GS} = 4.5 V, I _D = 7 A	Ch-1		2		
			Ch-2		2		
Gate Resistance	R _g	f = 1 MHz	Ch-1		1.5	Ω	
			Ch-2		1.5		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



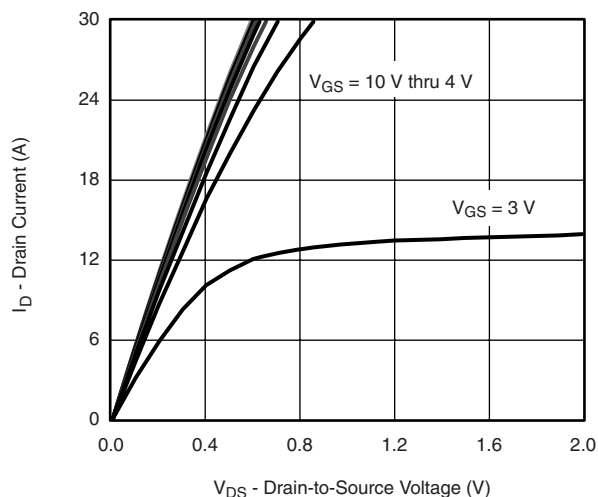
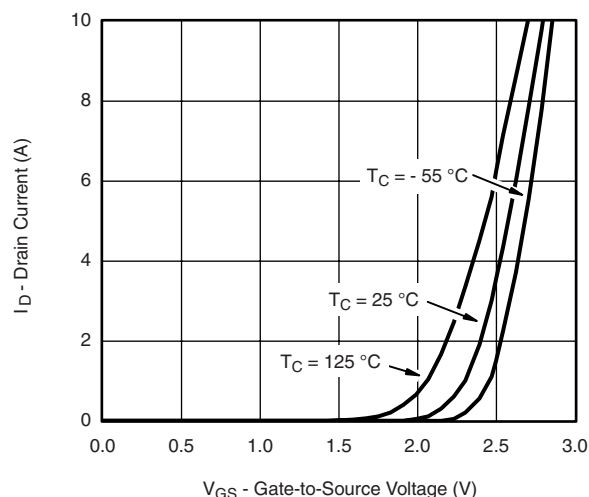
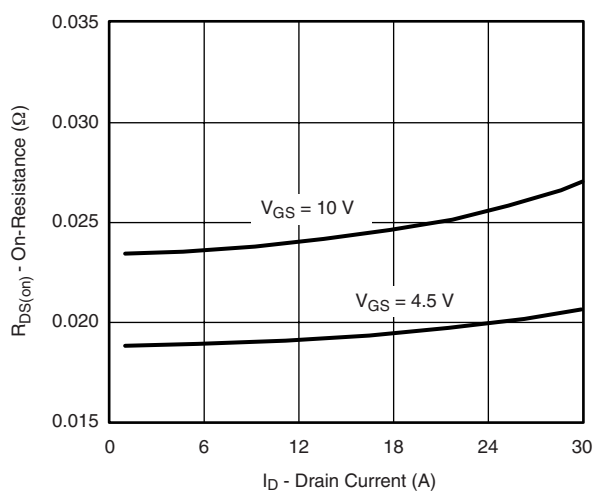
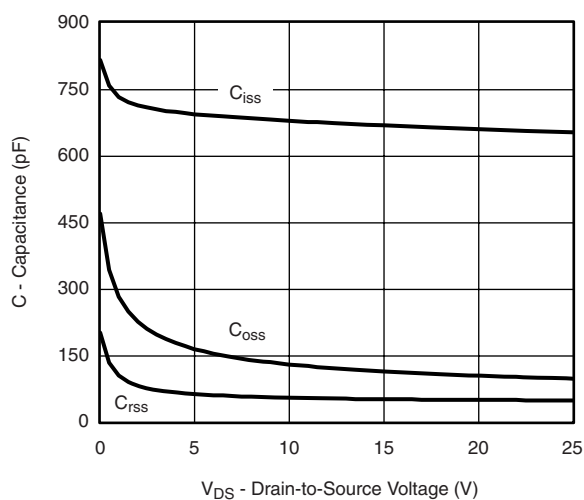
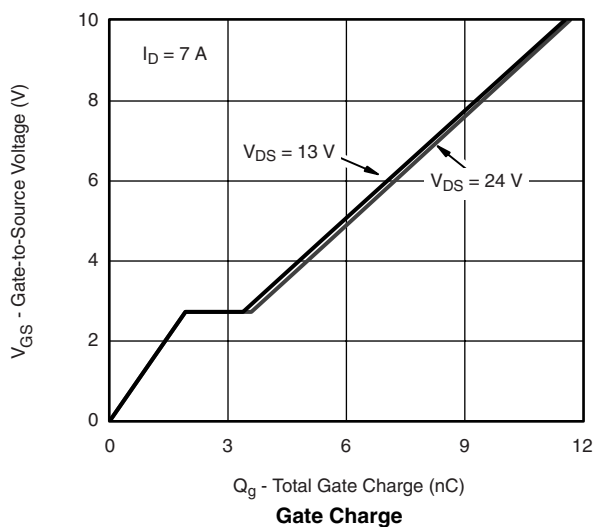
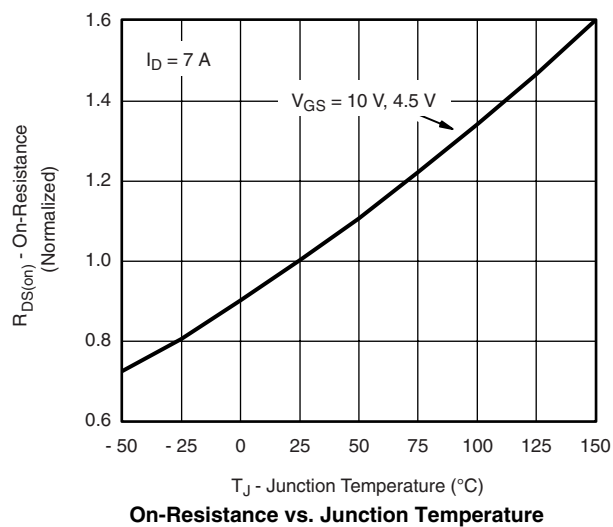
SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Dynamic ^a							
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 13 V, R _L = 2.3 Ω I _D ≅ 5.6 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1		15	25	ns
			Ch-2		15	25	
Rise Time	t _r		Ch-1		50	75	
			Ch-2		50	75	
Turn-Off Delay Time	t _{d(off)}	Ch-1		20	30		
		Ch-2		20	30		
Fall Time	t _f	Ch-1		10	15		
		Ch-2		10	15		
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 13 V, R _L = 2.3 Ω I _D ≅ 5.6 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1		10	15	
			Ch-2		10	15	
Rise Time	t _r		Ch-1		12	20	
			Ch-2		12	20	
Turn-Off Delay Time	t _{d(off)}	Ch-1		15	25		
		Ch-2		15	25		
Fall Time	t _f	Ch-1		10	15		
		Ch-2		10	15		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	Ch-1			2.3	A
			Ch-2			2.3	
Pulse Diode Forward Current ^a	I _{SM}		Ch-1			30	
			Ch-2			30	
Body Diode Voltage	V _{SD}	I _S = 5.6 A	Ch-1		0.8	1.2	V
		I _S = 1 A	Ch-2		0.37	0.43	
Body Diode Reverse Recovery Time	t _{rr}	Channel-1 I _F = 5.6 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1		15	30	ns
			Ch-2		15	30	
Body Diode Reverse Recovery Charge	Q _{rr}		Ch-1		8	16	nC
			Ch-2		8	16	
Reverse Recovery Fall Time	t _a	Channel-2 I _F = 5.6 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1		8.5		ns
			Ch-2		8.5		
Reverse Recovery Rise Time	t _b		Ch-1		6.5		
			Ch-2		6.5		

Notes:

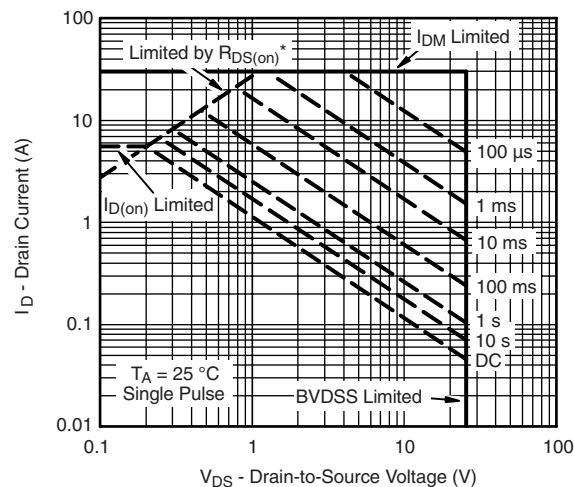
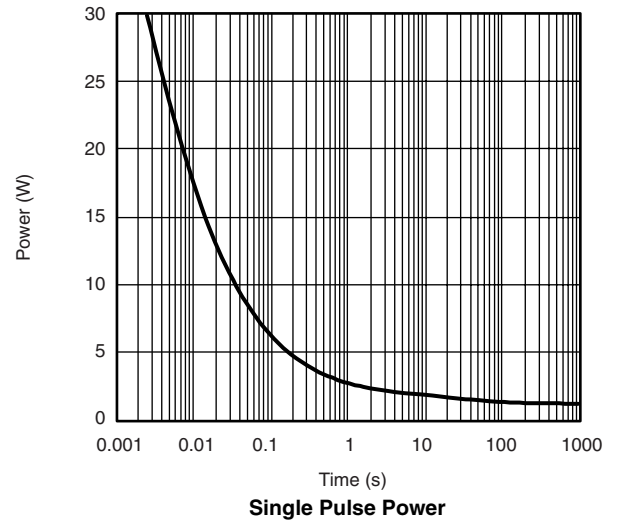
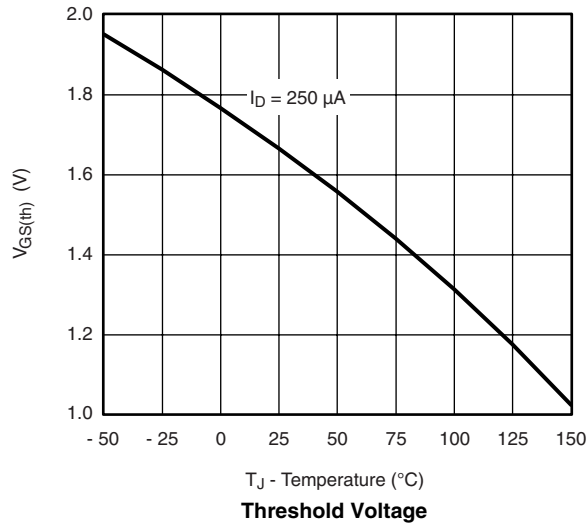
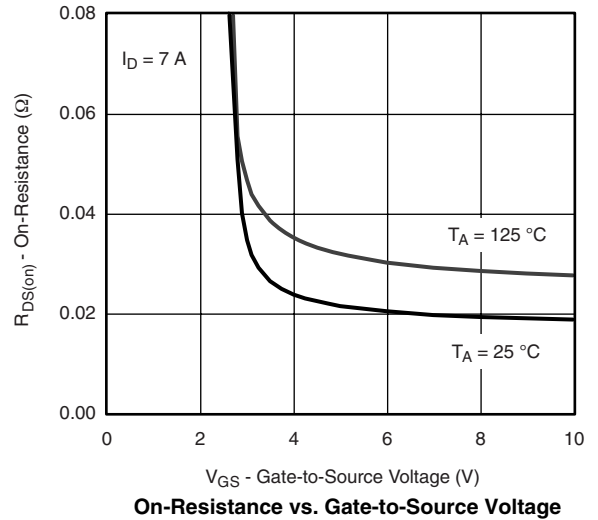
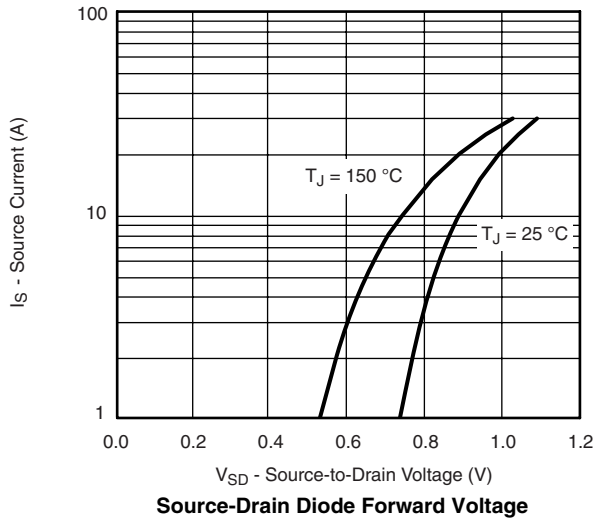
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

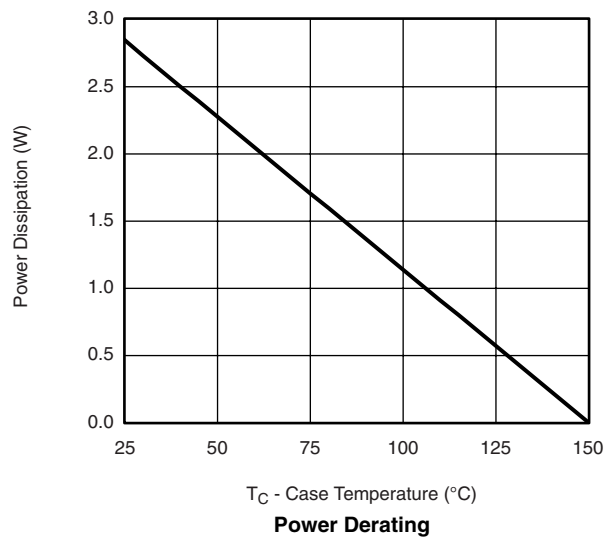
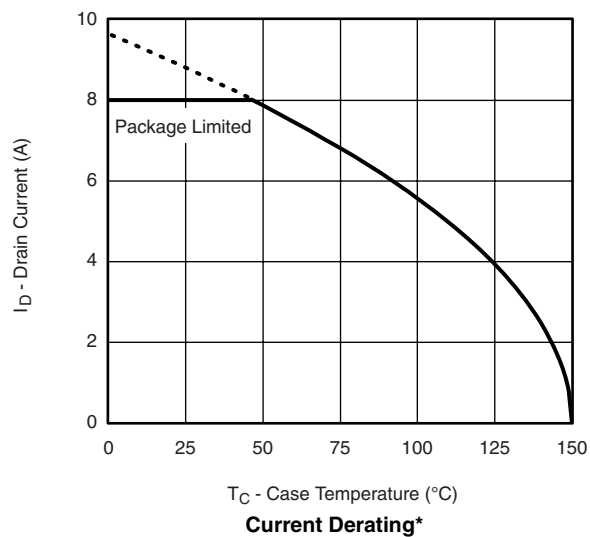
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



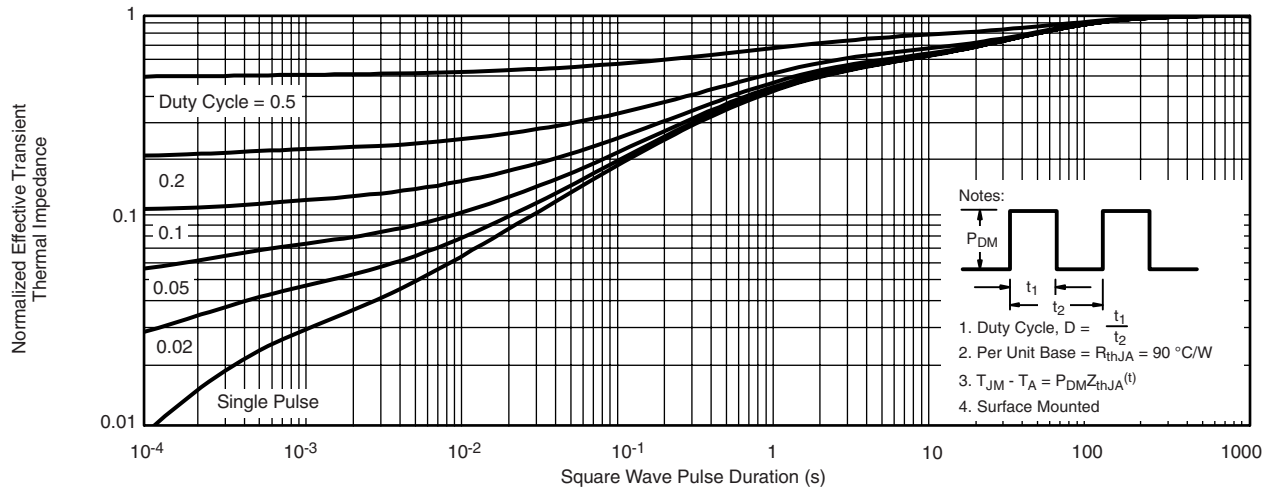
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

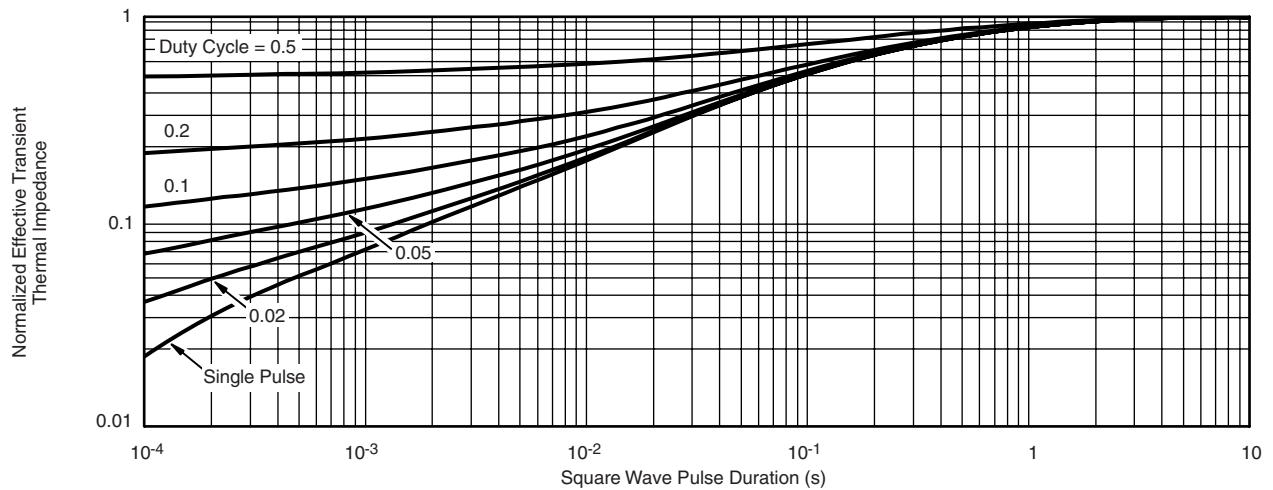
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

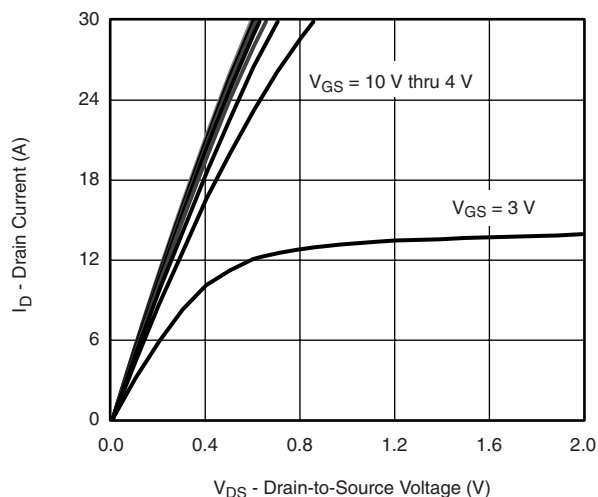
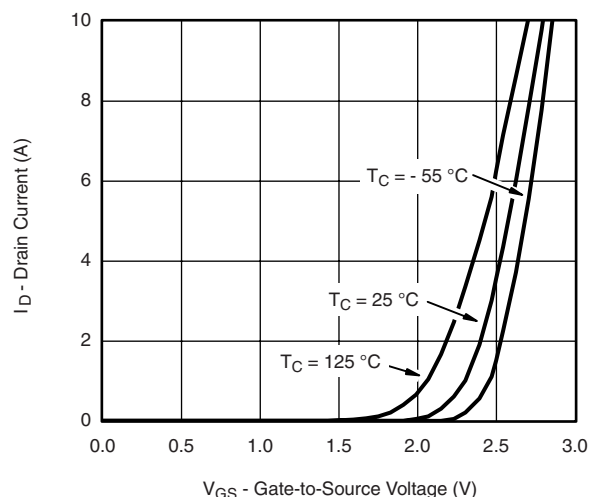
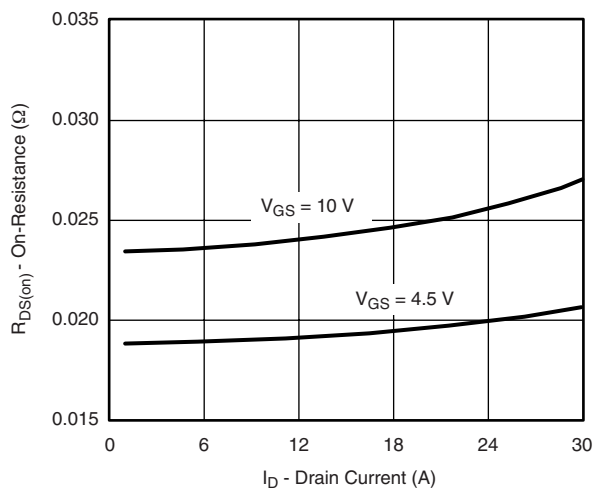
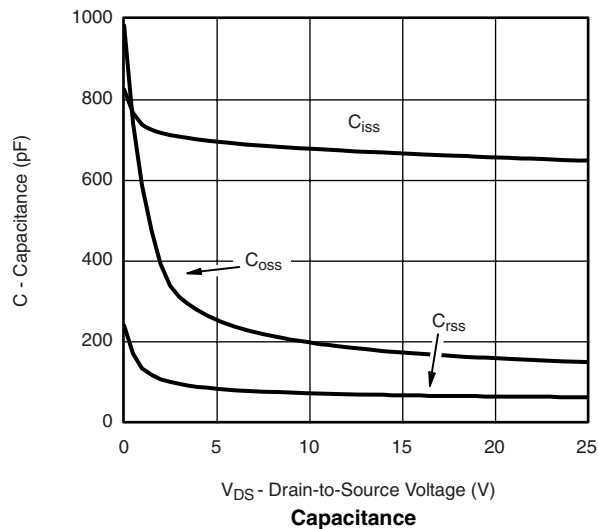
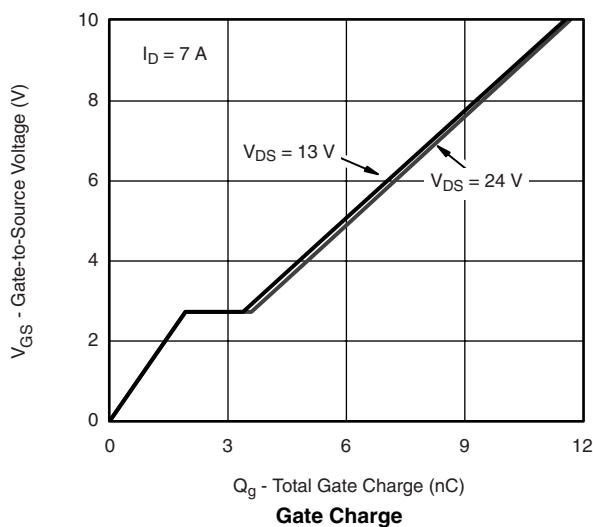
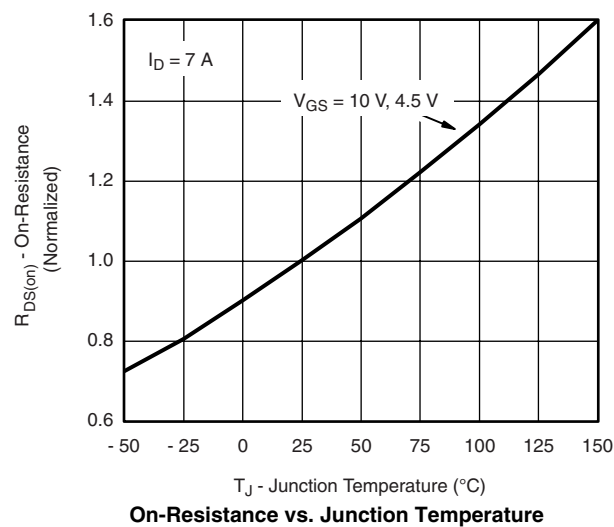
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



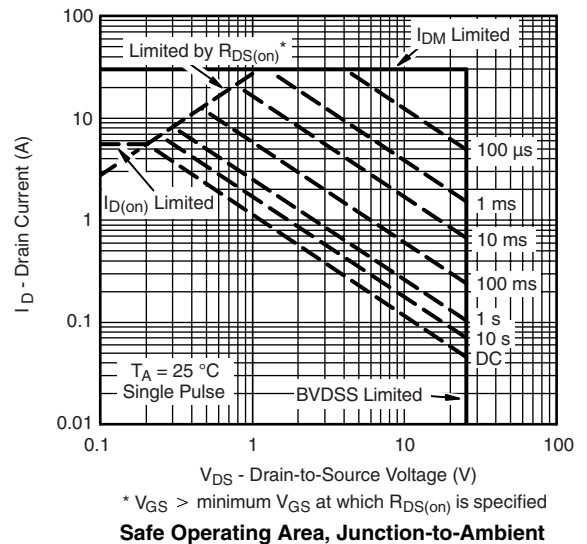
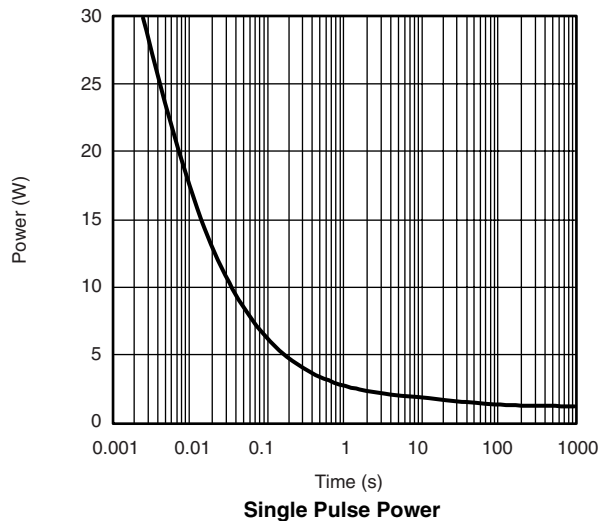
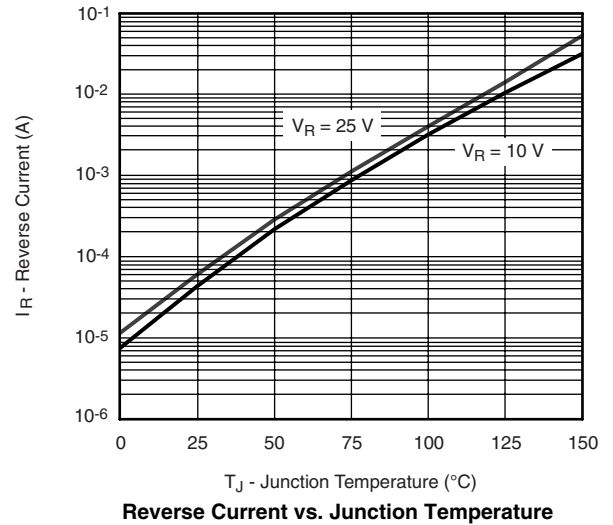
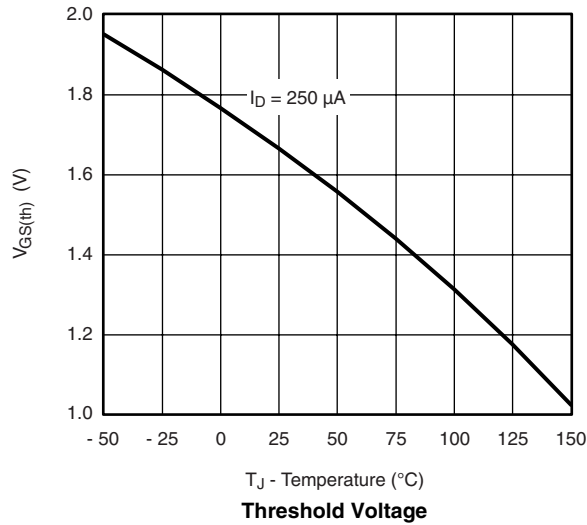
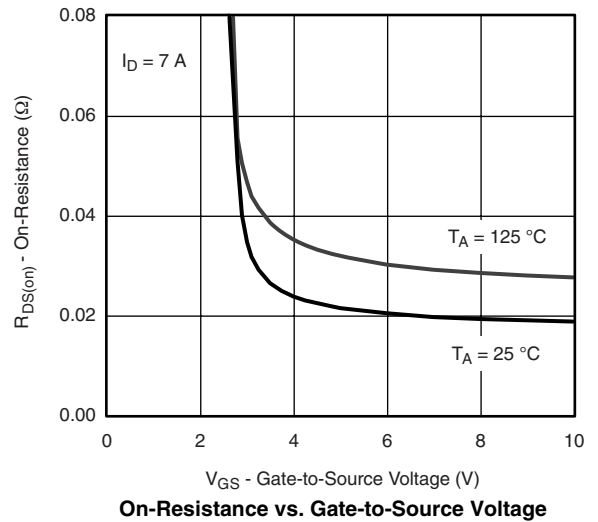
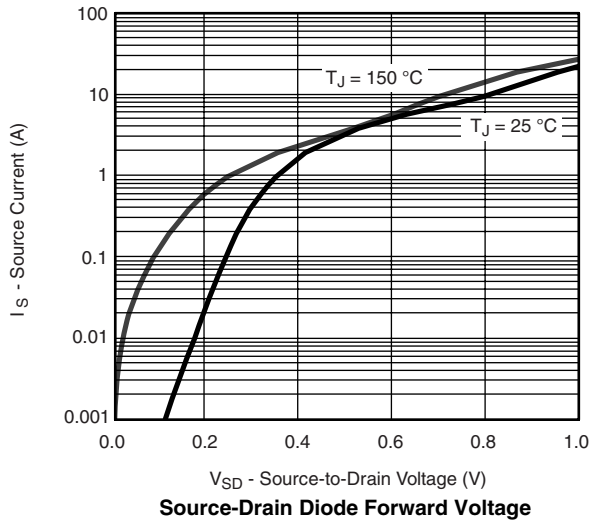
Normalized Thermal Transient Impedance, Junction-to-Ambient

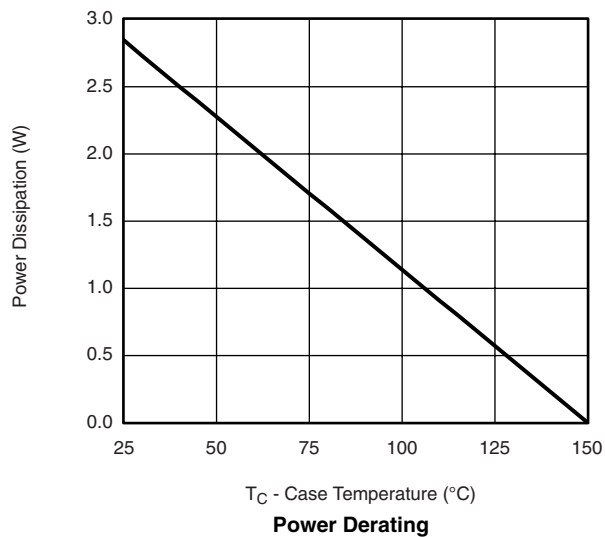
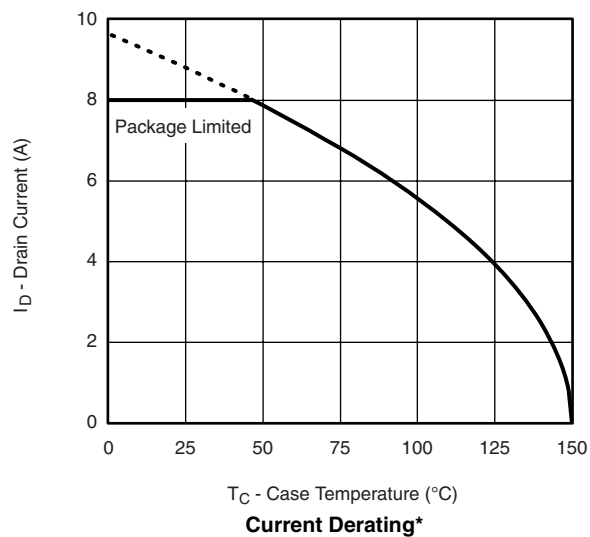


Normalized Thermal Transient Impedance, Junction-to-Foot

CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

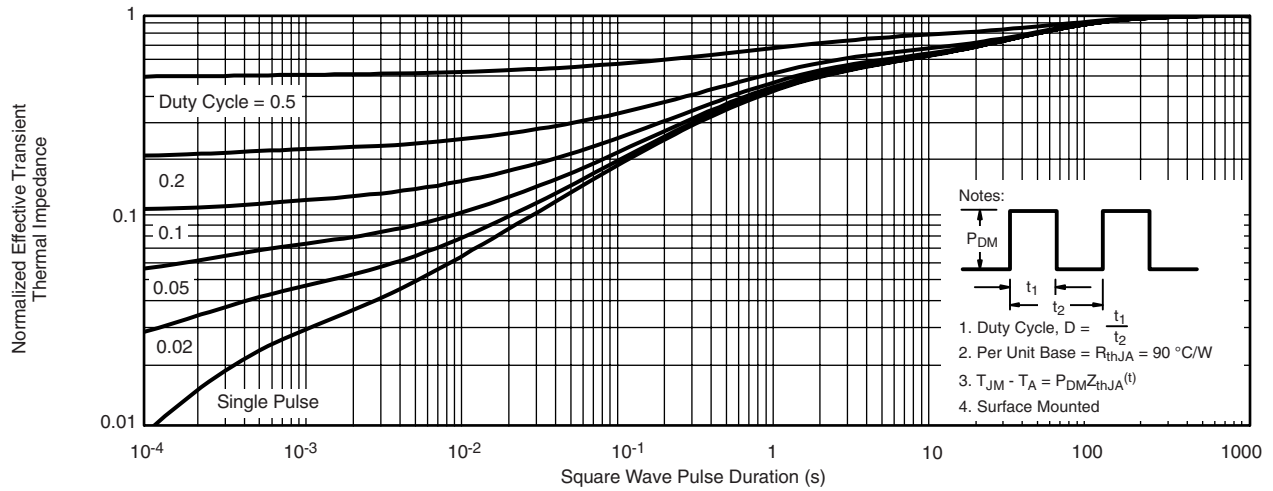
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



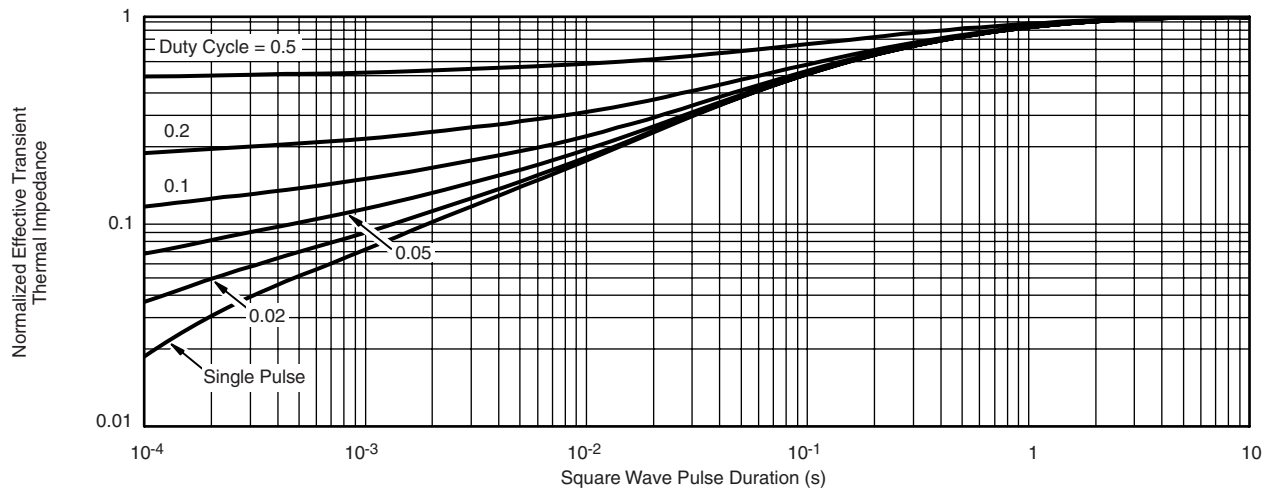
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69595.

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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