

## EL4340, EL4342

500MHz Triple Multiplexing Amplifiers

FN7421  
Rev.4.00  
Oct 4, 2017

The [EL4340](#), [EL4342](#) are fixed unity gain mux amps featuring high slew rates and excellent bandwidth for video switching. These devices feature a high impedance output state (HIZ) that enables the outputs of multiple devices to be wired together. A power-down mode ( $\overline{\text{ENABLE}}$ ) is included to turn off un-needed circuitry in power sensitive applications. The  $\overline{\text{ENABLE}}$  pin, when pulled high, sets the EL4340, EL4342 into standby power mode - consuming just 18mW. An added feature in the EL4340 is a latch enable function ( $\overline{\text{LE}}$ ) that allows independent logic control using a common logic bus.

### Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #
EL4340IUZ	EL4340IUZ	24 Ld QSOP	MDP0040
EL4342ILZA	4342ILZ	32 Ld 5x6 QFN	L32.5x6A
EL4340IUZ-EVAL	Evaluation Board		
EL4342ILZA-EVAL	Evaluation Board		

**NOTES:**

1. Add "-T13" suffix for 2.5k unit or "-T7" suffix for 1k unit tape and reel options. Refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see product information page for [EL4340](#), [EL4342](#). For more information on MSL, refer to [TB363](#).

### Related Literature

- For a full list of related documents, visit our website - [EL4340](#), [EL4342](#) product pages

### Features

- Triple 2:1 and 4:1 multiplexers for RGB
- Internally set gain-of-1
- High speed three-state outputs (HIZ)
- Power-down mode ( $\overline{\text{ENABLE}}$ )
- Latch enable (EL4340)
- $\pm 5\text{V}$  operation
- $\pm 870 \text{ V}/\mu\text{s}$  slew rate
- 500MHz bandwidth
- Typical supply currents 10mA/ch (EL4340) and 15.3mA/ch (EL4342)
- Pb-free (RoHS compliant)

### Applications

- HDTV/DTV analog inputs
- Video projectors
- Computer monitors
- Set-top boxes
- Security video
- Broadcast video equipment

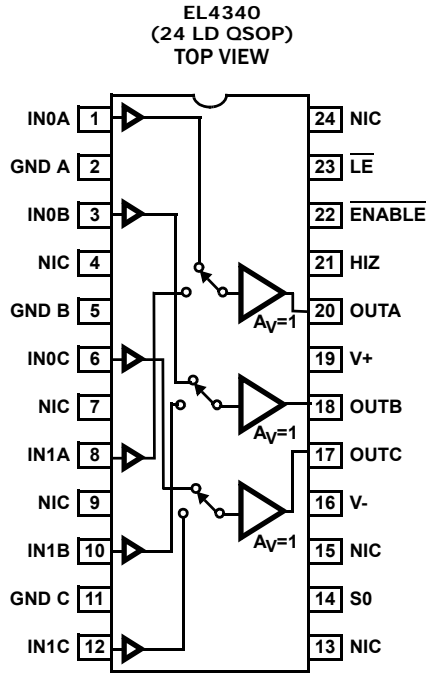
**TABLE 1. CHANNEL SELECT LOGIC TABLE EL4340**

S0	ENABLE	HIZ	$\overline{\text{LE}}$	OUTPUT
0	0	0	0	IN0 (A, B, C)
1	0	0	0	IN1 (A, B, C)
X	1	X	X	Power-down
X	0	1	X	High Z
X	0	0	1	Last S0 State Preserved

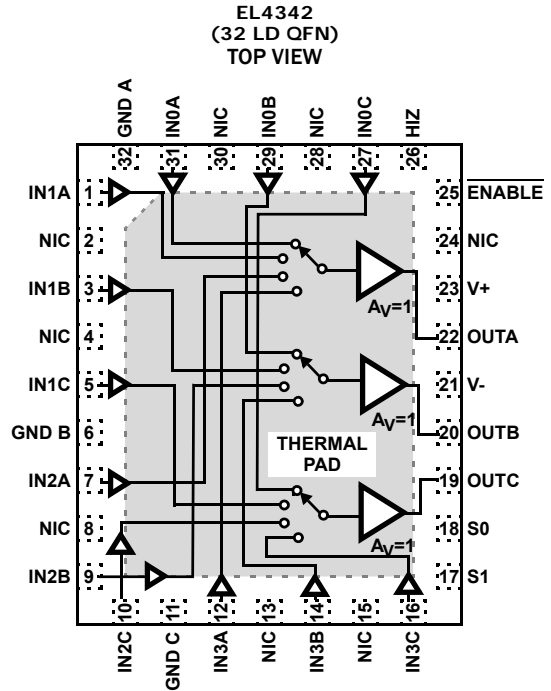
**TABLE 2. CHANNEL SELECT LOGIC TABLE EL4342**

S1	S0	ENABLE	HIZ	OUTPUT
0	0	0	0	IN0 (A, B, C)
0	1	0	0	IN1 (A, B, C)
1	0	0	0	IN2 (A, B, C)
1	1	0	0	IN3 (A, B, C)
X	X	1	X	Power-down
X	X	0	1	High Z

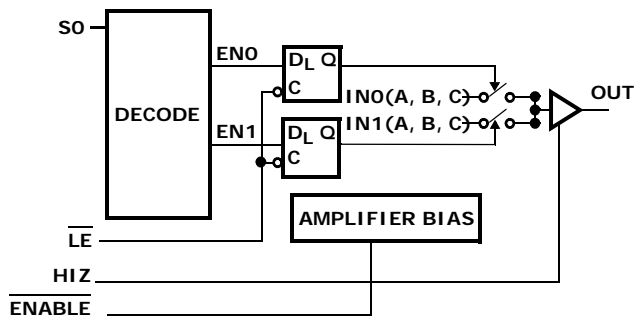
# Pin Configurations



LATCHED ON HIGH  $\overline{LE}$   
 NIC = NO INTERNAL CONNECTION



THERMAL PAD INTERNALLY CONNECTED TO V-.  
 PAD MUST BE TIED TO V-  
 NIC = NO INTERNAL CONNECTION



A LOGIC HIGH ON  $\overline{LE}$  WILL LATCH THE LAST S0 STATE.  
 THIS LOGIC STATE IS PRESERVED WHEN CYCLING HIZ  
 OR ENABLE FUNCTIONS.

FIGURE 1. FUNCTIONAL DIAGRAM EL4340

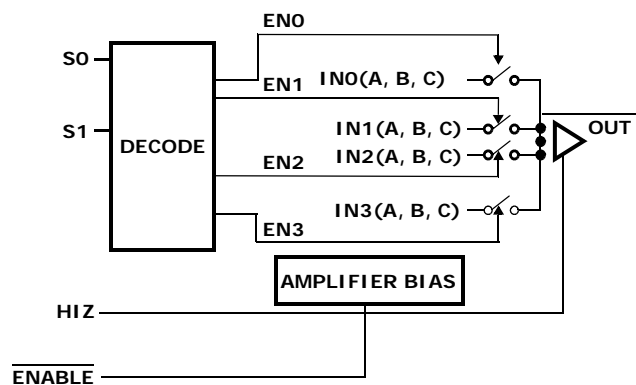
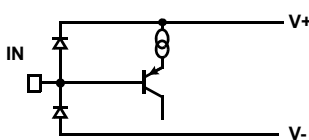


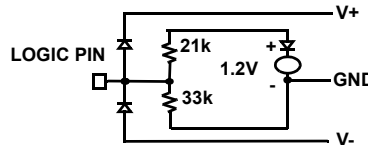
FIGURE 2. FUNCTIONAL DIAGRAM EL4342

## Pin Descriptions

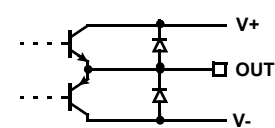
EL4342 (32 Ld QFN)	EL4340 (24 Ld QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	8	IN1A	Circuit 1	Channel 1 input for output amplifier "A"
2, 4, 8, 13, 15, 24, 28, 30	4, 7, 9, 13, 15, 24	NIC		Not Internally Connected; it is recommended these pins be tied to ground to minimize crosstalk.
3	10	IN1B	Circuit 1	Channel 1 input for output amplifier "B"
5	12	IN1C	Circuit 1	Channel 1 input for output amplifier "C"
6	5	GNDB	Circuit 4	Ground pin for output amplifier "B"
7	NA	IN2A	Circuit 1	Channel 2 input for output amplifier "A"
9	NA	IN2B	Circuit 1	Channel 2 input for output amplifier "B"
10	NA	IN2C	Circuit 1	Channel 2 input for output amplifier "C"
11	11	GNDC	Circuit 4	Ground pin for output amplifier "C"
12	NA	IN3A	Circuit 1	Channel 3 input for output amplifier "A"
14	NA	IN3B	Circuit 1	Channel 3 input for output amplifier "B"
16	NA	IN3C	Circuit 1	Channel 3 input for output amplifier "C"
17	NA	S1	Circuit 2	Channel selection pin MSB (binary logic code)
18	14	S0	Circuit 2	Channel selection pin. LSB (binary logic code)
19	17	OUTC	Circuit 3	Output of amplifier "C"
20	18	OUTB	Circuit 3	Output of amplifier "B"
21	16	V-	Circuit 4	Negative power supply
22	20	OUTA	Circuit 3	Output of amplifier "A"
23	19	V+	Circuit 4	Positive power supply
25	22	ENABLE	Circuit 2	Device enable (active low). Internal pull-down resistor ensures the device will be active with no connection to this pin. A logic High on this pin puts device into power-down mode. In power-down mode only logic circuitry is active. All logic states are preserved post power-down. This state is not recommended for logic control where more than one MUX-amp share the same video output line.
-	23	LE	Circuit 2	Device latch enable on the EL4340. A logic high on LE will latch the last (S0, S1) logic state. HIZ and ENABLE functions are not latched with the LE pin.
26	21	HIZ	Circuit 2	Output disable (active high). Internal pull-down resistor ensures the device will be active with no connection to this pin. A logic high, puts the outputs in a high impedance state. Use this state to control logic when more than one MUX-amp share the same video output line.
27	6	INOC	Circuit 1	Channel 0 for output amplifier "C"
29	3	INOB	Circuit 1	Channel 0 for output amplifier "B"
31	1	INOA	Circuit 1	Channel 0 for output amplifier "A"
32	2	GNDA	Circuit 4	Ground pin for output amplifier "A"



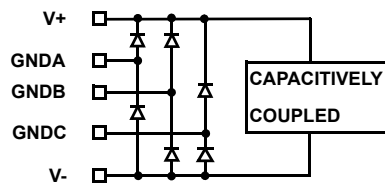
CIRCUIT 1



CIRCUIT 2

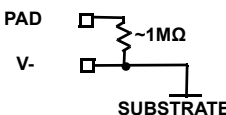


CIRCUIT 3



CIRCUIT 4

THERMAL HEAT SINK PAD



**Absolute Maximum Ratings** (T<sub>A</sub> = +25 °C)

Supply Voltage (V+ to V-)	11V
Input Voltage	V -0.5V, V+ +0.5V
Supply Turn-On Slewing Rate	1V/μs
Digital & Analog Input Current (Note 6)	50mA
Output Current (Continuous)	50mA
<b>ESD Rating</b>	
Human Body Model (Per MIL-STD-883 Method 3015.7)	2500V
Machine Model	300V

**Thermal Information**

Thermal Resistance (Typical)	θ <sub>JA</sub> (°C/W)	θ <sub>JC</sub> (°C/W)
32 Ld QFN Package (Notes 4, 5)	35	1.3 to 8
24 Ld QSOP Package (Note 4)	88	N/A
Storage Temperature Range	-65 °C to +150 °C	
Ambient Operating Temperature	-40 °C to +85 °C	
Operating Junction Temperature	-40 °C to +125 °C	
Power Dissipation	See Curves	
Pb-free reflow profile	see <a href="#">TB493</a>	

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

**NOTES:**

- θ<sub>JA</sub> is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. Refer to [TB379](#).
- For θ<sub>JC</sub>, the “case temp” location is the center of the exposed metal pad on the package underside.
- If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T<sub>J</sub> = T<sub>C</sub> = T<sub>A</sub>*

**Electrical Specifications** V+ = +5V, V- = -5V, GND = 0V, T<sub>A</sub> = +25 °C, Input Video = 1V<sub>p-p</sub> and R<sub>L</sub> = 500Ω to GND, C<sub>L</sub> = 5pF unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>GENERAL</b>						
Enabled Supply Current (EL4340)	+I <sub>S</sub> Enabled	No load, V <sub>IN</sub> = 0V, $\overline{\text{Enable}}$ Low	21.5	30	34	mA
Enabled Supply Current (EL4342)			39	46	50	mA
Enabled Supply Current (EL4340)	-I <sub>S</sub> Enabled	No load, V <sub>IN</sub> = 0V, $\overline{\text{Enable}}$ Low	-32	-30	-21	mA
Enabled Supply Current (EL4342)			-48	-46	-36.5	mA
Disabled Supply Current (EL4340)	+I <sub>S</sub> Disabled	No load, V <sub>IN</sub> = 0V, $\overline{\text{Enable}}$ High	1.75	2.8	4.2	mA
Disabled Supply Current (EL4342)		No load, V <sub>IN</sub> = 0V, $\overline{\text{Enable}}$ High	3	3.5	4	mA
Disabled Supply Current	-I <sub>S</sub> Disabled	No load, V <sub>IN</sub> = 0V, $\overline{\text{Enable}}$ High		10	100	μA
Positive and Negative Output Swing	V <sub>OUT</sub>	V <sub>IN</sub> = ±3.5V, R <sub>L</sub> = 500Ω	±3.1	±3.4		V
Output Current	I <sub>OUT</sub>	R <sub>L</sub> = 10Ω to GND	±80	±135		mA
Output Offset Voltage (EL4340)	V <sub>OS</sub>		-15	7	+15	mV
Output Offset Voltage (EL4342)	V <sub>OS</sub>		-10		+10	mV
Input Bias Current	I <sub>b</sub>	V <sub>IN</sub> = 0V	-0.5	-2	-3	μA
HIZ Output Resistance	R <sub>OUT</sub>	HIZ = Logic High		1.4		MΩ
Enabled Output Resistance	R <sub>OUT</sub>	HIZ = Logic Low		0.2		Ω
Input Resistance	R <sub>IN</sub>	V <sub>IN</sub> = ±3.5V		10		MΩ
Voltage Gain	A <sub>CL</sub> or A <sub>v</sub>	V <sub>IN</sub> = ±1.5V, R <sub>L</sub> = 500Ω	0.98	0.99	1.02	V/V
Output Current in Three-State	I <sub>TRI</sub>	V <sub>OUT</sub> = 0V	8	15	22	μA
<b>LOGIC</b>						
Input High Voltage (Logic Inputs)	V <sub>IH</sub>		2			V
Input Low Voltage (Logic Inputs)	V <sub>IL</sub>				0.8	V
Input High Current (Logic Inputs)	I <sub>IH</sub>	V <sub>H</sub> = 5V	215	270	340	μA
Input Low Current (Logic Inputs)	I <sub>IL</sub>	V <sub>L</sub> = 0V		2	3	μA
<b>AC GENERAL</b>						
0.1% Settling Time	t <sub>S</sub>	Step = 1V		10		ns
Power Supply Rejection Ratio	PSRR (EL4340)	DC, PSRR V+ and V- combined	52	72		dB
Power Supply Rejection Ratio	PSRR (EL4342)	DC, PSRR V+ and V- combined	52	56		dB

**Electrical Specifications**  $V_+ = +5V, V_- = -5V, GND = 0V, T_A = +25^\circ C$ , Input Video =  $1V_{p-p}$  and  $R_L = 500\Omega$  to GND,  $C_L = 5pF$  unless otherwise specified. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Channel Isolation	ISO	$f = 10MHz$ , Ch-Ch X-Talk and Off-Isolation, $C_L = 1.5pF$		75		dB	
Differential Gain Error	dG	NTC-7, $R_L = 150, C_L = 1.5pF$		0.02		%	
Differential Phase Error	dP	NTC-7, $R_L = 150, C_L = 1.5pF$		0.02		°	
-3dB Bandwidth	BW	$C_L = 1.5pF$		500		MHz	
0.1dB Bandwidth	FBW	$C_L = 1.5pF$		60		MHz	
0.1dB Bandwidth		$C_L = 4.7pF$		120		MHz	
Slew Rate	SR	25% to 75%, $R_L = 150\Omega$ , Input Enabled, $C_L = 1.5pF$		$\pm 870$		$V/\mu s$	
<b>SWITCHING CHARACTERISTICS</b>							
Channel-to-Channel Switching Glitch	$V_{GLITCH}$	$V_{IN} = 0V, C_L = 1.5pF$		40		$mV_{p-p}$	
Enable Switching Glitch		EL4340	$V_{IN} = 0V, C_L = 1.5pF$		300		$mV_{p-p}$
HIZ Switching Glitch			$V_{IN} = 0V, C_L = 1.5pF$		200		$mV_{p-p}$
Channel-to-Channel Switching Glitch	$V_{GLITCH}$	$V_{IN} = 0V, C_L = 1.5pF$		20		$mV_{p-p}$	
Enable Switching Glitch		EL4342	$V_{IN} = 0V, C_L = 1.5pF$		200		$mV_{p-p}$
HIZ Switching Glitch			$V_{IN} = 0V, C_L = 1.5pF$		200		$mV_{p-p}$
Channel Switching Time Low to High	$t_{SW-L-H}$	1.2V logic threshold to 10% movement of analog output		18		ns	
Channel Switching Time High to Low	$t_{SW-H-L}$	1.2V logic threshold to 10% movement of analog output		20		ns	
Rise and Fall Time	tr, tf	10% to 90%		1.1		ns	
Propagation Delay	tpd	10% to 10%		0.9		ns	
Latch Enable Hold time (EL4340 only)	$t_{LH}$	$\overline{LE} = 0$		10		ns	

**Typical Performance Curves**  $V_S = \pm 5V, R_L = 500\Omega$  to GND,  $T_A = +25^\circ C$ , unless otherwise specified.

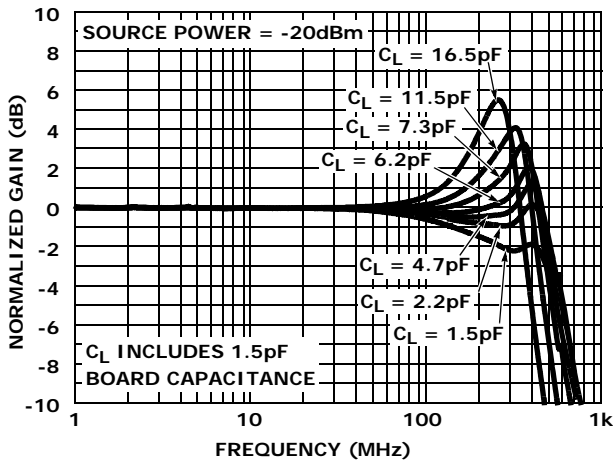


FIGURE 3. GAIN vs FREQUENCY vs  $C_L$

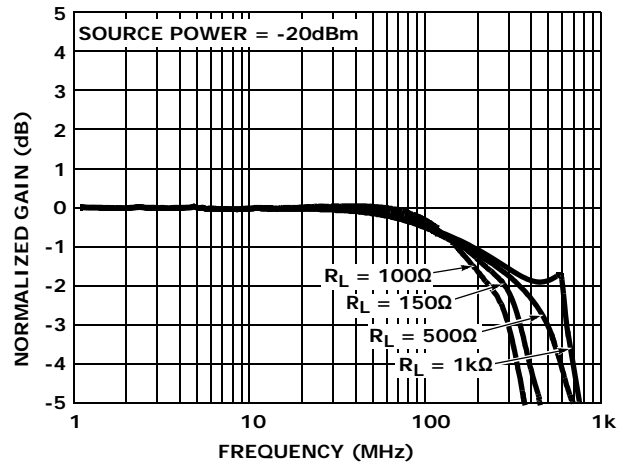


FIGURE 4. GAIN vs FREQUENCY vs  $R_L$

**Typical Performance Curves**  $V_S = \pm 5V$ ,  $R_L = 500\Omega$  to GND,  $T_A = +25^\circ C$ , unless otherwise specified. (Continued)

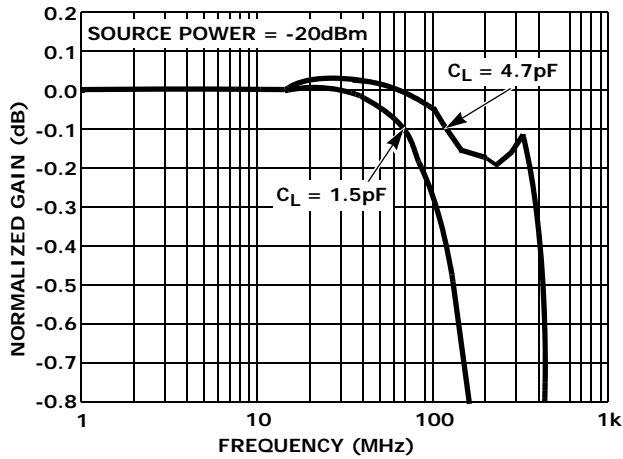


FIGURE 5. 0.1dB GAIN vs FREQUENCY

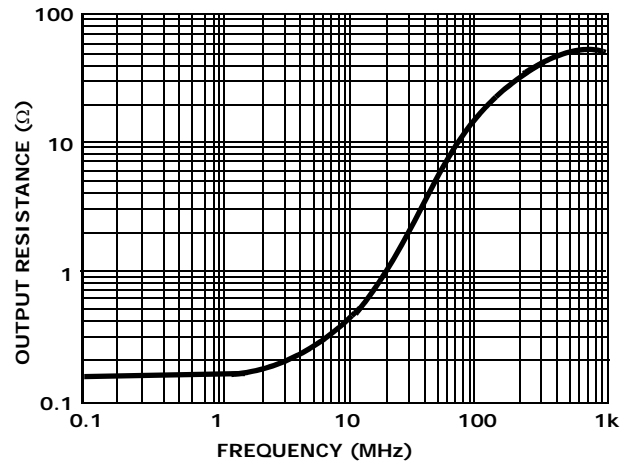


FIGURE 6.  $R_{OUT}$  vs FREQUENCY

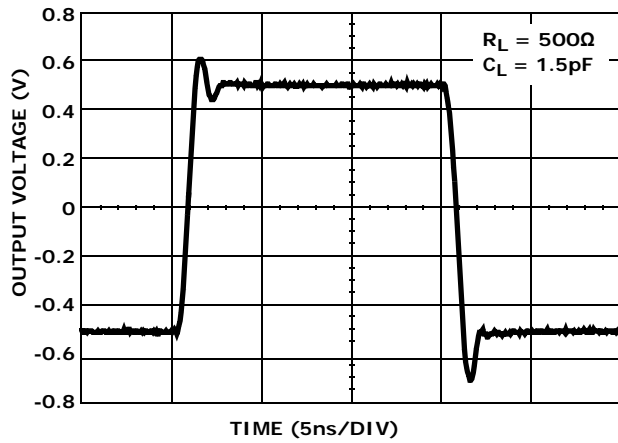


FIGURE 7. EL4340 TRANSIENT RESPONSE

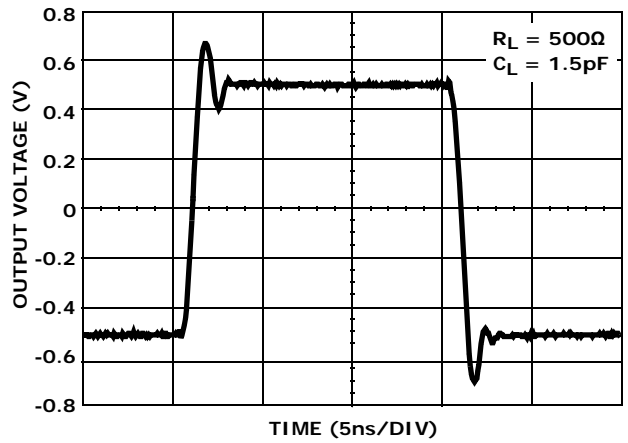


FIGURE 8. EL4342 TRANSIENT RESPONSE

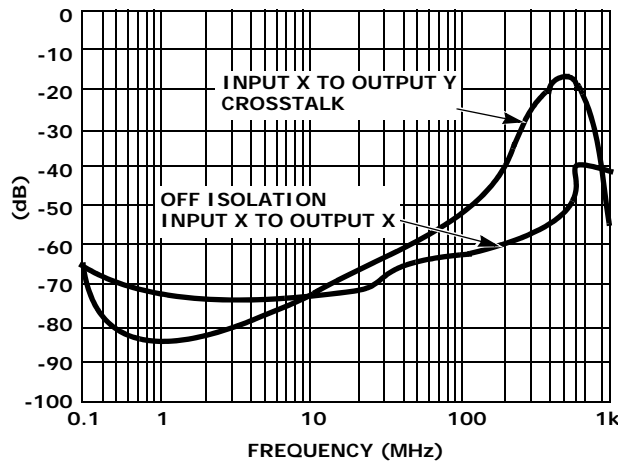


FIGURE 9. EL4340 CROSSTALK AND OFF-ISOLATION

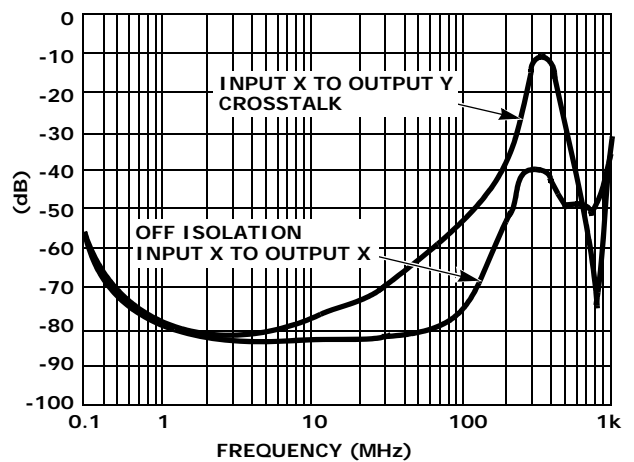


FIGURE 10. EL4342 CROSSTALK AND OFF-ISOLATION

**Typical Performance Curves**  $V_S = \pm 5V$ ,  $R_L = 500\Omega$  to GND,  $T_A = +25^\circ C$ , unless otherwise specified. (Continued)

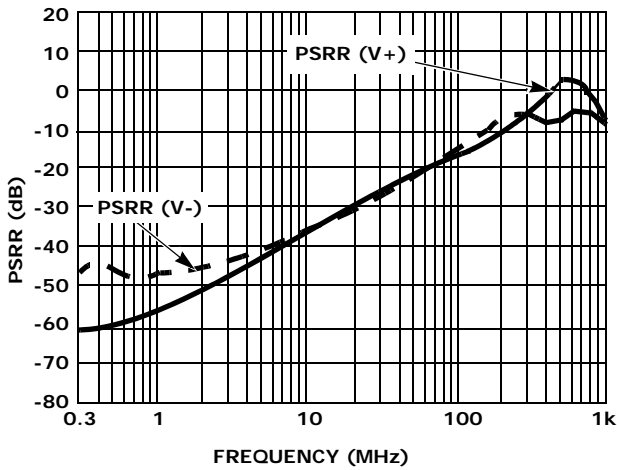


FIGURE 11. EL4340 PSRR CHANNELS A, B, C

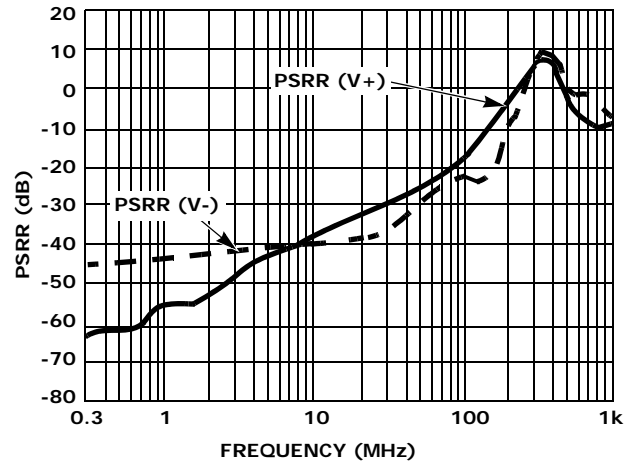


FIGURE 12. EL4342 PSRR CHANNELS A, B, C

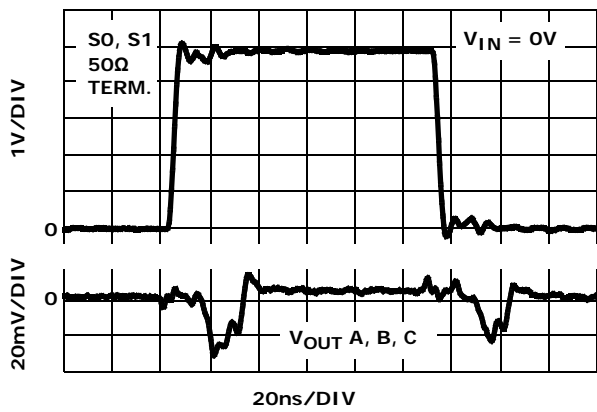


FIGURE 13. CHANNEL TO CHANNEL SWITCHING GLITCH  $V_{IN} = 0V$

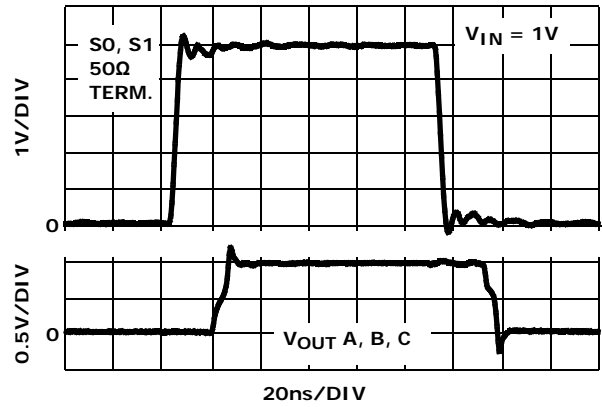


FIGURE 14. CHANNEL TO CHANNEL TRANSIENT RESPONSE  $V_{IN} = 1V$

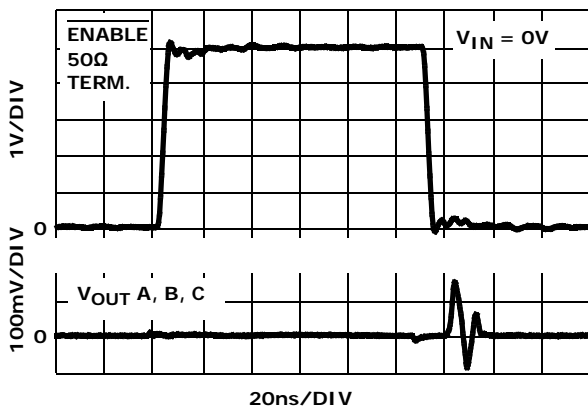


FIGURE 15. ENABLE SWITCHING GLITCH  $V_{IN} = 0V$

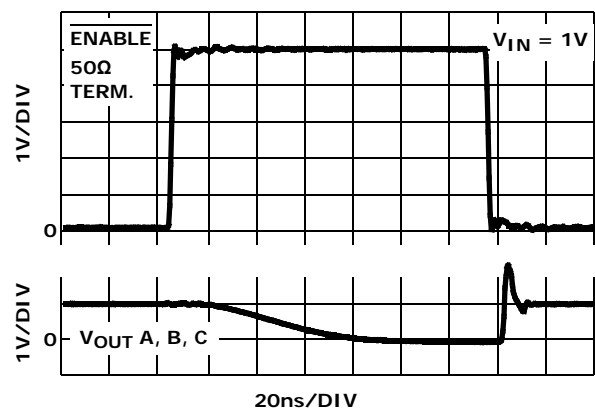


FIGURE 16. ENABLE TRANSIENT RESPONSE  $V_{IN} = 1V$

**Typical Performance Curves**  $V_S = \pm 5V$ ,  $R_L = 500\Omega$  to GND,  $T_A = +25^\circ C$ , unless otherwise specified. (Continued)

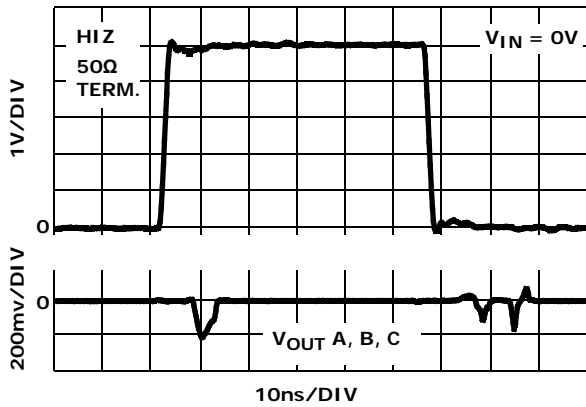


FIGURE 17. HIZ SWITCHING GLITCH  $V_{IN} = 0V$

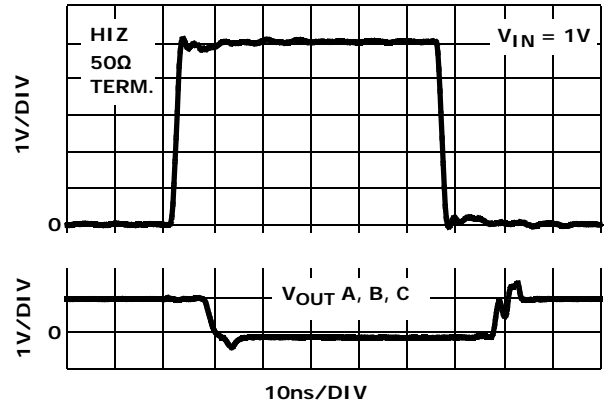


FIGURE 18. HIZ TRANSIENT RESPONSE  $V_{IN} = 1V$

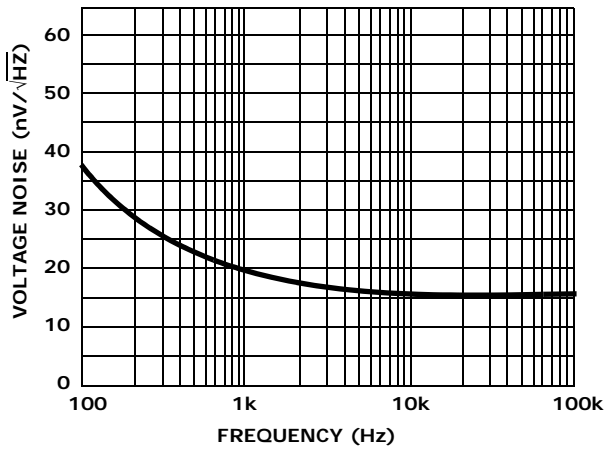


FIGURE 19. INPUT NOISE vs FREQUENCY (OUTPUT A, B, C)

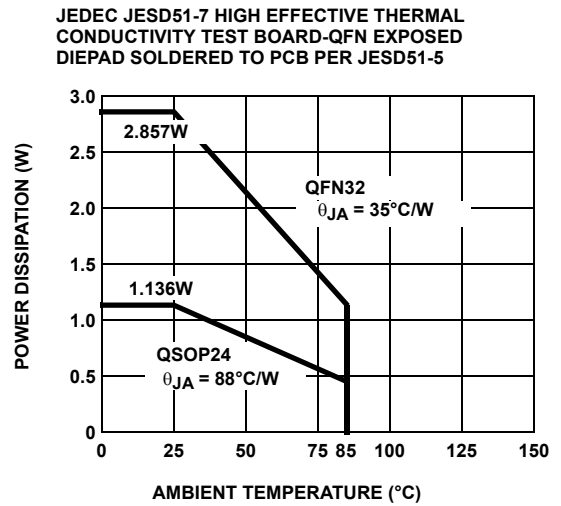


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

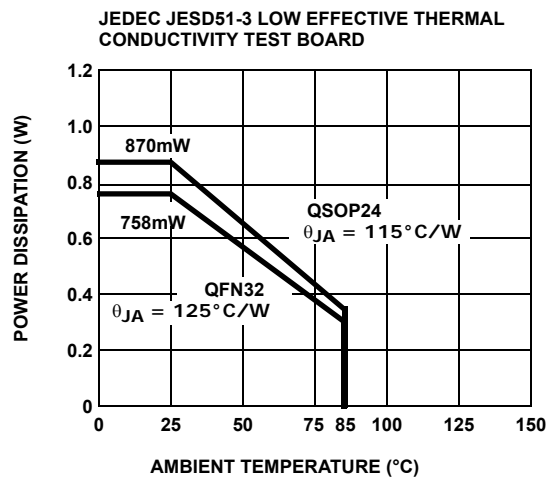


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE



## AC Test Circuits

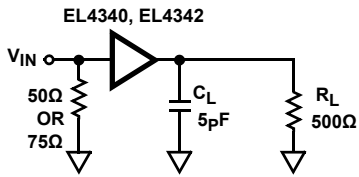


FIGURE 22A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD

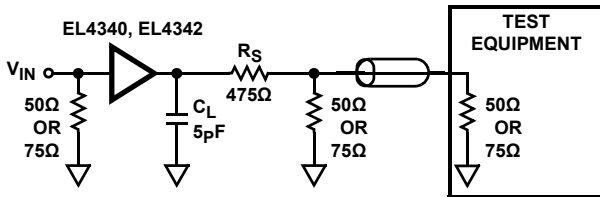


FIGURE 22B. TEST CIRCUIT FOR MEASURING WITH 50Ω OR 75Ω INPUT TERMINATED EQUIPMENT

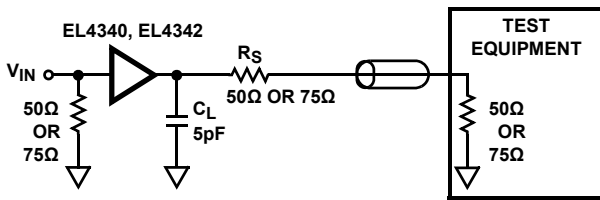


FIGURE 22C. BACKLOADED TEST CIRCUIT FOR VIDEO CABLE APPLICATION. BANDWIDTH AND LINEARITY FOR  $R_L$  LESS THAN 500Ω WILL BE DEGRADED.

FIGURE 22. TEST CIRCUITS

Figure 22A illustrates the optimum output load for testing AC performance. Figure 22B illustrates the optimum output load when connecting to 50Ω input terminated equipment.

## Application Information

### General

The EL4340, EL4342 triple 2:1 and 4:1 MUX amps are ideal as the matrix element of high performance switchers and routers. Key features include buffered high impedance analog inputs and excellent AC performance at output loads down to 150Ω for

video cable-driving. The unity-gain current feedback output amplifiers are stable operating into capacitive loads and bandwidth is optimized with a load of 5pF in parallel with a 500Ω. Total output capacitance can be split between the PCB capacitance and an external load capacitor.

### Ground Connections

For the best isolation and crosstalk rejection, all GND pins and NIC pins must connect to the GND plane.

### Control Signals

S0, S1, ENABLE, LE, HIZ - These are binary coded, TTL/CMOS compatible control inputs. The S0, S1 pins select the inputs. All three amplifiers are switched simultaneously from their respective inputs. The ENABLE, LE, HIZ pins are used to disable the part to save power, latch in the last logic state and three-state the output amplifiers, respectively. For control signal rise and fall times less than 10ns the use of termination resistors close to the part will minimize transients coupled to the output.

### Power-UP Considerations

The ESD protection circuits use internal diodes from all pins the V+ and V- supplies. In addition, a dV/dT-triggered clamp is connected between the V+ and V- pins, as shown in the Equivalent Circuits 1 through 4 section of the Pin Description table. The dV/dT triggered clamp imposes a maximum supply turn-on slew rate of 1V/μs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/μs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the rate of rise is not exceeded.

Consideration must be given to the order in which power is applied to the V+ and V- pins, as well as analog and logic input pins. Schottky diodes (Motorola MBR0550T or equivalent) connected from V+ to ground and V- to ground (Figure 23) will shunt damaging currents away from the internal V+ and V- ESD diodes in the event that the V+ supply is applied to the device before the V- supply.

If positive voltages are applied to the logic or analog video input pins before V+ is applied, current will flow through the internal ESD diodes to the V+ pin. The presence of large decoupling capacitors and the loading effect of other circuits connected to V+, can result in damaging currents through the ESD diodes and other active circuits within the device. Therefore, adequate current limiting on the digital and analog inputs is needed to prevent damage during the time the voltages on these inputs are more positive than V+.

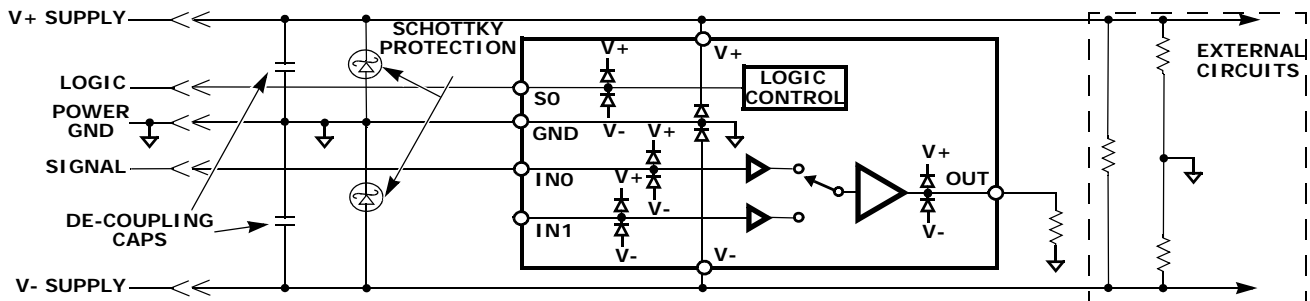


FIGURE 23. SCHOTTKY PROTECTION CIRCUIT

## HIZ State

An internal pull-down resistor ensures the device will be active with no connection to the HIZ pin. The HIZ state is established within approximately 15ns ([Figure 18 on page 8](#)) by placing a logic high (>2V) on the HIZ pin. If the HIZ state is selected, the output is a high impedance 1.4M $\Omega$  with approximately 1.5pF in parallel with a 10 $\mu$ A bias current from the output. Use this state when more than one mux shares a common output.

In the HIZ state the output is three-stated, and maintains its high Z even in the presence of high slew rates. The supply current during this state is same as the active state.

## ENABLE and Power-Down States

The enable pin is active low. An internal pull-down resistor ensures the device will be active with no connection to the ENABLE pin. The Power-down state is established within approximately 80ns ([Figure 16 on page 7](#)), if a logic high (>2V) is placed on the ENABLE pin. In the Power-down state, the output has no leakage but has a large variable capacitance (on the order of 15pF), and is capable of being back-driven. Under this condition, large incoming slew rates can cause fault currents of tens of mA. **Do not use this state as a high impedance output when several MUX amps share the same output line.**

## LE State

The EL4340 is equipped with a Latch Enable pin. A logic high (>2V) on the LE pin latches the last logic state. This logic state is preserved when cycling HIZ or ENABLE functions.

## Limiting the Output Current

No output short-circuit current limit exists on these parts. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

## Application Example

[Figure 24 on page 11](#) illustrates the use of the EL4342, two ISL84517 SPST switches, and one NC7ST00P5X NAND gate to mux 3 different component video signals and one RGB video signal. The SPDT switches provide the sync signal for the RGB video and disconnects the sync signal for the component signal.

## PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components such as chip resistors and chip capacitors is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners, use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High

frequency performance may be degraded for traces greater than one inch, unless strip line are used.

- Match channel-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (for example, no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- Minimum of two power supply de-coupling capacitors are recommended (1000pF, 0.01 $\mu$ F) as close to the devices as possible - Avoid vias between the cap and the device because vias add unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

## The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to V-supply through the high resistance IC substrate. Its primary function is to provide heat sinking for the IC. However, because of the connection to the V-supply through the substrate, the thermal pad must be tied to the V-supply to prevent unwanted current flow to the thermal pad. Do **not** tie this pin to GND as this could result in large back biased currents flowing between GND and V-. The EL4342 uses the package with pad dimensions of D2 = 2.48mm and E2 = 3.4mm.

Maximum AC performance is achieved if the thermal pad is attached to a dedicated de-coupled layer in a multi-layered PC board. In cases where a dedicated layer is not possible, AC performance may be reduced at upper frequencies.

The thermal pad requirements are proportional to power dissipation and ambient temperature. A dedicated layer eliminates the need for individual thermal pad area. When a dedicated layer is not possible a 1" x 1" pad area is sufficient for the EL4342 that is dissipating 0.5W in +50°C ambient. Pad area requirements should be evaluated on a case by case basis.

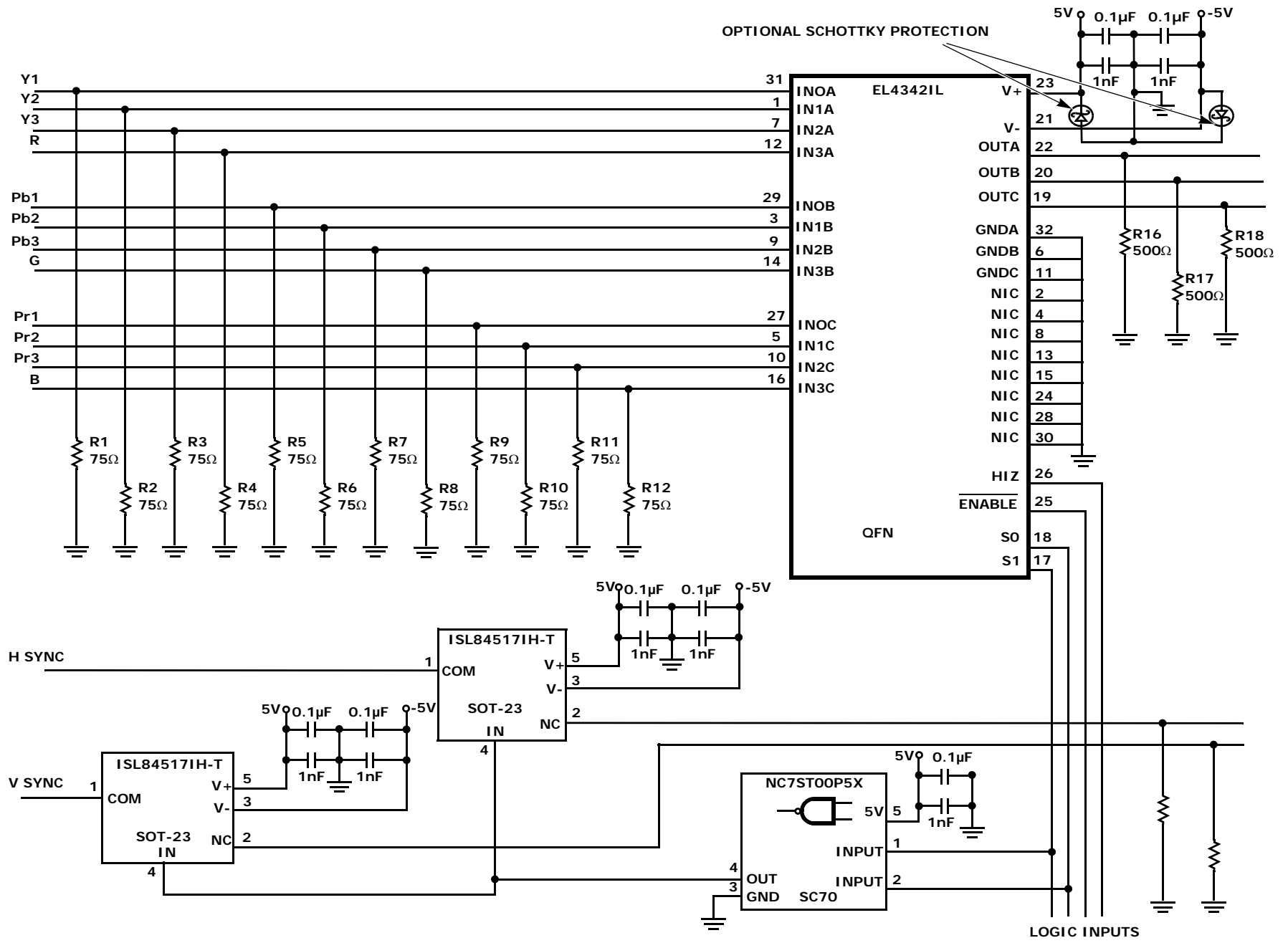


FIGURE 24. APPLICATION SHOWING THREE YBP CHANNELS AND ONE RGB+HV CHANNEL

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Oct 4, 2017	FN7421.4	Applied new header/footer and formatting. Updated Related Literature section Moved Pin descriptions after Pin Configurations. Updated the following specifications in the EC table: +IS Enabled: changed min spec from 26mA to 21.5mA -IS Enabled: changed max spec from -24mA to -21mA +IS Disable Current: changed min spec from 2.3mA to 1.75mA and max spec from 3.3mA to 4.2mA Input Hi Current (I <sub>IH</sub> ): changed max spec from 320μA to 340μA Input Bias Currents: changed min spec from -1μA to -0.5μA Added Revision History and About Intersil sections.

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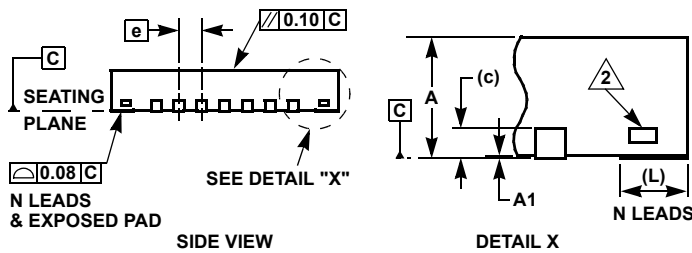
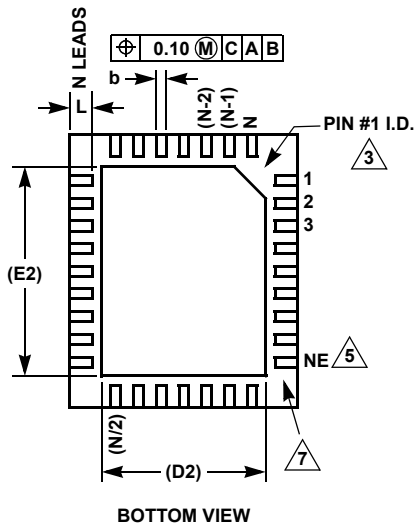
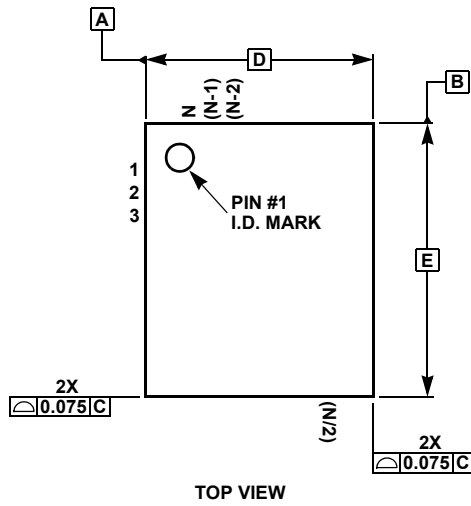
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**Quad Flat No-Lead Plastic Package (QFN)  
Micro Lead Frame Plastic Package (MLFP)**

**L32.5x6A** (One of 10 Packages in MDP0046)  
**32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE  
(COMPLIANT TO JEDEC MO-220)**



SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	0.00	0.02	0.05	-
D	5.00 BSC			-
D2	2.48 REF			-
E	6.00 BSC			-
E2	3.40 REF			-
L	0.45	0.50	0.55	-
b	0.17	0.22	0.27	-
c	0.20 REF			-
e	0.50 BSC			-
N	32 REF			4
ND	7 REF			6
NE	9 REF			5

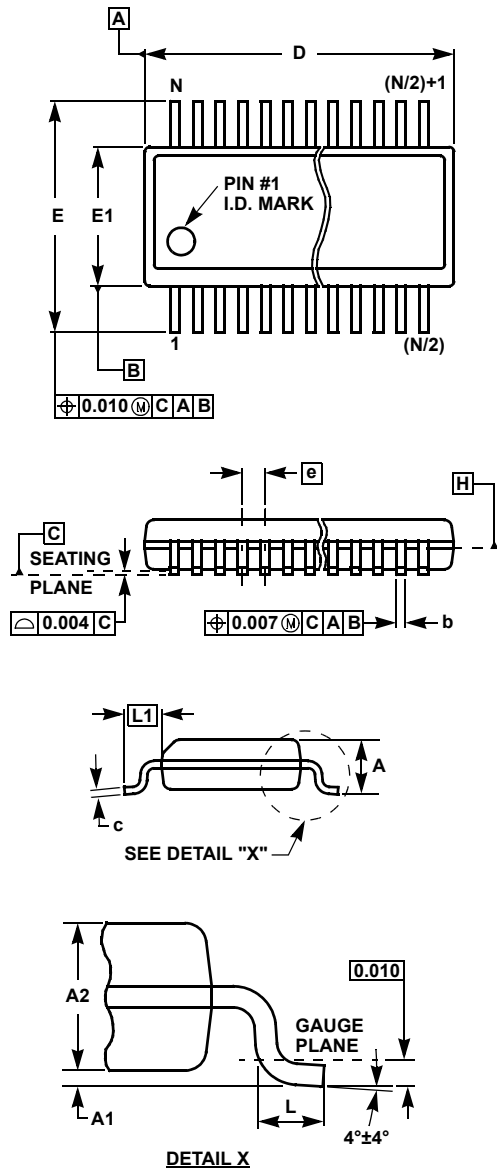
Rev 1 2/09

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y-direction).
6. ND is the number of terminals on the "D" side of the package (or X-direction).  $ND = (N/2) - NE$ .
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.

For the most recent package outline drawing, see [L32.5x6A](#).

**Quarter Size Outline Plastic Packages  
Family (QSOP)**



**MDP0040**

**QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY**

SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	$\pm 0.002$	-
A2	0.056	0.056	0.056	$\pm 0.004$	-
b	0.010	0.010	0.010	$\pm 0.002$	-
c	0.008	0.008	0.008	$\pm 0.001$	-
D	0.193	0.341	0.390	$\pm 0.004$	1, 3
E	0.236	0.236	0.236	$\pm 0.008$	-
E1	0.154	0.154	0.154	$\pm 0.004$	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	$\pm 0.009$	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

For the most recent package outline drawing, see [MDP0040](#).