

# NCV4264

## Linear Regulator, 100 mA, Low Dropout

The NCV4264 is a wide input range, precision 3.3 V and 5.0 V fixed output, low dropout integrated voltage regulator with a full load current rating of 100 mA.

The output voltage is accurate within  $\pm 2.0\%$ , and maximum dropout voltage is 500 mV at 100 mA load current.

It is internally protected against 45 V input transients, input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

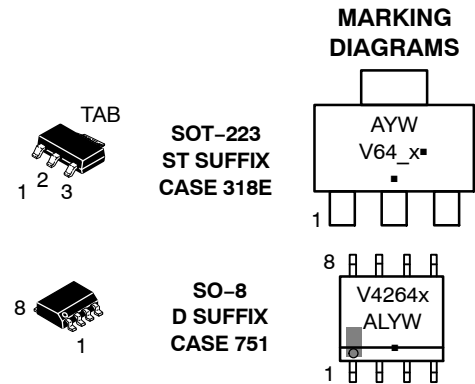
### Features

- 3.3 V and 5.0 V Fixed Output
- $\pm 2.0\%$  Output Accuracy, Over Full Temperature Range
- Quiescent Current 400  $\mu\text{A}$  at  $I_{\text{OUT}} = 1.0 \text{ mA}$
- 500 mV Maximum Dropout Voltage at 100 mA Load Current
- Wide Input Voltage Operating Range of 4.5 V to 45 V
- Internal Fault Protection
  - ◆ -42 V Reverse Voltage
  - ◆ Short Circuit/Overcurrent
  - ◆ Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices



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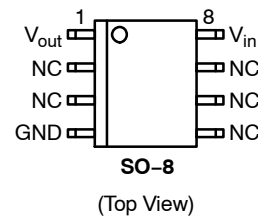
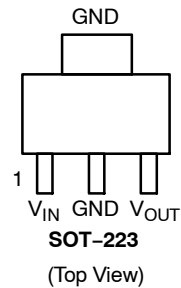
[www.onsemi.com](http://www.onsemi.com)



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- x = 3 (3.3 V Version)
- = 5 (5.0 V Version)
- = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

# NCV4264

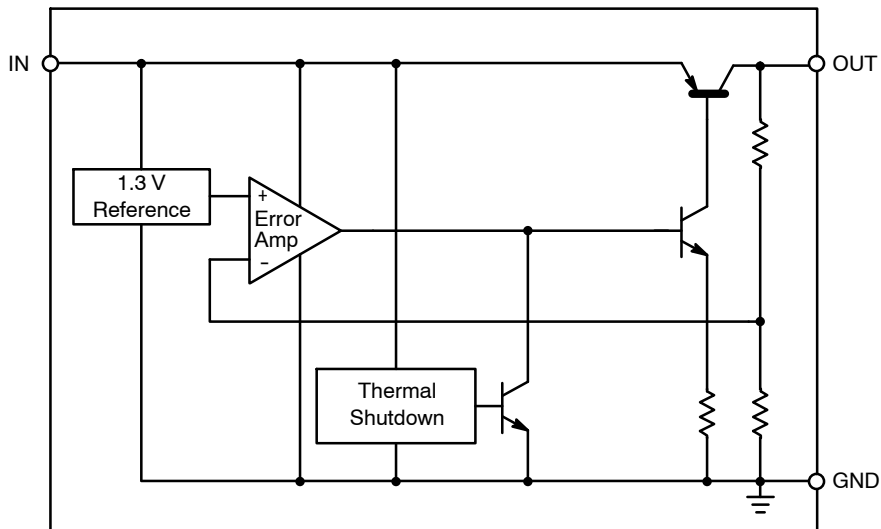


Figure 1. Block Diagram

## PIN FUNCTION DESCRIPTION

Pin No. SOT-223	Pin No. SO-8	Symbol	Function
1	8	$V_{IN}$	Unregulated input voltage; 4.5 V to 45 V.
2	4	GND	Ground; substrate.
3	1	$V_{OUT}$	Regulated output voltage; collector of the internal PNP pass transistor.
TAB	-	GND	Ground; substrate and best thermal connection to the die.
-	2,3,5,6,7	NC	Not Connected

## MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
$V_{IN}$ , DC Input Voltage	$V_{IN}$	-42	+45	V
$V_{OUT}$ , DC Voltage	$V_{OUT}$	-0.3	+16	V
Storage Temperature	$T_{stg}$	-55	+150	°C
Moisture Sensitivity Level	MSL	3 1		-
ESD Capability, Human Body Model (Note 1)	$V_{ESDHB}$	4000	-	V
ESD Capability, Machine Model (Note 1)	$V_{ESDMIM}$	200	-	V
Lead Temperature Soldering Reflow (SMD Styles Only), Lead Free (Note 2)	$T_{sld}$	-	265 pk	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- This device series incorporates ESD protection and is tested by the following methods:  
ESD HBM tested per AEC-Q100-002 (EIA/JESD22-A 114C)  
ESD MM tested per AEC-Q100-003 (EIA/JESD22-A 115C)
- Lead Free, 60 sec – 150 sec above 217°C, 40 sec max at peak.

## OPERATING RANGE

Pin Symbol, Parameter	Symbol	Min	Max	Unit
$V_{IN}$ , DC Input Operating Voltage	$V_{IN}$	4.5	+45	V
Junction Temperature Operating Range	$T_J$	-40	+150	°C

**THERMAL RESISTANCE**

Parameter	Symbol	Min	Max	Unit
Junction-to-Ambient SOT-223	$R_{\theta JA}$	-	99 (Note 3)	°C/W
Junction-to-Case SOT-223	$R_{\theta JC}$	-	17	
Junction-to-Ambient SO-8	$R_{\theta JA}$	-	162 (Note 3)	°C/W
Junction-to-Lead2 SO-8	$\Psi_{JL2}$	-	45	

3. 1 oz., 100 mm<sup>2</sup> copper area.

**ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 13.5\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage 5.0 V Version	$V_{OUT}$	$5.0\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$ (Note 4) $6.0\text{ V} \leq V_{IN} \leq 28\text{ V}$	4.900	5.000	5.100	V
Output Voltage 3.3 V Version	$V_{OUT}$	$5.0\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$ (Note 4) $4.5\text{ V} \leq V_{IN} \leq 28\text{ V}$	3.234	3.300	3.366	V
Line Regulation 5.0 V Version	$\Delta V_{OUT}$ vs. $V_{IN}$	$I_{OUT} = 5.0\text{ mA}$ $6.0\text{ V} \leq V_{IN} \leq 28\text{ V}$	-30	5.0	+30	mV
Line Regulation 3.3 V Version	$\Delta V_{OUT}$ vs. $V_{IN}$	$I_{OUT} = 5.0\text{ mA}$ $4.5\text{ V} \leq V_{IN} \leq 28\text{ V}$	-30	5.0	+30	mV
Load Regulation	$\Delta V_{OUT}$ vs. $I_{OUT}$	$5.0\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$ (Note 4)	-40	5.0	+40	mV
Dropout Voltage 5.0 V Version	$V_{IN}-V_{OUT}$	$I_{OUT} = 100\text{ mA}$ (Notes 4 & 5)	-	275	500	mV
Dropout Voltage 3.3 V Version	$V_{IN}-V_{OUT}$	$I_{OUT} = 100\text{ mA}$ (Notes 4 & 7)	-	-	1.266	V
Quiescent Current	$I_q$	$I_{OUT} = 1.0\text{ mA}$	-	100	400	$\mu\text{A}$
Active Ground Current	$I_{G(ON)}$	$I_{OUT} = 100\text{ mA}$ (Note 4)	-	4	15	mA
Power Supply Rejection	PSRR	$V_{RIPPLE} = 0.5\text{ V}_{P-P}$ , $F = 100\text{ Hz}$	-	67	-	dB
Output Capacitor for Stability 5.0 V Version	$C_{OUT}$ ESR	$I_{OUT} = 1.0\text{ mA}$ to $100\text{ mA}$ (Note 4)	10	-	9.0	$\mu\text{F}$ $\Omega$
Output Capacitor for Stability 3.3 V Version	$C_{OUT}$ ESR	$I_{OUT} = 1.0\text{ mA}$ to $100\text{ mA}$ (Note 4)	22 -	- -	- 16	$\mu\text{F}$ $\Omega$

**PROTECTION**

Current Limit	$I_{OUT(LIM)}$	$V_{OUT} = 4.5\text{ V}$ (5.0 V Version) (Note 4) $V_{OUT} = 3.0\text{ V}$ (3.3 V Version) (Note 4)	150 150	- -	500 500	mA
Short Circuit Current Limit	$I_{OUT(SC)}$	$V_{OUT} = 0\text{ V}$ (Note 4)	40	-	500	mA
Thermal Shutdown Threshold	$T_{TSD}$	(Note 6)	150	-	200	°C

4. Use pulse loading to limit power dissipation.
5. Dropout voltage =  $(V_{IN}-V_{OUT})$ , measured when the output voltage has dropped 100 mV relative to the nominal value obtained with  $V_{IN} = 13.5\text{ V}$ .
6. Not tested in production. Limits are guaranteed by design.
7.  $V_{DO} = V_{IN} - V_{OUT}$ . For output voltage set to  $< 4.5\text{ V}$ ,  $V_{DO}$  will be constrained by the minimum input voltage.

# NCV4264

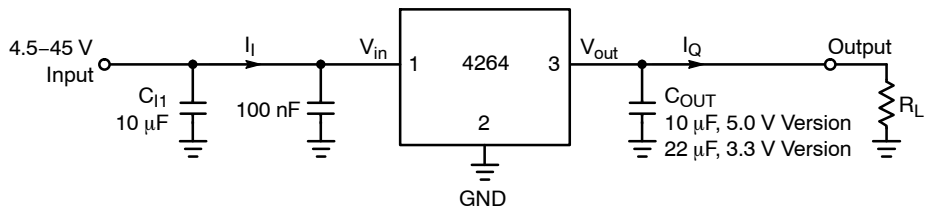


Figure 2. Measurement Circuit

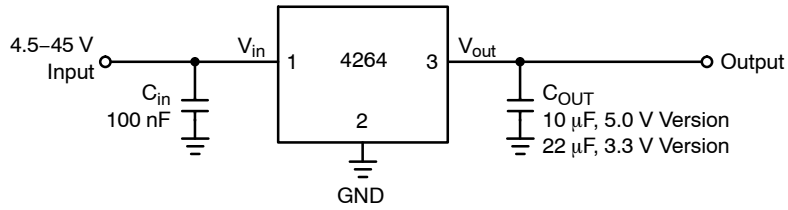


Figure 3. Applications Circuit

## TYPICAL CHARACTERISTIC CURVES – 5 V Version

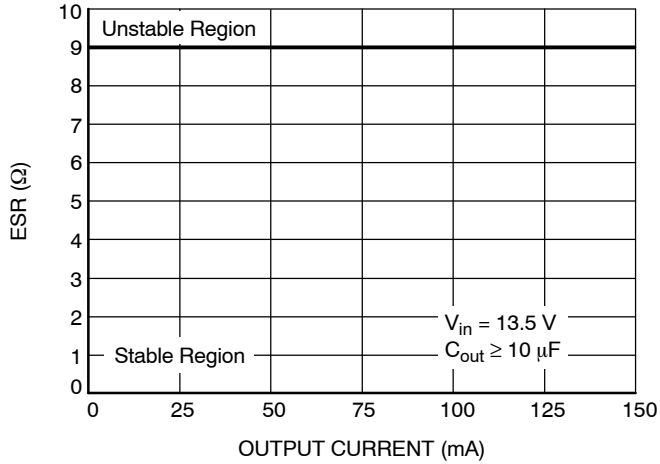


Figure 4. ESR Characterization (5 V Version)

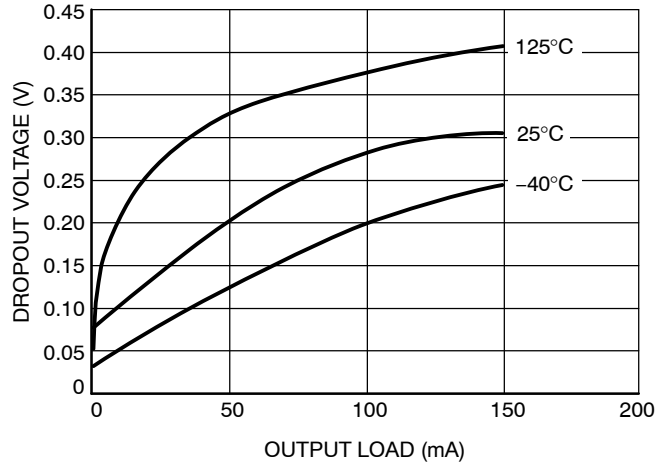
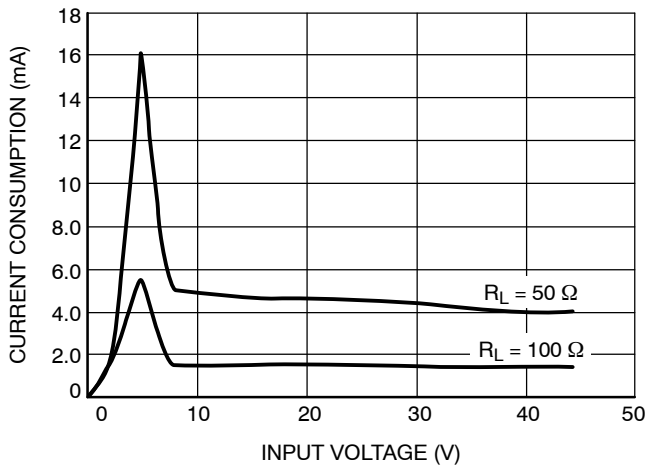
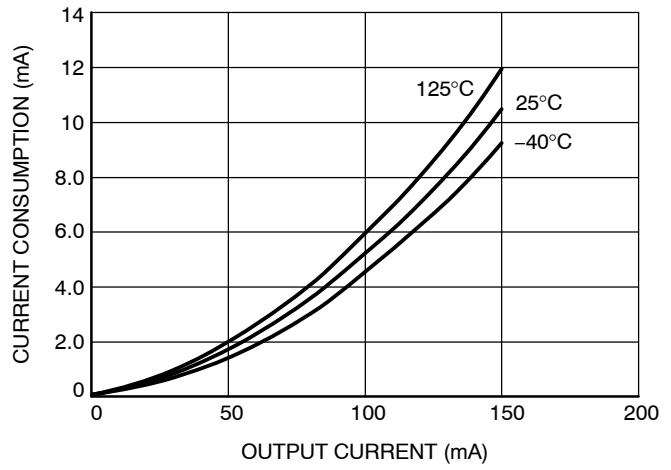


Figure 5. Dropout Voltage vs. Output Load (5 V Version)

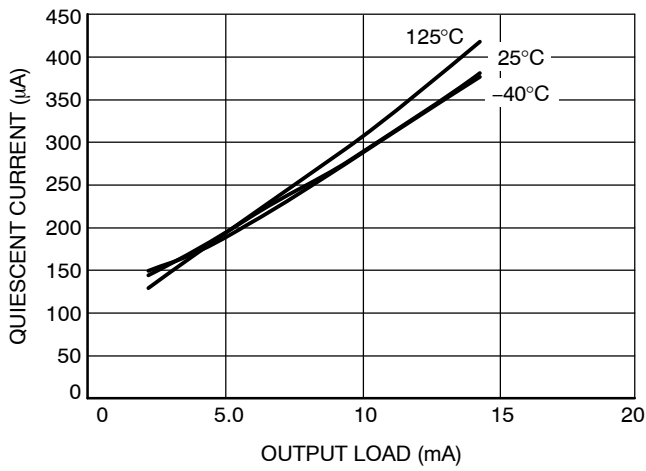
# NCV4264



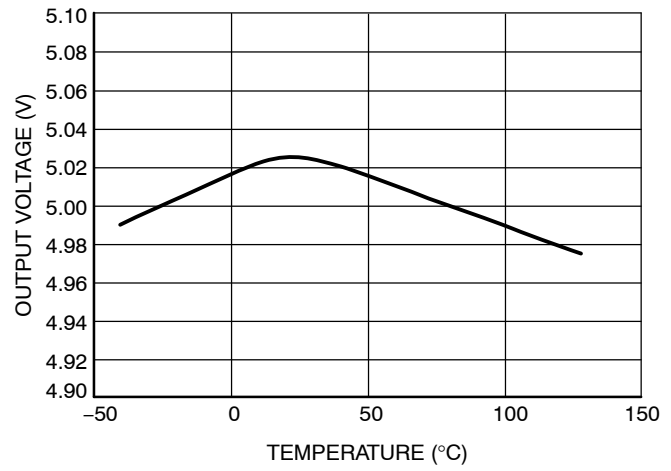
**Figure 6. Current Consumption vs. Input Voltage (5 V Version)**



**Figure 7. Current Consumption vs. Output Current (5 V Version)**



**Figure 8. Quiescent Current vs. Output Load (5 V Version)**



**Figure 9. Output Voltage vs. Temperature (5 V Version)**

TYPICAL CHARACTERISTIC CURVES – 5 V Version

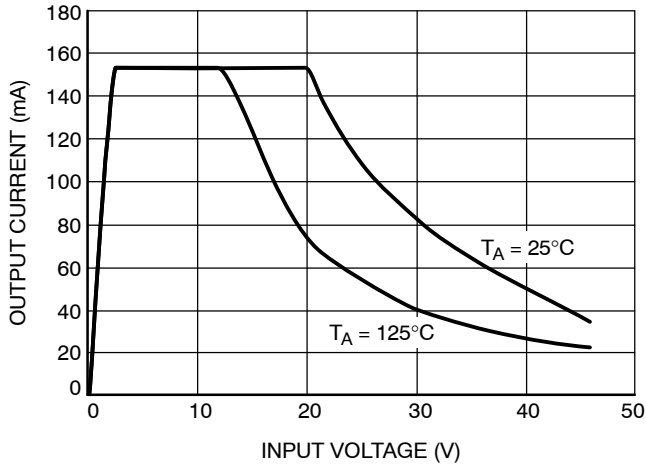


Figure 10. Output Current vs. Input Voltage (5 V Version)

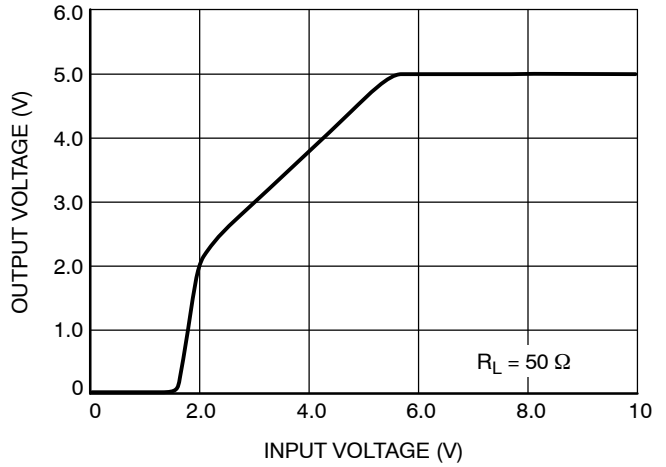


Figure 11. Input Voltage vs. Output Voltage (5 V Version)

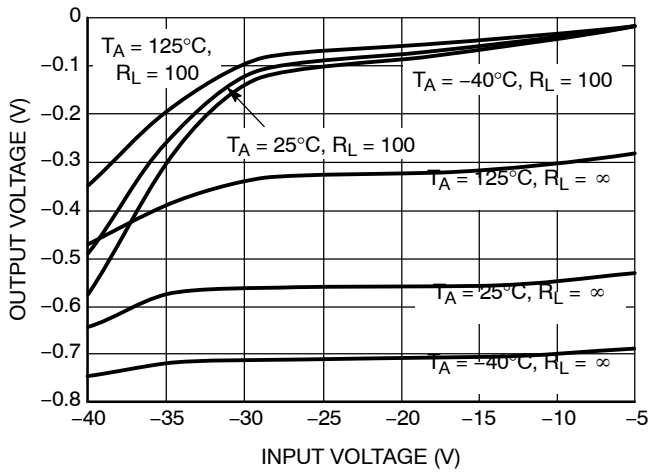
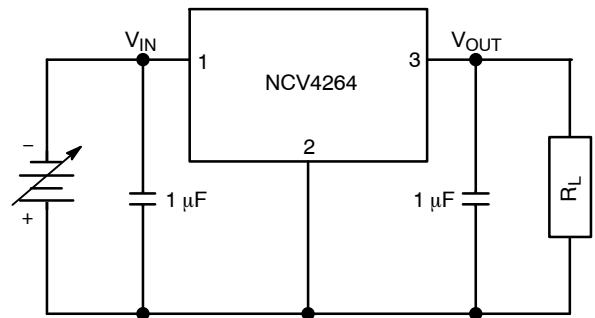


Figure 12. Reverse Voltage Characteristics (5 V Version)



MEASUREMENT CIRCUIT

TYPICAL CHARACTERISTIC CURVES – 3.3 V Version

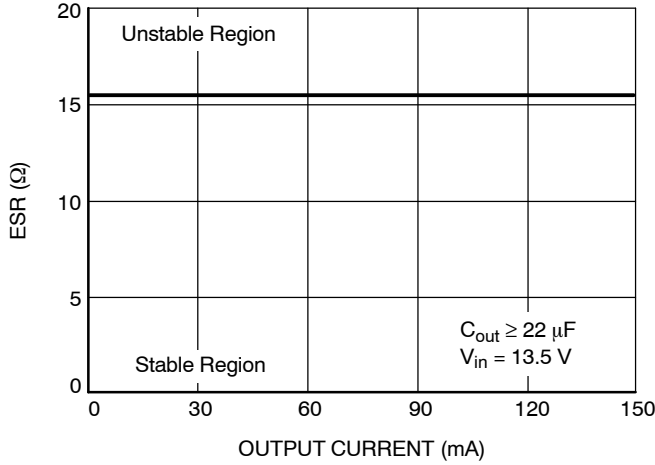


Figure 13. ESR Stability vs. Output Current (3.3 V Version)

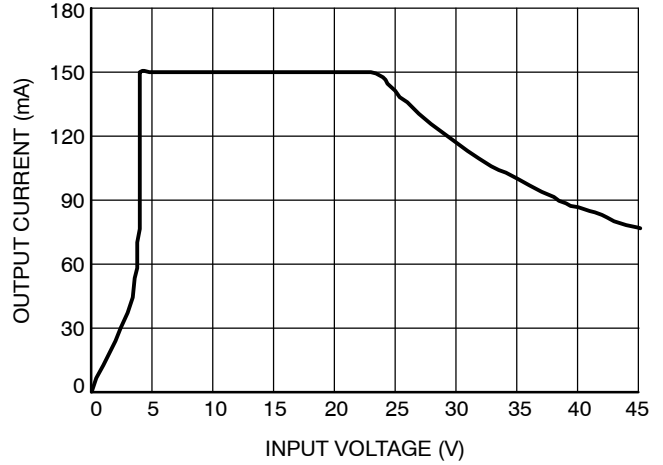


Figure 14. Output Current vs. Input Voltage (3.3 V Version)

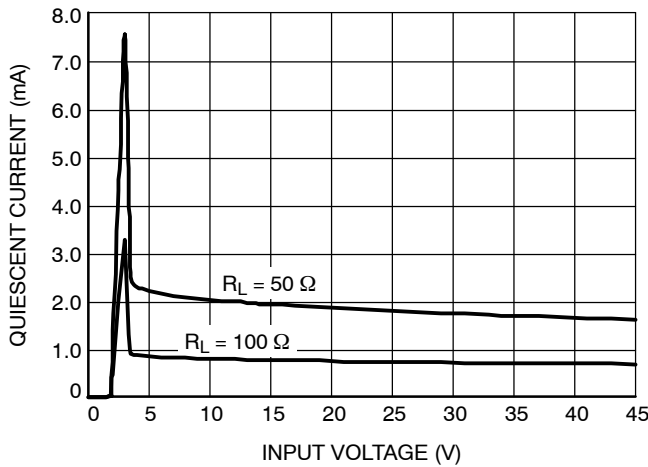


Figure 15. Input Voltage vs. Quiescent Current (3.3 V Version)

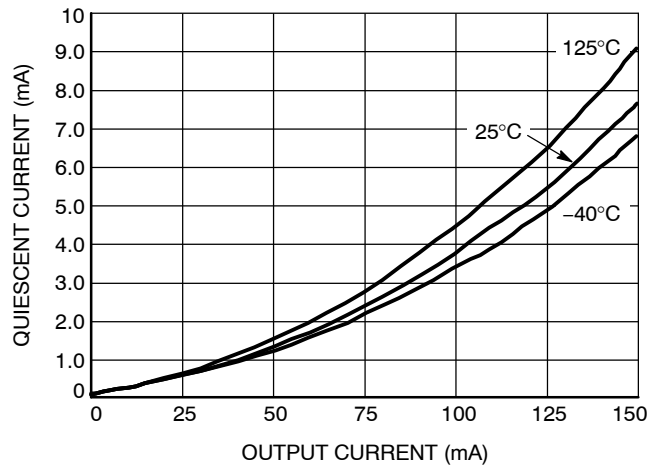


Figure 16. Quiescent Current vs. Output Current (3.3 V Version)

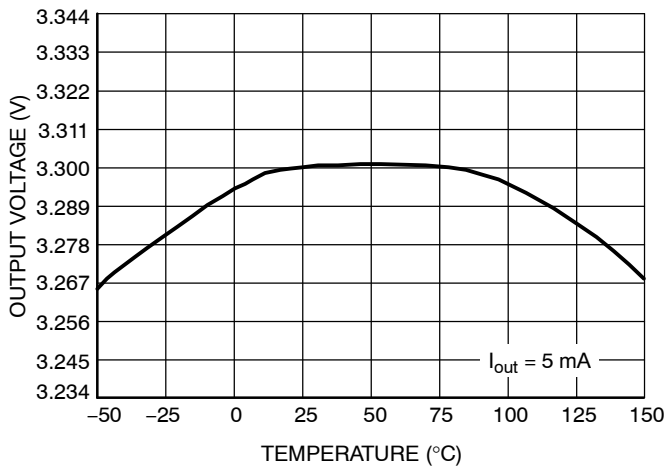


Figure 17. Output Voltage vs. Temperature (3.3 V Version)

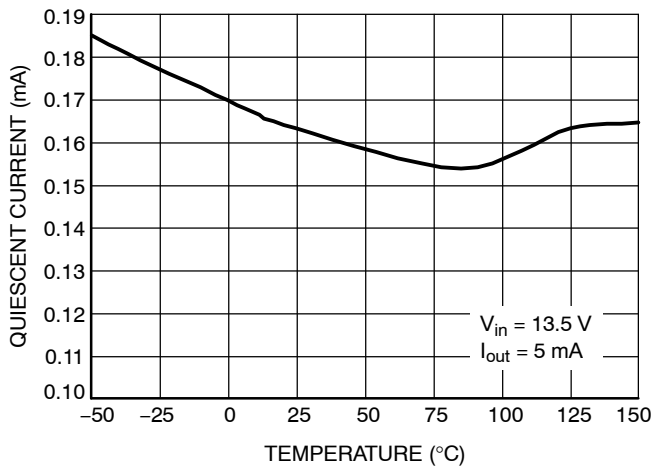


Figure 18. Quiescent Current vs. Temperature (3.3 V Version)

TYPICAL CHARACTERISTIC CURVES – 3.3 V Version

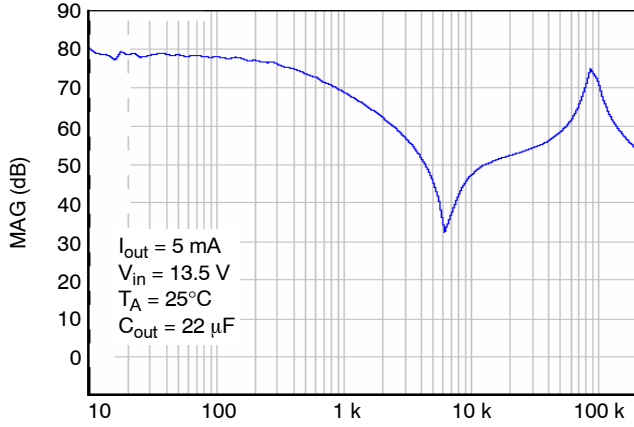


Figure 19. Power Supply Rejection Ratio (3.3 V Version)

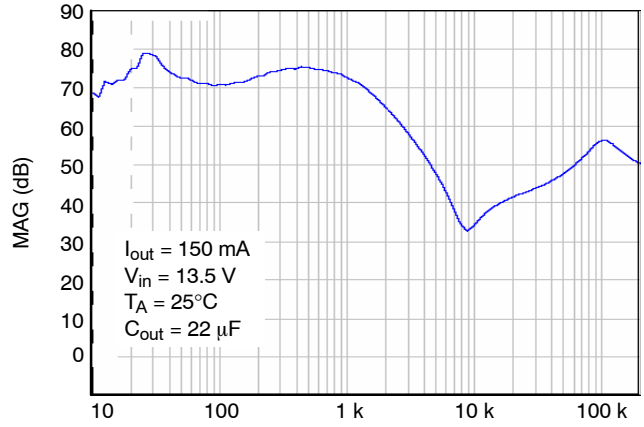


Figure 20. Power Supply Rejection Ratio (3.3 V Version)



**Circuit Description**

The NCV4264 is a precision trimmed 5.0 V and 3.3 V fixed output regulator. The device has current capability of 100 mA, with 500 mV of dropout voltage at 100 mA of current. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference. The regulator is protected by both current limit and short circuit protection. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

**Regulator**

The error amplifier compares the reference voltage to a sample of the output voltage ( $V_{out}$ ) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature-stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

**Regulator Stability Considerations**

The input capacitor  $C_{IN1}$  in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1  $\Omega$  in series with  $C_{IN2}$ . The output or compensation capacitor,  $C_{OUT}$  helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures ( $-25^{\circ}\text{C}$  to  $-40^{\circ}\text{C}$ ), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor  $C_{OUT}$  shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values of  $C_Q \geq 10 \mu\text{F}$ , with an ESR  $\leq 9 \Omega$  for the 5.0 V Version, and  $C_Q \geq 22 \mu\text{F}$  with an ESR  $\leq 16 \Omega$  for the 3.3 V Version within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

**Calculating Power Dissipation in a Single Output Linear Regulator**

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}] \cdot I_{Q(max)} + V_{I(max)} \cdot I_q \quad (\text{eq. 1})$$

Where:

$V_{IN(max)}$  is the maximum input voltage,

$V_{OUT(min)}$  is the minimum output voltage,

$I_{Q(max)}$  is the maximum output current for the application, and  $I_q$  is the quiescent current the regulator consumes at  $I_{Q(max)}$ .

Once the value of  $P_{D(Max)}$  is known, the maximum permissible value of  $R_{\theta JA}$  can be calculated:

$$P_{\theta JA} = \frac{150^{\circ}\text{C} - T_A}{P_D} \quad (\text{eq. 2})$$

The value of  $R_{\theta JA}$  can then be compared with those in the package section of the data sheet. Those packages with  $R_{\theta JA}$ 's less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

**Heat Sinks**

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of  $R_{\theta JA}$ :

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (\text{eq. 3})$$

Where:

$R_{\theta JC}$  = the junction-to-case thermal resistance,

$R_{\theta CS}$  = the case-to-heat sink thermal resistance, and

$R_{\theta SA}$  = the heat sink-to-ambient thermal resistance.

$R_{\theta JA}$  appears in the package section of the data sheet.

Like  $R_{\theta JA}$ , it too is a function of package type.  $R_{\theta CS}$  and  $R_{\theta SA}$  are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.

# NCV4264

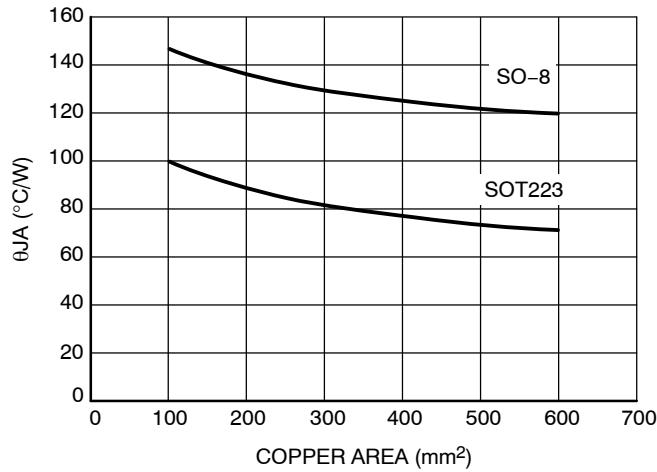


Figure 21.

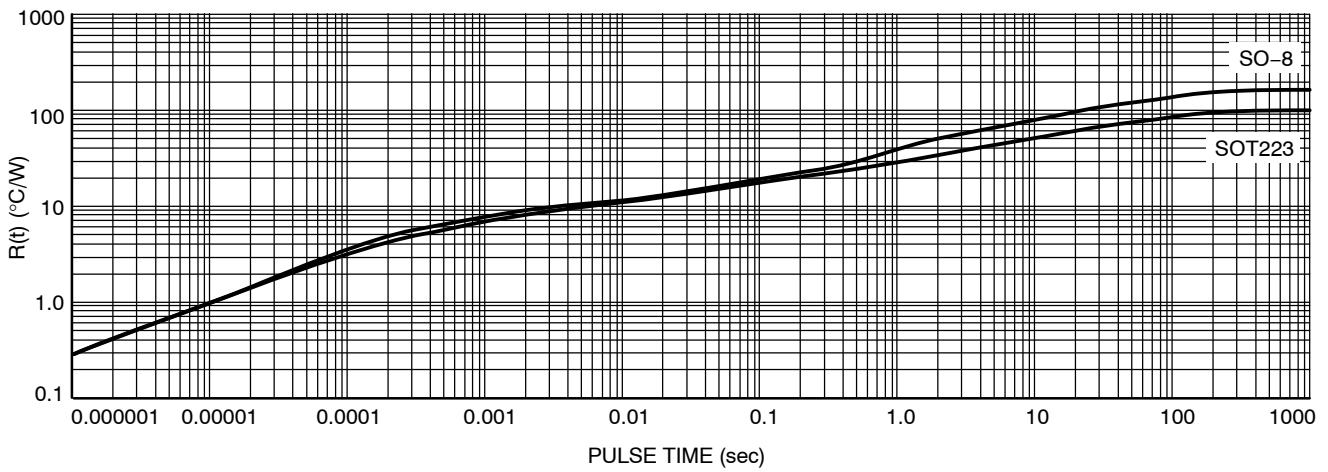


Figure 22.

## ORDERING INFORMATION

Device*	Marking	Package	Shipping†
NCV4264ST50T3G	V64_5	SOT-223	4000 / Tape & Reel
NCV4264ST33T3G	V64_3	SOT-223	4000 / Tape & Reel
NCV4264D50R2G	V42645	SO-8	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

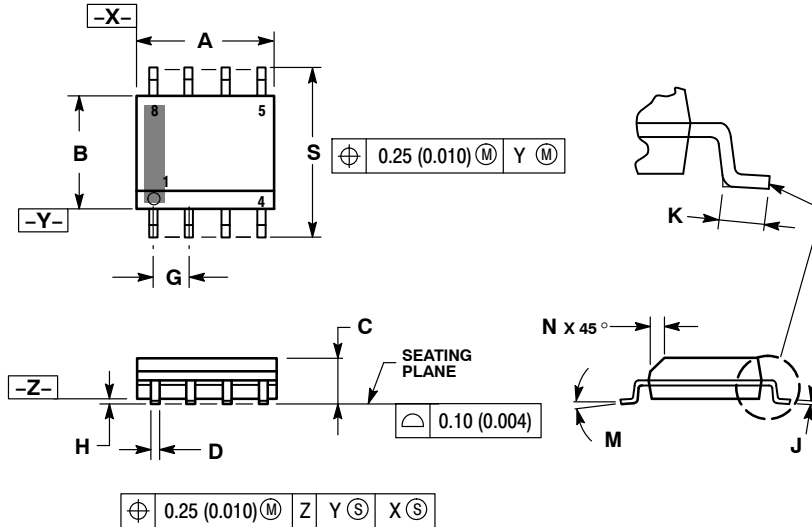


**SOIC-8 NB**  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



SCALE 1:1

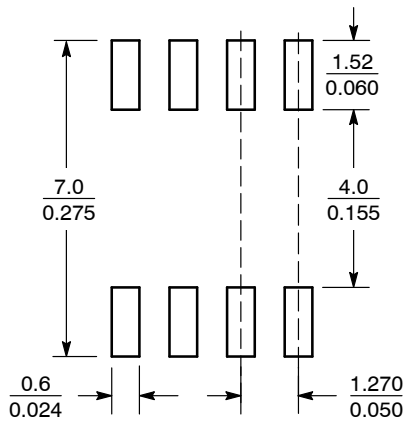


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

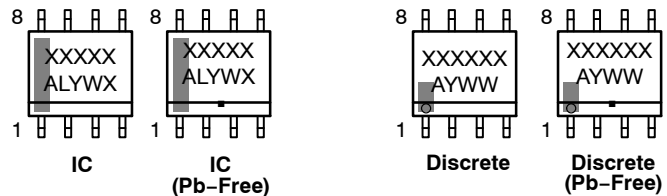
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

**SOLDERING FOOTPRINT\***



SCALE 6:1 (mm/inches)

**GENERIC MARKING DIAGRAM\***



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

XXXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>STATUS:</b>	<b>ON SEMICONDUCTOR STANDARD</b>	
<b>NEW STANDARD:</b>		
<b>DESCRIPTION:</b>	<b>SOIC-8, NB</b>	<b>PAGE 1 OF 3</b>

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

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