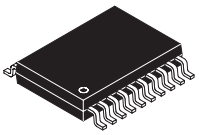
TEXAS INSTRUMENTS



SLAS360 − DECEMBER 2001

PCM CODEC

FEATURES

- **Designed for Analog and Digital Wireless Handsets, Voice-Enabled Terminals, and Telecommunications Applications**
- **2.7-V to 3.3-V Operation**
- **Selectable 13-Bit Linear or 8-Bit A-Law Companded Conversion**
- **Differential Microphone Input With External Gain Setting**
- **Differential Earphone Output Capable of Driving a 32-Ω to 8-Ω Load**
- **Programmable Volume Control in Linear Mode**
- **Microphone (MIC) and Earphone (EAR) Mute Functions**
- **Typical Power Dissipation of 0.03 mW in Power-Down Mode**
- **2.048-MHz Master Clock Rate**
- **300-Hz to 3.4-kHz Passband**
- **Low Profile 20-Terminal TSSOP Packaging**

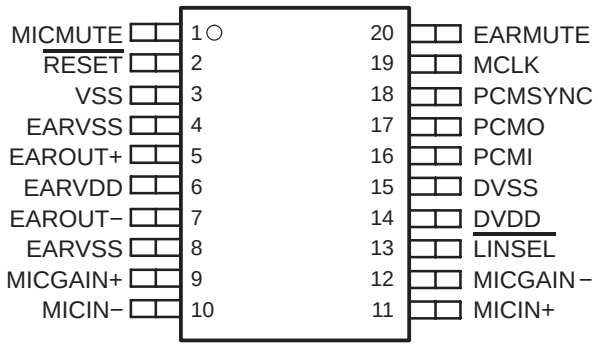
APPLICATIONS

- **Digital Handset**
- **Digital Headset**
- **Cordless Phones**
- **Digital PABX**
- **Digital Voice Recording**

DESCRIPTION

The TLV320AIC1107 PCM codec is designed to perform the transmit encoding analog-to-digital (A/D) conversion, the receive decoding digital-to-analog (D/A) conversion, and the transmit and receive filtering for voice-band communications systems. The TLV320AIC1107 device operates in either the 13-bit linear or 8-bit companded (A-law) mode. The PCM codec generates its own internal clocks from a 2.048-MHz master clock input.

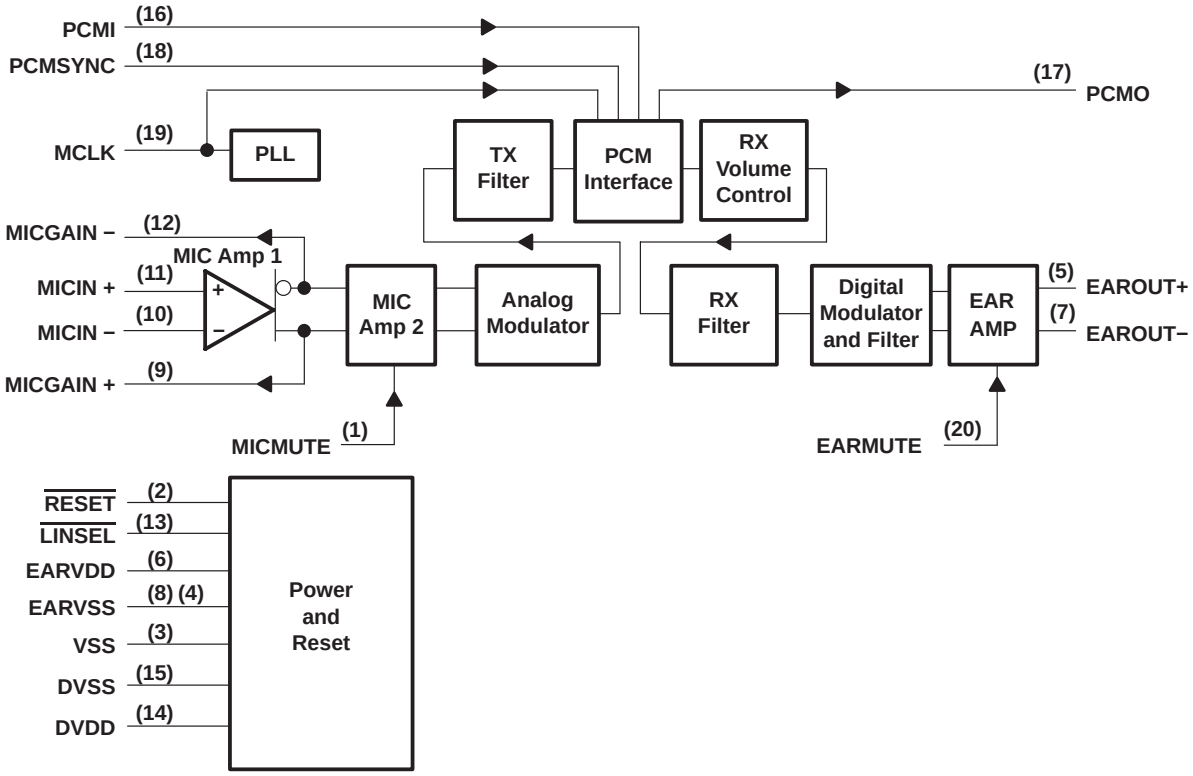
PW PACKAGE
(TOP VIEW)



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



RX = Receive
TX = Transmit

detailed description

power up/reset

An external reset must be applied to the active-low $\overline{\text{RESET}}$ terminal while MCLK is active to ensure reset at power up.

reference

A precision band-gap reference voltage is generated internally and supplies all required references to operate the transmit and receive channels.

phase-locked loop

The phase-locked loop generates the internal clock frequency required for internal digital filters and modulators by phase locking to 2.048-MHz master clock input.

PCM interface

The PCM interface transmits and receives data at the PCMO and PCMI terminals respectively. The data is transmitted or received at the MCLK speed once on each PCMSYN cycle. The PCMSYN can be driven by an external source that is derived from the master clock and used as an interrupt to the host controller.

microphone input

The microphone input circuit consists of two differential input/differential output amplifiers (MIC Amp 1 and MIC Amp 2). MIC Amp 1 is a low-noise differential amplifier capable of an externally set gain. MIC Amp 2 is a differential amplifier with a fixed gain of 6 dB.

analog modulator

The transmit channel modulator is a third-order sigma-delta design.

transmit filter

The transmit filter is a digital filter designed to meet Consultive Committee on International Telegraphy and Telephony (CCITT) G.714 requirements. The TLV320AIC1107 device operates in either the 13-bit linear or 8-bit companded A-law mode.

receive filter

The receive (RX) filter is a digital filter that meets CCITT G.714 requirements. The TLV320AIC1107 device operates in either the 13-bit linear or 8-bit A-law companded mode, which is selected at the $\overline{\text{LINSEL}}$ input.

receive volume control

In linear mode, the three least significant bits of the 16-bit PCMI data sample is used to control volume. The volume range is −18 dB to 3 dB in 3-dB steps.

digital modulator and filter

The second-order digital modulator and filter convert the received digital PCM data to the analog output required by the earphone interface.

earphone amplifiers

EAROUT is recommended for use as a differential output; however, it can be connected in single-ended topology as well. Clicks and pops are suppressed from the differential output.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EARVSS	4	I	Analog ground for EAROUT+
DVDD	14	I	Digital positive power supply
DVSS	15	I	Digital negative power supply
EARMUTE	20	I	Earphone mute
EAROUT−	7	O	Earphone amplifier negative output
EAROUT+	5	O	Earphone amplifier positive output
EARVDD	6	I	Analog positive power supply for the earphone amplifiers
EARVSS	8	I	Analog ground for EAROUT−
$\overline{\text{LINSEL}}$	13	I	Companding enable
MCLK	19	I	Master system clock input (2.048 MHz) (digital)
MICGAIN+	9	I	Microphone gain positive feedback
MICGAIN−	12	I	Microphone gain negative feedback
MICMUTE	1	I	Microphone mute
MICIN−	10	I	Microphone negative input (−)
MICIN+	11	I	Microphone positive input (+)
PCMI	16	I	Receive PCM input
PCMO	17	O	Transmit PCM output
PCMSYNC	18	I	PCM frame synchronization
$\overline{\text{RESET}}$	2	I	Active-low reset
VSS	3	I	Ground return for band-gap internal reference

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, DVDD, EARVDD . . . . . −0.5 V to 3.6 V
Output voltage range, V_O . . . . . −0.5 V to 3.6 V
Input voltage range, V_I . . . . . −0.5 V to 3.6 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
PW	680 W	6.8 W/°C	270 W

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
Supply voltage, DVDD, EARVDD	2.7		3.3	V
High-level input voltage, V_{IH}	$0.7\times V_{DD}$			V
Low-level input voltage, V_{IL}			$0.3\times V_{DD}$	V
Load impedance between EAROUT+ and EAROUT−, R_L		8 to 32		Ω
Input voltage, MICIN			$0.9\times V_{DD}$	V
Operating free-air temperature, T_A	−40		85	°C

NOTES: 1. To avoid possible damage and resulting reliability problems to these CMOS devices, follow *power-on initialization* paragraph, described in the *Principles of Operations*.
2. Voltages are with respect to DV_{SS} and $EARV_{SS}$.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	Operating		5	7	mA
		Power down, MCLK not present		10	30	μA
t_{pu}	Power-up time from power down				10	ms

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, PCMO	I_{OH} = −3.2 mA, V_{DD} = 3 V	DV_{DD}−0.25			V
V_{OL}	Low-level output voltage, PCMO	I_{OL} = 3.2 mA, V_{DD} = 3 V			0.2	V
I_{IH}	High-level input current, any digital input	V_I = 2.2 V to V_{DD}			10	μA
I_{IL}	Low-level input current, any digital input	V_I = 0 V to 0.8 V			10	μA
C_I	Input capacitance				10	pF
C_o	Output capacitance				20	pF

microphone interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	See Note 3	−5		5	mV
I_{IB}	Input bias current		−250		250	nA
C_i	Input capacitance			5		pF
V_n	Microphone input referred noise, psophometric weighted	MIC Amp 1 gain = 23.5 dB, See Note 4		2.9	4	μV_{rms}
	MICMUTE		−80			dB

NOTES: 3. Measured while MICIN+ and MICIN− are connected together. Less than 0.5 mV offset results in 0 value code on PCMOUT.
4. Configured as shown in Figure 3

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

speaker interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Earphone AMP output power (see Note 5)		V_{DD} = 2.7 V, fully differential, 8-Ω load, 3-dBm0 output, volume control = −3 dB, PCMI data input to −4 dB level		161	200	mW
		V_{DD} = 2.7 V, fully differential, 16-Ω load, 3-dBm0 output, volume control = −3 dB, PCMI data input to −2 dB level		128	160	
		V_{DD} = 2.7 V, fully differential, 32-Ω load, 3-dBm0 output, volume control = −3 dB, PCMI data input to −1 dB level		81	100	
$I_O$max	Maximum output current for EAROUT (rms)	3-dBm0 input, 8-Ω load		141	178	mA
		3-dBm0 input, 16-Ω load		90	112	
		3-dBm0 input, 32-Ω load		50	63	
EARMUTE			−80			dB

NOTE 5: Maximum power is with a load impedance of −20%, at 25°C.

transmit gain and dynamic range, companded mode (A-law) or linear mode selected (see Notes 6 and 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit reference-signal level (0dB)	Differential, MIC Amp 1 configured for 23.5-dB gain			88	mV_{pp}
Overload-signal level (3 dBm0)	Differential, MIC Amp 1 configured for 23.5-dB gain			124	mV_{pp}
Absolute gain error	0 dBm0 input signal, 2.7 V ≤ V_{DD} ≤ 3.3 V	−1		1	dB
Gain error with input level relative to gain at −10 dBm0 MICIN, MICIN+ to PCMO	MICIN−, MICIN+ to PCMO at 3 dBm0 to −30 dBm0	−0.5		0.5	dB
	MICIN−, MICIN+ to PCMO at −31 dBm0 to −45 dBm0	−1		1	
	MICIN−, MICIN+ to PCMO at −46 dBm0 to −55 dBm0	−1.2		1.2	

NOTES: 6. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.

7. The reference signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 124-mV_{pp}.

transmit filter transfer, companded mode (A-law) or linear mode selected

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	f_{MIC} < 100 Hz	−0.5		0.5	dB
	f_{MIC} = 200 Hz	−0.5		0.5	
	f_{MIC} = 300 Hz to 3 kHz	−0.5		0.5	
	f_{MIC} = 3.4 kHz	−1.5		0	
	f_{MIC} = 4 kHz			−14	
	f_{MIC} = 4.6 kHz			−35	
	f_{MIC} = 8 kHz			−47	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

transmit idle channel noise and distortion, companded mode (A-law) selected

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit idle channel noise, psophometrically weighted	MIC Amp 1 configured for 23.5-dB gain (see Note 8)		−80	−70	$dBm0_p$
Transmit signal-to-distortion ratio with 1.02-kHz sine-wave input	MICIN−, MICIN+ to PCMO at 3 dBm0	27			dBm0
	MICIN−, MICIN+ to PCMO at 0 dBm0	30			
	MICIN−, MICIN+ to PCMO at −5 dBm0	33			
	MICIN−, MICIN+ to PCMO at −10 dBm0	36			
	MICIN−, MICIN+ to PCMO at −20 dBm0	35			
	MICIN−, MICIN+ to PCMO at −30 dBm0	26			
	MICIN−, MICIN+ to PCMO at −40 dBm0	24			
	MICIN−, MICIN+ to PCMO at −45 dBm0	19			
Intermodulation distortion, 2-tone CCITT method, composite power level, −13 dBm0	CCITT G.712 (7.1), R2	49			dB
	CCITT G.712 (7.2), R2	51			

NOTE 8: With recommended impedances and resistor tolerance of 1%

transmit idle channel noise and distortion, linear mode selected

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit idle channel noise, psophometrically weighted	MIC Amp 1 configured for 23.5 dB gain (see Note 8)		−80	−74	$dBm0_p$
Transmit signal-to-total distortion ratio with 1.02-kHz sine-wave input	MICIN−, MICIN+ to PCMO at 3 dBm0	40	55		dB
	MICIN−, MICIN+ to PCMO at 0 dBm0	50	61		
	MICIN−, MICIN+ to PCMO at −5 dBm0	52	62		
	MICIN−, MICIN+ to PCMO at −10 dBm0	56	66		
	MICIN−, MICIN+ to PCMO at −20 dBm0	52	68		
	MICIN−, MICIN+ to PCMO at −30 dBm0	51	61		
	MICIN−, MICIN+ to PCMO at −40 dBm0	43	59		
	MICIN−, MICIN+ to PCMO at −45 dBm0	38	55		

NOTE 8: With recommended impedances and resistor tolerance of 1%

receive gain and dynamic range, linear or companded (A-law) mode selected (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overload-signal level (3 dB)	Load = 8 Ω, volume control = −3 dB, PCMI data input to −4 dB level		3.20		V_{pp}
	Load = 16 Ω, volume control = −3 dB, PCMI data input to −2 dB level		4.05		
	Load = 32 Ω, volume control = −3 dB, PCMI data input to −1 dB level		4.54		
Absolute gain error	0 dBm0 input signal, 2.7 V ≤ V_{DD} ≤ 3.3 V	−1		1	dB
Gain error with output level relative to gain at −10 dBm0	PCMI to EAROUT−, EAROUT+ at 3 dBm0 to −40 dBm0	−0.5		0.5	dB
	PCMI to EAROUT−, EAROUT+ at −41 dBm0 to −50 dBm0	−1		1	
	PCMI to EAROUT−, EAROUT+ at −51 dBm0 to −55 dBm0	−1.2		1.2	

NOTE 9: 1020-Hz input signal at PCMI, output measured differentially between EAROUT− and EAROUT+

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

receive filter transfer, companded mode (A-law) or linear mode selected (MCLK = 2.048 MHz) (see Note 10)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	f_{EAROUT} < 100 Hz			−15	dB
	f_{EAROUT} = 200 Hz			−5	
	f_{EAROUT} = 300 Hz to 3 kHz	−0.5		0.5	
	f_{EAROUT} = 3.4 kHz	−1.5		0	
	f_{EAROUT} = 4 kHz			−14	
	f_{EAROUT} = 4.6 kHz			−35	
	f_{EAROUT} = 8 kHz			−47	

NOTE 10: Volume control = −3 dB, PCMI data input to −1 dB level (32-Ω load)

receive idle channel noise and distortion, companded mode (A-law) selected (see Note 10)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive noise, C-message weighted	PCMI = 11111111 (A-law)		−90	−88	dBm0
Receive signal-to-distortion ratio with 1.02-kHz sine-wave input	PCMI to EAROUT−, EAROUT+ at 3 dBm0	21			dB
	PCMI to EAROUT−, EAROUT+ at 0 dBm0	25			
	PCMI to EAROUT−, EAROUT+ at −5 dBm0	36			
	PCMI to EAROUT−, EAROUT+ at −10 dBm0	43			
	PCMI to EAROUT−, EAROUT+ at −20 dBm0	40			
	PCMI to EAROUT−, EAROUT+ at −30 dBm0	38			
	PCMI to EAROUT−, EAROUT+ at −40 dBm0	28			
	PCMI to EAROUT−, EAROUT+ at −45 dBm0	23			

NOTE 10: Volume control = −3 dB, PCMI data input to −1 dB level (32-Ω load)

receive idle channel noise and distortion, linear mode selected (see Note 10)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive noise, (20 Hz to 20 kHz brickwall window)	PCMI = 0000000000000		−83	−78	dBm0
Receive signal-to-distortion ratio with 1.02-kHz sine-wave input (0−4 kHz)	PCMI to EAROUT−, EAROUT+ at 3 dBm0	48	52		dB
	PCMI to EAROUT−, EAROUT+ at 0 dBm0	51	56		
	PCMI to EAROUT−, EAROUT+ at −5 dBm0	57	59		
	PCMI to EAROUT−, EAROUT+ at −10 dBm0	55	62		
	PCMI to EAROUT−, EAROUT+ at −20 dBm0	51	53		
	PCMI to EAROUT−, EAROUT+ at −30 dBm0	45	47		
	PCMI to EAROUT−, EAROUT+ at −40 dBm0	42	47		
	PCMI to EAROUT−, EAROUT+ at −45 dBm0	35	45		
Intermodulation distortion, 2-tone CCITT method, composite power level, −13 dBm0	CCITT G.712 (7.1), R2	50			dB
	CCITT G.712 (7.2), R2	54			

NOTE 10: Volume control = −3 dB, PCMI data input to −1 dB level (32-Ω load)

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

power supply rejection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage rejection, transmit channel	MICIN−, MICIN+ = 0 V, V_{DD} = 2.7 V + 100 mV_{pp}, f = 1 kHz, Resistor tolerance of 1%		−74	−50	dB
Supply voltage rejection, receive channel (differential)	PCM code = positive zero, V_{DD} = 2.7 V + 100 mV_{pp}, f = 1 kHz, Resistor tolerance of 1%		−80	−65	dB

crosstalk attenuation, linear mode selected

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crosstalk attenuation, transmit-to-receive (differential)	MICIN−, MICIN+ = 0 dB, f = 300 Hz to 3400 Hz measured differentially between EAROUT− and EAROUT+	70			dB
Crosstalk attenuation, receive-to-transmit	PCMI = 0 dBm0, f = 300 Hz to 3400 Hz measured at PCMO	70			dB

timing requirements

clock

		MIN	NOM	MAX	UNIT
t_t	Transition time, MCLK			10	ns
f_{mclk}	MCLK frequency		2.048		MHz
	MCLK jitter			37%	
	MCLK clock cycles per PCMSYN frame	256		256	cycles

transmit (see Figure 1)

		MIN	MAX	UNIT
$t_{su(PCMSYN)}$	Setup time, PCMSYN high before MCLK ↓	20	$t_{c(MCLK)}$−20	ns
$t_{h(PCMSYN)}$	Hold time, PCMSYN high after MCLK ↓	20	$t_{c(MCLK)}$−20	

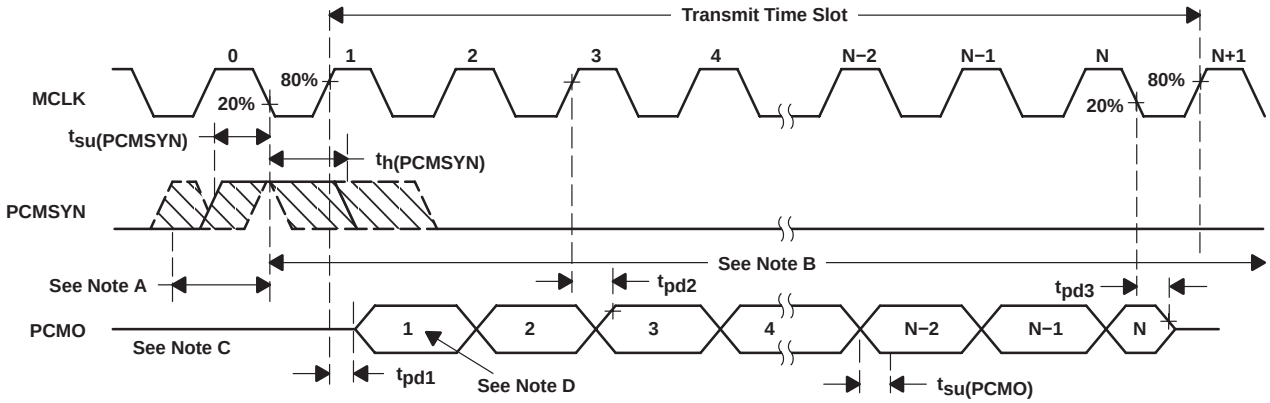
receive (see Figure 2)

		MIN	MAX	UNIT
$t_{su(PCSYN)}$	Setup time, PCMSYN high before MCLK ↓	20	$t_{c(MCLK)}$−20	ns
$t_{h(PCSYN)}$	Hold time, PCMSYN high after MCLK ↓	20	$t_{c(MCLK)}$−20	ns
$t_{su(PCMI)}$	Setup time, PCMI high or low before MCLK ↓	20		ns
$t_{h(PCMI)}$	Hold time, PCMI high or low after MCLK ↓	20		ns

switching characteristics over recommended operating conditions, $C_{L(max)}$ = 10 pF (see Figure 1)

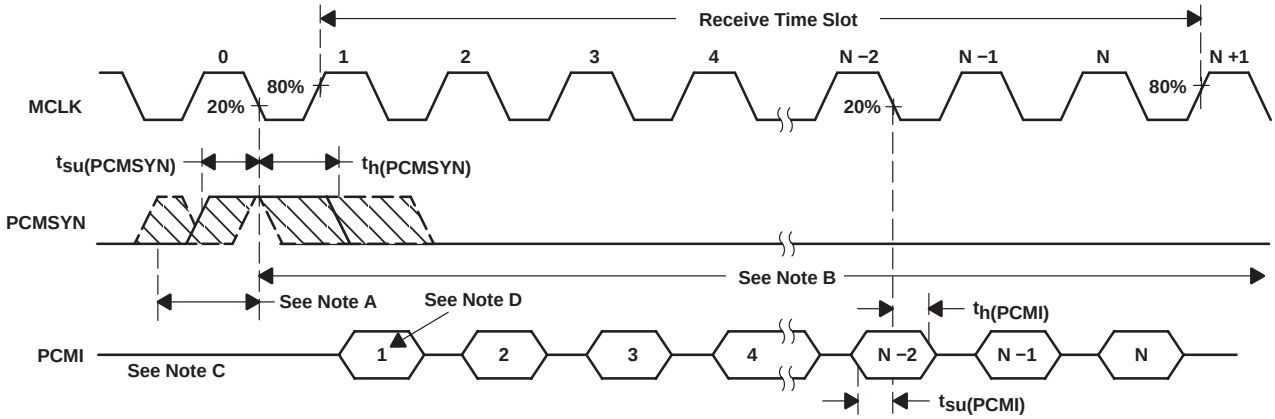
		MIN	MAX	UNIT
t_{pd1}	Propagation delay time, MCLK bit 1 high to PCMO bit 1 valid		35	ns
t_{pd2}	Propagation delay time, MCLK high to PCMO valid, bits 2 to n		35	ns
t_{pd3}	Propagation delay time, MCLK bit n low to PCMO bit n Hi-Z	30		ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for PCMSYN high.
B. This window is allowed for PCMSYN low ($t_{h(PCMSYN)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.
D. Bit 1 = Most significant bit (MSB), Bit N = Least significant bit (LSB)

Figure 1. Transmit Timing Diagram



NOTES: A. This window is allowed for PCMSYN high.
B. This window is allowed for PCMSYN low.
C. Transitions are measured at 50%.
D. Bit 1 = Most significant bit (MSB), Bit N = Least significant bit (LSB)

Figure 2. Receive Timing Diagram

PRINCIPLES OF OPERATION

power-up initialization

An external reset with a minimum pulse width of 500 ns must be applied to the active-low $\overline{\text{RESET}}$ terminal with MCLK active to ensure reset upon power up.

Table 1. Power-Up and Power-Down Power Consumption (V_{DD} = 2.7 V, Earphone Amplifier Loaded)

DEVICE STATUS	MAXIMUM POWER CONSUMPTION
Power up	16.2 mW
Power down	81 μW

The loss of MCLK (no transition detected) automatically enters the device into a power-down state with PCMO in the high-impedance state. If an asynchronous power down occurs during a pulse code modulation (PCM) data transmit cycle, the PCM interface remains powered up until the PCM data is completely transferred.

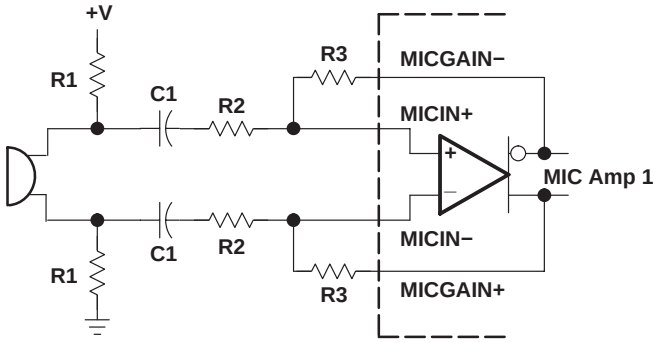
conversion laws

The device can be programmed either for a 13-bit linear or 8-bit (A-law) companding mode. The companding operation approximates the CCITT G.711 recommendation. The linear mode operation uses a 13-bit twos-complement format. Linear mode is selected with $\overline{\text{LINSEL}}$ low. $\overline{\text{LINSEL}}$ is high for companding.

transmit operation

microphone input

The microphone input stage is a low-noise differential amplifier. The microphone must be capacitively coupled to the MICIN− and MICIN+ terminals. Preamplifier (MIC Amp 1) gain is determined by selection of external resistors R2 and R3. To achieve the recommended gain setting of 23.5 dB for MIC Amp 1, resistor values of R2 = 34 kΩ and R3 = 510 kΩ are suggested. A 1% tolerance is recommended for all resistors to meet the specification. The recommended input impedance is 35 kΩ to 100 kΩ.



R1 = 2 kΩ

C1 = 0.22 μF

$$\text{MIC Amp 1 Gain in dB} = 20 \log\left(\frac{R3}{R2}\right)$$

Figure 3. Typical Microphone Interface

PRINCIPLES OF OPERATION

microphone mute function

Transmit channel muting can be selected by setting MICMUTE high. Muting provides 80-dB attenuation of the input microphone signal.

receive operation

earphone amplifier

The analog signal is routed to the earphone amplifier differential output (EAROUT− or EAROUT+), which is capable of driving a load as low as 8 Ω. EAROUT is recommended to be used as a differential output.

earphone mute function

Receive channel muting can be selected by setting the EARMUTE terminal to high.

receive PCM data format

- Companded mode: 8 bits are received, the MSB first.
- Linear mode: 13 bits are received, the MSB first.

Table 2. Receive Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
1	CD7	LD12
2	CD6	LD11
3	CD5	LD10
4	CD4	LD9
5	CD3	LD8
6	CD2	LD7
7	CD1	LD6
8	CD0	LD5
9	−	LD4
10	−	LD3
11	−	LD2
12	−	LD1
13	−	LD0
14	−	RXVOL2
15	−	RXVOL1
16	−	RXVOL0

PRINCIPLES OF OPERATION

receive volume control

In linear mode, RXVOL [2:0] PCM data bits are used for volume control according to Table 3. Volume control bits must be sent on PCMI for each 13-bit receive word. In companded mode, volume control is fixed at 0 dB.

Table 3. Volume Control Bit Definition in Linear Mode

RXVOL [2:0]	GAIN SETTING
000	3 dB
001	0 dB
010	−3 dB
011	−6 dB
100	−9 dB
101	−12 dB
110	−15 dB
111	−18 dB

support section

The clock generator and control circuit uses the master clock input (MCLK) to generate internal clocks to drive internal counters, filters, and converters.

clock frequencies and sample rates

A fixed PCMSYN rate of 8 kHz determines the sampling rate. The PCMSYN signal must be derived from the master clock. The divide ratio must be set to 256 for the device to work properly.

TYPICAL CHARACTERISTICS

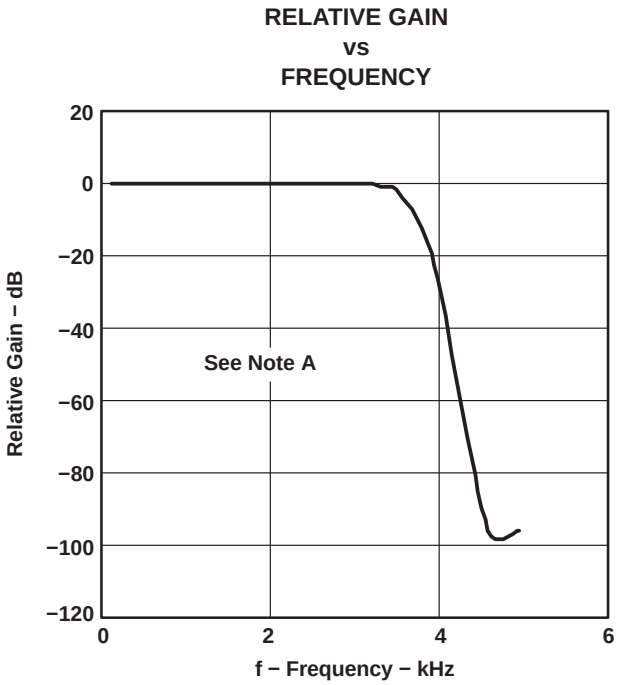


Figure 4

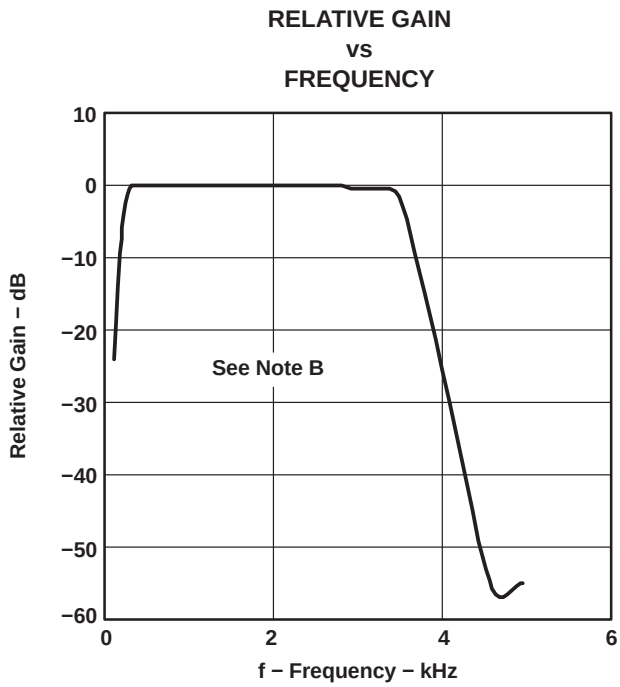


Figure 5

NOTES: A. Transmit channel frequency response shown relative to the gain at 1.02-kHz input signal in linear mode.
B. Receive channel frequency response shown relative to the gain at 1.02-kHz input signal in linear mode.

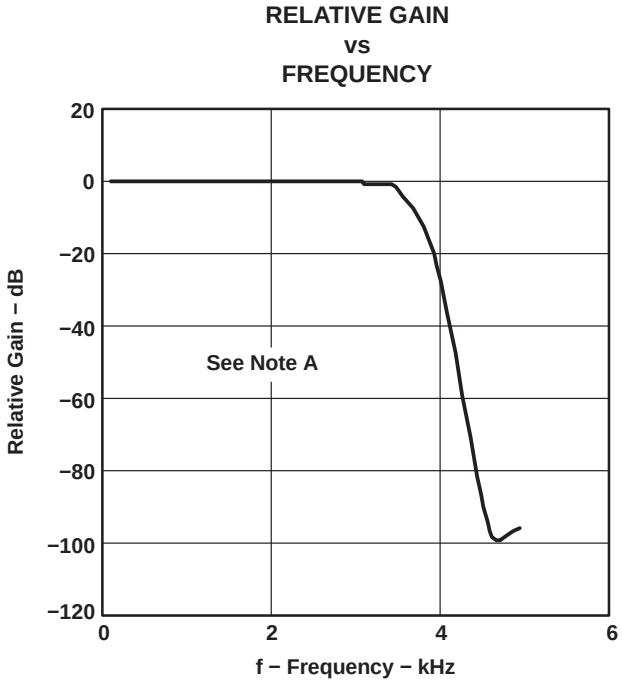


Figure 6

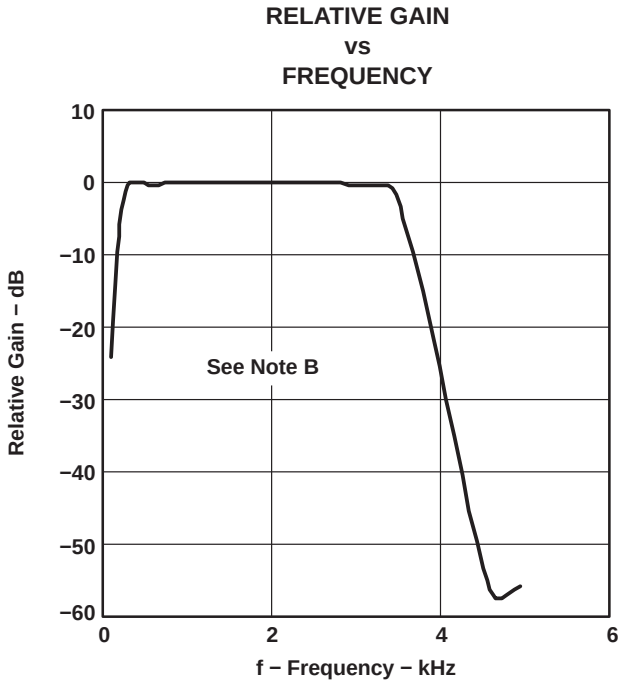


Figure 7

NOTES: A. Transmit channel frequency response shown relative to the gain at 1.02-kHz input signal in A-law mode.
B. Receive channel frequency response shown relative to the gain at 1.02-kHz input signal in A-law mode.

TYPICAL CHARACTERISTICS

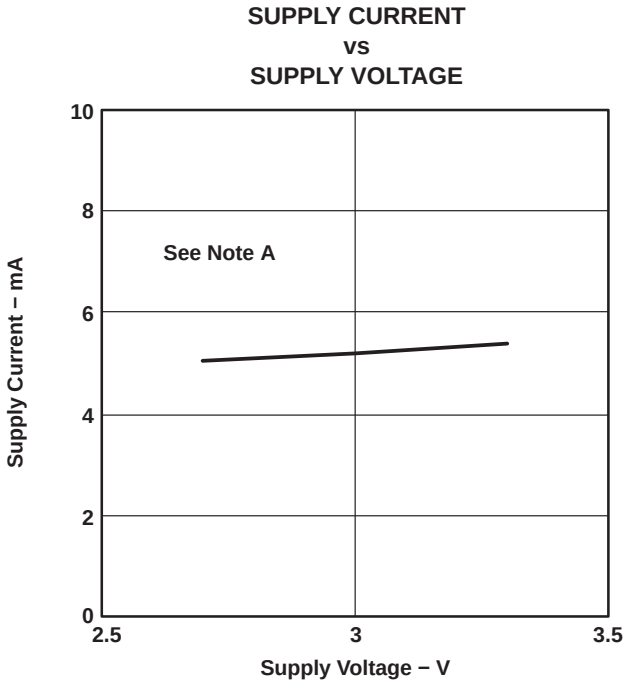


Figure 8

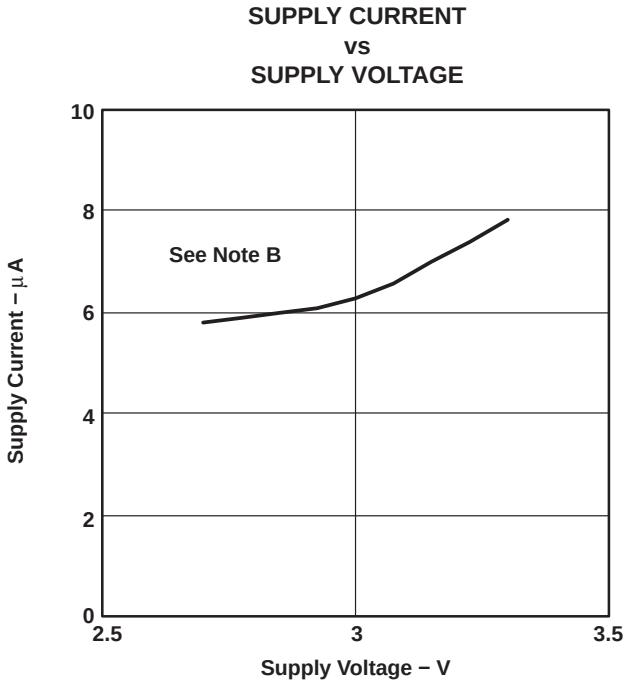


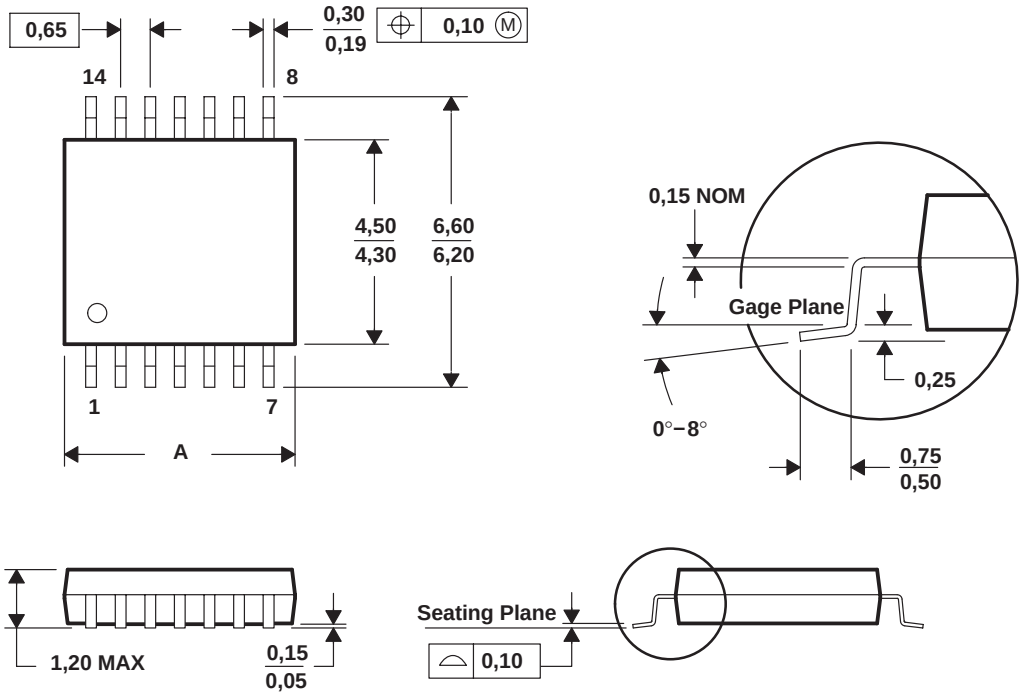
Figure 9

NOTES: A. Supply current as a function of supply voltage in power-up mode
B. Supply current as a function of supply voltage in power-down mode

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV320AIC1107PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		AIC1107	Samples
TLV320AIC1107PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIC1107	Samples
TLV320AIC1107PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIC1107	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

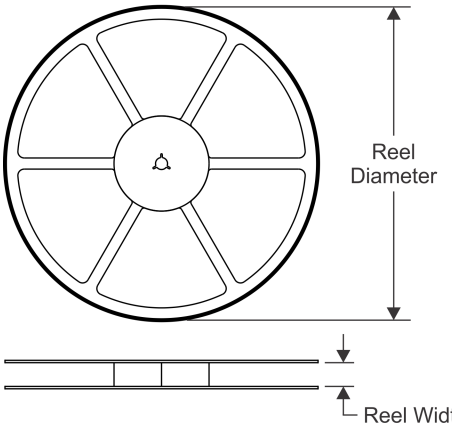
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

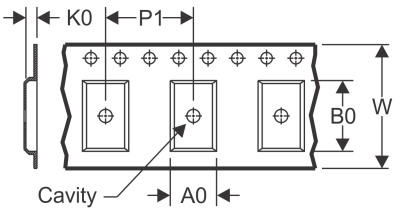
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

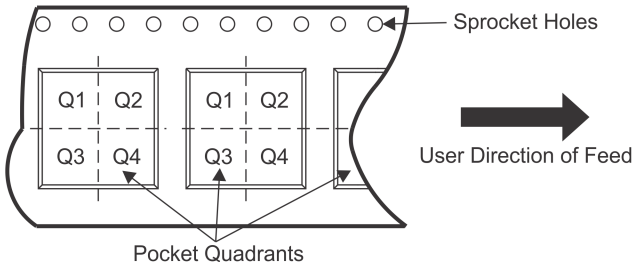


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

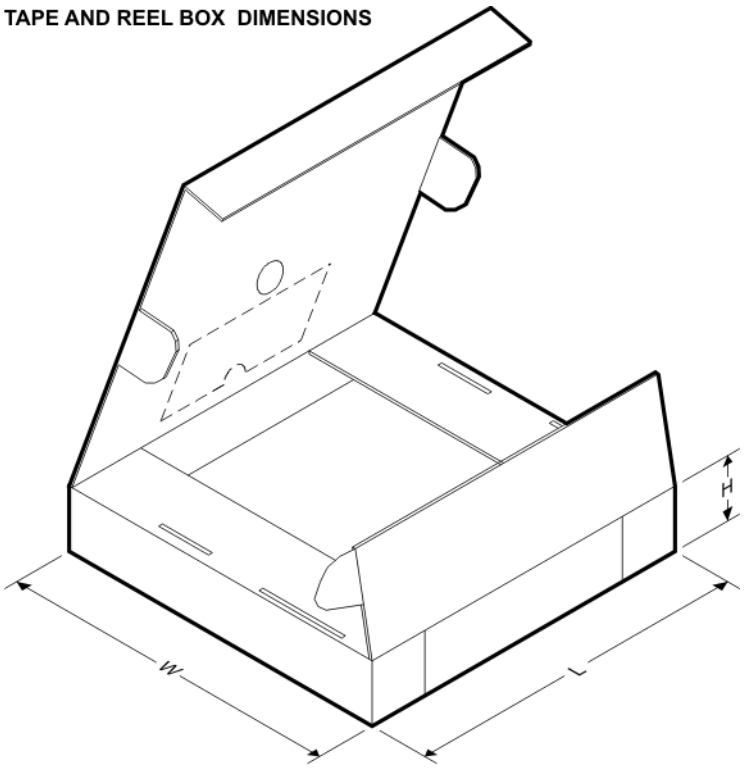
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC1107PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC1107PWR	TSSOP	PW	20	2000	350.0	350.0	43.0

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