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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD
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November 2013
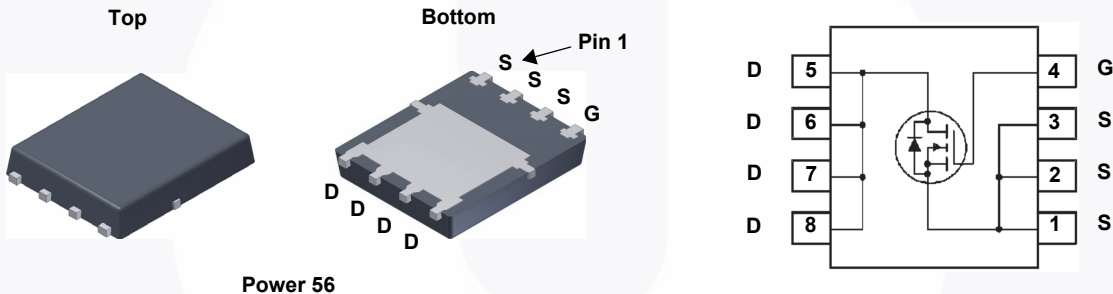
FDMS030N06B

N-Channel PowerTrench® MOSFET
60 V, 100 A, 3 mΩ

Features

- $R_{DS(on)}$ = 2.4 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 50 A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies
- Renewable system

Top

Bottom

S S S G — Pin 1

D D D D

Power 56

D	5		4	G
D	6		3	S
D	7		2	S
D	8		1	S

MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FDMS030N06B	Unit
V_{DSS}	Drain to Source Voltage			60	V
V_{GSS}	Gate to Source Voltage			±20	V
I_D	Drain Current	- Continuous (T_C = 25°C)	(Note1)	100	A
		- Continuous (T_A = 25°C)	(Note 2a)	22.1	
I_{DM}	Drain Current	- Pulsed	(Note 3)	400	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 4)	248	mJ
P_D	Power Dissipation	(T_C = 25°C)		104	W
		(T_A = 25°C)	(Note 2a)	2.5	W
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C

Thermal Characteristics

Symbol	Parameter		FDMS030N06B	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.		1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	(Note 2a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS030N06B	FDMS030N06B	Power 56	13 "	12 mm	3000 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

| Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV$_{DSS}$	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0V	60	-	-	V
∆BV$_{DSS}$ / ∆T$_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	-	0.03	-	V/^{o}C
I$_{DSS}$	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	-	-	1	µA
I$_{GSS}$	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
V$_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	2.5	3.3	4.5	V
R$_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 50 A	-	2.4	3.0	mΩ
g$_{FS}$	Forward Transconductance	V_{DS} = 10 V, I_D = 50 A	-	119	-	S
Dynamic Characteristics						
C$_{iss}$	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V f = 1 MHz	-	5685	7560	pF
C$_{oss}$	Output Capacitance		-	1720	2290	pF
C$_{rss}$	Reverse Transfer Capacitance		-	59	-	pF
C$_{oss}$(er)	Engry Releted Output Capacitance	V_{DS} = 30 V, V_{GS} = 0 V	-	2504	-	pF
Q$_{g(tot)}$	Total Gate Charge at 10V		-	75	-	nC
Q$_{gs}$	Gate to Source Gate Charge	V_{DS} = 30 V, I_D = 50 A V_{GS} = 0 V to 10 V	-	30	-	nC
Q$_{gd}$	Gate to Drain "Miller" Charge		-	14	-	nC
V$_{plateau}$	Gate Plateau Volatge	(Note 5)	-	5.4	-	V
Q$_{sync}$	Total Gate Charge Sync.	V_{DS} = 0 V, I_D = 50 A	-	66.2	-	nC
Q$_{oss}$	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V	-	174	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	1.05	-	Ω
Switching Characteristics						
t$_{d(on)}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 50 A V_{GS} = 10 V, R$_G$ = 4.7 Ω	-	39	88	ns
t$_r$	Turn-On Rise Time		-	20	50	ns
t$_{d(off)}$	Turn-Off Delay Time		-	52	114	ns
t$_f$	Turn-Off Fall Time	(Note 5)	-	16	42	ns
Drain-Source Diode Characteristics						
I$_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	100	A
I$_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	400	A
V$_{SD}$	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 50 A	-	-	1.25	V
t$_{rr}$	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 50 A	-	71	-	ns
Q$_{rr}$	Reverse Recovery Charge	dI$_F$/dt = 100 A/µs	-	85	-	nC

Notes:

1. Silicon limited I_D rating = 147 A.
2. R$_{θJA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R$_{θJC}$ is guaranteed by design while R$_{θCA}$ is determined by the user's board design.
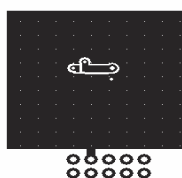
a. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.

b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

3. Repetitive rating: pulse-width limited by maximum junction temperature.
4. L = 0.3 mH, I_{AS} = 40.7 A, V_{DD} = 50 V, V_{GS} = 10 V, starting T$_J$ = 25°C.
5. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics
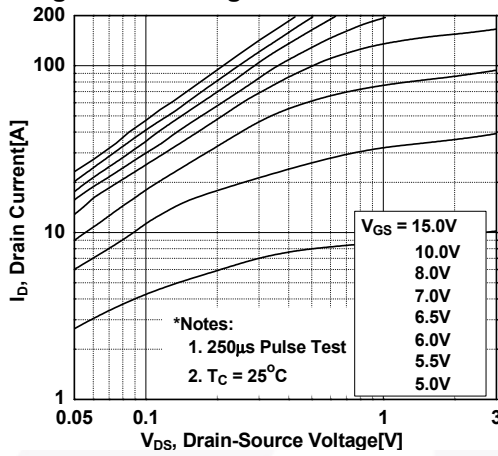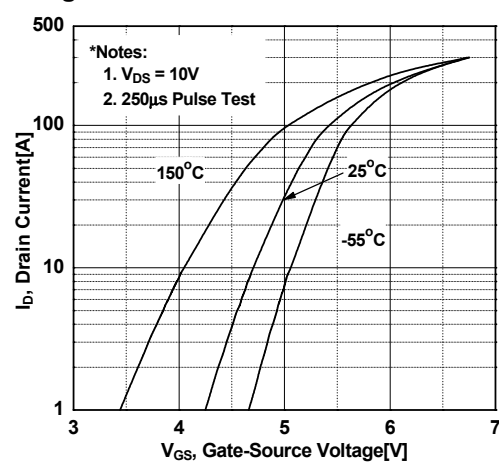
Figure 1. On-Region Characteristics

$V_{GS} = 15.0V$
10.0V
8.0V
7.0V
6.5V
6.0V
5.5V
5.0V

*Notes:
1. 250µs Pulse Test
2. $T_C = 25^oC$

I_D, Drain Current[A]
V_{DS}, Drain-Source Voltage[V]

Figure 2. Transfer Characteristics

*Notes:
1. $V_{DS} = 10V$
2. 250µs Pulse Test

150°C   25°C
-55°C

I_D, Drain Current[A]
V_{GS}, Gate-Source Voltage[V]

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

$V_{GS} = 10V$

$V_{GS} = 20V$

*Note: $T_C = 25^oC$

$R_{DS(ON)}$ [mΩ], Drain-Source On-Resistance
I_D, Drain Current [A]
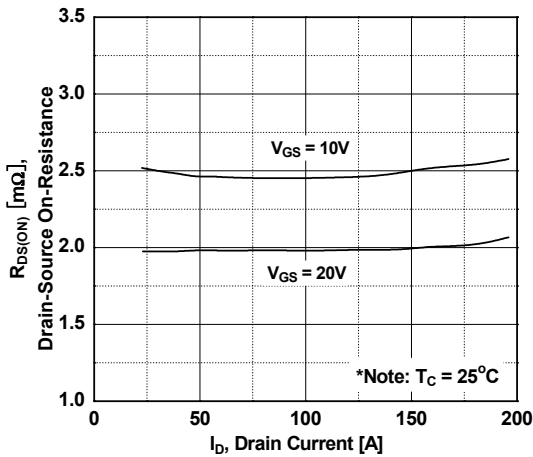
Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

150°C   25°C

*Notes:
1. $V_{GS} = 0V$
2. 250µs Pulse Test

I_S, Reverse Drain Current [A]
V_{SD}, Body Diode Forward Voltage [V]
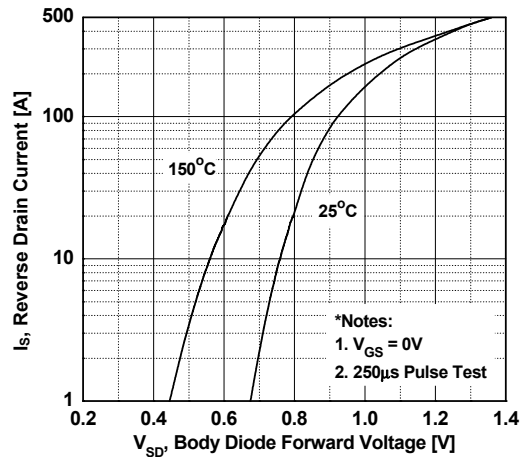
Figure 5. Capacitance Characteristics

C_{iss}
C_{oss}
C_{rss}

*Note:
1. $V_{GS} = 0V$
2. f = 1MHz

$C_{iss} = C_{gs} + C_{gd}$ (C_{ds} = shorted)
$C_{oss} = C_{ds} + C_{gd}$
$C_{rss} = C_{gd}$

Capacitances [pF]
V_{DS}, Drain-Source Voltage [V]
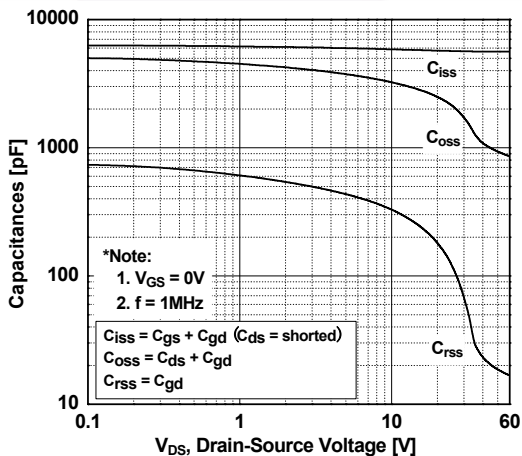
Figure 6. Gate Charge Characteristics

$V_{DS} = 12V$
$V_{DS} = 30V$
$V_{DS} = 48V$

*Note: I_D = 50A

V_{GS}, Gate-Source Voltage [V]
Q_g, Total Gate Charge [nC]
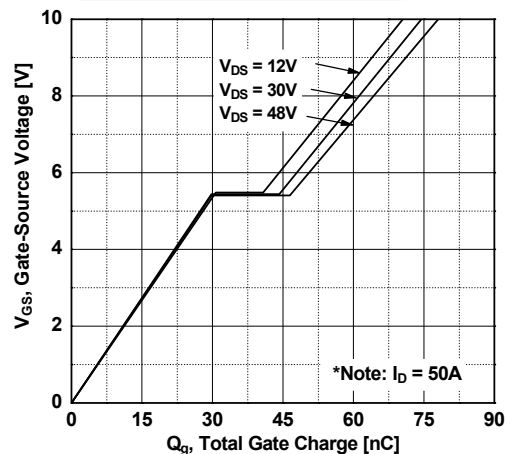
Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

*Notes:
1. $V_{GS} = 0V$
2. $I_D = 250\mu A$

Axes: BV_{DSS}, [Normalized] Drain-Source Breakdown Voltage vs. T_J, Junction Temperature [°C]
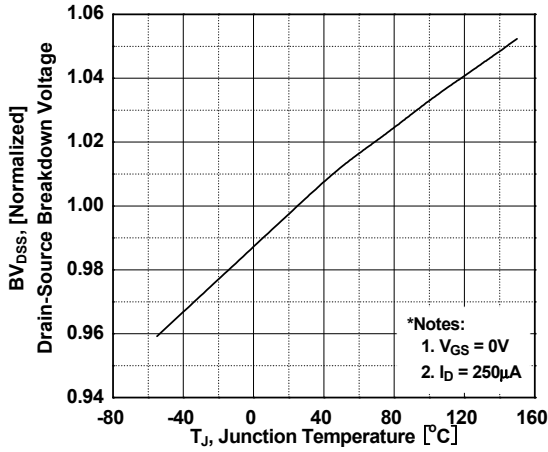
Figure 8. On-Resistance Variation vs. Temperature

*Notes:
1. $V_{GS} = 10V$
2. $I_D = 50A$

Axes: $R_{DS(on)}$, [Normalized] Drain-Source On-Resistance vs. T_J, Junction Temperature [°C]
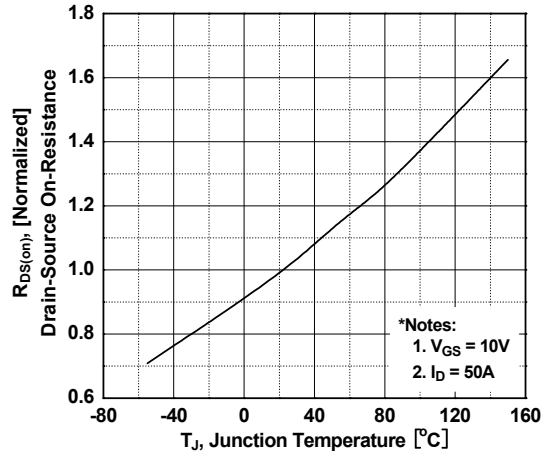
Figure 9. Maximum Safe Operating Area

1ms
10ms
100ms
DC

Operation in This Area is Limited by $R_{DS(on)}$
*Notes:
1. $T_a = 25°C$
2. $T_J = 150°C$
3. Single Pulse

Axes: I_D, Drain Current [A] vs. V_{DS}, Drain-Source Voltage [V]
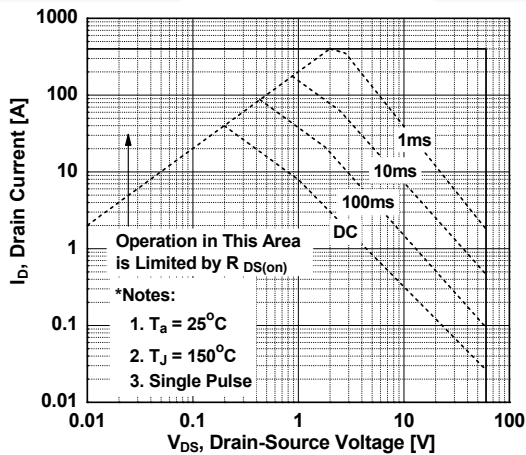
Figure 10. Maximum Drain Current vs. Case Temperature

$V_{GS} = 10V$

$R_{\theta JC} = 1.2°C/W$

Axes: I_D, Drain Current [A] vs. T_C, Case Temperature [°C]
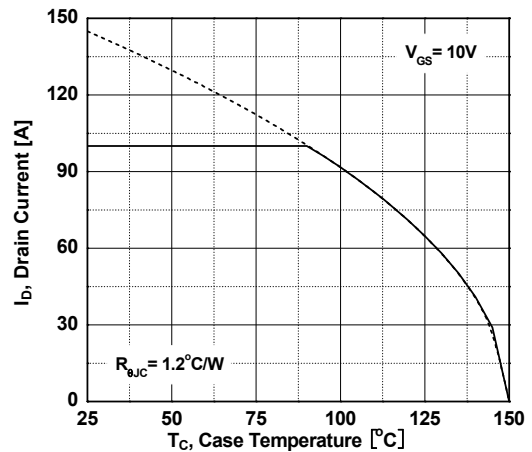
Figure 11. Eoss vs. Drain to Source Voltage

Axes: E_{OSS}, [µJ] vs. V_{DS}, Drain to Source Voltage [V]
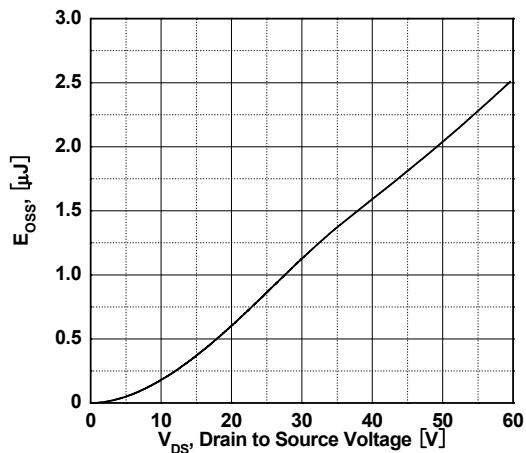
Figure 12. Unclamped Inductive Switching Capability

$T_J = 25°C$
$T_J = 125°C$

Axes: I_{AS}, Avalanche Current [A] vs. t_{AV}, Time In Avalanche [ms]
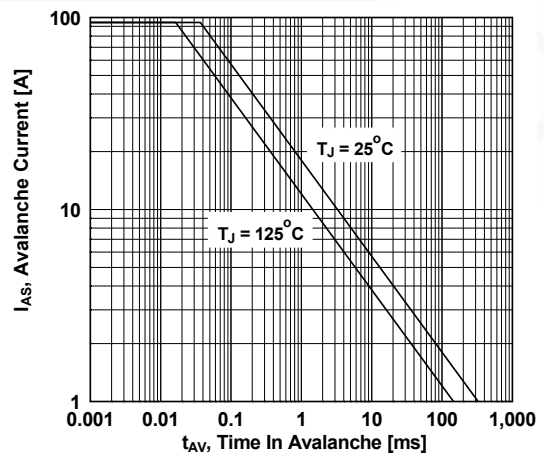
Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve
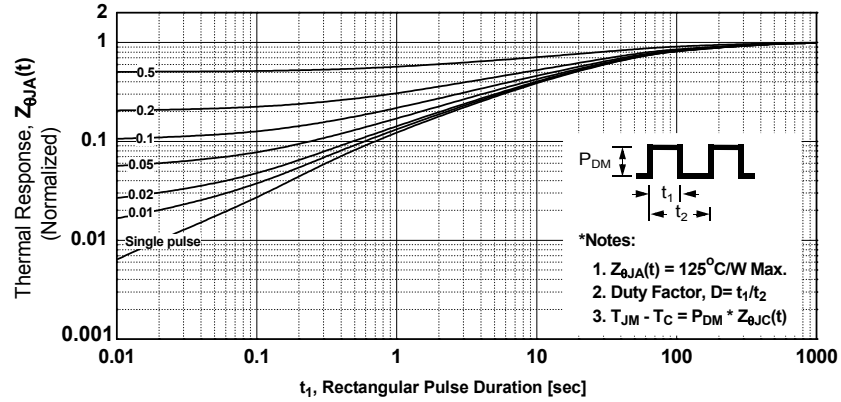
Figure 14. Gate Charge Test Circuit & Waveform
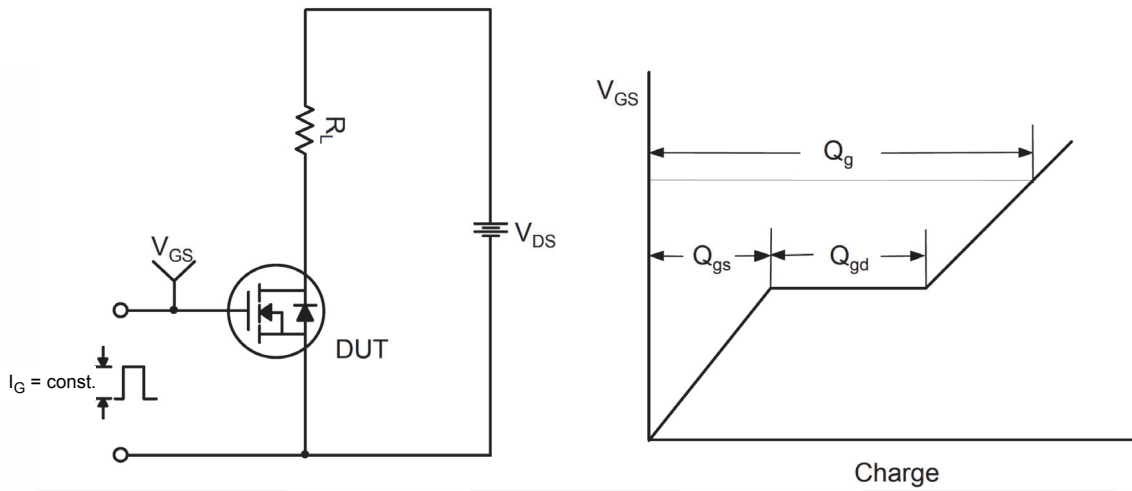
Figure 15. Resistive Switching Test Circuit & Waveforms
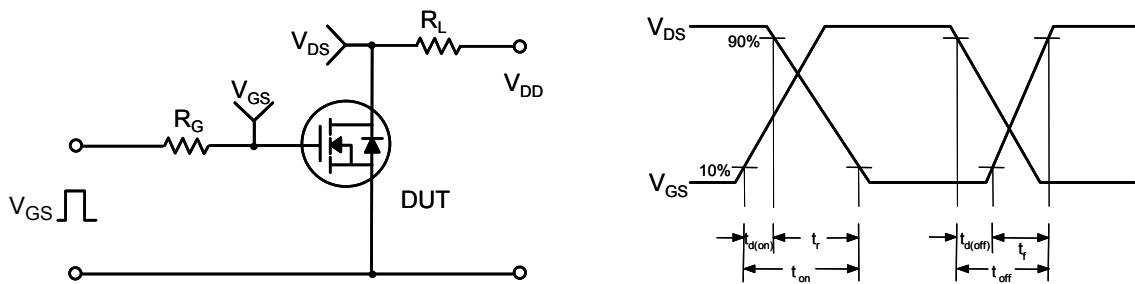
Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms
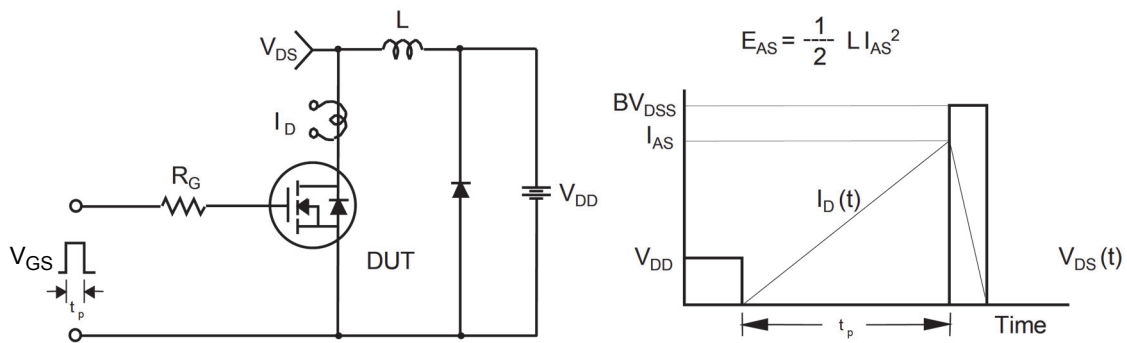
$$E_{AS} = \frac{1}{2} L I_{AS}^2$$
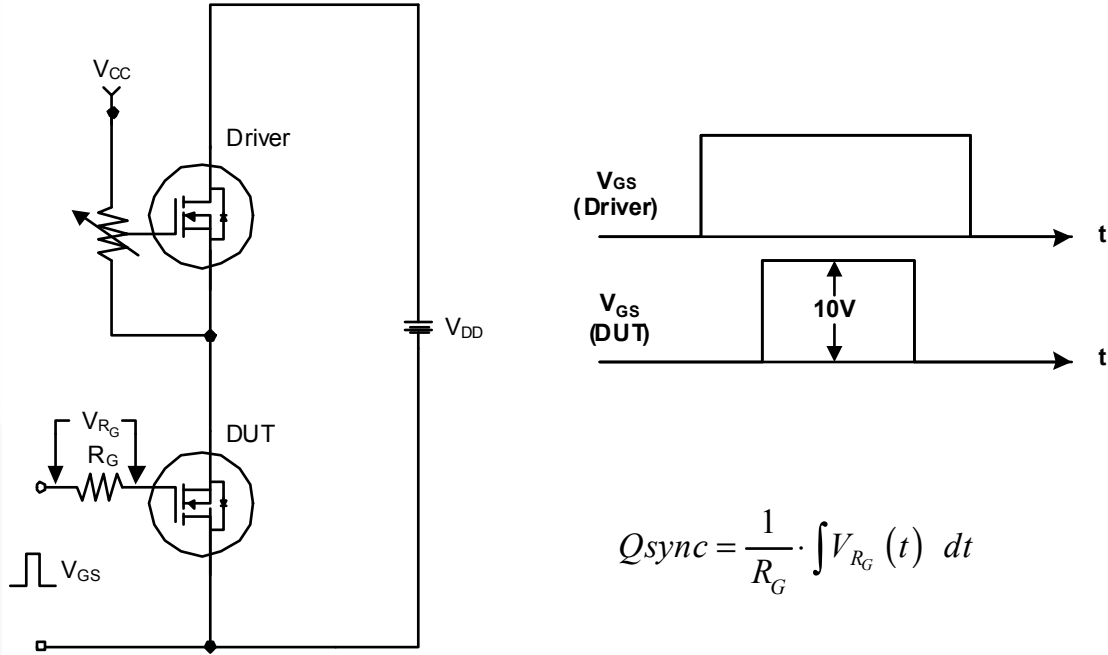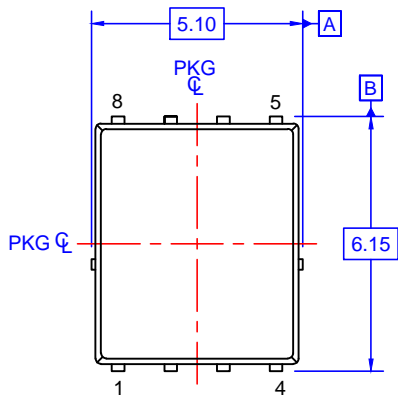
Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop
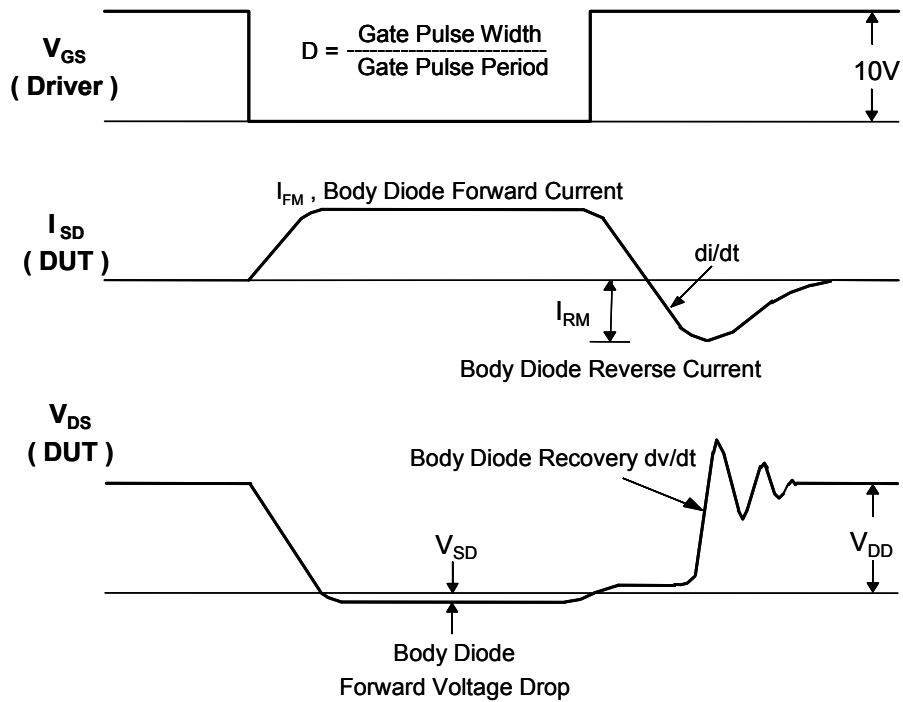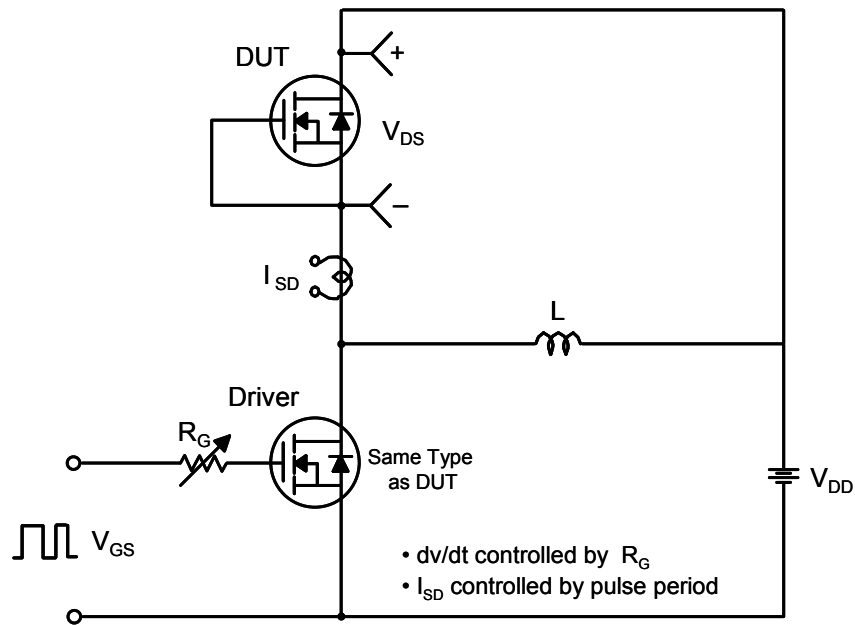
Figure 18. Total Gate Charge Qsync. Test Circuit & Waveforms

$$Qsync = \frac{1}{R_G} \cdot \int V_{R_G}\left(t\right) \; dt$$

PQFN8 5X6, 1.27P
CASE 483AE
ISSUE A

TOP VIEW

5.10 | A |
PKG C̸L
8   5
| B |
PKG C̸L
6.15

1   4

SEE DETAIL B

5.85
5.65
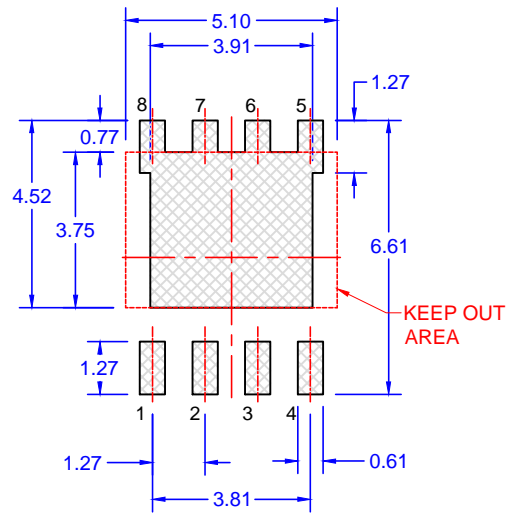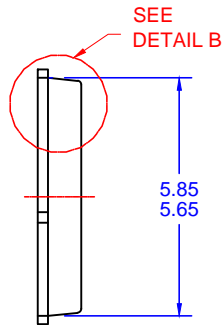
LAND PATTERN RECOMMENDATION

5.10
3.91
1.27
8 7 6 5
0.77
4.52
3.75
6.61
KEEP OUT AREA
1.27
1 2 3 4
1.27
3.81
0.61

SIDE VIEW

5.00
4.80
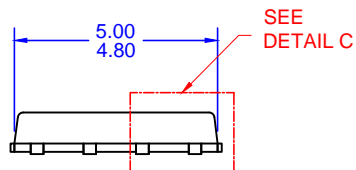
SEE DETAIL C

DETAIL C
SCALE: 2:1

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE

| // | 0.10 | C |
0°-12°
0.05
0.00
8X
| ⌒ | 0.08 | C |
0.35
0.15
1.10
0.90
| C |
SEATING PLANE

DETAIL B
SCALE: 2:1

0.35
0.15
0.30
0.05
0°-12°

BOTTOM VIEW

5.20
4.80
3.81
1.27
0.51 (8X)
0.31
(0.34)
| ⊕ | 0.10 Ⓜ | C | A | B |
1 2   3 4
0.76
0.51
(0.52)
6.25
5.90
(0.50)
(0.30)
(2X)
3.48 +0.30 / -0.10
8 7   6 5
0.20 +0.10 / -0.15 (8X)
3.96
3.61
0.44±0.10
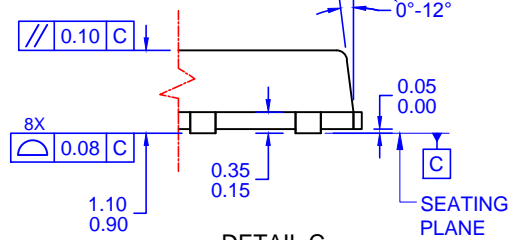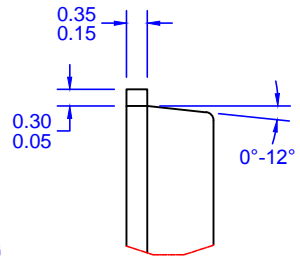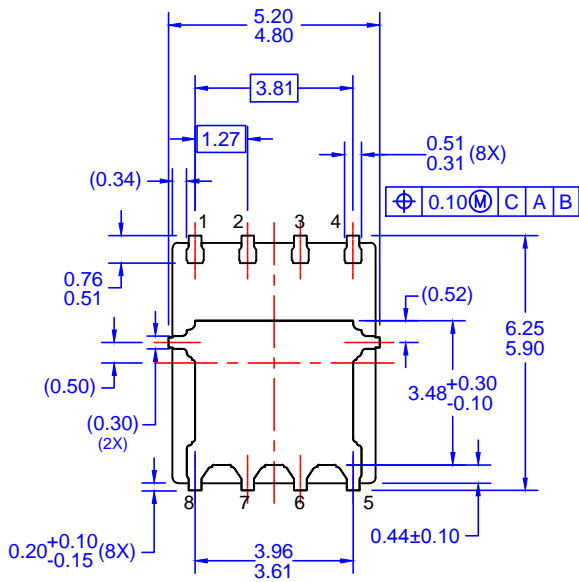
NOTES: UNLESS OTHERWISE SPECIFIED
A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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ON

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