

## LMH0202 Dual SMPTE 292M / 259M Serial Digital Cable Driver

Check for Samples: [LMH0202](#)

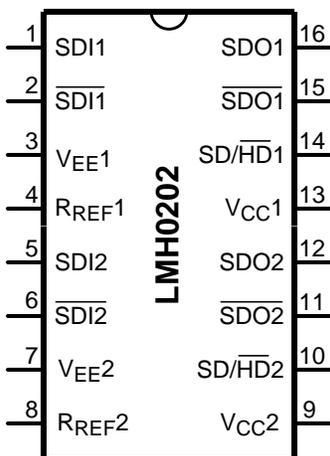
### FEATURES

- **SMPTE 292M, SMPTE 344M and SMPTE 259M Compliant**
- **Data Rates to 1.485 Gbps**
- **Dual Differential Inputs**
- **Dual 75Ω Differential Outputs**
- **Two Selectable Slew Rates**
- **Adjustable Output Amplitude**
- **Single 3.3V Supply Operation**
- **Commercial Temperature Range: 0°C to +70°C**
- **Typical Power Consumption: 250 mW in SD Mode and 300 mW in HD Mode**

### APPLICATIONS

- **SMPTE 292M, SMPTE 344M, and SMPTE 259M Serial Digital Interfaces**
- **DVB-ASI Applications**
- **Sonet/SDH and ATM Interfaces**
- **Digital Routers and Switches**
- **Distribution Amplifiers**
- **Buffer Applications**
- **Video Cameras**

### Connection Diagram



**Figure 1. 16-Pin TSSOP  
See PW Package**

### DESCRIPTION

The LMH0202 Dual SMPTE 292M / 259M serial digital cable driver is a monolithic, high-speed cable driver designed for use in SMPTE 292M / 259M serial digital video and ITU-T G.703 serial digital data transmission applications. The LMH0202 drives 75Ω transmission lines (Belden 8281, Belden 1694A or equivalent) at data rates up to 1.485 Gbps.

The LMH0202 provides two selectable slew rates for SMPTE 259M and SMPTE 292M compliance. The output voltage swing is adjustable via a single external resistor.

The LMH0202 offers the flexibility to implement either dual differential inputs or a single differential input (externally routed via PCB) to dual differential outputs. The latter option provides an ideal solution for DVB-ASI applications where only the non-inverted outputs are typically used.

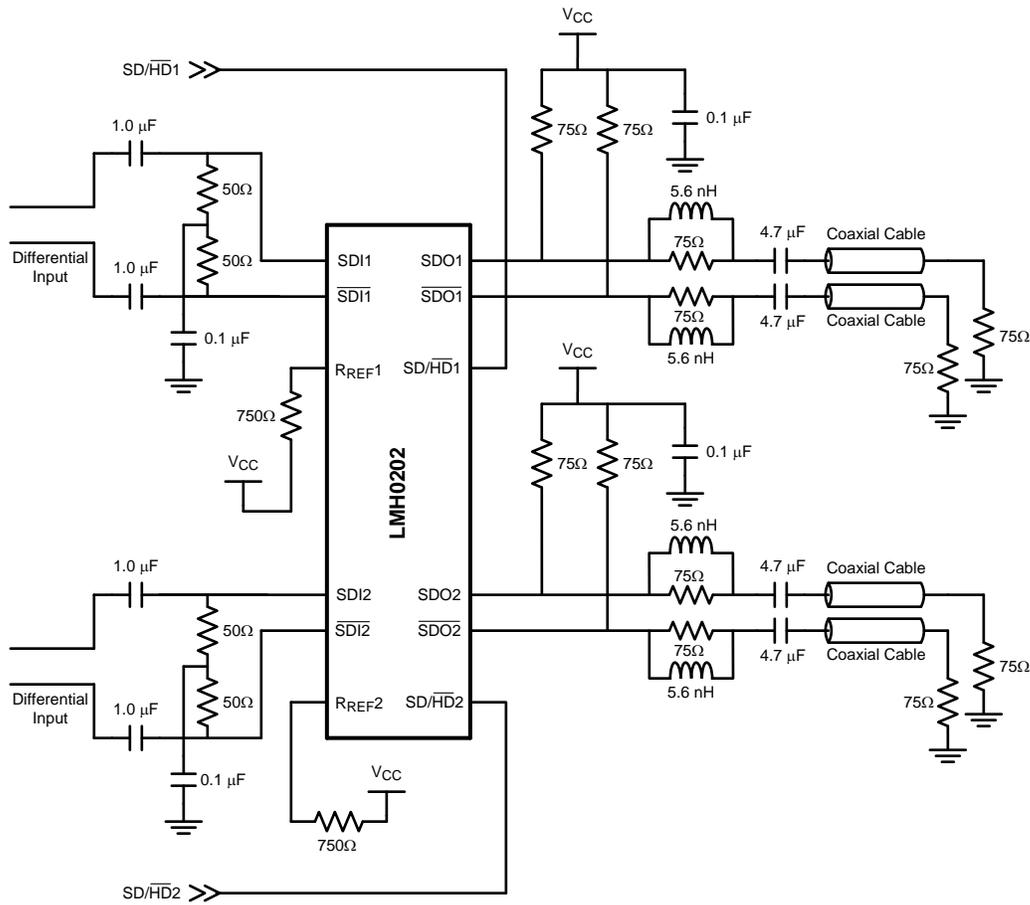
The LMH0202 is powered from a single 3.3V supply. Power consumption is typically 250 mW in SD mode and 300 mW in HD mode.



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Typical Application





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage:	-0.5V to 3.6V
Input Voltage (all inputs)	-0.3V to $V_{CC}+0.3V$
Output Current	28 mA
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering 4 Sec)	+260°C
Package Thermal Resistance $\theta_{JA}$ 16-pin TSSOP $\theta_{JC}$ 16-pin TSSOP	+125°C/W +105°C/W
ESD Rating (HBM)	5 kV
ESD Rating (MM)	250V

- (1) Absolute Maximum Ratings are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of [Electrical Characteristics](#) specifies acceptable device operating conditions.

### Recommended Operating Conditions

Supply Voltage ( $V_{CC} - V_{EE}$ ):	3.3V $\pm 5\%$
Operating Free Air Temperature ( $T_A$ )	0°C to +70°C

### DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(1)(2)</sup>.

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
$V_{CMIN}$	Input Common Mode Voltage		SDI1, $\overline{SDI1}$ , SDI2, $\overline{SDI2}$	1.6 + $V_{SDI}/2$		$V_{CC} -$ $V_{SDI}/2$	V
$V_{SDI}$	Input Voltage Swing	Differential		100		2000	mV <sub>P-P</sub>
$V_{CMOUT}$	Output Common Mode Voltage		SDO1, $\overline{SDO1}$ , SDO2, $\overline{SDO2}$		$V_{CC} -$ $V_{SDO}$		V
$V_{SDO}$	Output Voltage Swing	Single-ended, 75 $\Omega$ load, $R_{REF1} = 750\Omega$ 1%, $R_{REF2} = 750\Omega$ 1%		750	800	850	mV <sub>P-P</sub>
		Single-ended, 75 $\Omega$ load, $R_{REF1} = 590\Omega$ 1%, $R_{REF2} = 590\Omega$ 1%		900	1000	1100	mV <sub>P-P</sub>
$V_{SDHD}$	SD/ $\overline{HD}$ Input Voltage	Min for SD	SD/ $\overline{HD1}$ , SD/ $\overline{HD2}$	2.4			V
		Max for HD				0.8	V
$I_{SDHD}$	SD/ $\overline{HD}$ Input Current				3.7		$\mu$ A
$I_{CC}$	Supply Current	SD/ $\overline{HD1} = 0$ , SD/ $\overline{HD2} = 0$ <sup>(3)</sup>			90	98	mA
		SD/ $\overline{HD1} = 1$ , SD/ $\overline{HD2} = 1$ <sup>(3)</sup>			76	86	mA

- (1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to  $V_{EE} = 0$  Volts.  
 (2) Typical values are stated for  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ .  
 (3) Maximum  $I_{CC}$  is measured at  $V_{CC} = +3.465V$  and  $T_A = +70^\circ C$ .

## AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(1)</sup>.

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units	
DR <sub>SDI</sub>	Input Data Rate		<sup>(2)</sup> SDI1, $\overline{\text{SDI1}}$ , SDI2, $\overline{\text{SDI2}}$			1485	Mbps	
t <sub>jit</sub>	Additive Jitter	1.485 Gbps	SDO1, $\overline{\text{SDO1}}$ , SDO2, $\overline{\text{SDO2}}$		26		pSp-p	
		270 Mbps			18		pSp-p	
t <sub>r</sub> , t <sub>f</sub>	Output Rise Time, Fall Time	SD/ $\overline{\text{HD1}}$ = 0, SD/ $\overline{\text{HD2}}$ = 0, 20% – 80% <sup>(3)</sup>				120	220	ps
		SD/ $\overline{\text{HD1}}$ = 1, SD/ $\overline{\text{HD2}}$ = 1, 20% – 80% <sup>(3)</sup>		400	560	800	ps	
	Mismatch in Rise/Fall Time	<sup>(2)</sup>					30	ps
t <sub>OS</sub>	Output Overshoot	<sup>(2)</sup>					8	%
RL <sub>SDO</sub>	Output Return Loss	<sup>(4)</sup>			15	20		dB

(1) Typical values are stated for V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C.

(2) Specification is ensured by characterization.

(3) Specification is ensured by characterization and verified by test.

(4) Output return loss is dependent on board design. The LMH0202 meets this specification on the SD202 evaluation board from 5 MHz to 1.5 GHz.

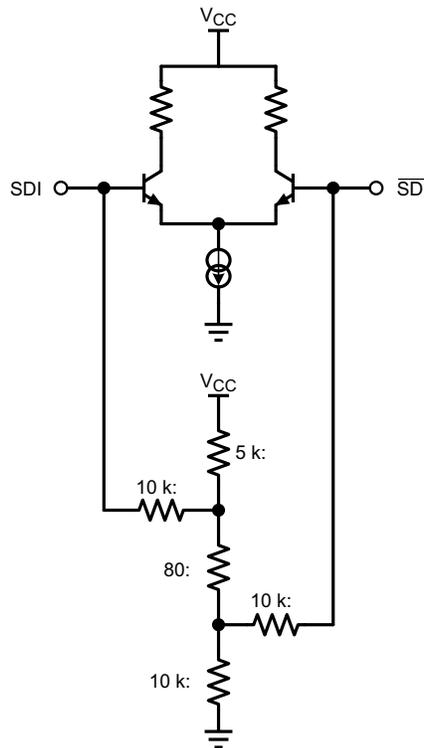
**Table 1. PIN DESCRIPTIONS**

Pin #	Name	Description
1	SDI1	Serial data true input.
2	$\overline{\text{SDI1}}$	Serial data complement input.
3	$V_{EE1}$	Negative power supply (ground).
4	$R_{REF1}$	Output driver level control. Connect a resistor to $V_{CC}$ to set output voltage swing.
5	SDI2	Serial data true input.
6	$\overline{\text{SDI2}}$	Serial data complement input.
7	$V_{EE2}$	Negative power supply (ground).
8	$R_{REF2}$	Output driver level control. Connect a resistor to $V_{CC}$ to set output voltage swing.
9	$V_{CC2}$	Positive power supply (+3.3V).
10	SD/HD2	Output slew rate control. Output rise/fall time complies with SMPTE 292M when low and SMPTE 259M when high.
11	$\overline{\text{SDO2}}$	Serial data complement output.
12	SDO2	Serial data true output.
13	$V_{CC1}$	Positive power supply (+3.3V).
14	SD/HD1	Output slew rate control. Output rise/fall time complies with SMPTE 292M when low and SMPTE 259M when high.
15	$\overline{\text{SDO1}}$	Serial data complement output.
16	SDO1	Serial data true output.

**DEVICE OPERATION**

**INPUT INTERFACING**

The LMH0202 accepts either differential or single-ended input. The inputs are self-biased, allowing for simple AC or DC coupling. DC-coupled inputs must be kept within the specified common-mode range. SDI and  $\overline{\text{SDI}}$  are self-biased at approximately 2.1V with  $V_{CC} = 3.3V$ . Figure 2 shows the differential input stage for SDI and  $\overline{\text{SDI}}$ .



**Figure 2. Differential Input Stage for SDI and  $\overline{\text{SDI}}$ .**

## DVB-ASI APPLICATIONS

The dual differential inputs of the LMH0202 may be externally routed to a single differential input as shown in Figure 3. This provides a solution for DVB-ASI applications where two non-inverted outputs are needed.

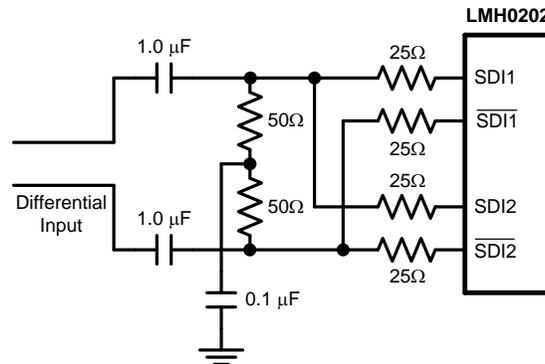


Figure 3. Single Differential Input for DVB-ASI

## OUTPUT INTERFACING

The LMH0202 uses current mode outputs. Single-ended output levels are 800 mV<sub>P,P</sub> into 75 Ω AC-coupled coaxial cable (with  $R_{REF} = 750\Omega$ ). Output level is controlled by the value of the resistor connected between the  $R_{REF}$  pin and  $V_{CC}$ .

The  $R_{REF}$  resistor should be placed as close as possible to the  $R_{REF}$  pin. In addition, the copper in the plane layers below the  $R_{REF}$  network should be removed to minimize parasitic capacitance.

## OUTPUT SLEW RATE CONTROL

The LMH0202 output rise and fall times are selectable for either SMPTE 259M or SMPTE 292M compliance via the  $SD/\overline{HD}$  pin. For slower rise and fall times, or SMPTE 259M compliance,  $SD/\overline{HD}$  is set high. For faster rise and fall times, or SMPTE 292M compliance,  $SD/\overline{HD}$  is set low.

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**REVISION HISTORY**

<b>Changes from Revision B (April 2013) to Revision C</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<a href="#">6</a>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0202MT/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 70	L202	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

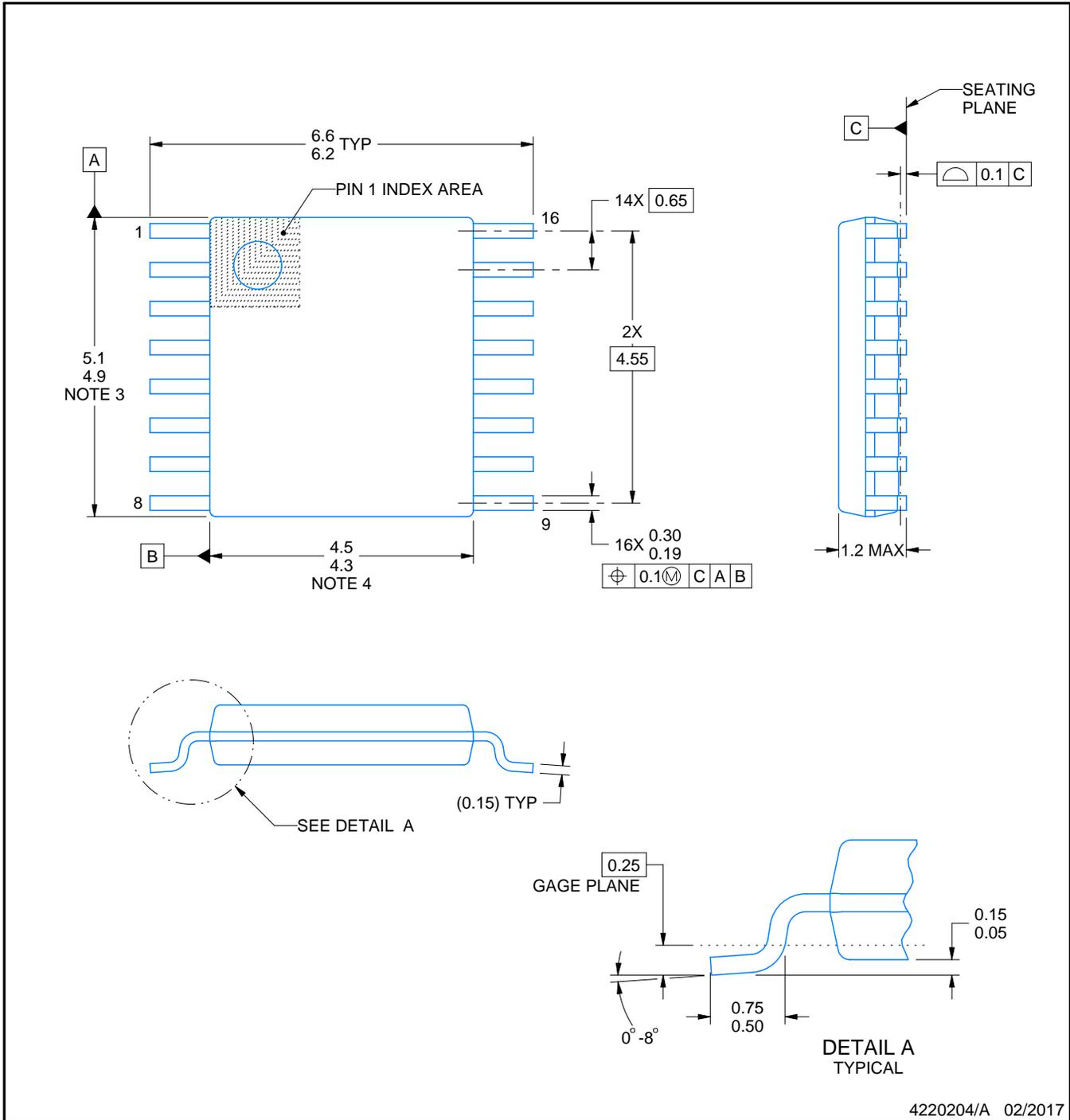
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

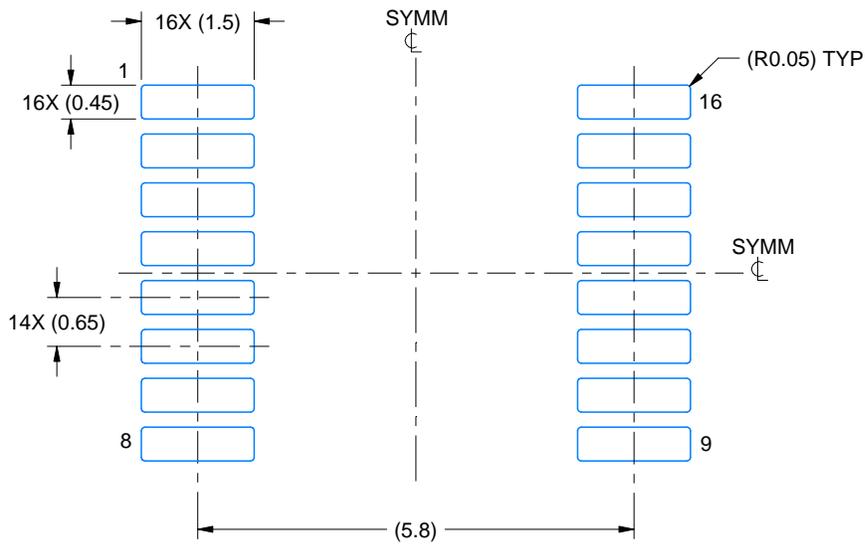
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

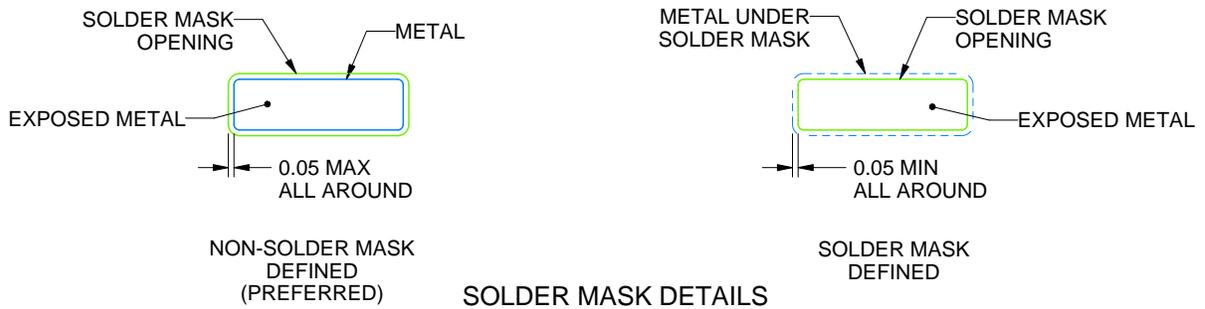
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

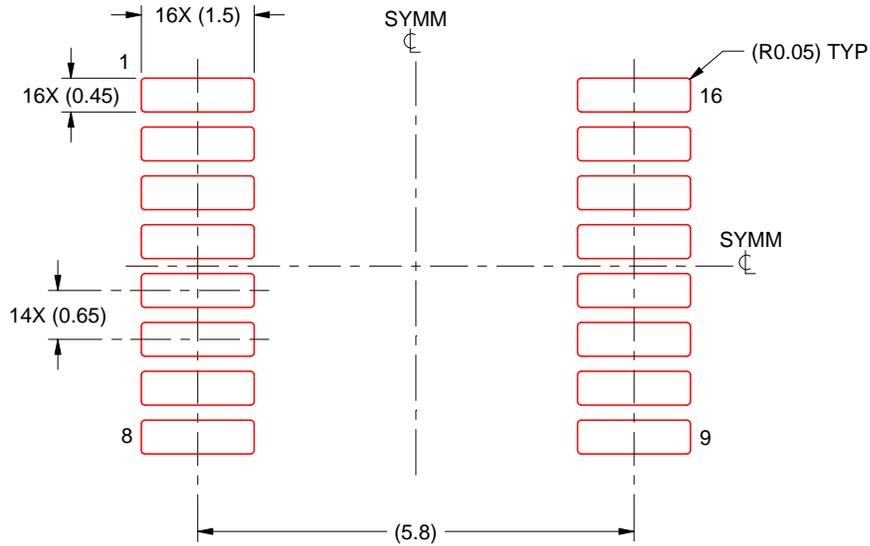
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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