

### Standalone Power Factor Correction (PFC) Controller in Continuous Conduction Mode (CCM)

#### Product Highlights

- High efficiency over the whole load range
- Lowest count of external components
- Accurate and adjustable switching frequency
- Bulk voltage good signal for inrush relay control or PWM IC enabling
- Integrated digital voltage loop compensation
- Fast output dynamic response during load jump
- External synchronization
- Extra low peak current limitation

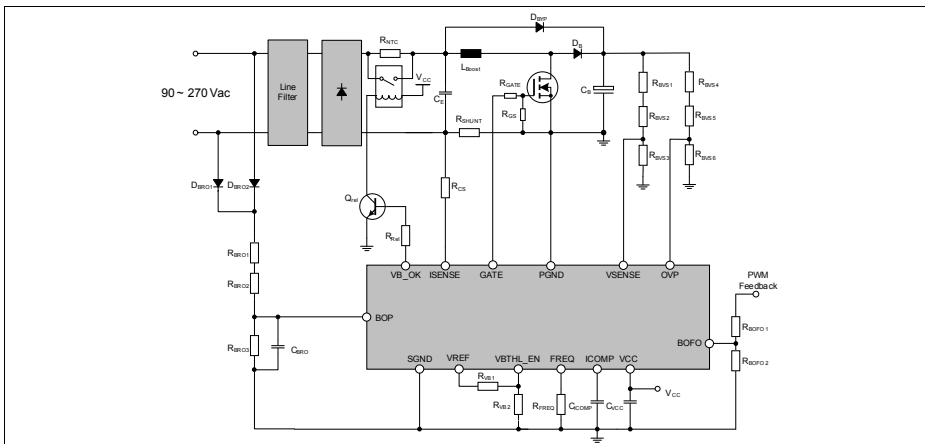


#### Features

- Continuous current operation mode PFC
- Wide input range of V<sub>CC</sub> up to 25V
- Programmable boost follower step level according to input line and output power conditions
- Enhanced dynamic response without input current distortion
- Accurate brown-out protection threshold
- External current loop compensation for greater user flexibility
- Open loop protection
- Second over bulk voltage protection
- PFC enable function
- Separate signal and power ground pins
- Maximum duty cycle of 95% (typical)

#### Description

The ICE3PCS01G is a 14-pins wide input range controller IC for active power factor correction converters. It is designed for converters in boost topology, and requires few external components. Its power supply is recommended to be provided by an external auxiliary supply which will switch on and off the IC.



Type	Package
ICE3PCS01G	PG-DSO-14

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# 1 Pin Configuration and Functionality

## 1.1 Pin Configuration

Pin	Symbol	Function
1	BOFO	Boost Follower Setting
2	ISENSE	Current Sense Input
3	SGND	Signal Ground
4	ICOMP	Current Loop Compensation
5	FREQ	Switching Frequency Setting
6	VB_OK	Bulk Voltage OK signal
7	VBTHL_EN	PFC Enable Function
8	VREF	Voltage Reference
9	BOP	Brownout Protection
10	OVP	Over Voltage Protection
11	VSENSE	Bulk Voltage Sense
12	VCC	IC Supply Voltage
13	GATE	Gate Drive
14	PGND	Power Ground

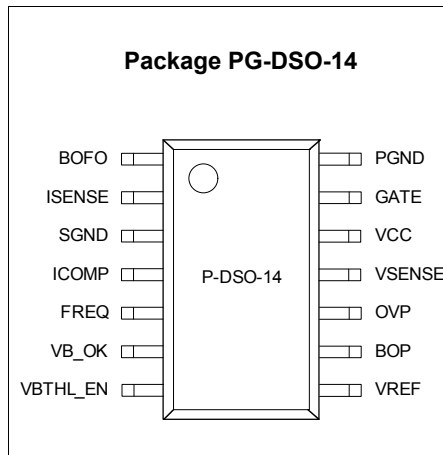


Figure 1 Pin Configuration (top view)

## 1.2 Pin Functionality

### BOFO (Boost Follower setting)

An external DC voltage to this pin indicating the PWM output power which can be set to enter the Boost follower low step.

### ISENSE (Current Sense Input)

The ISENSE Pin senses the voltage drop at the external sense resistor ( $R_{SHUNT}$ ). This is the input signal for the average current regulation in the current loop. It is also fed to the peak current limitation block.

During power up time, high inrush currents cause high negative voltage drop at  $R_{SHUNT}$ , driving currents out of pin 2 which could be beyond the absolute maximum ratings. Therefore a series resistor ( $R_{CS}$ ) of around  $50\Omega$  is recommended in order to limit this current into the IC.

### SGND (Signal Ground)

The ground potential of the IC.

### ICOMP (Current Loop Compensation)

Low pass filter and compensation of the current control loop. The capacitor which is connected at this pin integrates the output current of OTA6 and averages the current sense signal.

### FREQ (Frequency Setting)

This pin allows the setting of the operating switching frequency by connecting a resistor to ground. The frequency range is from 21kHz to 100kHz.

### VB\_OK (Bulk Voltage OK signal)

This pin is pulled up to 5V internally once the bulk voltage is higher than 95% rated voltage and pulled down to ground once VSENSE pin is lower than preset VBTHL\_EN threshold. This signal can enable the PWM IC or control the inrush relay.

### VBTHL\_EN

An external voltage reference can be applied to VBTHL\_EN to set the turn-off threshold of VB\_OK signal. The IC can be shut down by pulling the pin lower than 0.5V

### VREF (Voltage Reference)

This pin is the 5V regulator output with a 5mA sourcing current (minimum).

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**Pin Configuration and Functionality****BOP (Brownout Protection)**

BOP monitors the AC input voltage for Brownout Protection and line range selection

**OVP**

A resistive voltage divider from bulk voltage to SGND can set the over voltage protection threshold. This additional OVP is able to ensure system safety operation.

**VSENSE**

VSENSE is connected via a resistive divider to the bulk voltage. The voltage of VSENSE relative to SGND represents the output voltage. The bulk voltage is monitored for voltage regulation, over voltage protection and open loop protection.

**VCC**

VCC provides the power supply of the ground related to IC section.

**GATE**

GATE is the output for driving the PFC MOSFET. Its gate drive voltage is clamped at 15V (typically).

**PGND (Power Ground)**

Gate switching ground.

## 2 Block Diagram

A functional block diagram is given in Figure 2. Note that the figure only shows the brief functional block and does not represent the implementation of the IC.

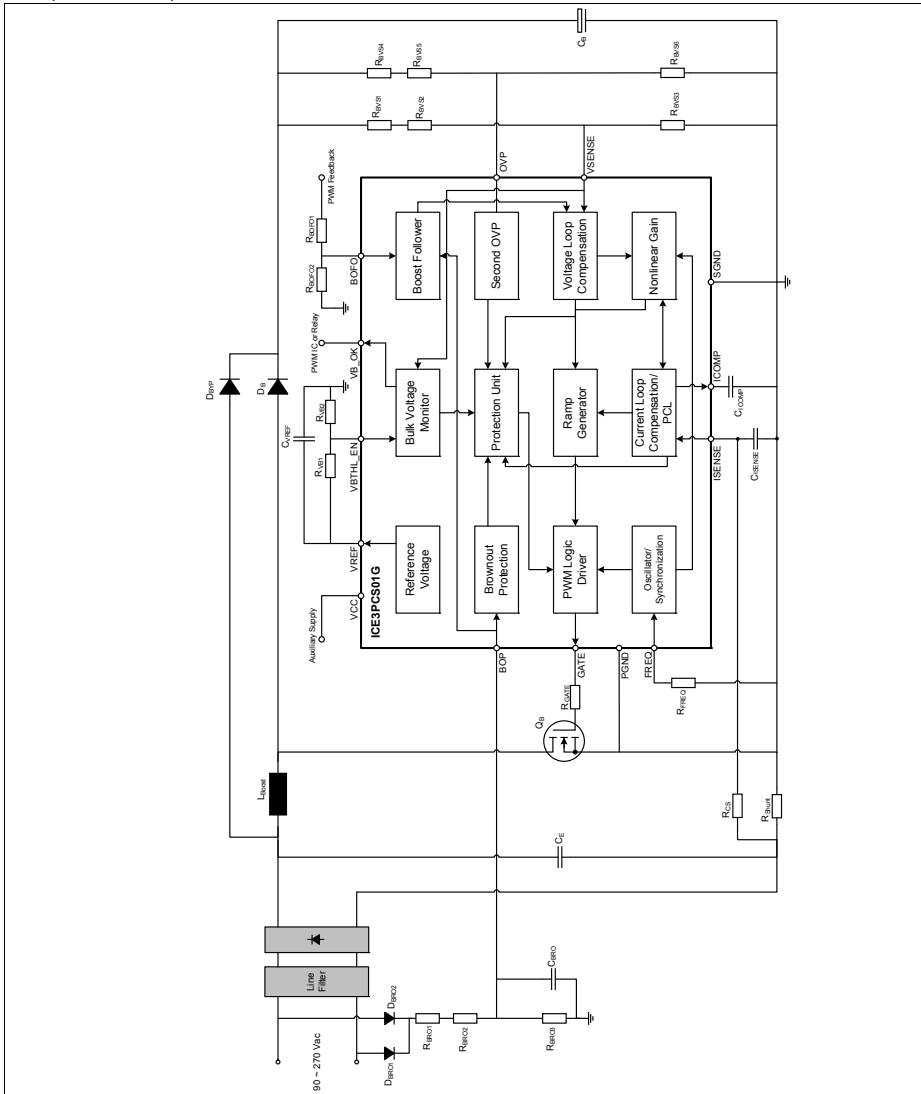


Figure 2 Block Diagram

**Table 1 Bill Of Material**

Component	Parameters
Rectifier Bridge	GBU8J
$C_E$	100nF/X2/275V
$L_{Boost}$	750uH
$Q_B$	IPP60R199CP
$D_{BYP}$	MUR360
$D_B$	IDT04S60C
$C_B$	220μF/450V
$D_{BRO1...2}$	1N4007
$R_{BRO1...2}$	3.9MΩ
$R_{BRO3}$	130kΩ
$C_{BRO}$	3μF
$R_{shunt}$	30mΩ
$C_{isense}$	1nF
$R_{CS}$	50Ω
$R_{GATE}$	3.3Ω
$R_{FREQ}$	67kΩ
$C_{ICOMP}$	4.7nF/25V
$R_{BVS1...2}$	1.5MΩ
$R_{BVS3}$	18.85kΩ
$R_{BVS4...5}$	2MΩ
$R_{BVS6}$	23kΩ
$R_{VB1}$	330kΩ
$R_{VB2}$	200kΩ
$C_{VREF}$	100nF/25V
$R_{BOFO1...2}$	200kΩ

## 3 Functional Description

### 3.1 General

The ICE3PCS01G is a 14-pins control IC for power factor correction converters. It is suitable for wide range line input applications from 85 to 265 VAC with overall efficiency above 90%. The IC supports converters in boost topology and it operates in continuous conduction mode (CCM) with average current control. The IC operates with a cascaded control; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load condition, depending on the choke inductance, the system may enter into discontinuous conduction mode (DCM) resulting in a higher harmonics but still meeting the Class D requirement of IEC 1000-3-2.

The outer voltage loop controls the output bulk voltage, integrated digitally within the IC. Depending on the load condition, internal PI compensation output is converted to an appropriate DC voltage which controls the amplitude of the average input current.

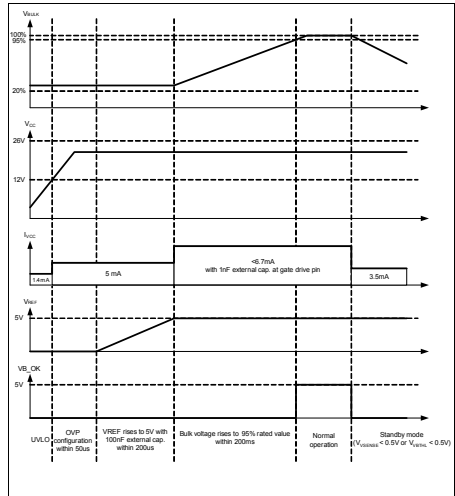
The IC is equipped with various protection features to ensure safe operating condition for both the system and device.

### 3.2 Power Supply

An internal under voltage lockout (UVLO) block monitors the VCC power supply. As soon as it exceeds 12.0V and both voltages at pin 11 (VSENSE) >0.5V and pin 9 (BOP) >1.25V, the IC begins operating its gate drive and performs its startup as shown in Figure 3.

If VCC drops below 11V, the IC is off. The IC will then be consuming typically 1.4mA, whereas consuming 6.7mA during normal operation

The IC can be turned off and forced into standby mode by pulling down the voltage at pin 11 (VSENSE) below 0.5V or the voltage at pin 7 (VBTHL\_EN) below 0.5V.



**Figure 3 State of Operation respect to VCC**

### 3.3 Start-up

During power up when the  $V_{out}$  is less than 95% of the rated level, internal voltage loop output increases from initial voltage under the soft-start control. This results in a controlled linear increase of the input current from 0A thus reducing the stress in the external components.

Once  $V_{out}$  has reached 95% of the rated level, the soft-start control is released to achieve good regulation and dynamic response and  $VB\_OK$  pin outputs 5V indicating PFC stage in normal operation.

### 3.4 Frequency Setting and External Synchronization

The IC can provide external switching frequency setting by an external resistor  $R_{FREQ}$  and the online synchronization by external pulse signal at FREQ pin.

#### 3.4.1 Frequency Setting

The switching frequency of the PFC converter can be set with an external resistor  $R_{FREQ}$  at FREQ pin as shown Figure 2. The pin voltage at  $V_{FREQ}$  is typical 1V. The corresponding capacitor for the oscillator is integrated in the device and the  $R_{FREQ}$ /frequency is given in Figure 4. The recommended operating frequency range is from 21kHz to 100kHz. As an example, a  $R_{FREQ}$  of 67k $\Omega$  at pin FREQ will set a switching frequency  $F_{SW}$  of 65kHz typically.



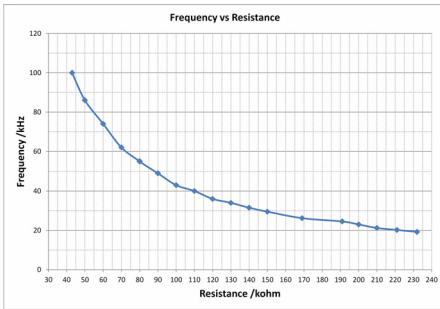


Figure 4 Frequency Versus  $R_{FREQ}$

### 3.4.2 External Synchronization

The switching frequency can be synchronized to the external pulse signal after 6 external pulses delay once the voltage at the FREQ pin is higher than 2.5V. The synchronization means two points. Firstly, the PFC switching frequency is tracking the external pulse signal frequency. Secondly, the falling edge of the PFC signal is triggered by the rising edge of the external pulse signal. Figure 5 shows the blocks of frequency setting and synchronization. The external  $R_{SYN}$  combined with  $R_{FREQ}$  and the external diode  $D_{SYN}$  can ensure pin voltage to be kept between 1.0V (clamped externally) and 5V (maximum pin voltage). If the external pulse signal has disappeared longer than 108 $\mu$ s (typical) the switching frequency will be synchronized to internal clock set by the external resistor  $R_{FREQ}$ .

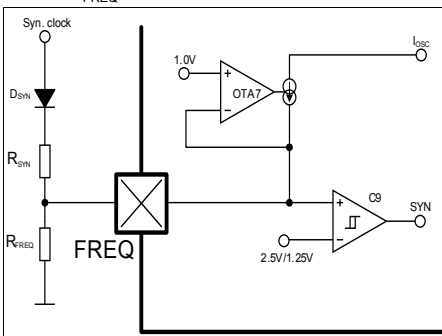


Figure 5 Frequency Setting and Synchronization

## 3.5 Voltage Loop

The voltage loop is the outer loop of the cascaded control scheme which controls the PFC output bus voltage  $V_{OUT}$ . This loop is closed by the feedback sensing voltage at VSENSE which is a resistive divider tapping from  $V_{OUT}$ . The pin VSENSE is the input of sigma-delta ADC which has an internal reference of 2.5V and sampling rate of 3.55kHz (typical). The voltage loop compensation is integrated digitally for better dynamic response and saving design effort. Figure 6 shows the important blocks of this voltage loop.

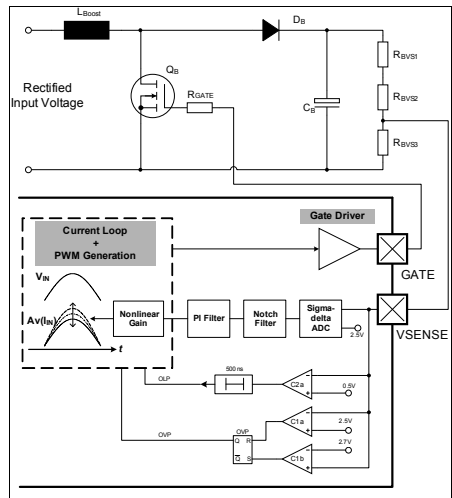


Figure 6 Voltage Loop

### 3.5.1 Notch Filter

In the PFC converter, an averaged current through the output diode of rectified sine waveform charges the output capacitor and results in a ripple voltage at the output capacitor with a frequency two times of the line frequency. In this digital PFC, a notch filter is used to remove the ripple of the sensed output voltage while keeping the rest of the signal almost uninfluenced. In this way, an accurate and fast output voltage regulation without influence of the output voltage ripple is achieved.

### 3.5.2 Voltage Loop Compensation

The Proportion-Integration (PI) compensation of the voltage loop is integrated digitally inside the IC. The digital data out of the PI compensator is converted to analog voltage for current loop control.

## Functional Description

The nonlinear gain block controls the amplitude of the regulated inductor current. The input of this block is the output voltage of integrated PI compensator. This block has been designed to reduce the voltage loop dependency on the input voltage in order to support the wide input voltage range (85VAC-265VAC). Figure 7 gives the relative output power transfer curve versus the digital word from the integrated PI compensator. The output power at the input voltage of 85VAC and maximum digital word of 256 from PI compensator is set as the normative power and the power curves at different input voltage present the relative power to the normative one.

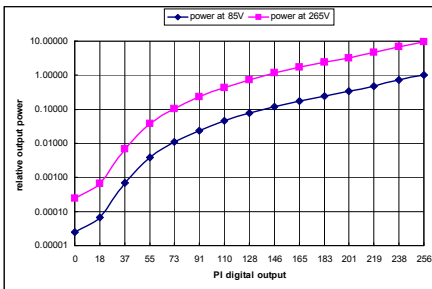


Figure 7 Power Transfer Curve

## 3.6 Average Current Control

The choke current is sensed through the voltage across the shunt resistor and averaged by the ICOMP pin capacitor so that the IC can control the choke current to track the instant variation of the input voltage.

### 3.6.1 Complete Current Loop

The complete system current loop is shown in Figure 8. It consists of the current loop block which averages the voltage at ISENSE pin resulted from the inductor current flowing across  $R_{shunt}$ . The averaged waveform is compared with an internal ramp in the ramp generator and PWM block. Once the ramp crosses the average waveform, the comparator C10 turns on the driver stage through the PWM logic block. The Nonlinear Gain block defines the amplitude of the inductor current. The following sections describe the functionality of each individual blocks.

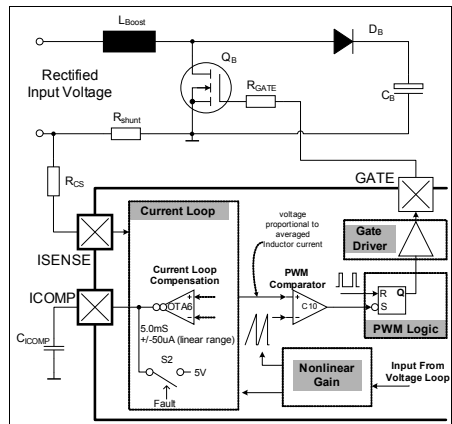


Figure 8 Complete System Current Loop

### 3.6.2 Current Loop Compensation

The compensation of the current loop is implemented at the ICOMP pin. This is OTA6 output and a capacitor  $C_{ICOMP}$  has to be installed at this node to ground (see Figure 8). Under normal mode of the operation, this pin gives a voltage which is proportional to the averaged inductor current. This pin is internally shorted to 5V in the event of standby mode.

### 3.6.3 Pulse Width Modulation (PWM)

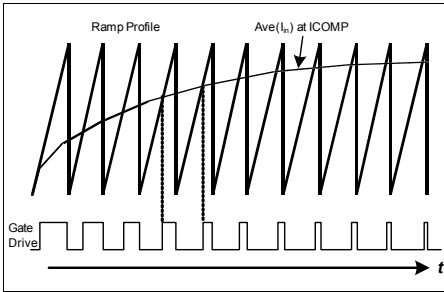
The IC employs an average current control scheme in continuous mode (CCM) to achieve the power factor correction. Assuming the loop voltage is working and output voltage is kept constant, the off duty cycle  $D_{OFF}$  for a CCM PFC system is given as:

$$D_{OFF} = V_{IN} / V_{OUT}$$

From the above equation,  $D_{OFF}$  is proportional to  $V_{IN}$ .

The objective of the current loop is to regulate the average inductor current such that it is proportional to the off duty cycle  $D_{OFF}$ , and thus to the input voltage  $V_{IN}$ . Figure 9 shows the scheme to achieve the objective.

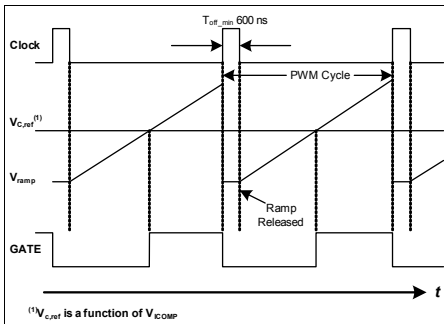
**Functional Description**



**Figure 9 Average Current Control in CCM**

The PWM is performed by the intersection of a ramp signal with the averaged inductor current at pin 4 (ICOMP). The PWM cycles starts with the Gate turn off for a duration of  $T_{OFFMIN}$  (600ns typ.) and the ramp is kept discharged. The ramp is allowed to rise after the  $T_{OFFMIN}$  expires. The off time of the boost transistor ends at the intersection of the ramp signal and the averaged current waveform. This results in the proportional relationship between the average current and the off duty cycle  $D_{OFF}$ .

Figure 10 shows the timing diagrams of the  $T_{OFFMIN}$  and the gate waveforms.



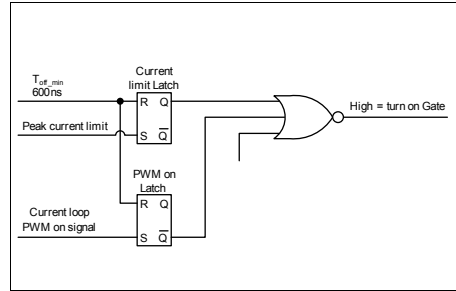
**Figure 10 Ramp and PWM waveforms**

**3.7 PWM Logic**

The PWM logic block prioritizes the control input signal and generates the final logic signal to turn on the driver stage. The speed of the logic gates in this block, together with the width of the reset pulse  $T_{OFFMIN}$ , are designed to meet a maximum duty cycle  $D_{MAX}$  of 95% at the GATE output under 65kHz of operation.

In case of high input currents which results in Peak Current Limitation, the GATE will be turned off

immediately and maintained in off state for the current PWM cycle. The signal  $T_{OFFMIN}$  resets (highest priority, overriding other input signals) both the current limit latch and the PWM on latch as illustrated in Figure 11.



**Figure 11 PWM LOGIC**

**3.8 System Protection**

The IC provides numerous protection features in order to ensure the PFC system in safe operation.

**3.8.1 Input Voltage Brownout Protection(BOP)**

Brownout occurs when the input voltage  $V_{IN}$  falls below the minimum input voltage of the design (i.e. 85V for universal input voltage range) and the  $V_{CC}$  has not entered into the  $V_{CCUVLO}$  level yet. For a system without BOP, the boost converter will increasingly draw a higher current from the mains at a given output power which may exceed the maximum design values of the input current.

ICE3PCS01G provides a new BOP feature whereby it senses directly the input voltage for Input Brown-Out condition via an external resistor/capacitor/diode network shown in Figure 12. This network provides a filtered value of  $V_{IN}$  which turns the IC on when the voltage at pin 9 (BOP) is more than 1.25V. The IC enters into the fault mode when BOP goes below 1.0V. The hysteresis prevents the system to oscillate between normal and fault mode. Note also that the peak of  $V_{IN}$  needs to be at least 20% of the rated  $V_{OUT}$  in order to overcome OLP and powerup system.

## Functional Description

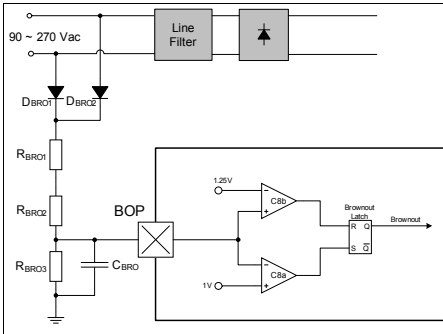


Figure 12 Input Brownout Protection

### 3.8.2 Peak Current Limit (PCL)

The IC provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at pin 2 (ISENSE) reaches  $-0.2\text{V}$ . This voltage is amplified by a factor of 5 and connected to comparator with a reference voltage of  $1.0\text{V}$  as shown in Figure 13. A deglitcher with  $200\text{ns}$  after the comparator improves noise immunity to the activation of this protection.

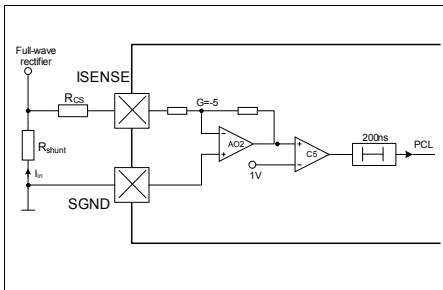


Figure 13 Peak Current Limit (PCL)

### 3.8.3 Open Loop Protection (OLP)

Whenever VSENSE voltage falls below  $0.5\text{V}$ , or equivalently  $V_{\text{OUT}}$  falls below 20% of its rated value, it indicates an open loop condition (i.e. VSENSE pin not connected) or an insufficient input voltage  $V_{\text{IN}}$  for normal operation. It is implemented using comparator C2a with a threshold of  $0.5\text{V}$  as shown in the IC block diagram in Figure 6.

### 3.8.4 First Over-Voltage Protection (OVP1)

Whenever  $V_{\text{OUT}}$  exceeds the rated value by 8%, the over-voltage protection OVP1 is active as shown in Figure 6. This is implemented by sensing the voltage at

VSENSE pin with respect to a reference voltage of  $2.7\text{V}$ . A VSENSE voltage higher than  $2.7\text{V}$  will immediately turn off the gate, thereby preventing damage to bus capacitor. After bulk voltage falls below the rated value, gate drive resumes switching again.

### 3.8.5 Second Over Voltage Protection (OVP2)

The second OVP is provided in case that the first one fails due to the aging or incorrect resistors connected to the VSENSE pin. This is implemented by sensing the voltage at pin OVP with respect to a reference voltage of  $2.5\text{V}$ . When voltage at OVP pin is higher than  $2.5\text{V}$ , the IC will immediately turn off the gate, thereby preventing damage to bus capacitor.

When the bulk voltage drops out of the hysteresis the IC can be latched further or begin auto soft-start. These two protection modes are distinguished through detecting the external equivalent resistance connecting to VBTHL\_EN pin after  $V_{\text{CC}}$  is higher than UVLO threshold as shown in Figure 3. If the equivalent resistance is higher than  $100\text{k}\Omega$  the IC selects latch mode for second OVP, otherwise auto soft-start mode.

In normal operation the trigger level of second OVP should be designed higher than the first. However in the condition of mains transient overshoot the bulk voltage may be pulled up to the peak value of mains that is higher than the threshold of OVP1 and OVP2. In this case the OVP1 and OVP2 are triggered in the same time the IC will shut down the gate drive until bulk voltage falls out of the two protection hysteresis, then resume the gate drive again.

### 3.8.6 Bulk Voltage Monitor and Enable Function

The IC monitors the bulk voltage through VSENSE pin and output a TTL signal to enable PWM IC or control inrush relay. During soft-start, once the bulk voltage is higher than 95% rated value, pin VB\_OK outputs a high level. The threshold to trigger the low level is decided by the pin VBTHL\_EN voltage which can be adjustable externally.

When pin VBTHL\_EN is pulled down externally lower than  $0.5\text{V}$ , IC will enter into standby mode and most of the function blocks are turned off. When the disable signal is released the IC recovers by soft-start.

### 3.8.7 Boost Follower

The IC provides adjustable lower bulk voltage in case of low line input and light output power. The low line condition is determined when pin BOP voltage is less than  $2.3\text{V}$ . Pin BOFO is connected to PWM feedback voltage through a voltage divider, representing the output power. The light load condition is determined when pin BOFO voltage is less than  $0.5\text{V}$ . Once these two conditions are met in the same time, a  $20\mu\text{A}$  current source is flowing out of pin VSENSE so that the bulk voltage should be reduced to a lower level in order

Functional Description

to keep the VSENSE voltage same as the internal reference 2.5V as shown in Figure 14.

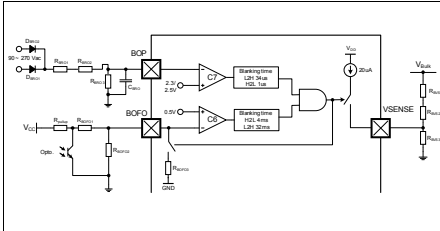


Figure 14 Boost Follower

The reduced bulk voltage can be designed by upper side resistance of voltage divider from pin VSENSE. Thus the low side resistance is designed by the voltage divider ratio from the reference 2.5V to the rated bulk voltage. A internal 300kΩ resistor will be paralleled with external low side resistor of BOFO pin to provide the adjustable hysteresis for PWM feedback voltage when boost follower is activated.

The boost follower feature will be disabled internally during PFC soft-start in order to prevent bulk voltage oscillation due to the unstable PWM feedback voltage. This feature can also be disabled externally by pulling up pin BOFO higher than 0.5V continuously.

### 3.9 Output Gate Driver

The output gate driver is a fast totem pole gate drive. It has an in-built cross conduction currents protection and a Zener diode Z1 (see Figure 15) to protect the external transistor switch against undesirable over voltages. The maximum voltage at pin 13 (GATE) is typically clamped at 15V.

The output is active HIGH and at VCC voltages below the under voltage lockout threshold  $V_{CCUVLO}$ , the gate drive is internally pull low to maintain the off state.

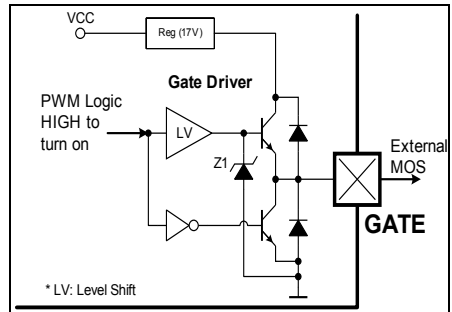


Figure 15 Gate Driver

**Functional Description**
**3.10 Protection Function**

Description of Fault	Fault-Type	Min. Duration of Effect	Consequence
Voltage at Pin ISENSE < -200mV	PCL	200 ns	Gate Driver is turned off immediately during current switching cycle
Voltage at Pin BOP < 1V	BOP	20 $\mu$ s	Gate Driver is turned off. Soft-restart after BOP voltage > 1.25V
Voltage at Pin VSENSE < 0.5V	OLP	1 $\mu$ s	Power down. Soft-restart after VSENSE voltage > 0.5V
Voltage at Pin VSENSE < 0.8V when boost follower is active	OLP	1 $\mu$ s	Disable boost follower function.
Voltage at Pin VSENSE > 108% of rated level	OVP1	12 $\mu$ s	Gate Driver is turned off until VSENSE voltage < 2.5V.
Voltage at Pin OVP > 2.5V and Voltage at Pin VSENSE > 108% of rated level	OVP1 and OVP2	12 $\mu$ s	Gate Driver is turned off until bulk voltage drops out of both OVP hysteresis
Voltage at Pin OVP > 2.5V	OVP2 (latch mode)	12 $\mu$ s	Latched fault mode. Soft-restart after $V_{CC}$ UVLO
Voltage at Pin OVP > 2.5V	OVP2 (auto-restart mode)	12 $\mu$ s	Gate Driver is turned off. Soft-restart after OVP voltage < 2.3V
Voltage at Pin VBTHL_EN < 0.5V after $V_{CC}$ > 7V	OVP2 mode detection	18 $\mu$ s	IC enters soft-restart mode after OVP2 released.
Voltage at Pin VBTHL_EN > 0.5V after $V_{CC}$ > 7V	OVP2 mode detection	18 $\mu$ s	IC enters latch mode after OVP2 released.
Voltage at Pin VBTHL_EN < 0.5V when Vref outputs 5V	Disable function	9 $\mu$ s	Power down. Soft-restart after disable signal is released.

## 4 Electrical Characteristics

All voltages are measured with respect to ground (pin 3). The voltage levels are valid if other ratings are not violated.

### 4.1 Absolute Maximum Ratings

Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 12 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Supply Voltage	$V_{VCC}$	-0.3		26	V	
GATE Voltage	$V_{GATE}$	-0.3		17	V	Clamped at 15V if driven internally.
ISENSE Voltage	$V_{ISENSE}$	-20		5.3	V	<sup>1)</sup>
ISENSE Current	$I_{ISENSE}$	-1		1	mA	
VSENSE Voltage	$V_{VSENSE}$	-0.3		5.3	V	
VSENSE Current	$I_{VSENSE}$	-1		1	mA	
ICOMP Voltage	$V_{ICOMP}$	-0.3		5.3	V	
FREQ Voltage	$V_{FREQ}$	-0.3		5.3	V	
VREF Voltage	$V_{VREF}$	-0.3		$V_{VREF\_0A}$	V	
BOP Voltage	$V_{BOP}$	-0.3		9.5	V	<sup>2)</sup>
BOP Current	$I_{BOP}$	-1		35	$\mu$ A	
VB_OK Voltage	$V_{VB\_OK}$	-0.3		5.3	V	
VBTHL/EN Voltage	$V_{VBTHL}$	-0.3		5.3	V	
BOFO Voltage	$V_{BOFO}$	-0.3		5.3	V	
OVP Voltage	$V_{OVP}$	-0.3		5.3	V	
Junction Temperature	$T_J$	-40		150	$^{\circ}$ C	
Storage Temperature	$T_{A\_STO}$	-55		150	$^{\circ}$ C	
Thermal Resistance	$R_{THJA}$			140	K/W	Junction to Air
Soldering Temperature	$T_{SLD}$			260	$^{\circ}$ C	Wave Soldering <sup>3)</sup>
ESD Capability	$V_{ESD}$			2	kV	Human Body Model <sup>4)</sup>

<sup>1)</sup> Absolute ISENSE current should not be exceeded

<sup>2)</sup> Absolute BOP current should not be exceeded

<sup>3)</sup> According to JESD22A111

<sup>4)</sup> According to EIA/JESD22-A114-B (discharging an 100 pF capacitor through an 1.5k $\Omega$  series resistor)

**Electrical Characteristics**
**4.2 Operating Range**

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Supply Voltage @ 25°C	$V_{VCC}$	$V_{VCC,OFF}$		25	V	$T_J=25^\circ\text{C}$
Junction Temperature	$T_J$	-25		125	°C	
PFC switching frequency	$F_{PFC}$	21		100	kHz	

**4.3 Characteristics**

Note: The electrical Characteristics involve the spread of values given within the specified supply voltage and junction temperature range  $T_J$  from  $-25^\circ\text{C}$  to  $125^\circ\text{C}$ . Typical values represent the median values, which are related to  $25^\circ\text{C}$ . If not otherwise stated, a supply voltage of  $V_{VCC} = 18\text{V}$ , a typical switching frequency of  $f_{req} = 65\text{kHz}$  are assumed and the IC operates in active mode. Furthermore, all voltages are referring to GND if not otherwise mentioned.

**4.3.1 Supply Section**

Parameter	Symbol	Limit Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
VCC Turn-On Threshold	$V_{CCon}$	11.5	12	12.9	V	
VCC Turn-Off Threshold/ Under Voltage Lock Out	$V_{CCUVLO}$	10.5	11.0	11.9	V	
VCC Turn-On/Off Hysteresis	$V_{CCHy}$	0.7	1	1.45	V	
Start Up Current Before $V_{CCon}$	$I_{CCstart1}$	-	380	700	μA	$V_{CCon}-1.2\text{V}$
Start Up Current Before $V_{CCon}$	$I_{CCstart2}$	-	1.4	2.4	mA	$V_{CCon}-0.2\text{V}$
Operating Current with active GATE	$I_{CCHG}$	-	6.7	9	mA	$C_L = 1\text{nF}$
Operating Current during Standby	$I_{CCStandy}$	-	3.5	4.7	mA	$V_{VSENSE} = 0.4\text{V}$ $V_{ICOMP} = 4\text{V}$



**Electrical Characteristics**
**4.3.2 Variable Frequency Section**

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Switching Frequency (Typical)	$F_{SWnom}$	62.5	65	67.5	kHz	$R5 = 67k\Omega$
Switching Frequency (Min.)	$F_{SWmin}$	-	21	-	kHz	$R5 = 212k\Omega$
Switching Frequency (Max.)	$F_{SWmax}$	-	100	-	kHz	$R5 = 43k\Omega$
Voltage at FREQ pin	$V_{FREQ}$	-	1	-	V	
Max. Duty Cycle	$D_{max}$	93	95	98.5	%	$f_{SW} = f_{SWnom}$ ( $R_{FREQ} = 67k\Omega$ )

**4.3.3 PWM Section**

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Min. Duty Cycle	$D_{MIN}$			0	%	$V_{VSENSE} = 2.5V$ $V_{ICOMP} = 4.3V$
Min. Off Time	$T_{OFFMIN}$	310	600	920	ns	$V_{VSENSE} = 2.5V$ $V_{ISENSE} = 0V$ ( $R5 = 67k\Omega$ )

**4.3.4 External Synchronization**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Detection threshold of external clock	$V_{thr\_EXT}$		2.5		V	
Synchronization range	$f_{EXT\_range}$	50		100	kHz	
Synchronization frequency ratio	$f_{EXT} : f_{PFC}$		1:1			
propagation delay from rising edge of external clock to falling edge of PFC gate drive	$T_{EXT2GATE}$			500	ns	$f_{EXT} = 65kHz$
Allowable external duty on time	$T_{D\_on}$	10		70	%	

**Electrical Characteristics**
**4.3.5 PFC Brownout Protection Section**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Brownout Protection High to Low Threshold	$V_{BOP\_H2L}$	0.98	1	1.02	V	
Input Brownout Protection Low to High Threshold	$V_{BOP\_L2H}$	1.2	1.25	1.3	V	
Blanking time for BOP turn_on	$T_{BOPon}$		20		$\mu$ s	
Input Brownout Protection BOP Bias Current	$I_{BOP}$	-0.5	-	0.5	$\mu$ A	$V_{BOP}=1.25V$

**4.3.6 System Protection Section**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Over Voltage Protection (OVP1) Low to High	$V_{OVP1\_L2H}$	2.65	2.7	2.77	V	108% $V_{BULKRated}$
Over Voltage Protection (OVP1) High to Low	$V_{OVP1\_H2L}$	2.45	2.5	2.55	V	
Over Voltage Protection (OVP1) Hysteresis	$V_{OVP1\_HYS}$	150	200	270	mV	
Blanking time for OVP1	$T_{OVP1}$		12		$\mu$ s	
Over Voltage Protection (OVP2) Low to High	$V_{OVP2\_L2H}$	2.45	2.5	2.55	V	
Over Voltage Protection (OVP2) High to Low	$I_{OVP2\_H2L}$	2.25	2.3	2.35	V	
Blanking time for OVP2	$T_{OVP2}$		12		$\mu$ s	
OVP2 mode detection threshold	$V_{OVP2\_mode}$		0.5		V	comparator at VBTHL pin
Current source for OVP2 mode detection <sup>1)</sup>	$I_{OVP2\_mode}$	4	5	6	$\mu$ A	current source at VBTHL pin
Peak Current Limitation (PCL) ISENSE Threshold	$V_{PCL}$	-180	-200	-220	mV	
Blanking time for PCL turn_on	$T_{PCLon}$		200		ns	

<sup>1)</sup> The parameter is not subject to production test - verified by design/characterization

**4.3.7 Internal Voltage Reference**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output Reference Voltage	$V_{VREF\_0A}$	4.9	5	5.1	V	$I_{VREF}=0mA$
Load Regulation	$\Delta V_{VREF\_5mA}$			50	mV	$I_{VREF}=-5mA$ <sup>1)</sup>
Line Regulation	$\Delta V_{VREF\_VCC}$			25	mV	$\Delta V_{CC}=3V$

**Electrical Characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum Source Current	$I_{VREF}$	-6			mA	
Temperature Stability	$\Delta V_{VREF\_temp}$		1.0		%	
Total Variation	$V_{VREF\_total}$	4.85		5.2		Line, Load, Temperature

<sup>1)</sup> Maximum pulling current depends on the maximum operating junction temperature

**4.3.8 Boost Follower Section**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
BOFO threshold	$V_{BOFO}$	0.47	0.5	0.53	V	
BOFO hysteresis resistor	$R_{BOFO\_hys}$	240	300	360	k $\Omega$	
Blanking time for BOFO on	$T_{BOFO\_L2H}$		32		ms	
Blanking time for BOFO off	$T_{BOFO\_H2L}$		4		ms	
High line detection threshold	$V_{LD\_H}$	2.46	2.5	2.56	V	
Low line detection threshold	$V_{LD\_L}$	2.25	2.3	2.35	V	
Blanking time for line detection	$T_{LD}$		32		$\mu$ s	
Current source for low step	$I_{BOFO}$	18.7	20	21	$\mu$ A	

**4.3.9 Bulk Voltage Good Section**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VB_OK turn-on threshold	$V_{VBOKon}$	2.25	2.375	2.5	V	sensed at pin VSENSE
VB_OK turn-off threshold	$V_{VBOKoff}$		$V_{VBTHL\_EN}$		V	set by pin VBTHL_EN
Disable function threshold	$V_{VBTHL\_EN}$	0.45	0.5	0.55	V	
Blanking time for disable function	$T_{VBTHL\_EN}$		9		$\mu$ s	
VB_OK max source current	$I_{VB\_OKMax}$	-1 <sup>1)</sup>			mA	

<sup>1)</sup> shared with the max source current of the VREF pin.

**Electrical Characteristics**
**4.3.10 Current Loop Section**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
OTA6 Transconductance Gain	$G_{M_{OTA6}}$	3.5	5.0	6.35	mS	At Temp = 25°C
OTA6 Output Linear Range <sup>1)</sup>	$I_{OTA6}$		± 50		μA	
ICOMP Voltage during OLP	$V_{ICOMP}$	4.8	5.0	5.2	V	$V_{VSENSE} = 0.4V$

<sup>1)</sup> The parameter is not subject to production test - verified by design/characterization

**4.3.11 Voltage Loop Section**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Trimmed Reference Voltage	$V_{VSREF}$	2.47	2.5	2.53	V	±1.2%
Open Loop Protection (OLP) VSENSE Threshold	$V_{VS\_OLP}$	0.45	0.5	0.55	V	
VSENSE Input Bias Current	$I_{VSENSE}$	-1	-	1	μA	$V_{VSENSE} = 2.5V$

**4.3.12 Driver Section**

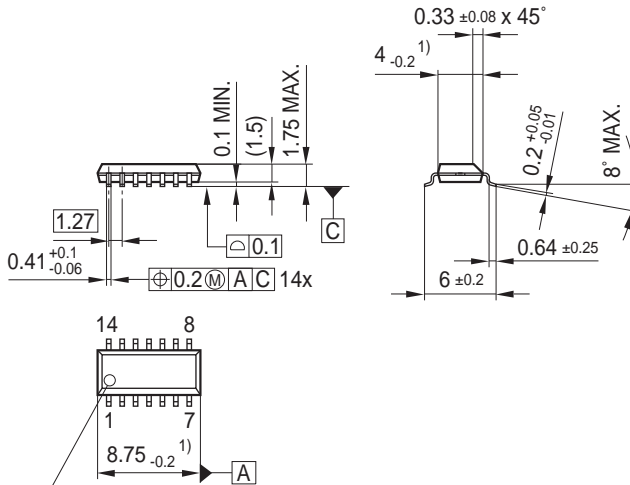
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GATE Low Voltage	$V_{GATEL}$	-	-	1.2	V	$V_{CC} = 10V$ $I_{GATE} = 5\text{ mA}$
		-	0.4	-	V	$I_{GATE} = 0\text{ A}$
		-	-	1.4	V	$I_{GATE} = 20\text{ mA}$
		-0.2	0.8	-	V	$I_{GATE} = -20\text{ mA}$
GATE High Voltage	$V_{GATEH}$	-	15	-	V	$V_{CC} = 25V$ $C_L = 1\text{ nF}$
		-	12.4	-	V	$V_{CC} = 15V$ $C_L = 1\text{ nF}$
		8.0	-	-	V	$V_{CC} = V_{VCCoff} + 0.2V$ $C_L = 1\text{ nF}$

**4.3.13 Gate Drive Section**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GATE Rise Time	$t_r$	-	30	-	ns	$V_{Gate} = 20\% - 80\%$ $V_{GATEH} C_L = 1\text{ nF}$
GATE Fall Time	$t_f$	-	25	-	ns	$V_{Gate} = 80\% - 20\%$ $V_{GATEH} C_L = 1\text{ nF}$

## 5 Outline Dimension

### PG-DSO-14 Outline Dimension



Index Marking

<sup>1)</sup> Does not include plastic or metal protrusion of 0.15 max. per side

### Notes:

1. You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.
2. Dimensions in mm.

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**CCM-PFC****Revision History:**

Datasheet

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Page 4/8/16/ 17	Maximum switching frequency was changed to 100kHz
Figure 4	Maximum switching frequency was changed to 100kHz
Page 17	Maximum synchronization frequency was changed to 100kHz

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