STB28N60M2, STI28N60M2, STP28N60M2, STW28N60M2

N-channel 600 V, 0.135 Ω typ., 22 A MDmesh™ M2 Power MOSFETs in D²PAK, I²PAK, TO-220 and TO-247

Datasheet - production data

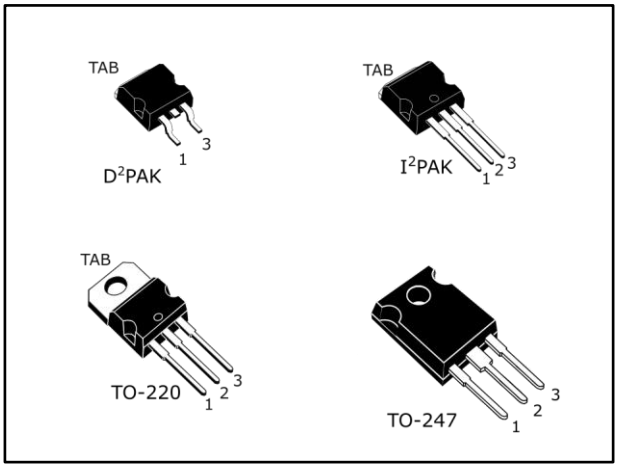
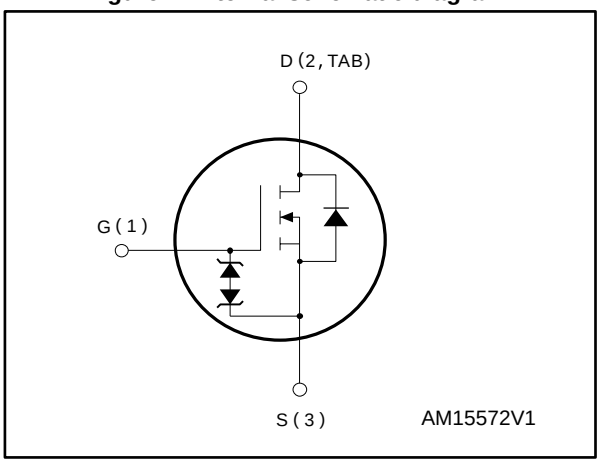


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STB28N60M2	650 V	0.150 Ω	22 A
STI28N60M2			
STP28N60M2			
STW28N60M2			

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LCC converters, resonant converters

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STB28N60M2	28N60M2	D²PAK	Tape and reel
STI28N60M2		I²PAK	Tube
STP28N60M2		TO-220	
STW28N60M2		TO-247	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	22	A
I_D	Drain current (continuous) at T_C = 100 °C	14	A
I_{DM}(1)	Drain current (pulsed)	88	A
P_{TOT}	Total dissipation at T_C = 25 °C	170	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 22 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.

(3)V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value				Unit
		D²PAK	I²PAK	TO-220	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.74				°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max(1)	30				°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max		62.5	62.5	50	°C/W

Notes:

(1)When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	3.6	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	350	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 11 A		0.135	0.150	Ω

Notes:

(1) Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	1440	-	pF
C_{oss}	Output capacitance		-	70	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	104	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.5	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 22 A, V_{GS} = 0 to 10 V (see *Figure 17: "Test circuit for gate charge behavior"*)	-	36	-	nC
Q_{gs}	Gate-source charge		-	7.2	-	nC
Q_{gd}	Gate-drain charge		-	16	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80 % V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 11 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16: "Test circuit for resistive load switching times"* and *Figure 21: "Switching time waveform"*)	-	14.5	-	ns
t_r	Rise time		-	7.2	-	ns
$t_{d(off)}$	Turn-off-delay time		-	100	-	ns
t_f	Fall time		-	8	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		22	A
I_{SDM} (1)	Source-drain current (pulsed)		-		88	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 22 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 22 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 21: "Switching time waveform"*)	-	350		ns
Q_{rr}	Reverse recovery charge		-	4.7		µC
I_{RRM}	Reverse recovery current		-	27		A
t_{rr}	Reverse recovery time	I_{SD} = 22 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 21: "Switching time waveform"*)	-	451		ns
Q_{rr}	Reverse recovery charge		-	6.5		µC
I_{RRM}	Reverse recovery current		-	29		A

Notes:

(1)Pulse width is limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for D²PAK, TO-220 and I²PAK

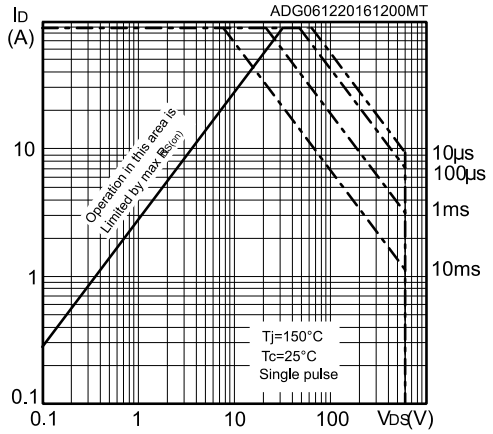


Figure 3: Thermal impedance for D²PAK, TO-220 and I²PAK

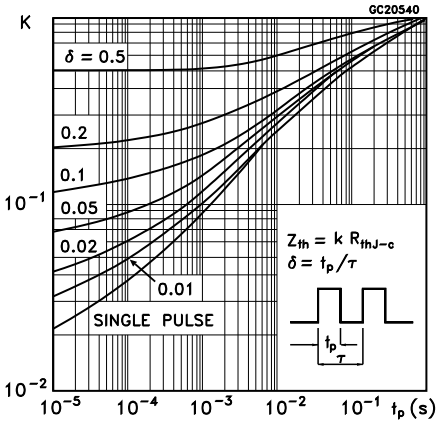


Figure 4: Safe operating area for TO-247

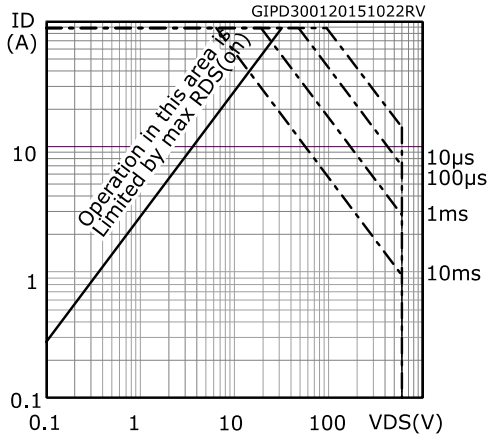


Figure 5: Thermal impedance for TO-247

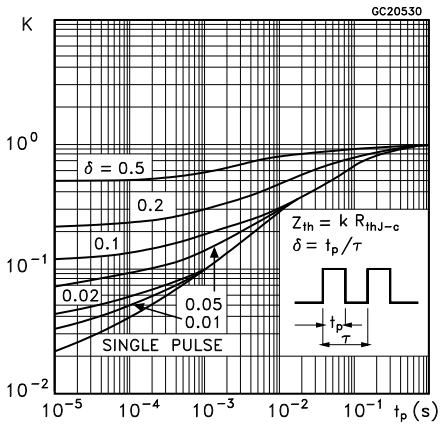


Figure 6: Output characteristics

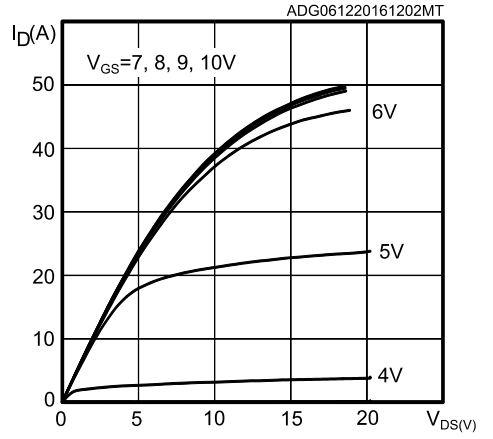


Figure 7: Transfer characteristics

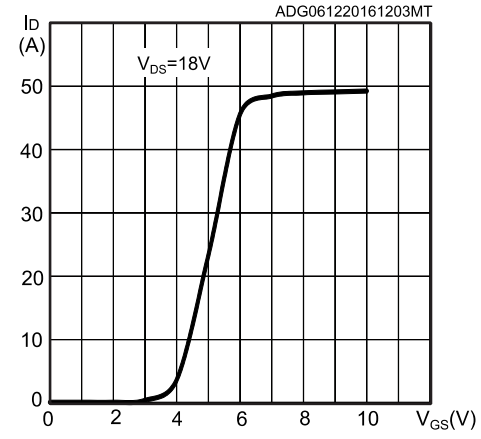


Figure 8: Gate charge vs gate-source voltage

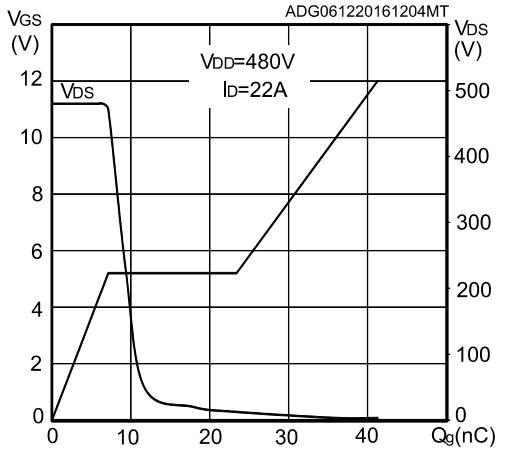


Figure 9: Static drain-source on-resistance

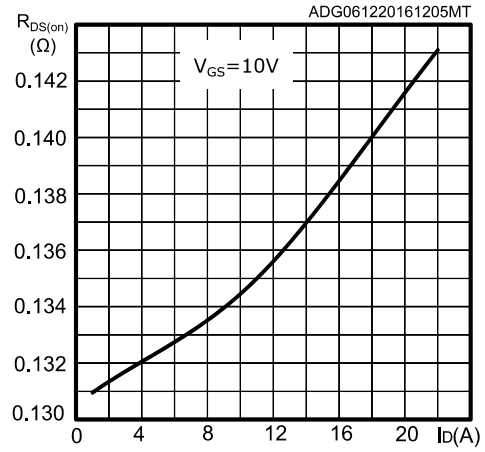


Figure 10: Capacitance variations

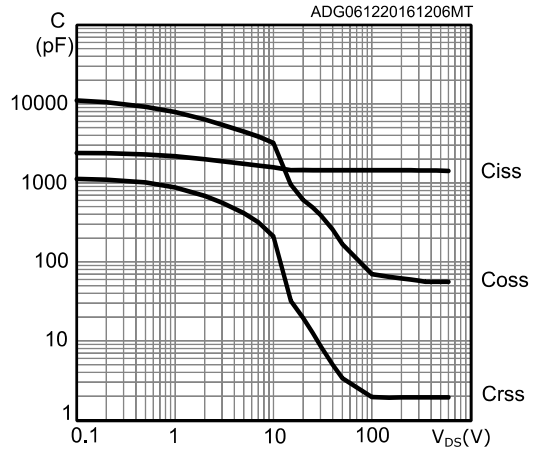


Figure 11: Output capacitance stored energy

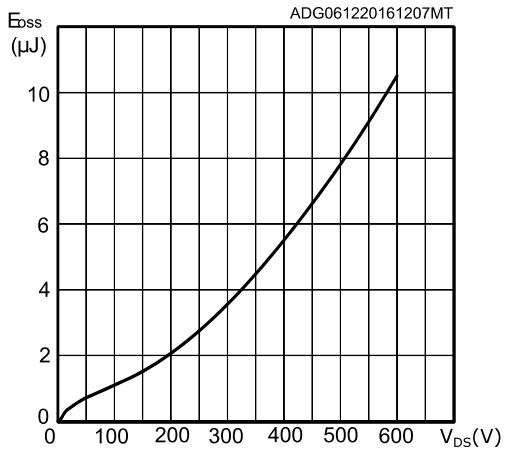


Figure 12: Normalized gate threshold voltage vs temperature

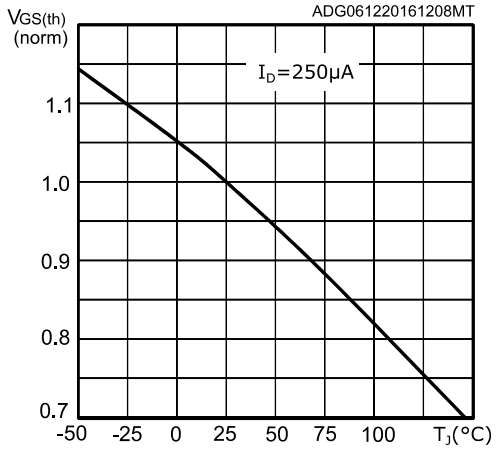


Figure 13: Normalized on-resistance vs temperature

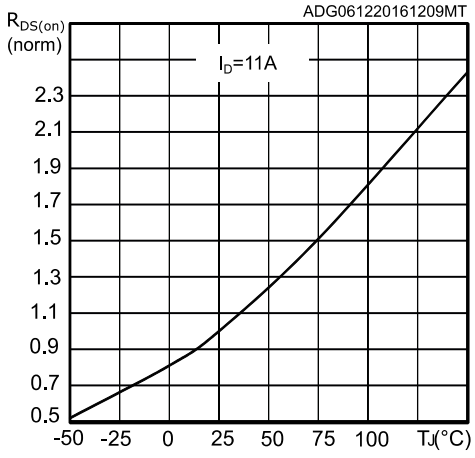


Figure 14: Normalized VDS vs temperature

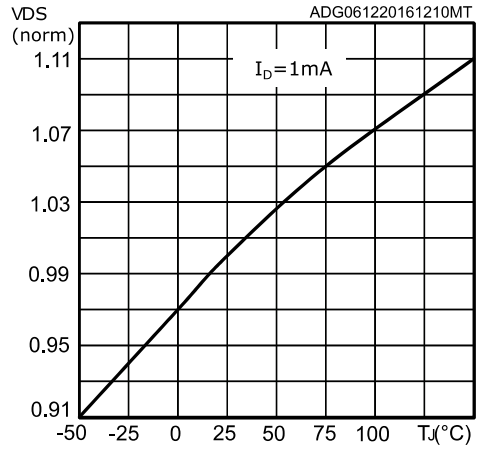
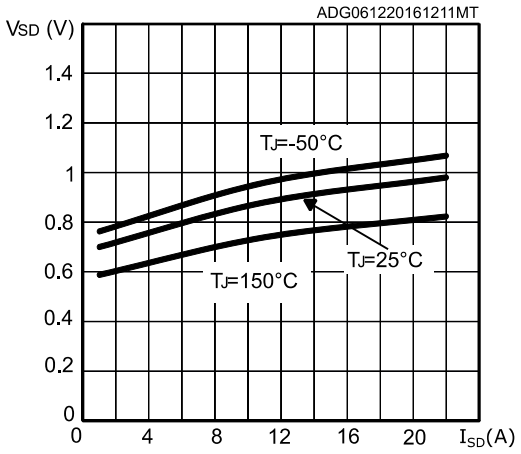


Figure 15: Source-drain diode forward characteristics



3 Test circuits

Figure 16: Test circuit for resistive load switching times

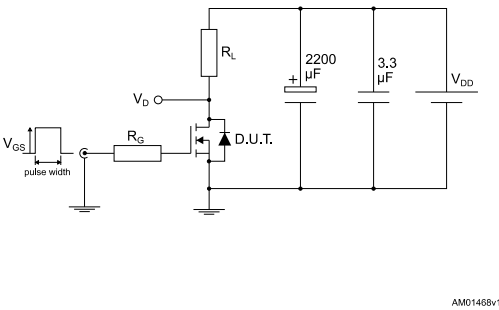


Figure 17: Test circuit for gate charge behavior

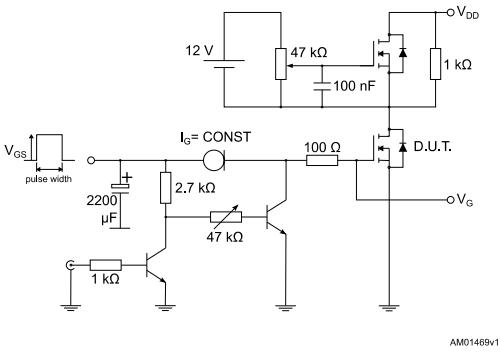


Figure 18: Test circuit for inductive load switching and diode recovery times

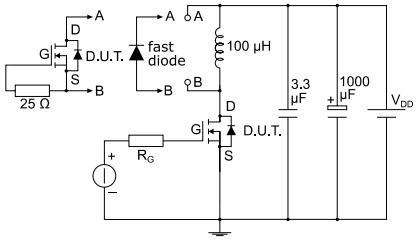


Figure 19: Unclamped inductive load test circuit

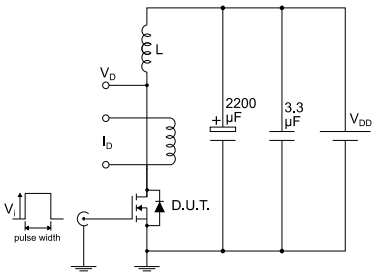


Figure 20: Unclamped inductive waveform

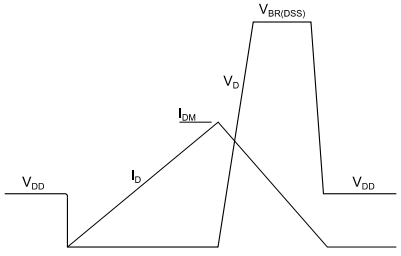
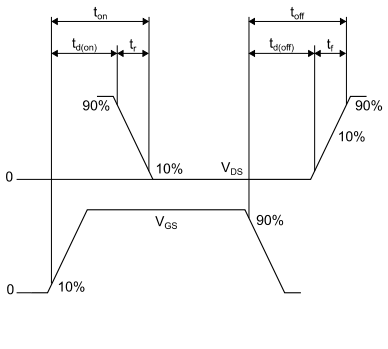


Figure 21: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 D²PAK package information

Figure 22: D²PAK (TO-263) type A package outline

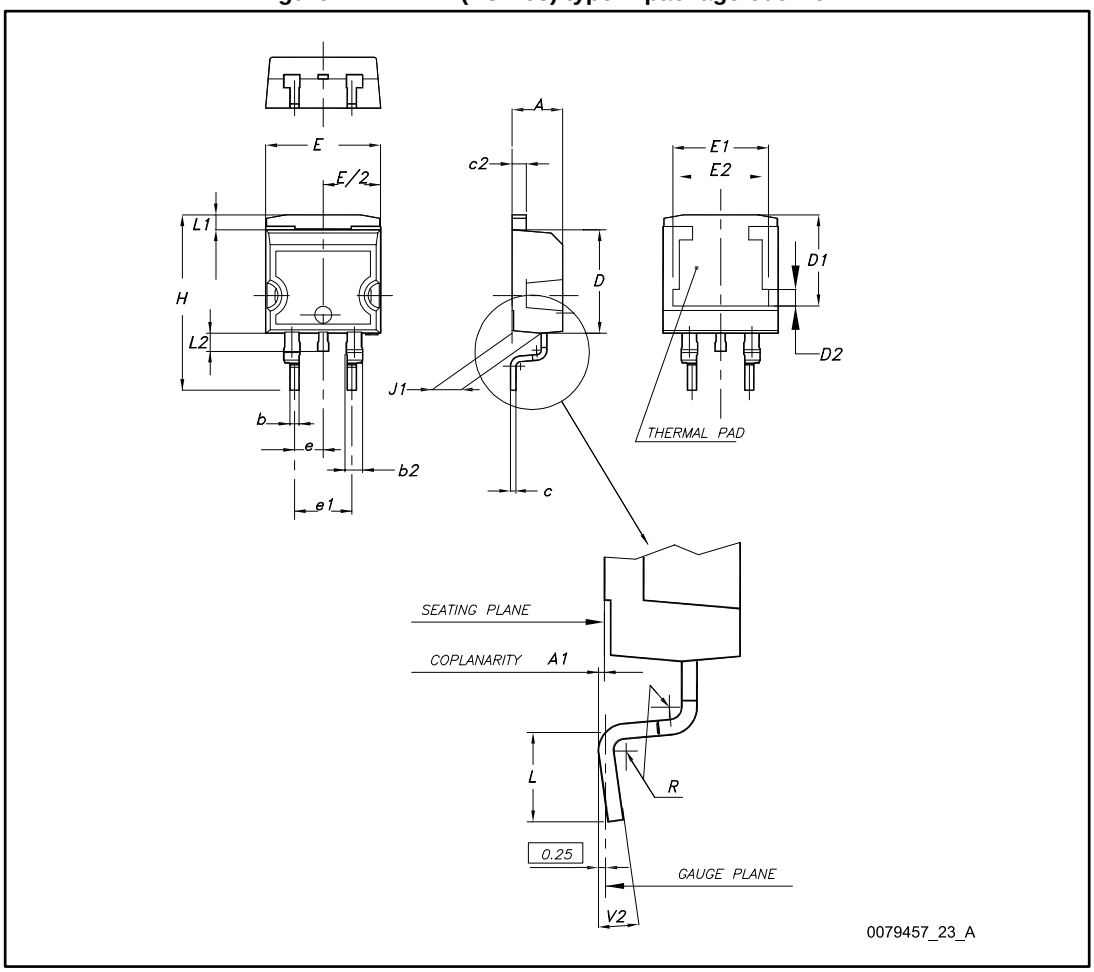
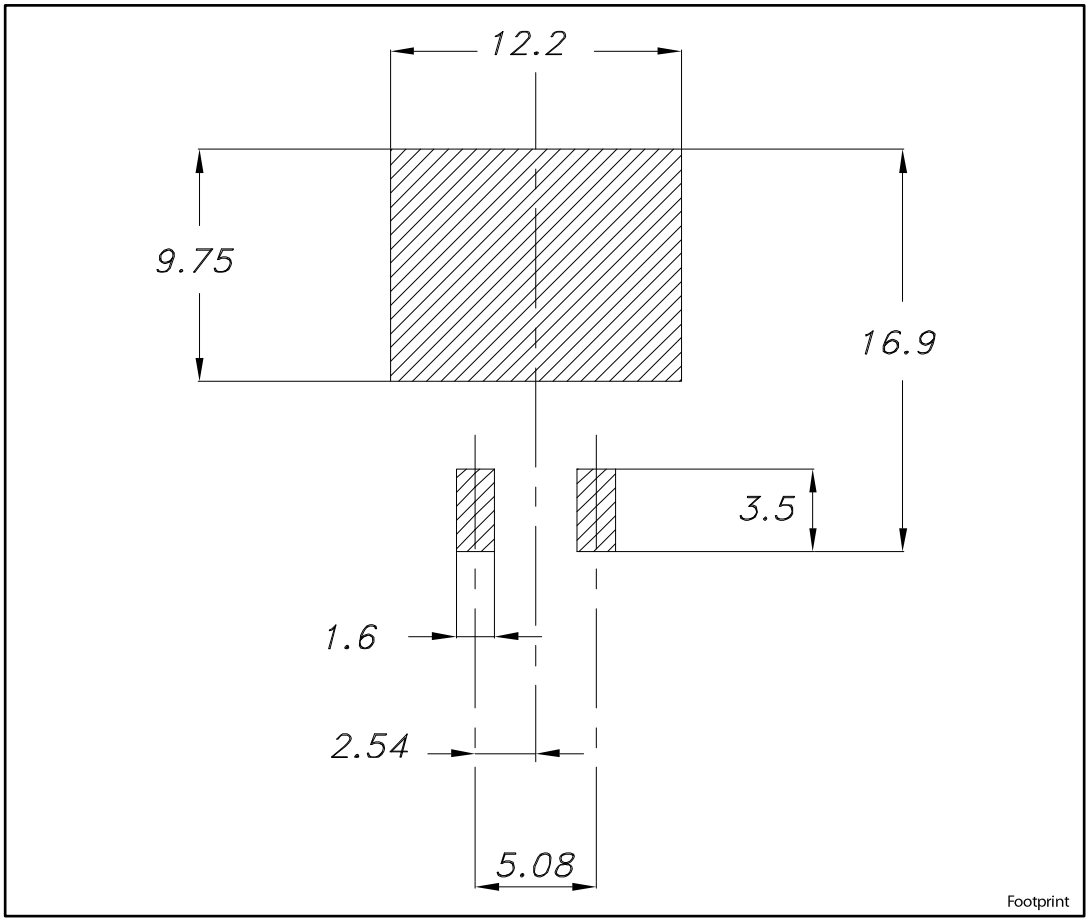


Table 9: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 23: D²PAK (TO-263) type A recommended footprint (dimensions are in mm)



4.2 D²PAK packing information

Figure 24: D2PAK type A tape outline

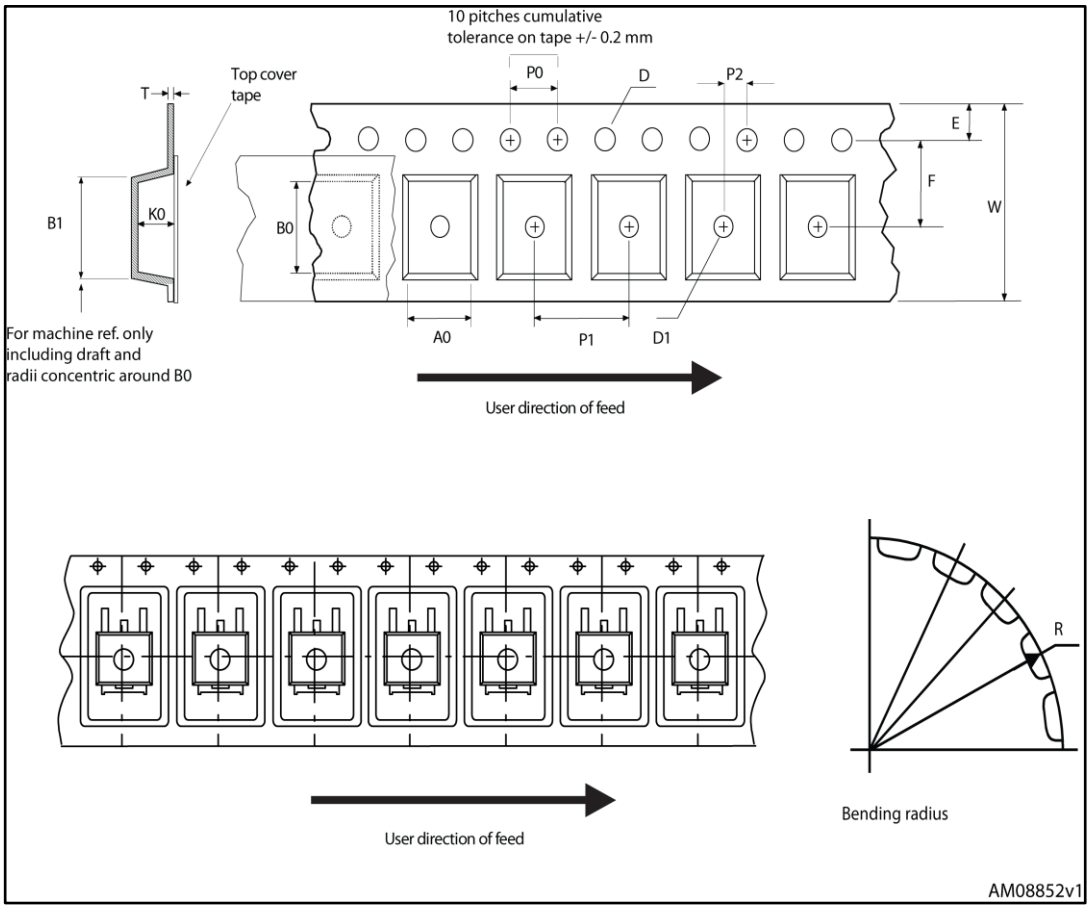


Figure 25: D2PAK type A reel outline

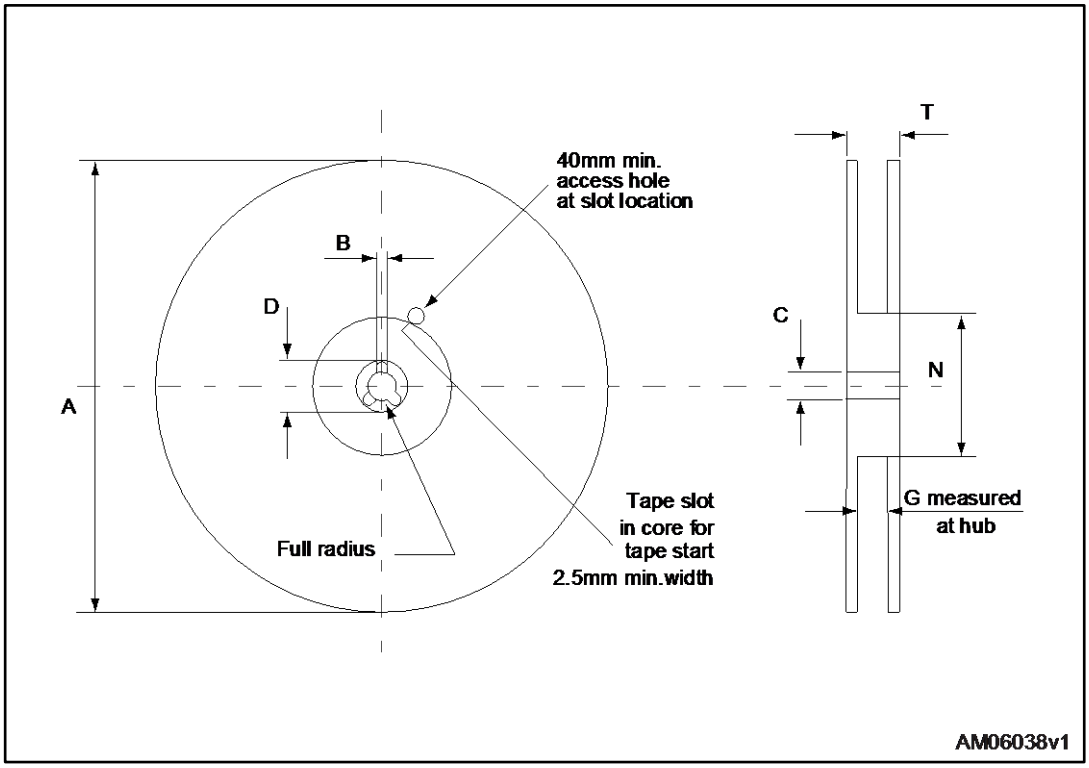


Table 10: D²PAK type A tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

4.3 I²PAK package information

Figure 26: I²PAK package outline

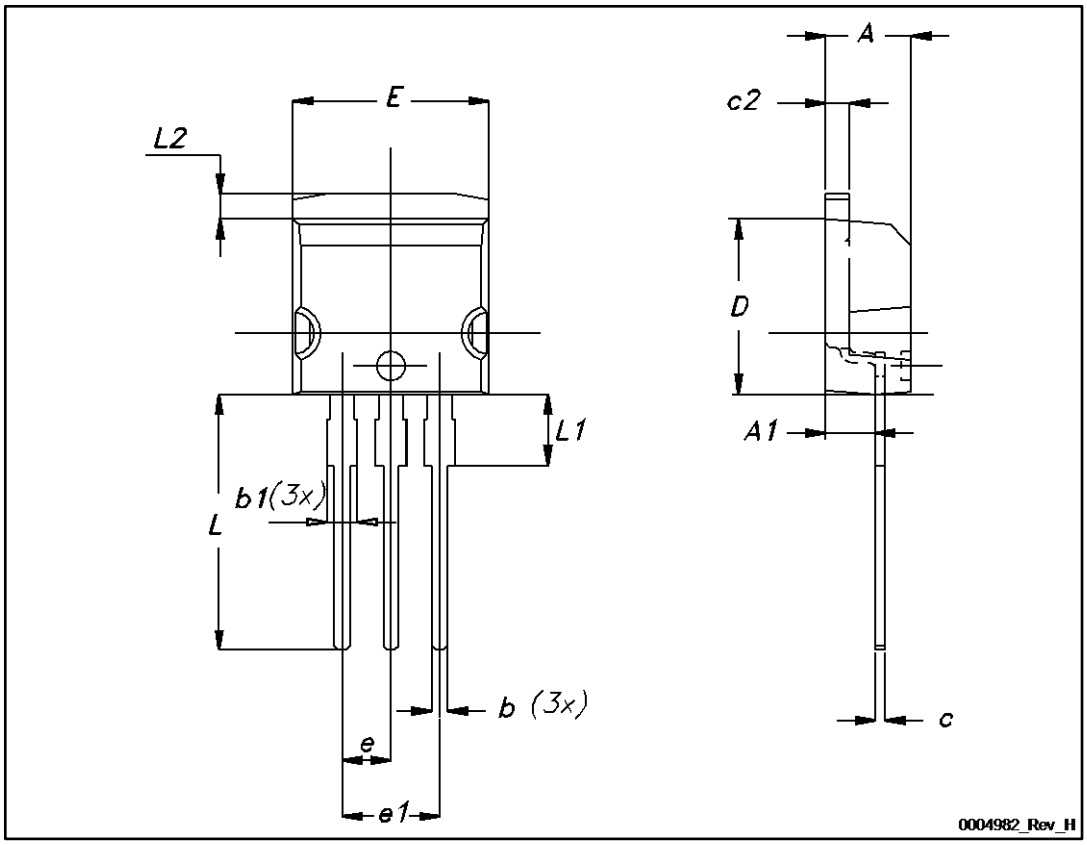


Table 11: I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

4.4 TO-220 type A package information

Figure 27: TO-220 type A package outline

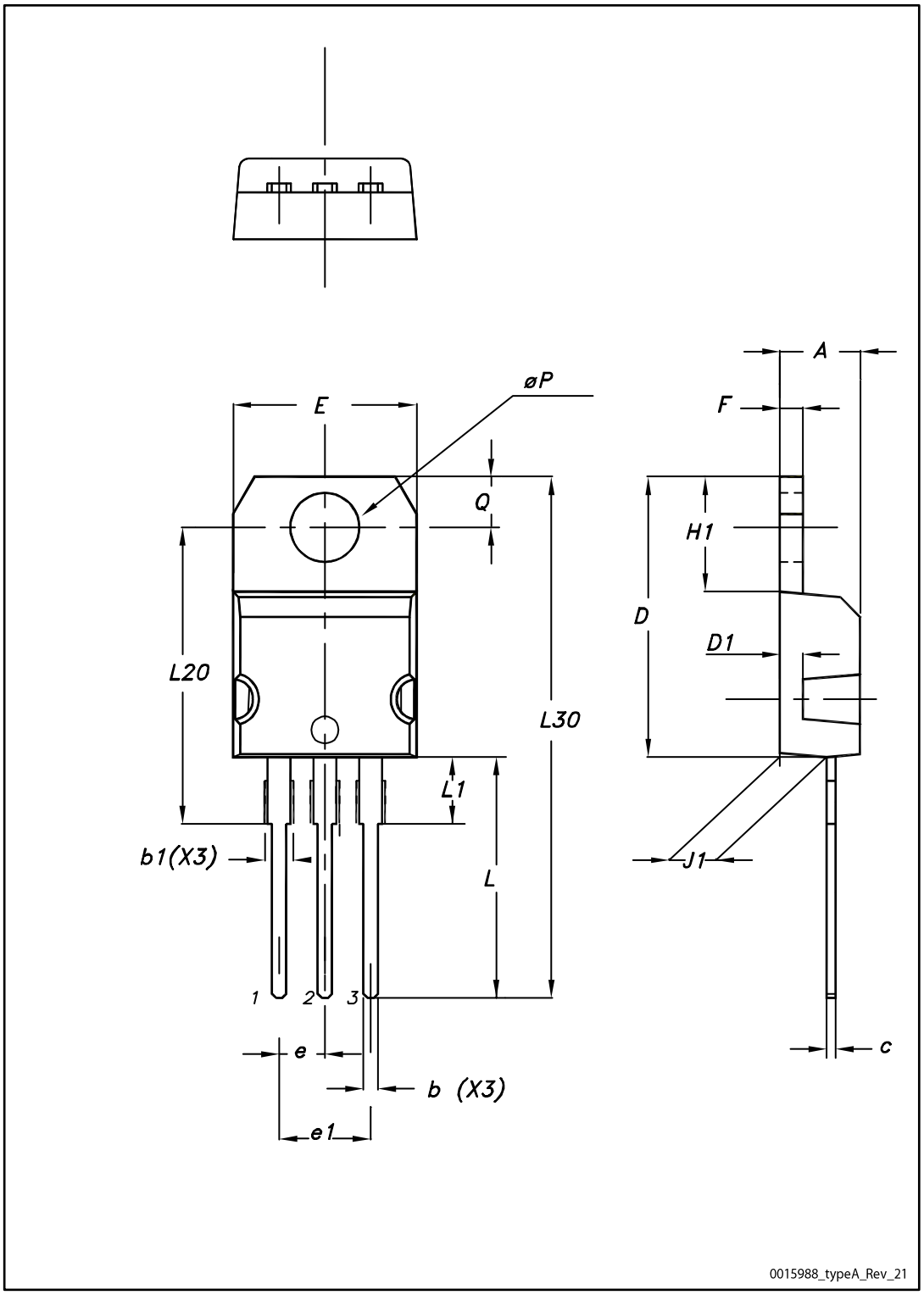


Table 12: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.5 TO-247 package information

Figure 28: TO-247 package outline

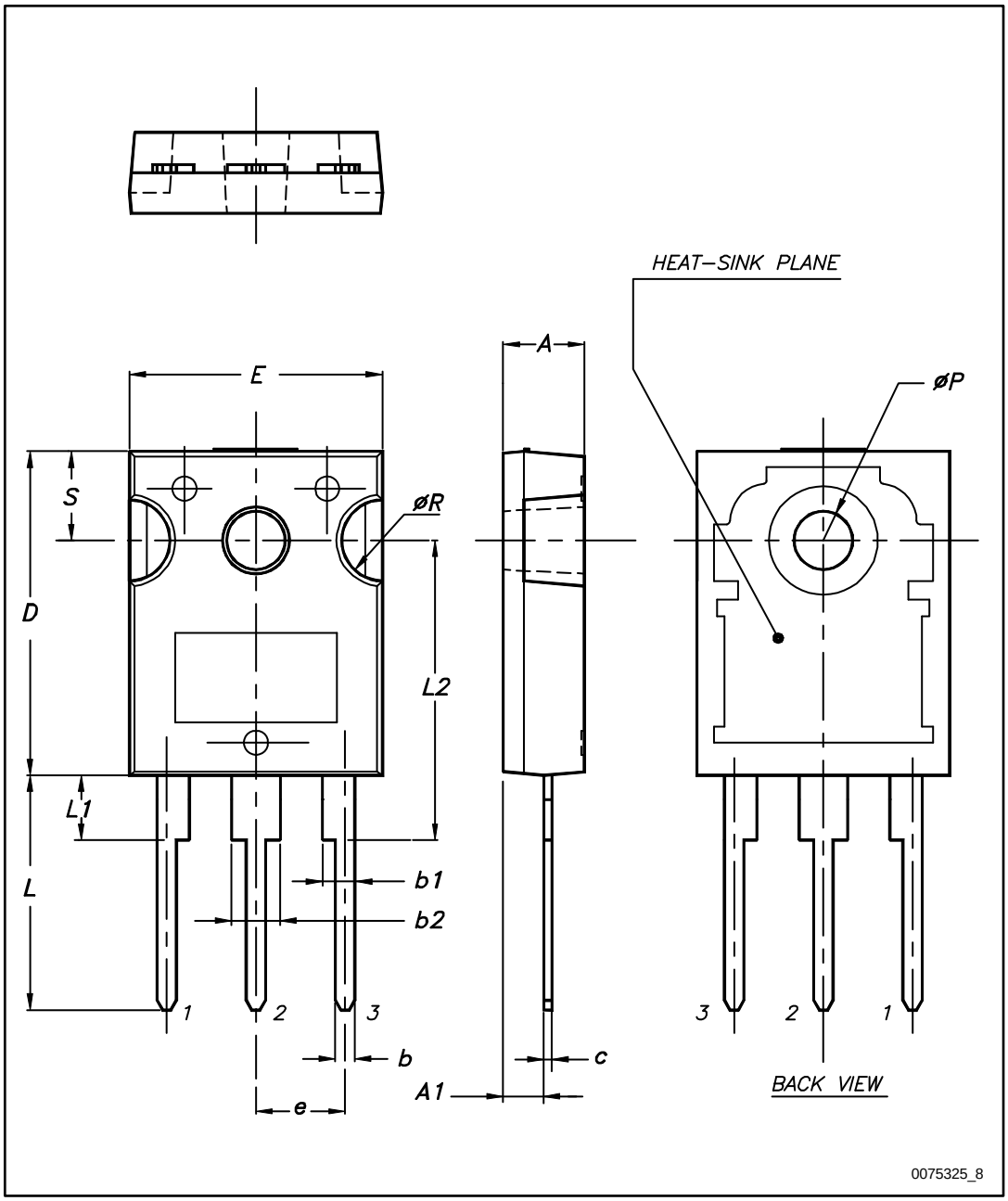


Table 13: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 14: Document revision history

Date	Revision	Changes
13-Sep-2013	1	First release.
29-Jan-2014	2	– Modified: title, ID value and features in cover page – Modified: ID, IDM and PTOT values in Table 2 – Modified: note 2 – Modified: Rthj-case value in Table 3 – Modified: the entire typical values in Table 4, 6, 7 and 8 – Modified: RDS(on) typical value in Table 5 – Modified: Figure 9 and 10 – Added: Section 4: Package information – Minor text changes
09-Feb-2015	3	– Updated title and description – Updated Table 2.: Absolute maximum ratings and Table 4.: Avalanche characteristics – Updated Figure 5.: Thermal impedance for TO-247 and Figure 6.: Output characteristics – Updated 4: Package information – Minor text changes.
14-Mar-2017	4	Added part number STI28N60M2. Updated title, silhouette, features and *Table 1: "Device summary"* in cover page. Updated *Table 3: "Thermal data"* and *Section 4: "Package information"*. Minor text changes.

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