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FAIRCHILD SEMICONDUCTOR®

November 2012

NC7SV08
TinyLogic® ULP-A 2-Input AND Gate

Features

- 0.9 V to 3.6 V V_{CC} Supply Operation
- 3.6 V Over-Voltage Tolerant I/Os at V_{CC} from 0.9 V to 3.6 V
- Extremely High Speed t_{PD}
  - 1.0 ns: Typical for 2.7 V to 3.6 V V_{CC}
  - 1.2 ns: Typical for 2.3 V to 2.7 V V_{CC}
  - 2.0 ns: Typical for 1.65 V to 1.95 V V_{CC}
  - 3.2 ns: Typical for 1.4 V to 1.6 V V_{CC}
  - 6.0 ns: Typical for 1.1 V to 1.3 V V_{CC}
  - 13.0 ns: Typical for 0.9 V V_{CC}
- Power-Off High-Impedance Inputs and Outputs
- High Static Drive (I_{OH}/I_{OL})
  - ±24 mA at 3.00 V V_{CC}
  - ±18 mA at 2.30 V V_{CC}
  - ±6 mA at 1.65 V V_{CC}
  - ±4 mA at 1.4 V V_{CC}
  - ±2 mA at 1.1 V V_{CC}
  - ±0.1 mA at 0.9 V V_{CC}
- Uses Proprietary Quiet Series™ Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Ultra-Low Dynamic Power

Description

The NC7SV08 is a single two-input AND gate from Fairchild's Ultra-Low Power (ULP-A) Series of TinyLogic®. ULP-A is ideal for applications that require extreme high speed, high drive, and low power. This product is designed for a wide low-voltage operating range (0.9 V to 3.6 V V_{CC}) and applications that require more drive and speed than the TinyLogic® ULP series, but still offer best-in-class, low-power operation.

The NC7SV08 is uniquely designed for optimized power and speed and is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SV08P5X	V08	5-Lead SC70, EIAJ SC-88a, 1.25 mm Wide	3000 Units on Tape & Reel
NC7SV08L6X	G3	6-Lead MicroPak™, 1.00 mm Wide	5000 Units on Tape & Reel
NC7SV08FHX	G3	6-Lead, MicroPak2, 1x1 mm Body, .35 mm Pitch	5000 Units on Tape & Reel

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Battery Life

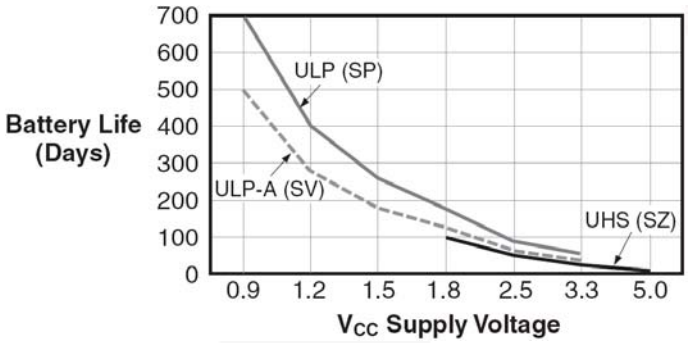

Figure 1. Battery Life vs. V_{CC} Supply Voltage

Notes:

1. TinyLogic® ULP and ULP-A with up to 50% less power consumption can extend battery life significantly.
   Battery Life = $(V_{battery} \bullet I_{battery} \bullet .9)/(P_{device})/24hrs/day$
   where, $P_{device} = (I_{CC} \bullet V_{CC}) + (C_{PD} + C_L) \bullet V_{CC2} \bullet f$.
2. Assumes ideal 3.6 V Lithium Ion battery with current rating of 90 0mAH and derated 90% and device frequency at 10MHz, with C_L = 15 pF load.

Connection Diagram

Figure 2. Logic Symbol

Pin Configurations

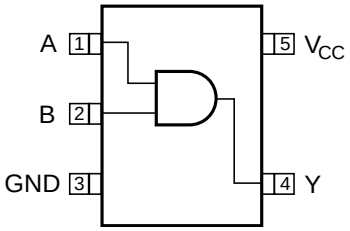

Figure 3. SC70 (Top View)

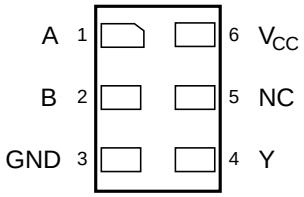

Figure 4. MicroPak (Top Through View)

Pin Definitions

Pin # SC70	Pin # MicroPak	Name	Description
1	1	A	Input
2	2	B	Input
3	3	GND	Ground
4	4	Y	Output
	5	NC	No Connect
5	6	V_{CC}	Supply Voltage

Function Table

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level

L = LOW Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	4.6	V
V_{IN}	DC Input Voltage		-0.5	4.6	V
V_{OUT}	DC Output Voltage	HIGH or LOW State[3]	-0.5	V_{CC} + 0.5	V
		V_{CC} = 0 V	-0.5	4.6	
I_{IK}	DC Input Diode Current	V_{IN} < 0 V		-50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V		-50	mA
		V_{OUT} > V_{CC}		+50	
I_{OH}/I_{OL}	DC Output Source/Sink Current			±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature, Soldering 10 Seconds			+260	°C
P_D	Power Dissipation at +85°C	SC70-5		150	mW
		MicroPak-6		130	
		MicroPak2-6		120	
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charge Device Model, JEDEC:JESD22-C101			2000	

Note:

3. IO absolute maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		0.9	3.6	V
V_{IN}	Input Voltage		0	3.6	V
V_{OUT}	Output Voltage	V_{CC} = 0 V	0	3.6	V
		HIGH or LOW State	0	V_{CC}	
I_{OH}/I_{OL}	Output Current in I_{OH}/I_{OL}	V_{CC} = 3.0 V to 3.6 V		±24	mA
		V_{CC} = 2.3 V to 3.6 V		±18	
		V_{CC} = 1.65 V to 1.95 V		±6	
		V_{CC} = 1.4 V to 1.6 V		±4	
		V_{CC} = 1.1 V to 1.3 V		±2	
		V_{CC} = 0.9 V		±0.1	
T_A	Operating Temperature, Free Air		-40	+85	°C
$\Delta t/\Delta V$	Minimum Input Edge Rate	V_{IN} = 0.8 V to 2.0, V_{CC} = 3.0 V		10	ns/V
θ_{JA}	Thermal Resistance	SC70-5		425	°C/W
		MicroPak-6		500	
		MicroPak2-6		560	

Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C		T_A=-40 to 85°C		Units
				Min.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	0.90		.65 x V_{CC}		.65 x V_{CC}		V
		1.10 ≤ V_{CC} ≤ 1.30		.65 x V_{CC}		.65 x V_{CC}		
		1.40 ≤ V_{CC} ≤ 1.60		.65 x V_{CC}		.65 x V_{CC}		
		1.65 ≤ V_{CC} ≤ 1.95		.65 x V_{CC}		.65 x V_{CC}		
		2.30 ≤ V_{CC} ≤ 2.70		1.6		1.6		
		2.70 ≤ V_{CC} ≤ 3.60		2.0		2.0		
V_{IL}	LOW Level Input Voltage	0.90			.35 x V_{CC}		.35 x V_{CC}	V
		1.10 ≤ V_{CC} ≤ 1.30			.35 x V_{CC}		.35 x V_{CC}	
		1.40 ≤ V_{CC} ≤ 1.60			.35 x V_{CC}		.35 x V_{CC}	
		1.65 ≤ V_{CC} ≤ 1.95			.35 x V_{CC}		.35 x V_{CC}	
		2.30 ≤ V_{CC} ≤ 2.70			0.7		0.7	
		2.70 ≤ V_{CC} ≤ 3.60			0.8		0.8	
V_{OH}	HIGH Level Output Voltage	0.90	I_{OH}=-100 µA	V_{CC}-0.1		V_{CC}-0.1		V
		1.10 ≤ V_{CC} ≤ 1.30		V_{CC}-0.1		V_{CC}-0.1		
		1.40 ≤ V_{CC} ≤ 1.60		V_{CC}-0.2		V_{CC}-0.2		
		1.65 ≤ V_{CC} ≤ 1.95		V_{CC}-0.2		V_{CC}-0.2		
		2.30 ≤ V_{CC} ≤ 2.70		V_{CC}-0.2		V_{CC}-0.2		
		2.70 ≤ V_{CC} ≤ 3.60		V_{CC}-0.2		V_{CC}-0.2		
		1.10 ≤ V_{CC} ≤ 1.30	I_{OH}=-2 mA	.75 x V_{CC}		.75 x V_{CC}		
		1.40 ≤ V_{CC} ≤ 1.60	I_{OH}=-4 mA	.75 x V_{CC}		.75 x V_{CC}		
		1.65 ≤ V_{CC} ≤ 1.95	I_{OH}=-6 mA	1.25		1.25		
		2.30 ≤ V_{CC} ≤ 2.70		2.00		2.00		
		2.30 ≤ V_{CC} ≤ 2.70	I_{OH}=-12 mA	1.8		1.8		
		2.70≤ V_{CC} ≤ 3.60		2.2		2.2		
		2.30 ≤ V_{CC} ≤ 2.70	I_{OH}=-18 mA	1.7		1.7		
		2.70 ≤ V_{CC} ≤ 3.60		2.4		2.4		
		2.70 ≤ V_{CC} ≤ 3.60	I_{OH}=-24 mA	2.2		2.2		

Continued on following page…

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C		T_A=-40 to 85°C		Units
				Min.	Max.	Min.	Max.	
V_{OL}	LOW Level Output Voltage	0.90	I_{OL}=100 µA		0.1		0.1	V
		1.10 ≤ V_{CC} ≤ 1.30			0.1		0.1	
		1.40 ≤ V_{CC} ≤ 1.60			0.2		0.2	
		1.65 ≤ V_{CC} ≤ 1.95			0.2		0.2	
		2.30 ≤ V_{CC} ≤ 2.70			0.2		0.2	
		2.70 ≤ V_{CC} ≤ 3.60			0.2		0.2	
		1.10 ≤ V_{CC} ≤ 1.30	I_{OL}=2 mA		0.25 x V_{CC}		0.25 x V_{CC}	
		1.40 ≤ V_{CC} ≤ 1.60	I_{OL}=4 mA		0.25 x V_{CC}		0.25 x V_{CC}	
		1.65 ≤ V_{CC} ≤ 1.95	I_{OL}=6 mA		0.3		0.3	
		2.30 ≤ V_{CC} ≤ 2.70	I_{OL}=12 mA		0.4		0.4	
		2.70 ≤ V_{CC} ≤ 3.60			0.4		0.4	
		2.30≤ V_{CC} ≤ 2.70	I_{OL}=18 mA		0.6		0.6	
		2.70 ≤ V_{CC} ≤ 3.60			0.4		0.4	
		2.70 ≤ V_{CC} ≤ 3.60	I_{OL}=24 mA		0.55		0.55	
I_{IN}	Input Leakage Current	0.90 to 3.60	0 ≤ V_{IN} ≤ 3.60		±0.1		±0.5	µA
I_{OFF}	Power Off Leakage Current	0	0 ≤ ($V_{IN,}$ v_O) ≤ 3.60		0.5		0.5	µA
I_{CC}	Quiescent Supply Current	0.90 to 3.60	V_{IN}=V_{CC}, or GND		0.9		0.9	µA
			V_{CC} ≤ V_{IN} ≤ 3.6 V				±0.9	

AC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C			T_A=-40 to 85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PHL}, t_{PLH}	Propagation Delay	0.90	C_L=15 pF, R_L=1 MΩ		13				ns	Figure 5 Figure 6
		1.10 ≤ V_{CC} ≤ 1.30	C_L=15 pF, R_L=2k Ω	3.0	6.0	10.0	1.0	14.6		
		1.40 ≤ V_{CC} ≤ 1.60		1.0	3.2	6.0	1.0	7.2		
		1.65 ≤ V_{CC} ≤ 1.95	C_L=30 pF, R_L=500 Ω	1.0	2.0	4.5	1.0	5.3		
		2.30 ≤ V_{CC} ≤ 2.70		0.8	1.2	2.6	0.7	3.7		
		2.70 ≤ V_{CC} ≤ 3.60		0.7	1.0	2.3	0.6	3.0		
C_{IN}	Input Capacitance	0			2				pF	
C_{PD}	Power Dissipation Capacitance	0.90 to 3.60	V_{IN}=0 V or V_{CC}, f=10 MHz		8				pF	

AC Loadings and Waveforms

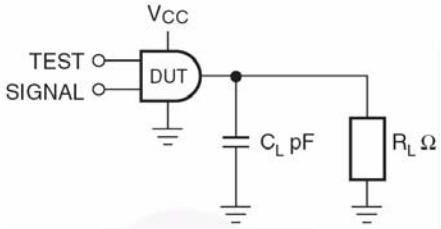

Figure 5. AC Test Circuit

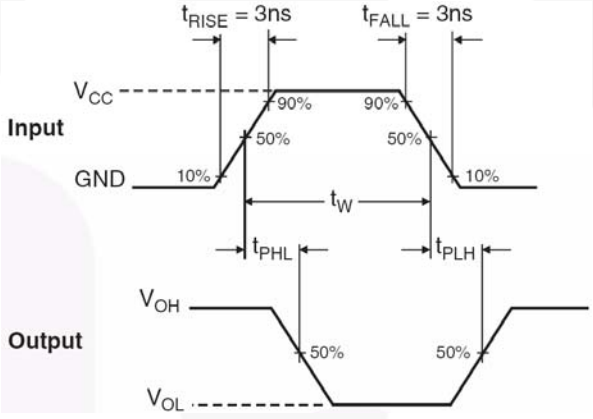

Figure 6. AC Waveforms

Symbol	V_{CC}					
	3.3 V ±0.3 V	**2.5 V ±0.2 V**	**1.8 V ±0.15 V**	**1.5 V ±0.1 V**	**1.2 V ±0.1 V**	**0.9 V**
V_{mi}	1.5 V	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5 V	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$

Physical Dimensions

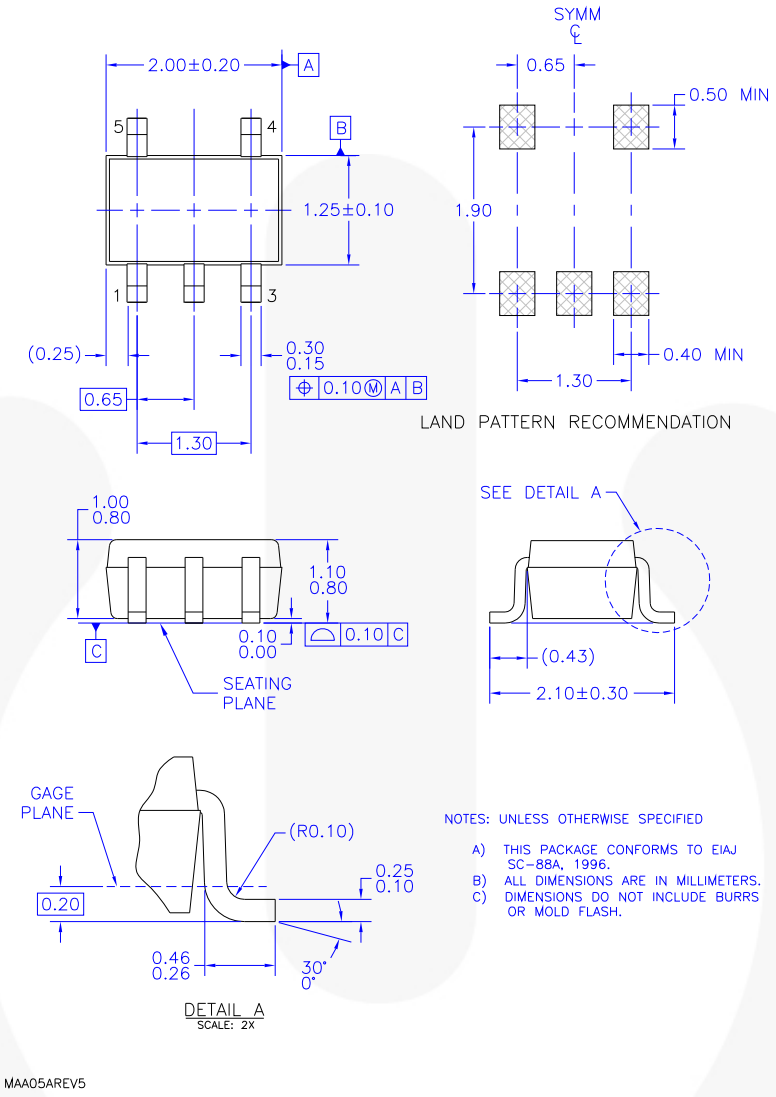

Figure 7. 5-Lead, SC70, EIAJ SC-88a, 1.25 mm Wide

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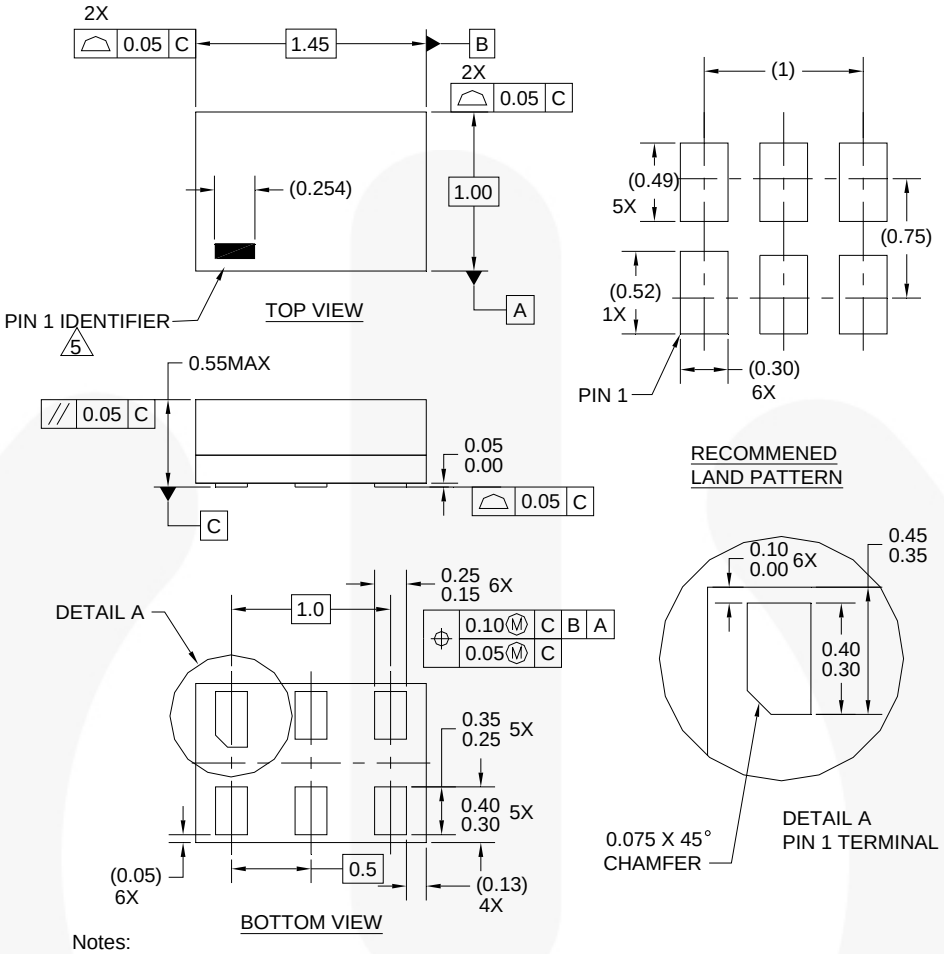
Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/analog/pdf/sc70-5_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
P5X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 8. 6-Lead, MicroPak™, 1.0 mm Wide

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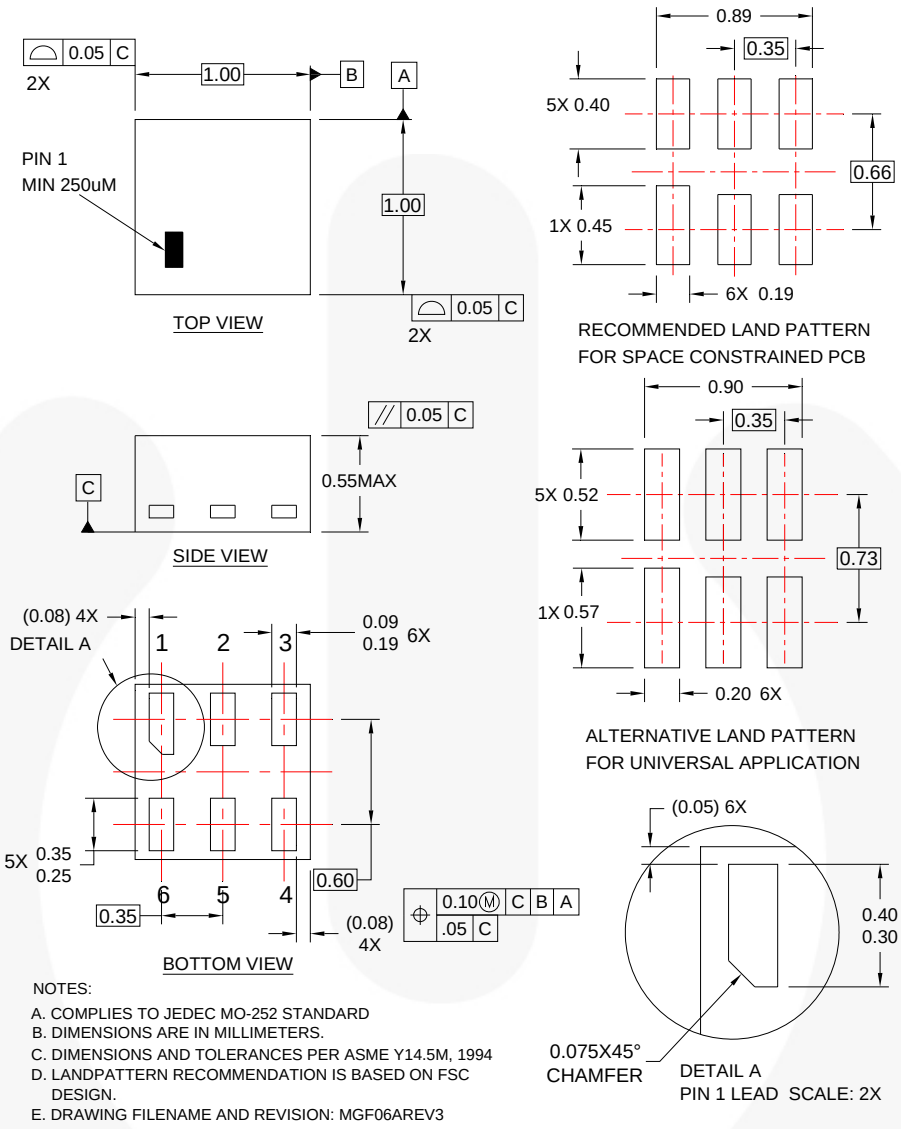
Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



NOTES:

A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. LANDPATTERN RECOMMENDATION IS BASED ON FSC DESIGN.
E. DRAWING FILENAME AND REVISION: MGF06AREV3

Figure 9. 6-Lead, MicroPak2, 1x1mm Body, .35 mm Pitch

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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I62

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