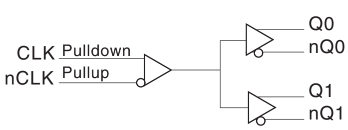
General Description

The 85311I is a low skew, high performance 1-to-2 Differential-to-2.5V/3.3V ECL/LVPECL Fanout Buffer. The CLK, nCLK pair can accept most standard differential input levels.The 85311I is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the 85311I ideal for those clock distribution applications demanding well defined performance and repeatability.

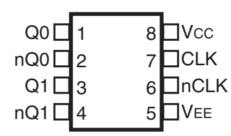
Features

- Two differential 2.5V/3.3V LVPECL / ECL outputs
- One CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 1GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 20ps (maximum)
- Part-to-part skew: 350ps (maximum)
- Propagation delay: 2.1ns (maximum)
- Additive phase jitter, RMS: 0.14ps (typical), 3.3V
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -2.375V to -3.465V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



85311I

8-Lead SOIC
3.90mm x 4.903mm x 1.37mm package body
M Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
5	V_{EE}	Power		Negative supply pin.
6	nCLK	Input	Pullup	Inverting differential clock input.
7	CLK	Input	Pulldown	Non-inverting differential clock input.
8	V_{CC}	Power		Positive supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA}	103°C/W (0 lfpm)

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{CC} = 3.3V±5% or 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Power Supply Current				25	mA

Table 3B. Differential DC Characteristics, V_{CC} = 3.3V±5% or 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			5	µA
		CLK	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	nCLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

Table 3C. LVPECL DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Current; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.65		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 3D. LVPECL DC Characteristics, V_{CC} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Current; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

AC Electrical Characteristics

Table 4A. AC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				1	GHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 1GHz	0.9		2.1	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range (12kHz – 20MHz)		0.14		ps
*t*sk(o)	Output Skew; NOTE 2, 4				20	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				350	ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters are measured 500MHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

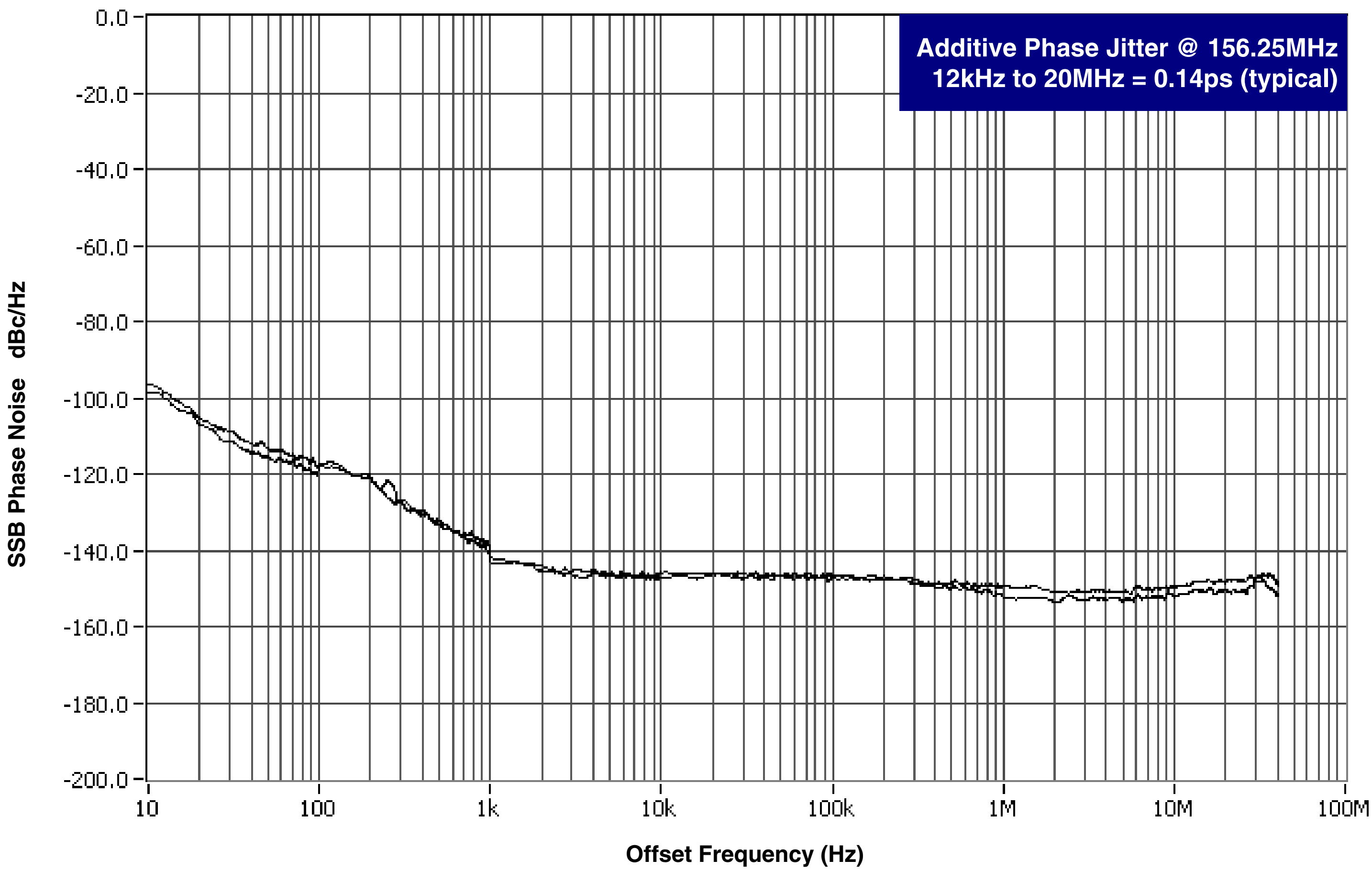
Table 4B. AC Characteristics, V_{CC} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				1	GHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 1GHz	0.9		2.1	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range (12kHz – 20MHz)		0.135		ps
*t*sk(o)	Output Skew; NOTE 2, 4				25	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	250		700	ps
odc	Output Duty Cycle		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters are measured 500MHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

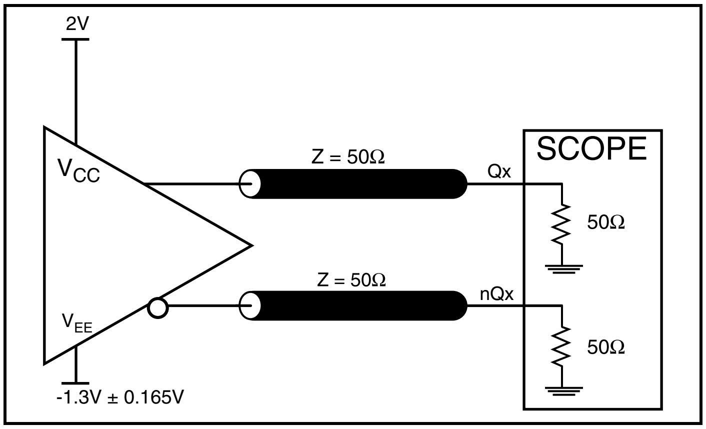
Additive Phase Jitter (3.3V)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

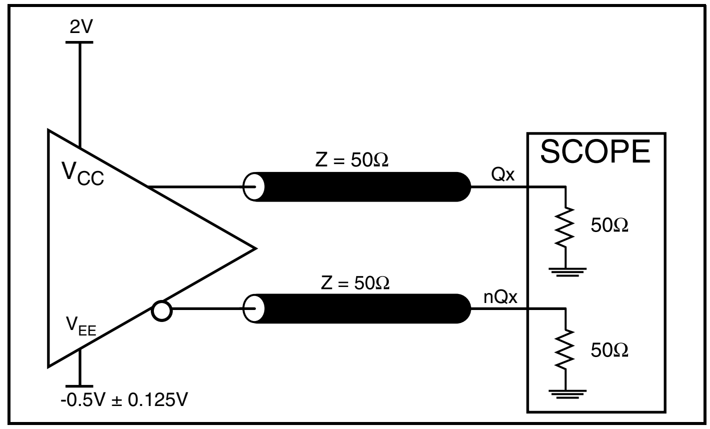


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

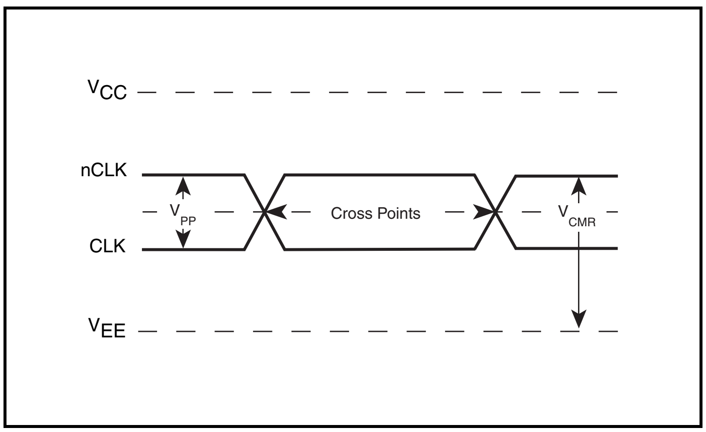
Parameter Measurement Information



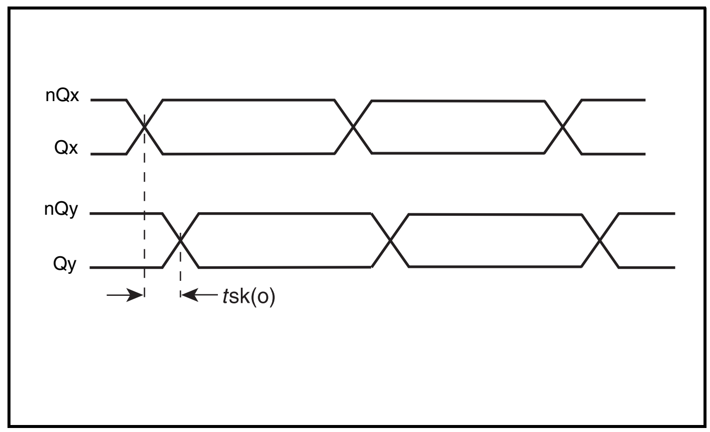
3.3V Core/ 3.3V LVPECL Output Load AC Test Circuit



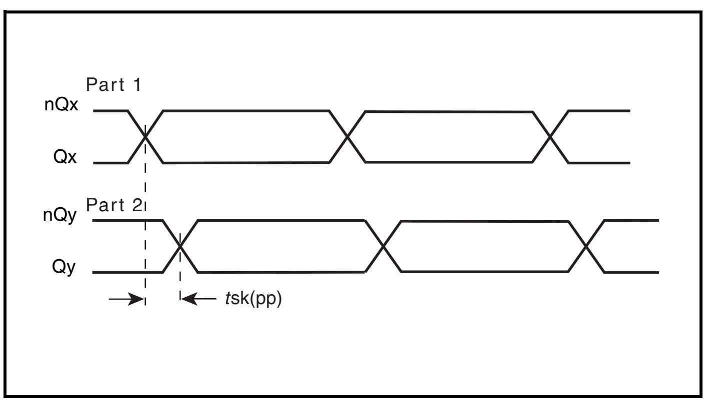
2.5V Core/ 2.5V LVPECL Output Load AC Test Circuit



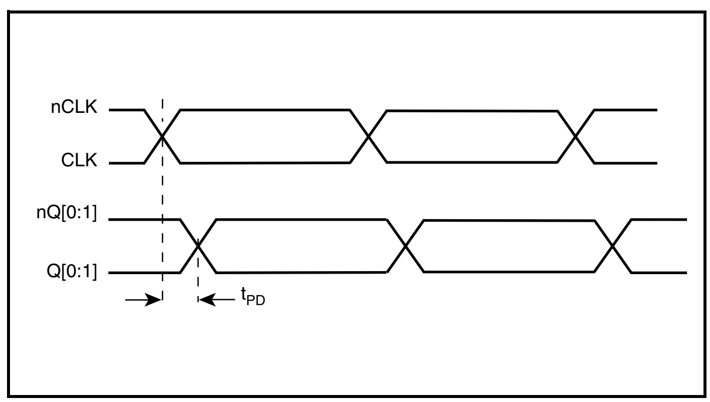
Differential Input Level



Output Skew

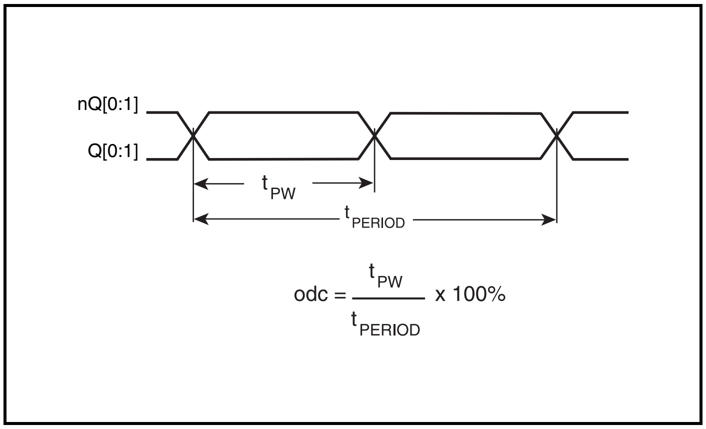


Part-to-Part Skew

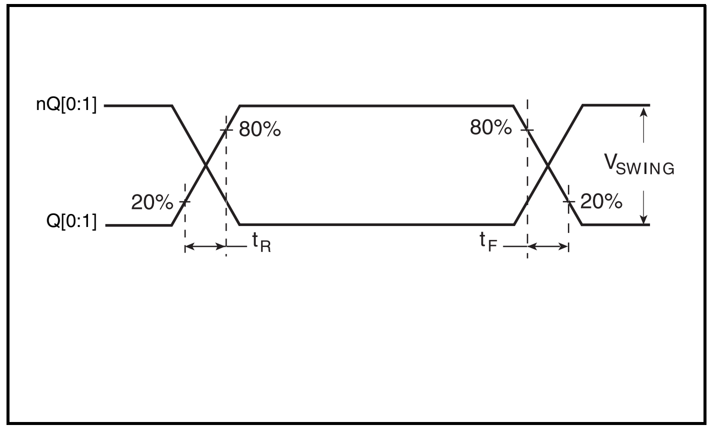


Propagation Delay

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Applications Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

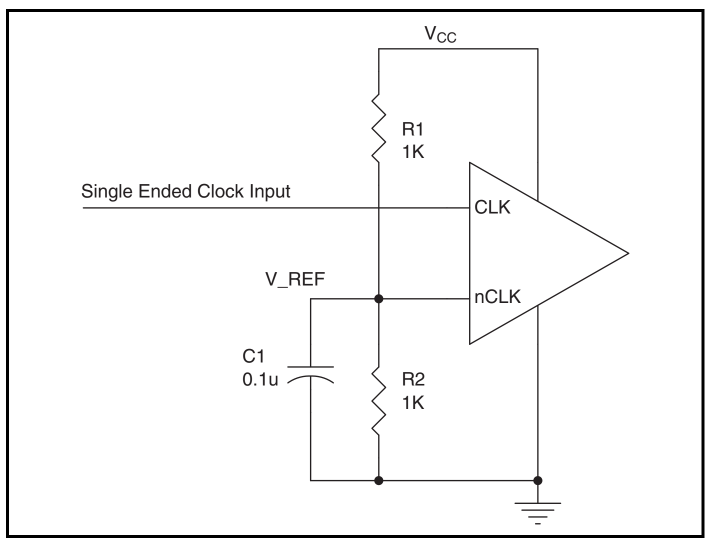


Figure 1. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

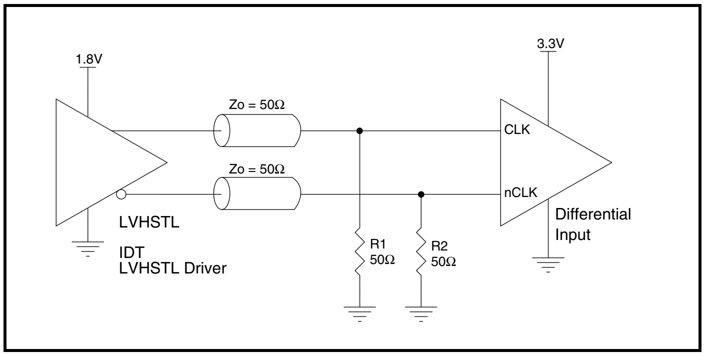


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

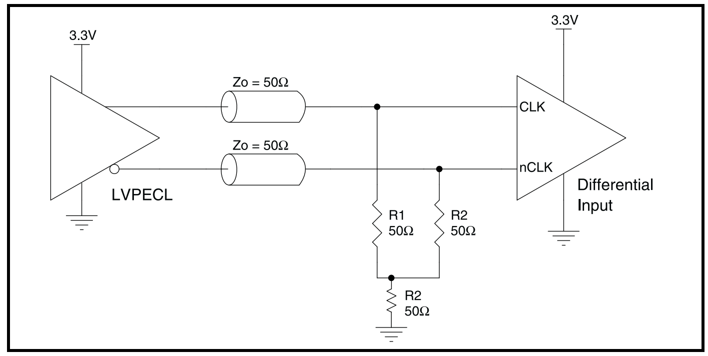


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

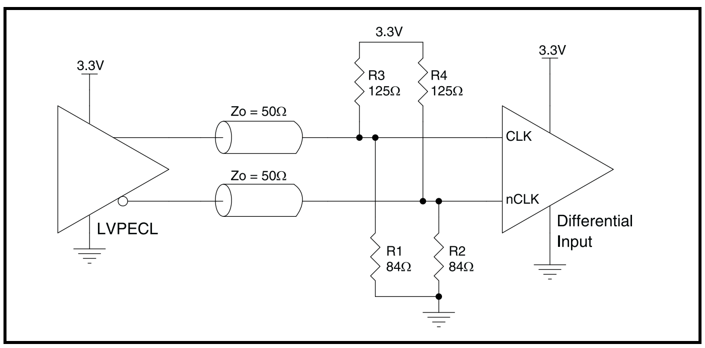


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

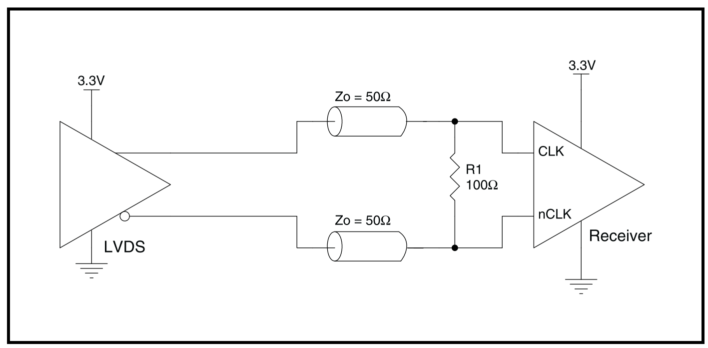


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

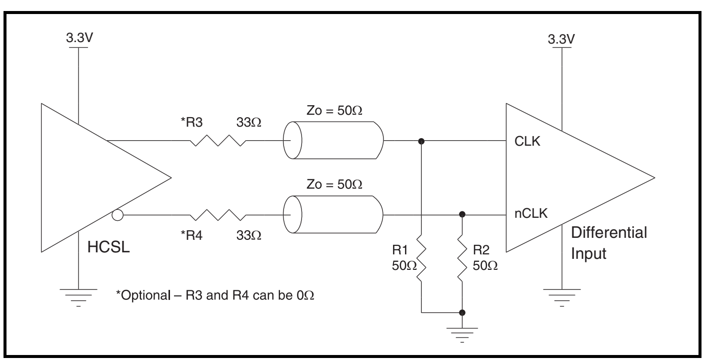


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

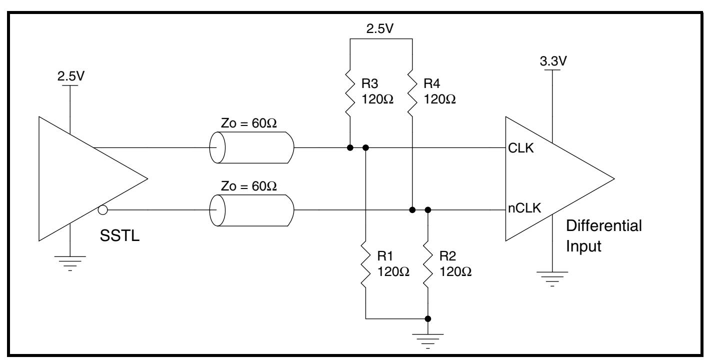


Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Output Pins

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

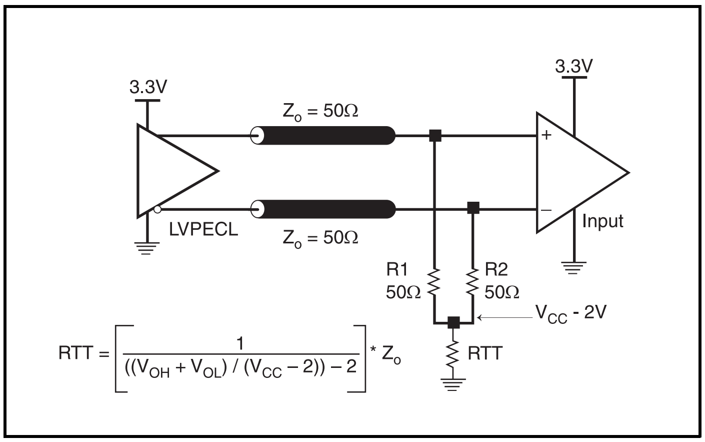


Figure 3A. 3.3V LVPECL Output Termination

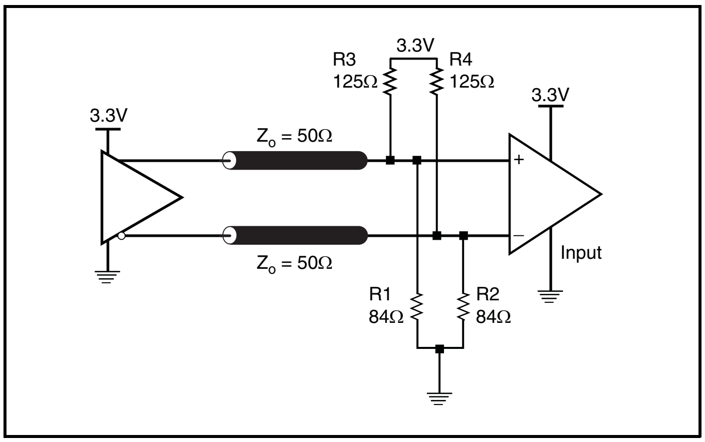


Figure 3B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

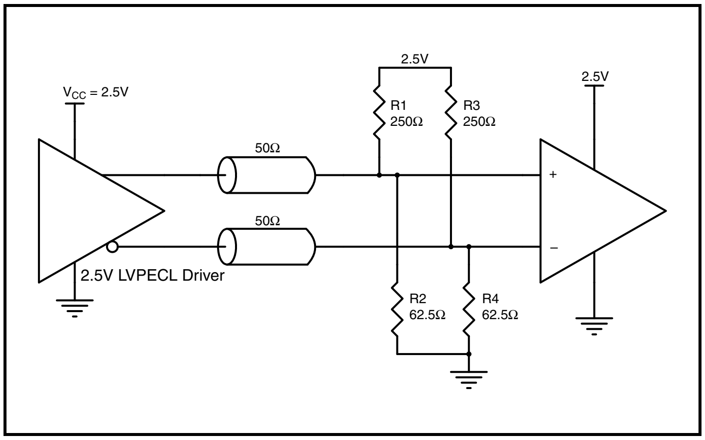


Figure 4A. 2.5V LVPECL Driver Termination Example

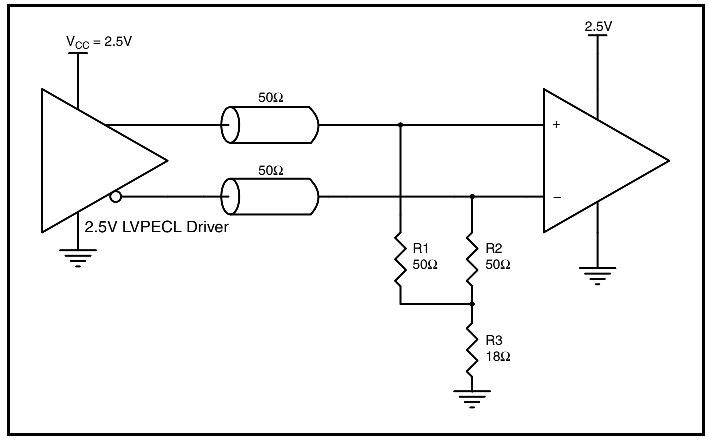


Figure 4B. 2.5V LVPECL Driver Termination Example

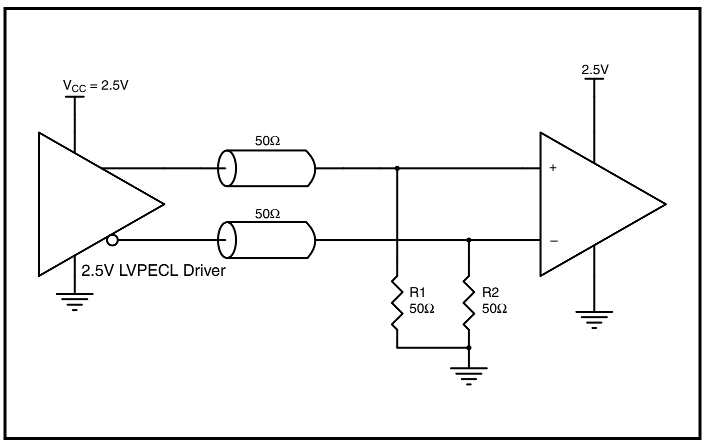


Figure 4C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 85311I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 85311I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC}= 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 25mA = **86.6mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 86.6mW + 60mW = **146.6mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 103°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.147W * 103°C/W = 100.1°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 8 Lead SOIC, Forced Convection

θ_{JA} **vs. Air Flow**			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

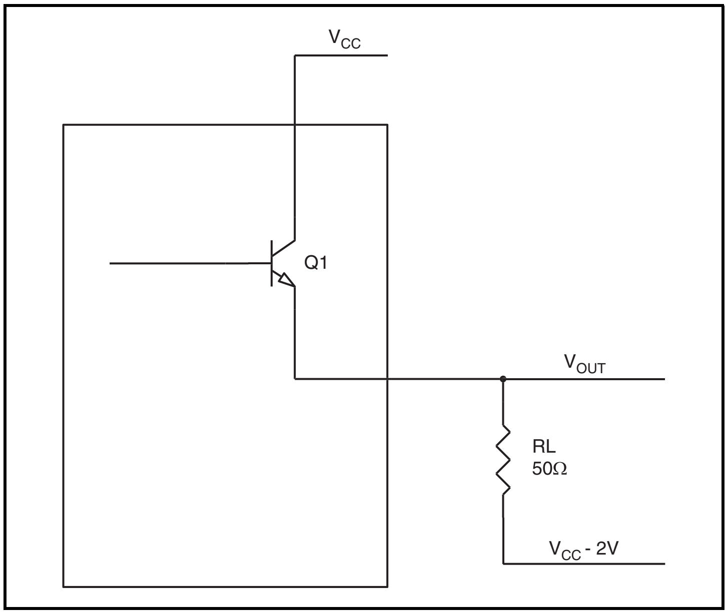


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 8 Lead SOIC

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

Transistor Count

The transistor count for 85311I is: 225

Package Outline and Package Dimensions

Package Outline - M Suffix for 8 Lead SOIC

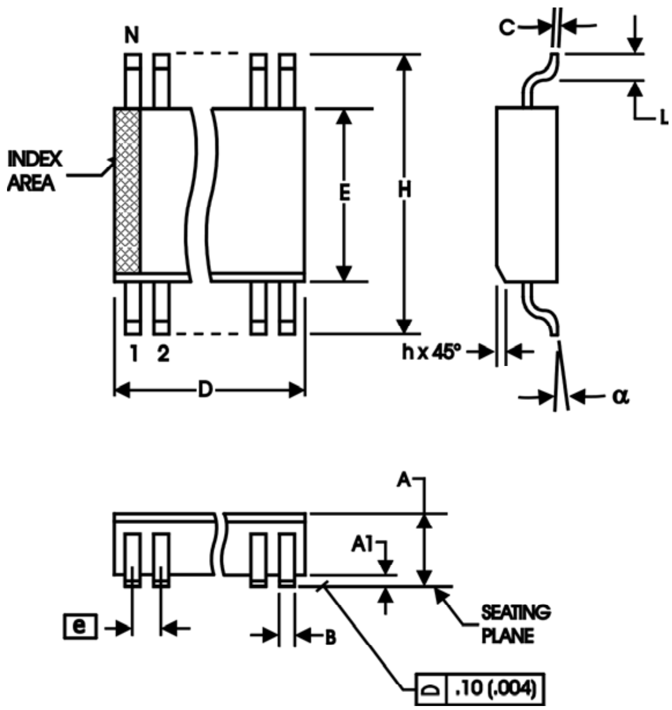


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85311AMILF	85311AIL	"Lead-Free" 8 Lead SOIC	Tube	-40°C to 85°C
85311AMILFT	85311AIL	"Lead-Free" 8 Lead SOIC	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T8	1 16	General Description - deleted HiperClockS logo. Ordering Information Table - deleted table note. Deleted HiperClockS references throughout the datasheet. Updated datasheet header/footer.	2/16/16

www.IDT.com

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com