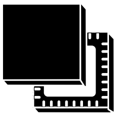
STPM32, STPM33, STPM34

ASSP for metering applications with up to four independent 24-bit 2^{nd} order sigma-delta ADCs, 4 MHz OSF and 2 embedded PGLNA

Datasheet - production data

QFN24L 4x4x1



QFN32L 5x5x1

Features

- Active power accuracy:
  - < 0.1% error over 5000: 1 dynamic range
  - < 0.5% error over 10000: 1 dynamic range
- Exceeds 50-60 Hz EN 50470-x, IEC 62053-2x, ANSI12.2x standard requirements for AC watt meters
- Reactive power accuracy:
  - < 0.1% error over 2000:1 dynamic range
- Dual mode apparent energy calculation
- Instantaneous and averaged power
- RMS and instantaneous voltage and current
- Under and overvoltage detection (sag and swell) and monitoring
- Overcurrent detection and monitoring
- UART and SPI serial interface with programmable CRC polynomial verification
- Programmable LED and interrupt outputs
- Four independent 24-bit 2^{nd} order sigma-delta ADCs
- Two programmable gain chopper stabilized low-noise and low-offset amplifiers
- Bandwidth 3.6 kHz at -3 dB
- V_{CC} supply range 3.3 V ± 10%
- Supply current I_{CC} 4.3 mA (STPM32)
- Input clock frequency 16 MHz, Xtal or external source
- Twin precision voltage reference: 1.18 V with independent programmable TC, 30 ppm/°C typ.
- Internal low drop regulator at 3 V (typ.)
- QFN packages
- Operating temperature from -40 °C to +105 °C

Description

The STPM3x is an ASSP family designed for high accuracy measurement of power and energies in power line systems using the Rogowski coil, current transformer or shunt current sensors. The STPM3x provides instantaneous voltage and current waveforms and calculates RMS values of voltage and currents, active, reactive and apparent power and energies. The STPM3x is a mixed signal IC family consisting of an analog and a digital section. The analog section consists of up to two programmable gain low-noise low-offset amplifiers and up to four 2^{nd} order 24-bit sigma-delta ADCs, two bandgap voltage references with independent temperature compensation, a low drop voltage regulator and DC buffers. The digital section consists of digital filtering stage, a hardwired DSP, DFE to the input and a serial communication interface (UART or SPI). The STPM3x is fully configurable and allows a fast digital system calibration in a single point over the entire current dynamic range.

Table 1. Device summary

Order code	Package	Packing
STPM34TR	QFN32L 5x5x1	Tape and reel
STPM33TR	QFN32L 5x5x1	Tape and reel
STPM32TR	QFN24L 4x4x1	Tape and reel

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Figure 1. STPM34 block diagram

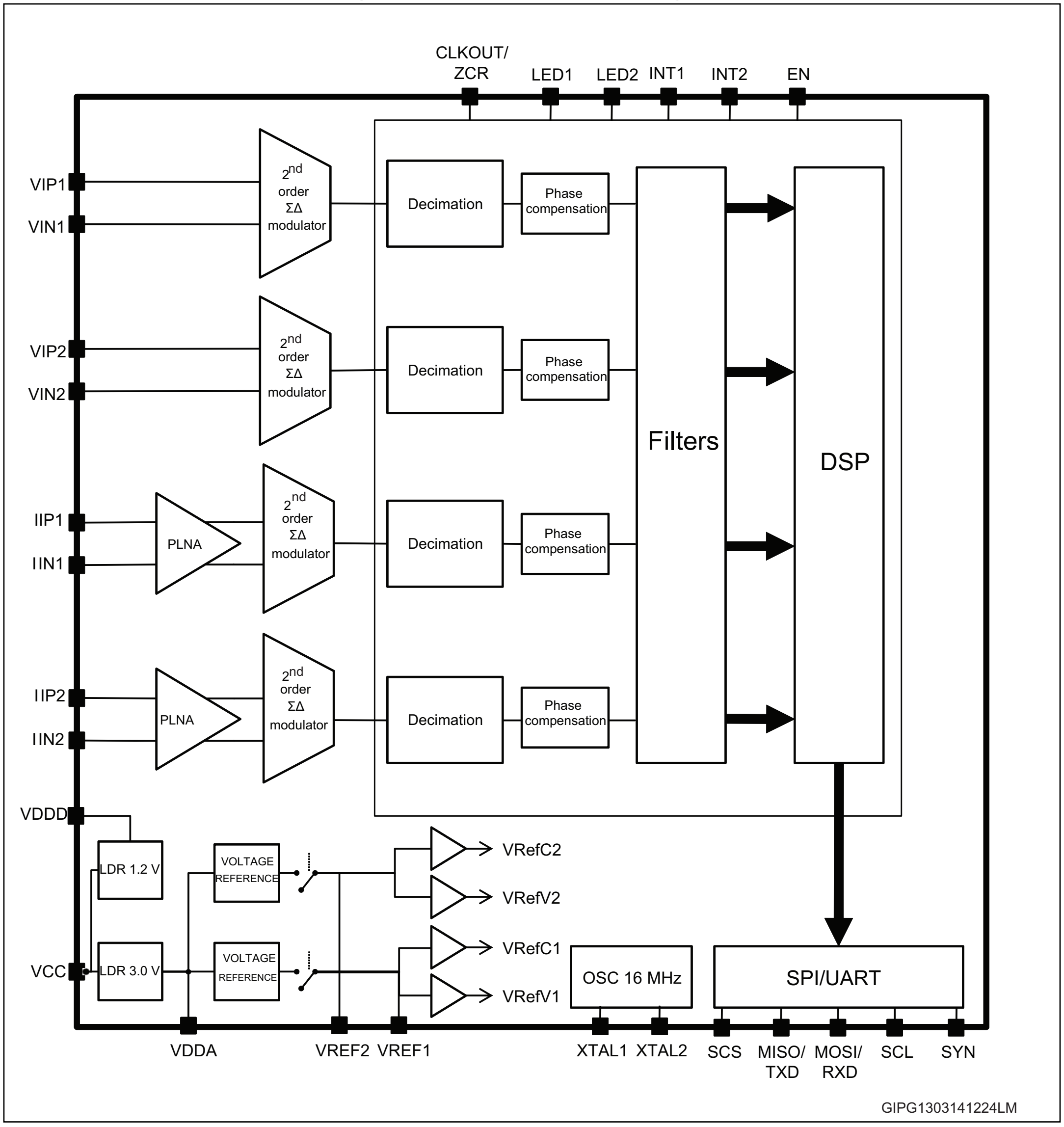


Figure 2. STPM33 block diagram

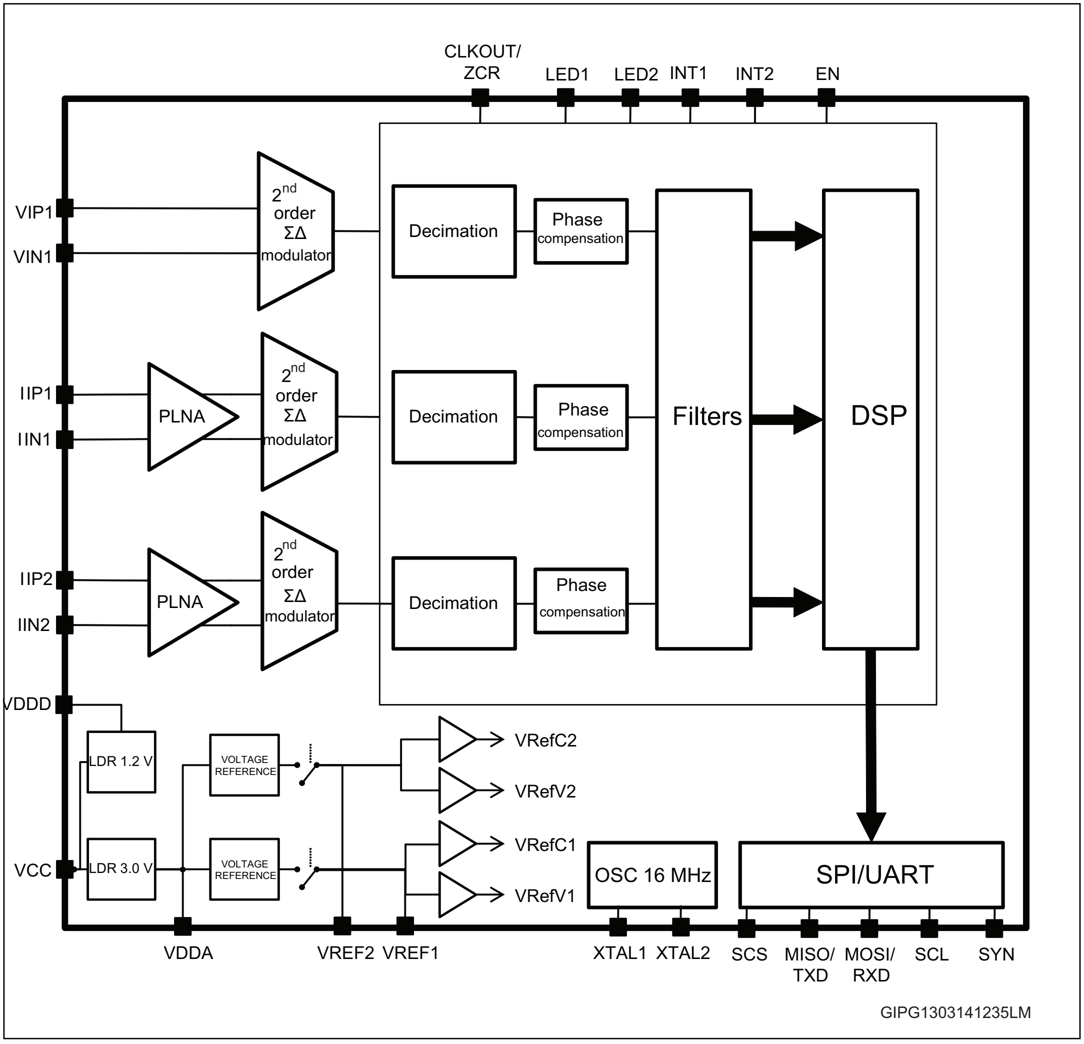
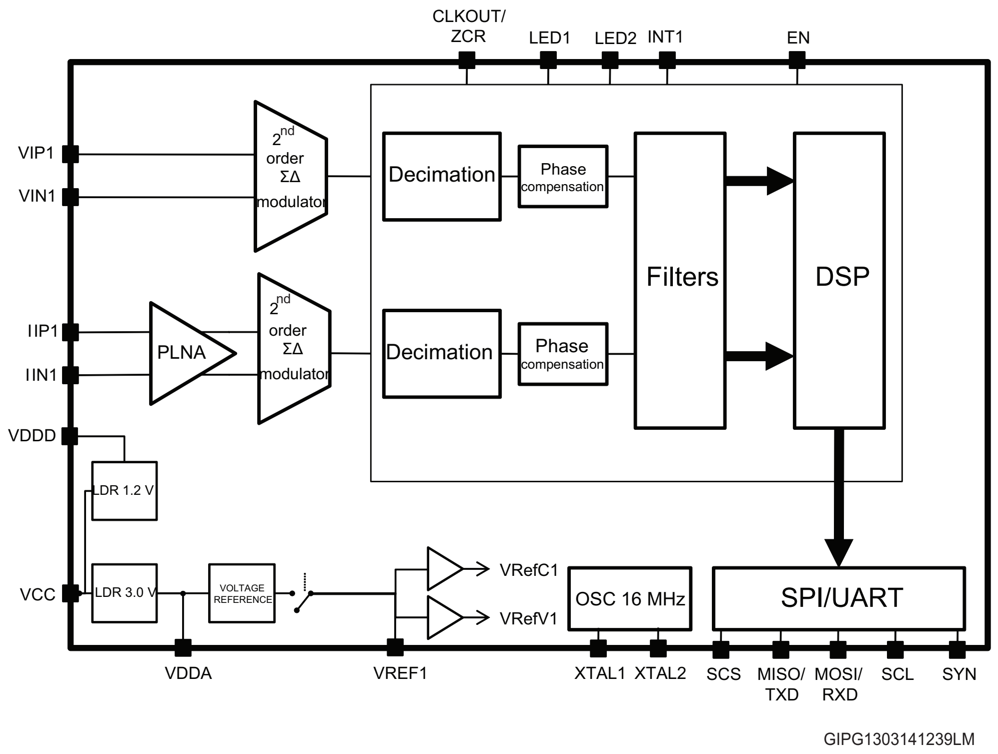


Figure 3. STPM32 block diagram



2 Pin configuration

Figure 4. STPM34 pinout (top view), QFN32L 5x5x1

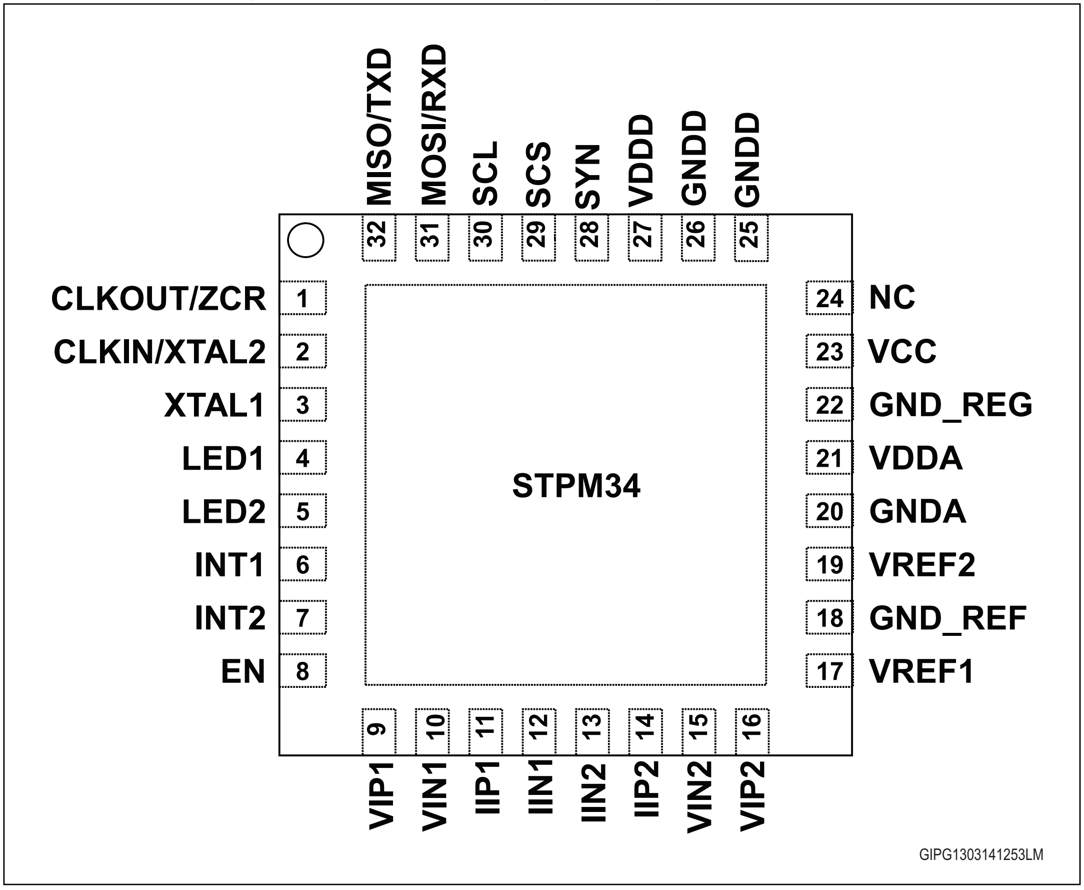


Figure 5. STPM33 pinout (top view), QFN32L 5x5x1

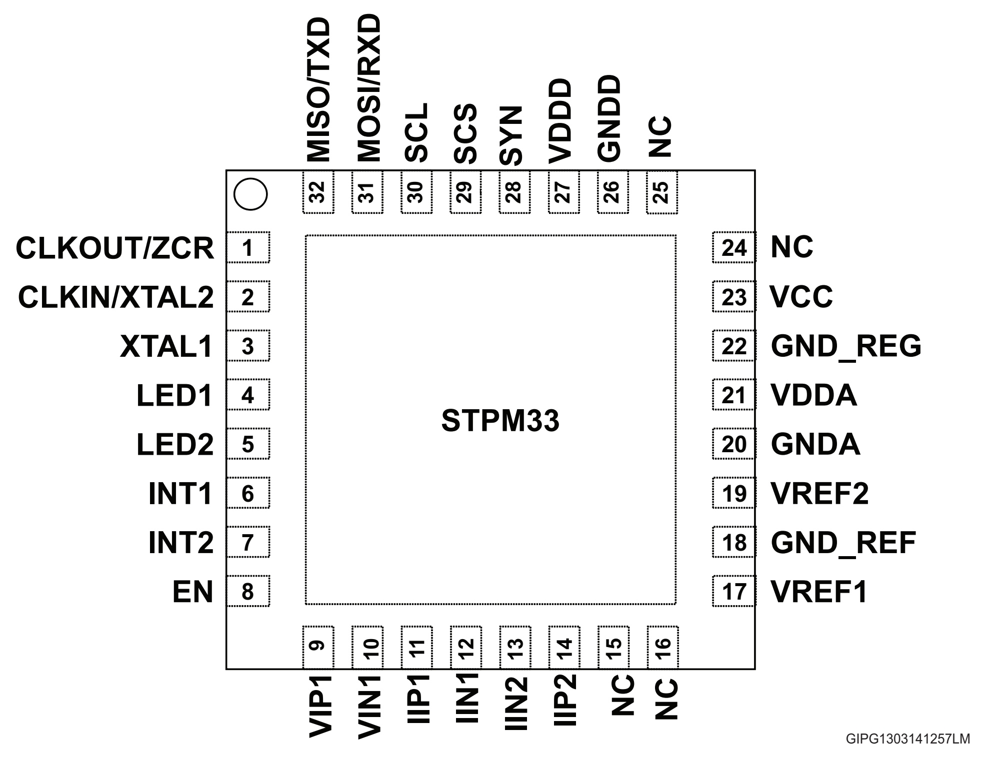


Figure 6. STPM32 pinout (top view), QFN24L 4x4x1

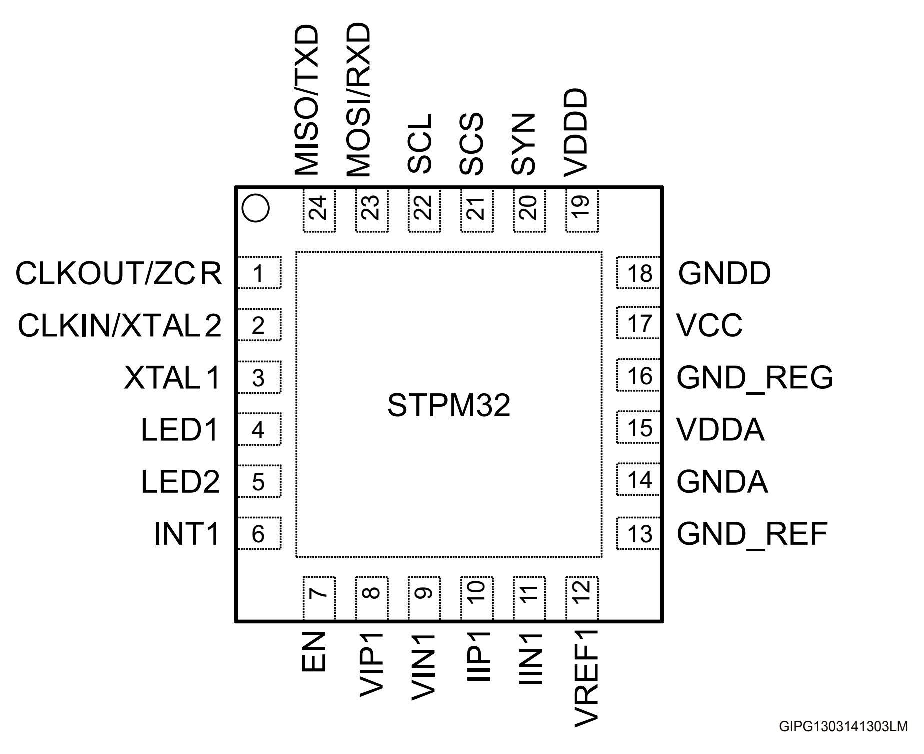


Table 2. STPM34, STPM33, STPM32 pin description

STPM34	STPM33	STPM32	Name	Description and multiplexed function	Voltage range	Functional section
1	1	1	CLKOUT/ZCR	-Zero-crossing output -System clock output	From 0 to V_{CC}	Multifunctional
2	2	2	CLKIN/XTAL2	-Input of external clock -External crystal input 2	From 0 to V_{CC}	Oscillator
3	3	3	XTAL1	-External crystal input 1	From 0 to V_{CC}	Oscillator
4	4	4	LED1	-Pulse output 1 -Primary current SD bitstream	From 0 to V_{CC}	Multifunctional
5	5	5	LED2	-Pulse output 2 -Secondary current SD bitstream	From 0 to V_{CC}	Multifunctional
6	6	6	INT1	-Interrupt 1 -Primary voltage SD bitstream	From 0 to V_{CC}	Multifunctional
7	7	-	INT2	-Interrupt 2 -Secondary voltage SD bitstream	From 0 to V_{CC}	Multifunctional
8	8	7	EN	Enable pin	From 0 to V_{CC}	Signal
9	9	8	VIP1	Positive voltage primary input	From -0.3 V to 0.3 V	Signal
10	10	9	VIN1	Negative voltage primary input	From -0.3 V to 0.3 V	Signal
11	11	10	IIP1	Positive current primary input	From -0.3 V to 0.3 V	Signal
12	12	11	IIN1	Negative current primary input	From -0.3 V to 0.3 V	Signal
13	13	-	IIN2	Negative current secondary input	From -0.3 V to 0.3 V	Signal
14	14	-	IIP2	Positive current secondary input	From -0.3 V to 0.3 V	Signal
15	-	-	VIN2	Negative voltage secondary input	From -0.3 V to 0.3 V	Signal
16	-	-	VIP2	Positive voltage secondary input	From -0.3 V to 0.3 V	Signal
17	17	12	VREF1	Output of voltage reference 1	From 1.16 V to 1.18 V	Power
18	18	13	GND_REF	Analog ground of VREF	-	Power
19	19	-	VREF2	Output of voltage reference 2	From 1.16 V to 1.18 V	Power
20	20	14	GNDA	Analog ground (shield)	-	Power
21	21	15	VDDA	Output of voltage regulator	3.0 V	Power
22	22	16	GND_REG	Ground	-	Power

Table 2. STPM34, STPM33, STPM32 pin description (continued)

STPM34	STPM33	STPM32	Name	Description and multiplexed function	Voltage range	Functional section
23	23	17	VCC	Voltage supply	From 3.0 V to 3.6 V	Power
24	15, 16, 24, 25	-	NC	Not connected	-	-
25, 26	26	18	GNDD	Digital ground	-	Power
27	27	19	VDDD	Output of voltage regulator	1.2 V	Power
28	28	20	SYN	Synchronization pin	From 0 to V_{CC}	SPI
29	29	21	SCS	Chip-select SPI/UART select	From 0 to V_{CC}	SPI/UART
30	30	22	SCL	SPI clock	From 0 to V_{CC}	SPI
31	31	23	MOSI/RXD	SPI master OUT slave IN UART RX	From 0 to V_{CC}	SPI/UART
32	32	24	MISO/TXD	SPI master IN slave OUT UART TX	From 0 to V_{CC}	SPI/UART

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC input voltage	-0.3 to 4.2	V
V_{ID}	Any pin input voltage	-0.3 to V_{CC} + 0.3	V
V_{IA}	Analog pin input voltage (VIP, VIN, IIP, IIN)	-0.7 to 0.7	V
ESD	Human body model (all pins)	±2	kV
I_{LATCH}	Current injection latch-up immunity	100	mA
T_j	Junction temperature	125	°C
T_{STG}	Storage temperature range	-40 to 150	°C

Note: *Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.*

Table 4. Thermal data

Symbol	Parameter	Package	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	QFN32L 5x5x1	30	°C/W
		QFN24L 4x4x1	35	

Note: *This value is referred to single-layer PCB, JEDEC standard test board.*

4 Electrical characteristics

V_{CC} = 3.3 V, C_L= 1 μF between V_{DDA} and GNDA, C_L = 4.7 μF between V_{DDD} and GNDD, C_L= 1 μF between V_{CC} and GND, C_L = 100 nF between VREF1, 2 and GNDREF, F_{CLK} = 16 MHz, T_{AMB} = 25 °C, EN = V_{CC}, SPI/UART not used, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
T_{OP}	Operating junction temperature range	-	-40	-	105	°C
V_{CC}	Operating supply voltage	-	2.95	3.3	3.65	V
I_{CC}	Operating current	STPM32	-	4.3	-	mA
		STPM33	-	5.0	-	
		STPM34	-	5.9	-	
		STPM34 Primary channel ON: ENVREF1 = 1, enV1 = enC1 = 1 Secondary channel OFF: ENVREF2 = 0, enV2 = enC2 = 0	-	4.5	-	
		STPM34 Primary current channel ON only: ENVREF1 = 1, enV1 = 0, enC1 = 1 Secondary channel OFF: ENVREF2 = 0, enV2 = enC2 = 0	-	4.0	-	
F_{CLK}	Nominal frequency	-	-	16	-	MHz
t_comm	Interface selection timing	-	125	-	-	ns
External Clock Source(1)						
Duty cycle	Duty cycle of CLKIN signal	-	40	-	60	%
t_rise	Rise time (10% to 90%) of CLKIN signal	-	-	-	3	ns
Crystal oscillator(1)						
Gm_crit_max	Maximum critical crystal g_m	-	-	-	0.46	mA/V
DL	Drive level	-	-	100	-	uW
C_{OSC_IN}	Internal capacitance of oscillator inputs	-	-	4	-	pF
Power management (VDDA, VDDD, GNDA, GNDD, GND_REG, EN)						
V_{POR}	Power-on-reset on V_{CC}	-	-	2.5	-	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{STBY}	Standby current consumption	EN = GND	-	< 1	-	µA
V_{DDA}	Analog regulated voltage	-	-	2.85	-	V
V_{DDD}	Digital regulated voltage	-	-	1.2	-	V
$PSRR_{REGS}$	Power supply rejection ratio[1]	50 Hz	-	50	-	dB
On-chip reference voltage (VREF1, VREF2)						
V_{REF}	Reference voltage	No load on V_{REF}, T_C = 010 (default)	-	1.18	-	V
T_C	Temperature coefficient[2]	Default	-	30	-	ppm/°C
T_{Cstep}	TC programmable step[2]	-	-	± 30	-	ppm/°C
Analog inputs (VIP1, VIN1, VIP2, VIN2, IIP1, IIN1, IIP2, IIN2)						
V_{MAX}	Maximum input signal levels	Voltage channels (VIP1-VIN1, VIP2-VIN2)	-300	-	+300	mV
		Current channels (IIP1-IIN1, IIP2-IIN2)		-		mV
		Gain 2X	-300		+300	
		Gain 4X	-150		+150	
		Gain 8X	-75		+75	
		Gain 16X	-37.5		+37.5	
V_{off}	Amplifier offset[2]	Shorted and grounded input	-	1	-	mV
Z_{Vin}	Voltage channel input impedance[1]	-	-	8	-	MΩ
Z_{Iin}	Current channel input differential impedance[1]	Gain 2X	-	90	-	kΩ
		Gain 4X		170		
		Gain 8X		300		
		Gain 16X		510		
G_{ERR}	Channel gain error	Input $V_{MAX}/2$	-	± 5	-	%
	Crosstalk[1]	Voltage to current channels	-	-120	-	dB
		Current to voltage channels	-	-120	-	
Digital I/O (CLKOUT/ZCR, LED1, LED2, INT1, INT2, MISO, MOSI, SCL, SCS, SYN)						
V_{IH}	Input high-voltage	-	0.75 V_{CC}	-	3.3	V
V_{IL}	Input low-voltage	V_{CC} = 3.2 V	-0.3	-	0.6	V
V_{OH}	Output high-voltage	I_O = -1 mA, V_{CC} = 3.2 V	V_{CC}-0.4	-	-	V
V_{OL}	Output low-voltage	I_O = +1 mA, V_{CC} = 3.2 V	-	-	0.4	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
External Clock Input (CLKIN/XTAL2)(3)						
V_{IH}	Input high-voltage	Vcc=3.3V	0.8	-	3.3	V
V_{IL}	Input low-voltage	Vcc=3.3V	-0.3	-	0.1	V
Energy measurement accuracy						
AP	Active power	Over dynamic range 5000:1 PGA = 2 to 16	-	0.1	-	%
		Over dynamic range 10000:1 PGA = 2 to 16	-	0.5	-	
RP	Reactive power	Over dynamic range 2000:1 PGA = 2 to 16	-	0.1	-	
RMS	Voltage RMS	Over dynamic range 1:200	-	0.5	-	%
	Current RMS	Over dynamic range 1:500	-	0.5	-	-
f_{BW}	Effective bandwidth	-3 dB, HPF = 1	4	-	3600	Hz
Sigma-delta ADC performance						
OSF	Oversampling frequency	-	-	4	-	MHz
DR	Decimation ratio	-	-	1/512	-	-
F_s	Sampling frequency	-	-	7.8125	-	kHz
FBW	Flat band	< 0.05 dB allowed ripple	2	-	-	kHz
BW	Effective bandwidth	-3 dB, HPF = 0	0	-	3600	Hz
DC measurement accuracy						
$PSRR_{AC}$	Power supply AC rejection(2)	Voltage input shorted Current input shorted V_{CC} = 3.3 V ± 150 mVp at 1 kHz	-	65	-	dB
SPI timings(3)						
t_en	Time between selection and clock	-	50	-	-	ns
t_clk	Clock period	-	50	-	-	ns
t_cpw	Clock pulse width	-	25	-	-	ns
t_setup	Set-up time before slave sampling	-	10	-	-	ns
t_hold	Hold time after slave sampling	-	40	-	-	ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
tpZL	Enable to low level time	V_{CC} = 3.3 V ± 10%, V_{IN} = 0 to 3 V, 1 MHz, Rise time = fall time = 6 ns RL = 1 kΩ, CL = 50 pF see *Figure 10*	-	25	-	ns
tpLZ	Disable from low level time		-	15	-	ns
UART timings[3]						
t_1	-	CS enable to RX start	5	-	-	ns
t_2	-	Stop bit to CS disable	1	-	-	µs
t_3	-	CS disable to TX idle hold time	-	-	250	ns
tpZH	Enable to high level time	V_{CC} = 3.3 V ± 10%, V_{IN} = 0 to 3 V, 1 MHz, Rise time = fall time = 6 ns RL = 1 kΩ, CL = 50 pF see *Figure 10*	-	21	-	ns
tpHZ	Disable from high level time		-	11	-	ns
SYN timings[3]						
t_ltch	Time between de-selection and latch	-	20	-	-	ns
t_lpw	Latch pulse width	-	4	-	-	µs
t_w	Time between two consecutive latch pulses	-	4	-	-	µs
t_rpw	Reset pulse width	-	4	-	-	µs
t_rel	Time between pulse and selection	-	40	-	-	ns
t_startup	Time between power-on and reset	-	35	-	-	ms

1. Guaranteed by design.
2. Guaranteed by characterization.
3. Guaranteed by application.

Figure 7. SPI timings

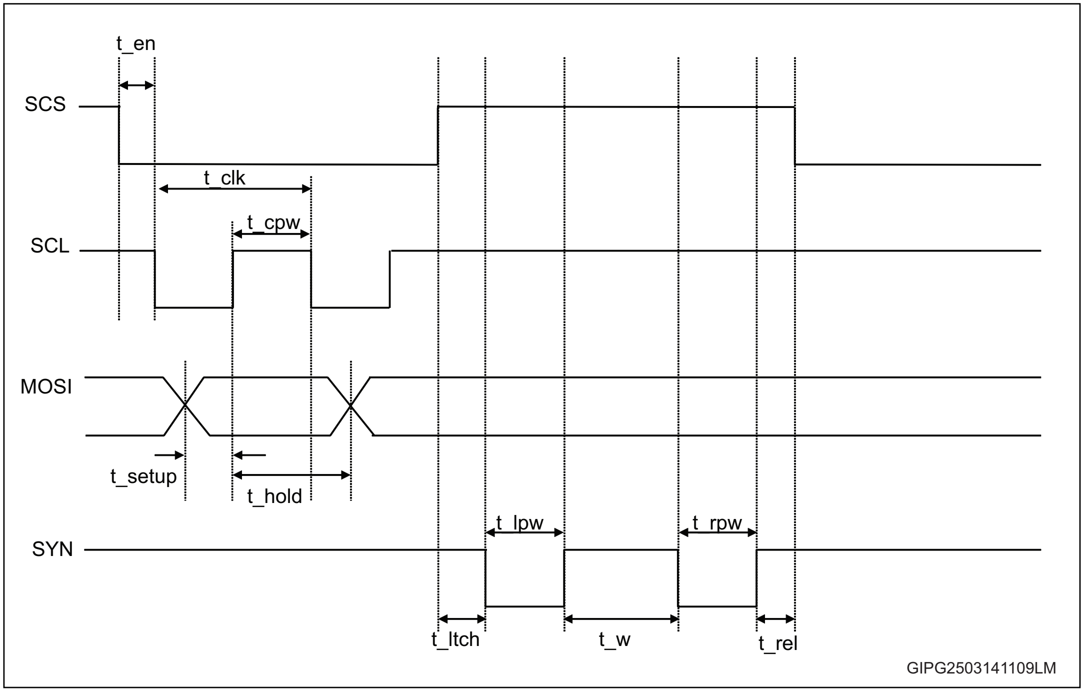


Figure 8. SPI enable and disable timing diagrams

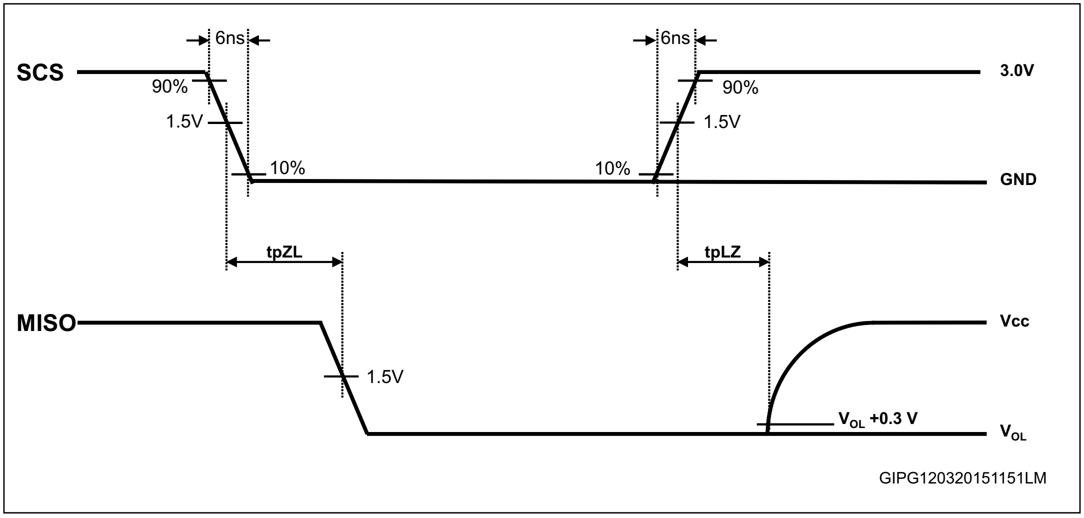


Figure 9. UART enable and disable timing diagrams

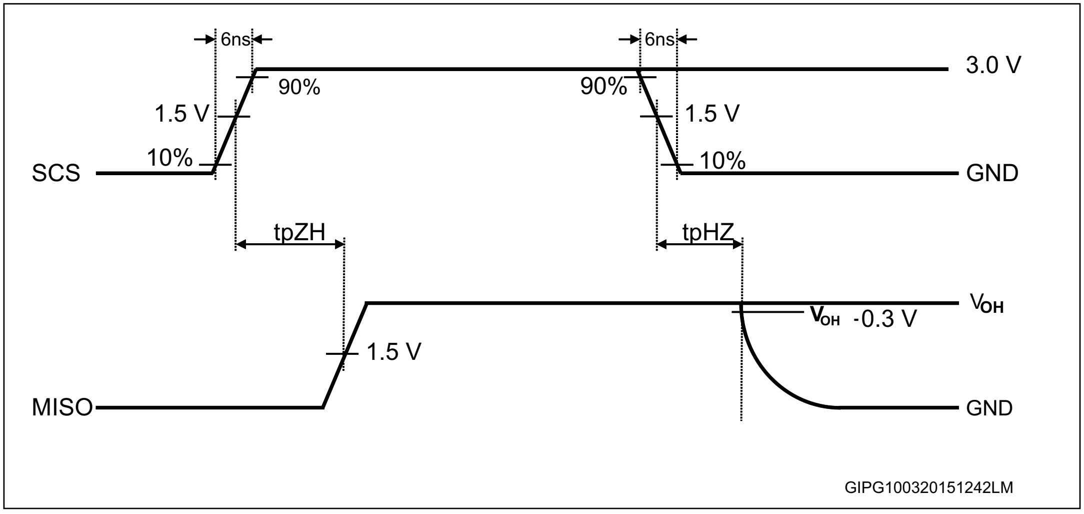
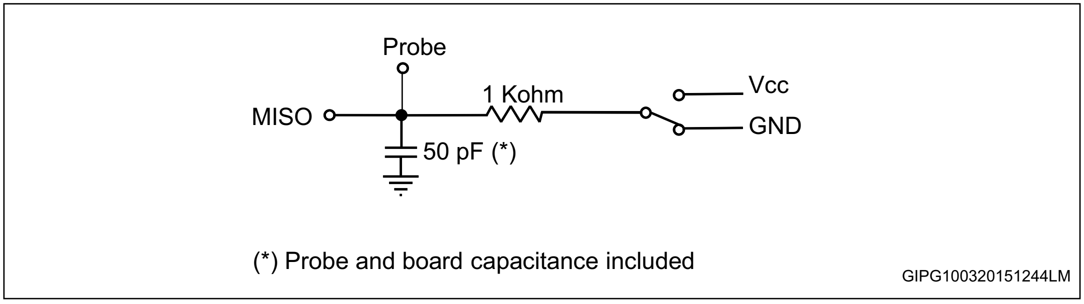


Figure 10. Output load circuit for enable and disable times



Pin programmability

Table 6. Programmable pin functions

Name	Multiplexed function	Functional description	I/O
CLKOUT/ZCR	System clock signal	Clock signals (*DCLK, SCLK, MCLK, CLKIN*)	Output
	Zero-crossing	Line voltage/current zero-crossing	
LED1	Programmable pulse 1	Primary channel energies (A, AF, R, S)(1)	Output
		Secondary channel energies (A, AF, R, S)	
		Primary ± secondary channel energies (A, AF, R, S)	
	SD out current (DATI1)	Sigma-delta bitstream of primary current channel	
LED2	Programmable pulse 2	Primary channel energies (A, AF, R, S)	Output
		Secondary channel energies (A, AF, R, S)	
		Primary ± secondary channel energies (A, AF, R, S)	
	SD current (DATI2)	Sigma-delta bitstream of secondary current channel	
INT1	Interrupt	Programmable interrupt 1	Output
	SD voltage (DATV1)	Sigma-delta bitstream of primary voltage	
INT2	Interrupt	Programmable interrupt 2	Output
	SD out voltage (DATV2)	Sigma-delta bitstream of secondary voltage	
SCS	SPI/UART select	Serial port selection at power-up	Output
	Chip-select	SPI/UART chip-select	
MOSI/RXD	SPI master OUT slave IN	SPI	Input
	UART RX	UART	
MISO/TXD	SPI master IN slave OUT	SPI	Output
	UART TX	UART	

1. A: active wideband; AF: active fundamental; R: reactive; S: apparent.

5 Typical application example

Figure 11 below shows the reference schematic of an application with the following properties:

- Constant pulses C_P = 41600 imp/kWh
- I_{NOM} = 5 A
- I_{MAX} = 90 A

Typical values for current sensor sensitivity are indicated in *Table 7*.

For more information about the application dimensioning and calibration please refer to *Section 9 on page 78*.

Figure 11. STPM34 application schematic

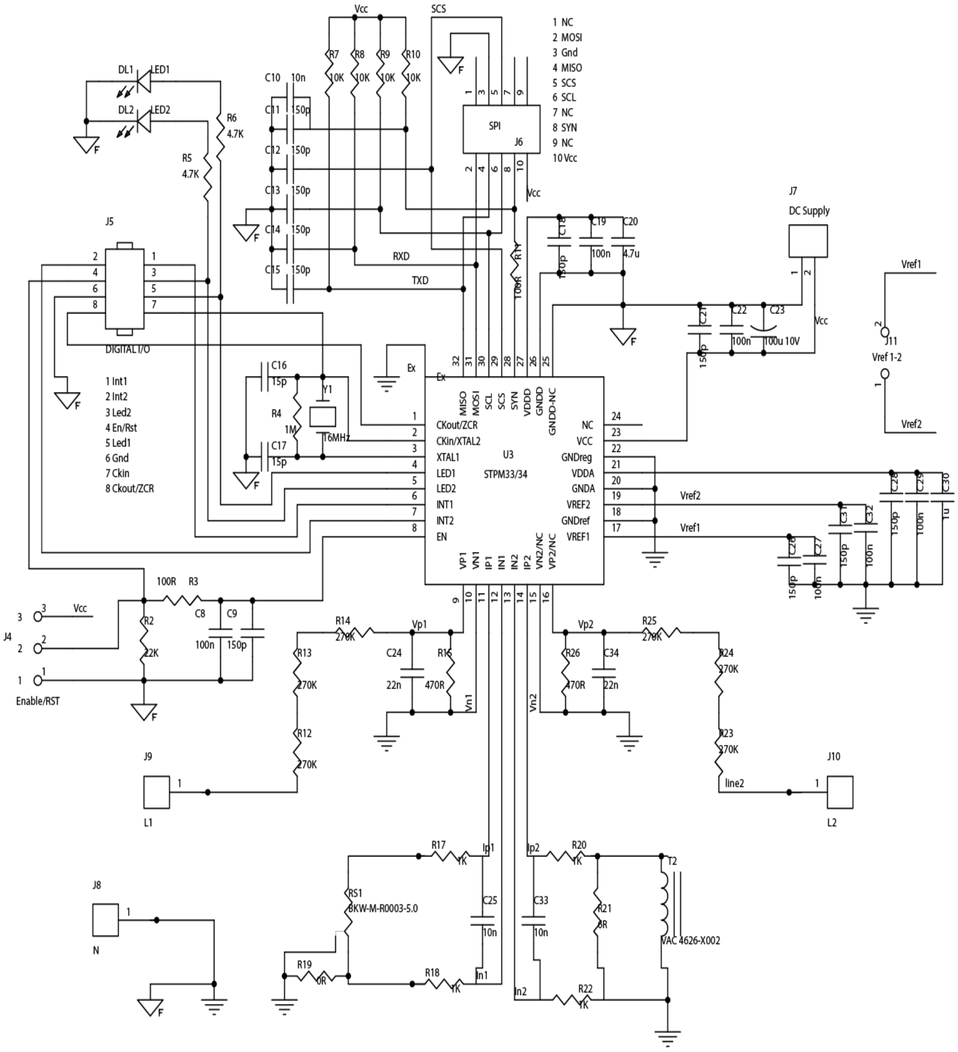


Table 7. Suggested external components in metering applications

Function	Component	Description	Value	Tolerance		Unit
Line voltage interface	Resistor divider	R to R ratio V_{RMS} = 230 V	1:1650	± 1%	50 ppm/°C	V/V
		R to R ratio V_{RMS} = 110 V	1:830			
Line current interface	Rogowski coil	Current to voltage ratio k_S	0.15	± 5%	50 ppm/°C	mV/A
	CT		2.4	± 5%		
	Shunt		0.3	± 5%		

Note: Above listed components refer to typical metering applications. The STPM3x operation is not limited to the choice of these external components.

6 Terminology

6.1 Conventions

The lowest analog and digital power supply voltage is named GND and represents the system ground. All voltage specifications for digital input/output pins are referred to GND. The highest power supply voltage is named V_{CC}. The highest core power supply is internally generated and is named V_{DDA}. Positive currents flow to a pin. Sinking current means that the current is flowing to the pin and it is positive. Sourcing current means that the current is flowing out of the pin and it is negative. A positive logic convention is used in all equations.

Table 8. Convention table

Type	Convention	Example
Pins	All capitals	VDDA
Internal signal	All capitals are italic	*VDDA*
Configuration bit	All capitals are underlined	<u>ROC1</u>
Register name	All capitals are bold	**DSP_CR1**

6.2 Measurement error

The power measurement error is defined by the following equation:

Equation 1

$$e\% = \frac{\text{measuredpower} - \text{truepower}}{\text{truepower}}$$

All measurements come from the comparison with a higher class power (0.02% error) meter reference. Output bitstream of modulator is indicated as *bsV* and *bsC* for voltage and current channel respectively.

6.3 ADC offset error

This is the error due to DC component associated with the analog inputs of the A/D converters. Due to the internal automatic DC offset cancellation, the STPM3x measurement is not affected by DC components in voltage and current channel. DC offset cancellation is implemented in DSP thanks to a dedicated HPF.

6.4 Gain error

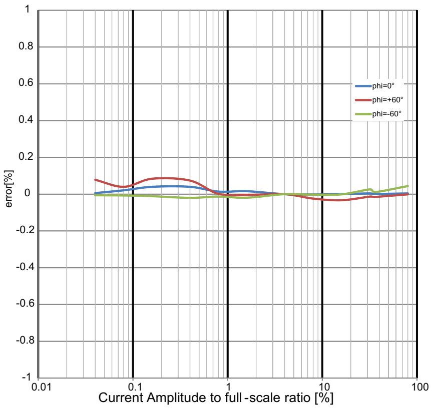
The gain error is due to the signal channel gain amplifiers. This is the difference between the measured ADC code and the ideal output code. The difference is expressed as percentage of the ideal code.

7 Typical performance characteristics

Active energy error is measured at T= 25 °C, over phi (0°, 60°, -60°).

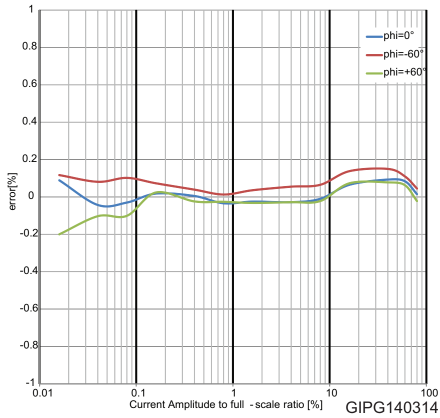
Reactive energy error is measured at T= 25 °C, over phi (90°, -90°, 60°, -60°).

Figure 12. Active energy error vs. current gain=2x integrator off



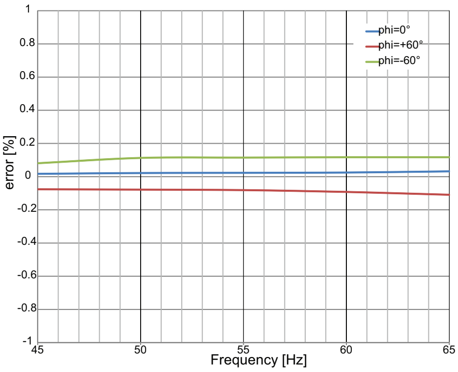
GIPG1403141112LM

Figure 13. Active energy error vs. current gain=16x integrator off



GIPG1403141120LM

Figure 14. Active energy error vs. frequency gain=2x integrator off



GIPG1403141123LM

Figure 15. Active energy error vs. frequency gain=16x integrator off

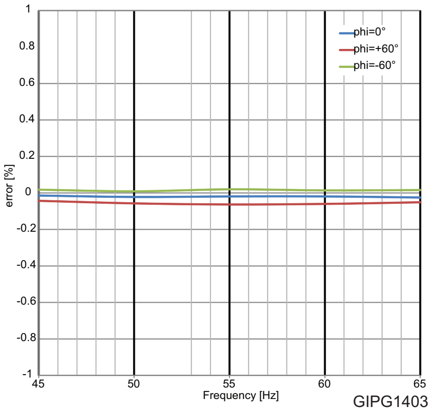


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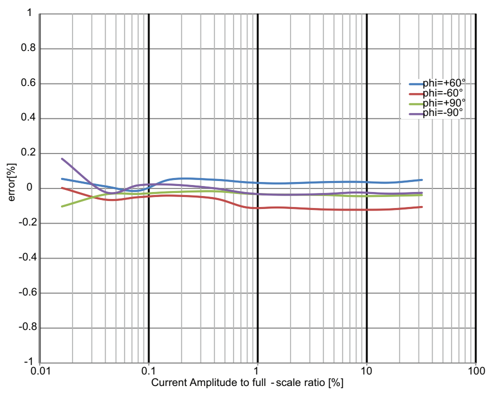
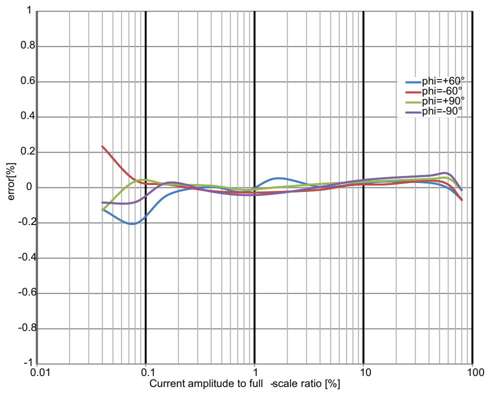
Figure 16. Reactive energy error vs. current gain=2x integrator off



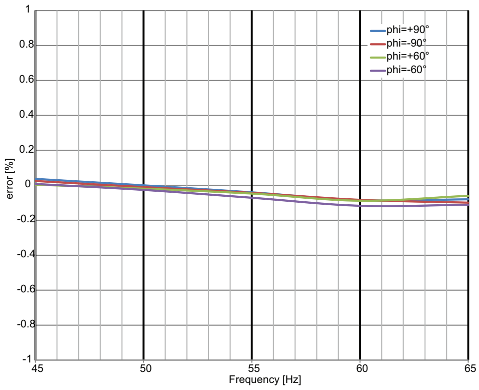
GIPG1403141132LM

Figure 17. Reactive energy error vs. current gain=16x integrator off



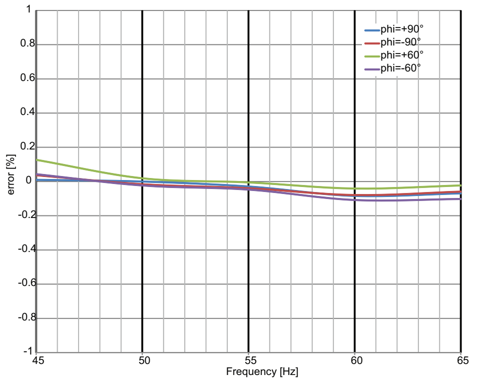
GIPG1403141135LM

Figure 18. Reactive energy error vs. frequency gain=2x integrator off



GIPG1403141137LM

Figure 19. Reactive energy error vs. frequency gain=16x integrator off



GIPG1403141141LM

Figure 20. Active energy error vs. current gain=16x integrator on

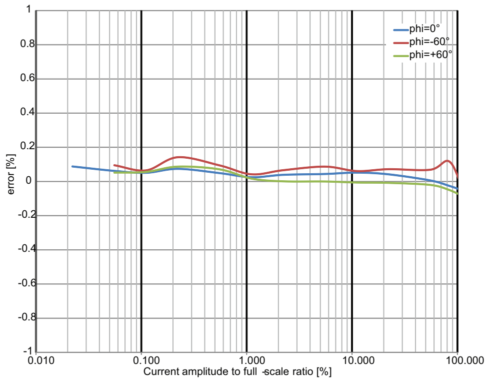


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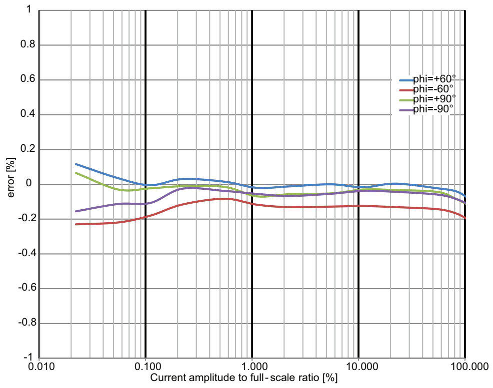
Figure 21. Reactive energy error vs. current gain=16x integrator on



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8 Theory of operation

8.1 General operation description

The STPM3x product family measures up to two line voltages and two line currents to perform active, reactive and apparent power and energy, RMS and instantaneous values, and line frequency information measurement of a single, split or poly-phase metering system.

The STPM3x generates up to two independent train pulse output signals proportional to the active, reactive, apparent or cumulative power. It also generates up to two programmable interrupt output signals.

The internal register map and the configuration registers can be accessed by SPI or UART interface.

The STPM3x converts analog signals, through four independent channels in parallel via sigma-delta analog-to-digital converters, into a binary stream of sigma-delta signals with the appropriate not overlapped control signal generator.

This technique fits to measure electrical line parameters (voltage and current) via analog signals from voltage sensors and current sensors (inductive Rogowski coil, current transformer or shunt resistors). Current channel inputs are connected, through external anti-aliasing RC filter, to a Rogowski coil or current transformer (CT) or shunt current sensor which converts line current into the appropriate voltage signal. Each current channel includes a low-noise voltage preamplifier with a programmable gain. Voltage channels are connected to a line voltage modulator (ADC). All channels have quiescent zero signal point on GND, so the STPM3x samples differential signals on both channels with their zero point around GND.

The converted sigma-delta signals feed an internal decimation filter stage that decimates 4 MHz bitstreams of a factor 512 allowing a 3.6 kHz bandwidth at -3 dB. The 24-bit voltage and current data feed an internal configurable filtering block and the hardwired DSP that performs the final computation of metrology quantities.

The STPM3x also includes two programmable temperature compensated bandgap reference voltage generators and low drop supply voltage regulator. All reference voltages are designed to eliminate the channel crosstalk.

The mode of operation and configuration of the device can be selected by dedicated configuration registers.

8.2 Functional description of the analog part

The analog part of the STPM3x consists of the following sections:

- Power management section:
  - Reference voltage generators with programmable independent temperature compensation
  - +3 V low drop supply voltage regulator
  - +1.2 V low drop supply voltage regulator
- Analog front end section:
  - Preamplifiers in the two current channels
  - 2nd order sigma-delta modulators
- Clock generator
- Power-on-reset (POR)

8.2.1 Power management section

Supply pins for the analog part are: VCC, VDDA, VDDD and GND.

GND pins represent the reference point.

VCC pin is the power supply input namely +3.3 V to GND_REG, it has to be connected to GND_REG via a 1 µF capacitor.

VDDA and VDDD are analog output pins of internal +3.0 V and +1.2 V low drop voltage regulators.

At least 1 µF capacitor should be connected between VDDA and GNDA. At least 1 µF (better 4.7 µF) capacitor should be connected between VDDD and GNDD. The input of the mentioned regulators is VCC.

There are two voltage references embedded in the STPM33 and STPM34, while the STPM32 embeds a single reference.

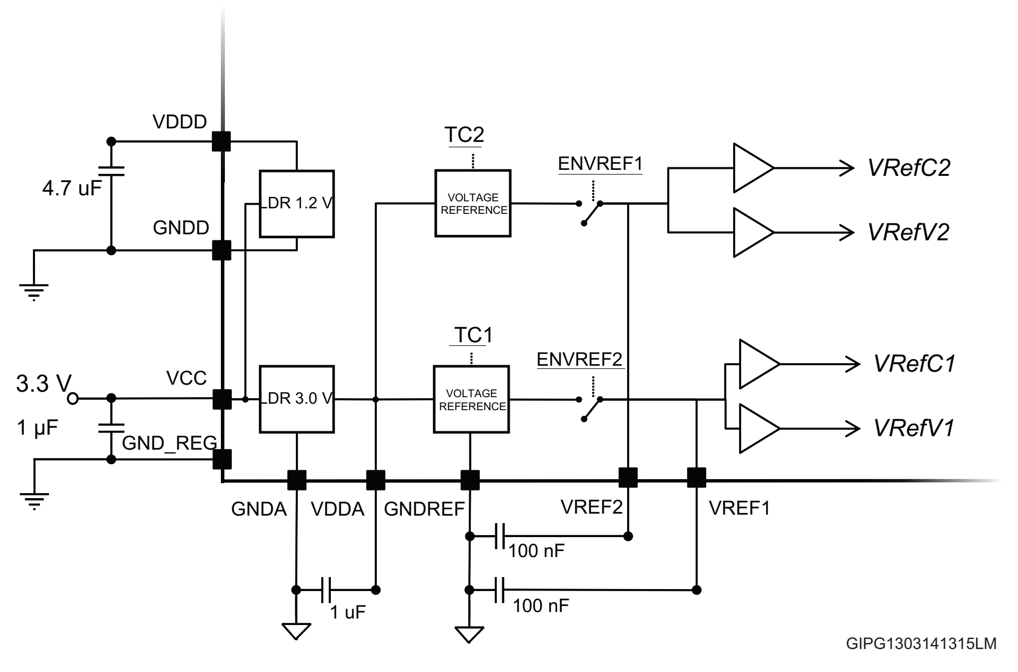
It is possible to switch off each reference voltage and each voltage or current channel independently for power saving purpose.

EN_REF1 and EN_REF2 bits in **DSP_CR1** and **DSP_CR2** switch on/off the voltage reference.

To disable a single voltage or current channel, enV1, enC1 bits for primary channel and enV2, enC2 for secondary channel should be cleared in **DFE_CR1** and **DFE_CR2** respectively. Switching off some channels allows an operating current reduction as reported in *Table 5 on page 17*.

As described in *Figure 22*, two EN_REF1 and EN_REF2 bits enable the voltage references; if a unique voltage reference is used, one of these two bits must be disabled and VREF1 and VREF2 pins must be shorted; if an external reference is used both bits must be disabled and the external reference must be connected to VREF1, VREF2 pins. VREF1 and VREF2 outputs should be connected to GNDREF via a 100 nF capacitor independently.

Figure 22. Power management internal connection scheme and polarization



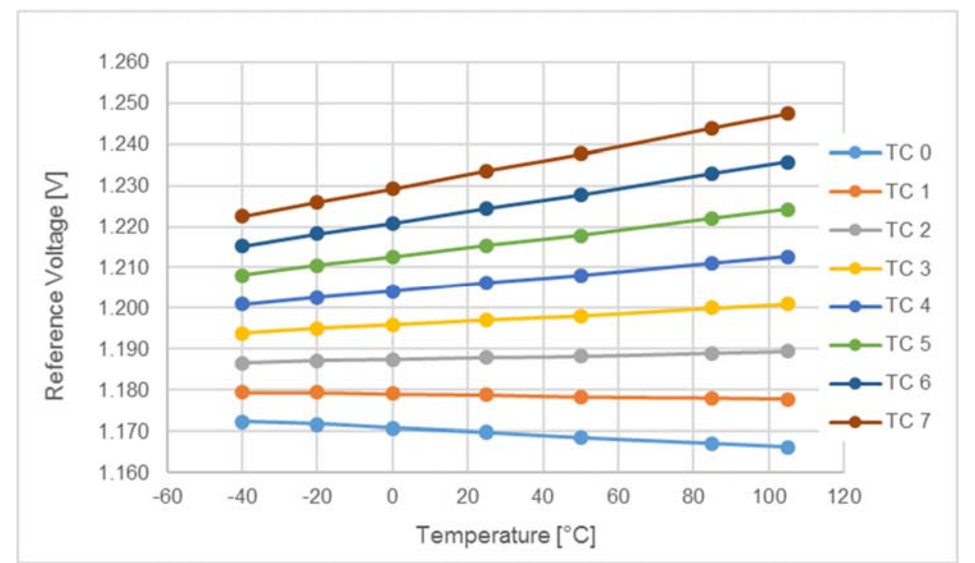
Temperature compensated reference voltage generators produce VREF1 = VREF2 = 1.18 V at default settings. The primary voltage reference is always on and supplies the voltage and the primary current channel, the secondary voltage reference is by default in on-state and supplies the secondary channel.

These reference temperature compensation curves can be selected through three configuration bits: TCx[2:0] (**DSP_CR1** and **DSP_CR2**).

Table 9. Temperature compensation selection

TCx0	TCx1	TCx2	TC_V_{REF} (ppm/°C)
0	0	0	-30
0	0	1	0
0	1	0	30 (default)
0	1	1	60
1	0	0	90
1	0	1	120
1	1	0	150
1	1	1	180

Figure 23. Temperature compensation typical curves



8.2.2 Analog front end

Analog channel inputs of voltages VIP1, VIN1, VIP2, VIN2 and currents IIP1, IIN1; IIP2, IIN2 are fully differential.

Voltage channels have a preamplification gain of 2, which defines the maximum differential voltage on voltage channel inputs to ± 300 mV.

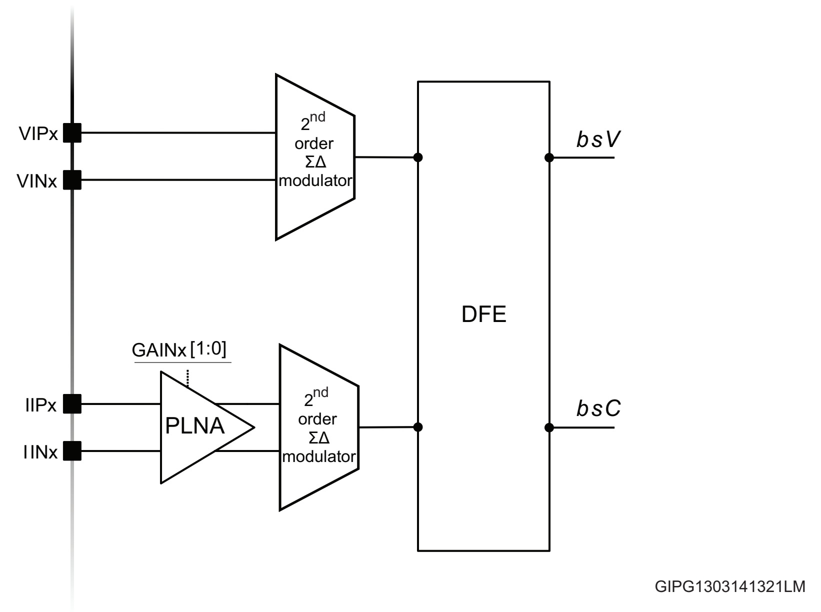
Current channels have a programmable gain selectable among 2, 4, 8 and 16, which defines the maximum differential voltage on current channel to ± 300 mV, 150 mV, 75 mV or ± 37.5 mV respectively. The selection is given by GAINx[1:0] (**DFE_CR1**, **DFE_CR2**) bits as described in *Table 10*.

Table 10. Current channel input preamplifier gain selection

GAINx0	GAINx1	Gain	Differential input
0	0	X2	± 300 mV
0	1	X4	± 150 mV
1	0	X8	± 75 mV
1	1	X16	± 37.5 mV

The oversampling frequency of the modulators is 4 MHz, the output bitstreams of the 2nd order sigma-delta modulators relative to the voltage and to the two current channels are available on INT and LED output pins through the proper configuration (see configuration bit map).

Figure 24. Analog front end internal scheme



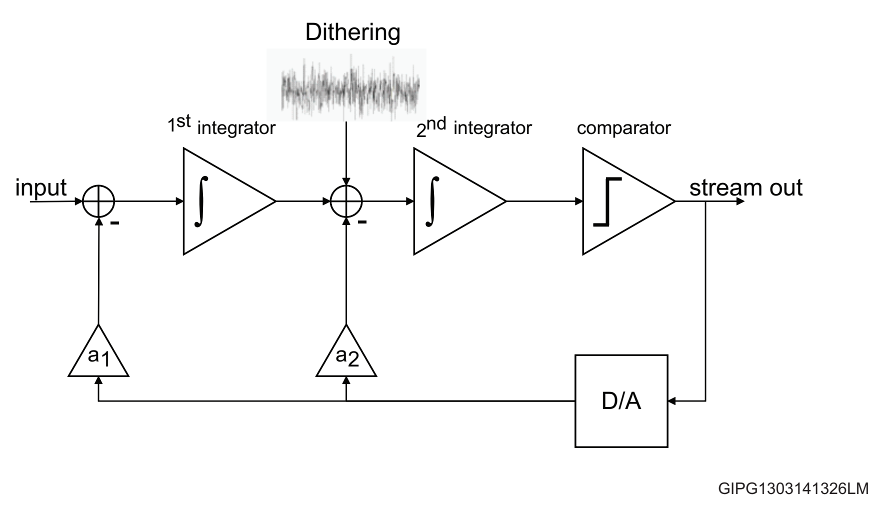
PLNA uses the chopping technique to cancel the intrinsic offset of the amplifier.

A dedicated block generates chopper frequencies for voltage and current channels.

The amplified signals are fed to the 2nd order sigma-delta modulator.

The analog-to-digital conversion in the STPM3x is carried out using four 2nd order sigma-delta converters. A pseudo-random block generates pseudo-random signals for voltage and current channels. These random signals implement the dithering technique in order to de-correlate the output of the modulators and avoid accumulation points on the frequency spectrum. The device performs A/D conversions of analog signals on four independent channels in parallel.

Figure 25. Block diagram of the modulator



The sigma-delta modulators convert the input signals into a continuous serial stream of “1” and “0” at a rate determined by the sampling clock. In the STPM3x, the oversampling clock is equal to 4 MHz.

1-bit DAC in the feedback loop is driven by the serial data stream. DAC output is subtracted from the input signal and from the integrated error. If the loop gain is high enough, the average value of DAC output (and therefore the bitstream) can approach to the input signal level. When a large number of samples are averaged, a very precise value of the analog signal is obtained. This average is described in DSP section.

The converted sigma-delta bitstreams of voltage and current channels are fed to the internal hardwired DSP unit, which decimates, filters and processes those signals in order to boost the resolution and to yield all necessary signals for computations.

8.2.3 Clock generator

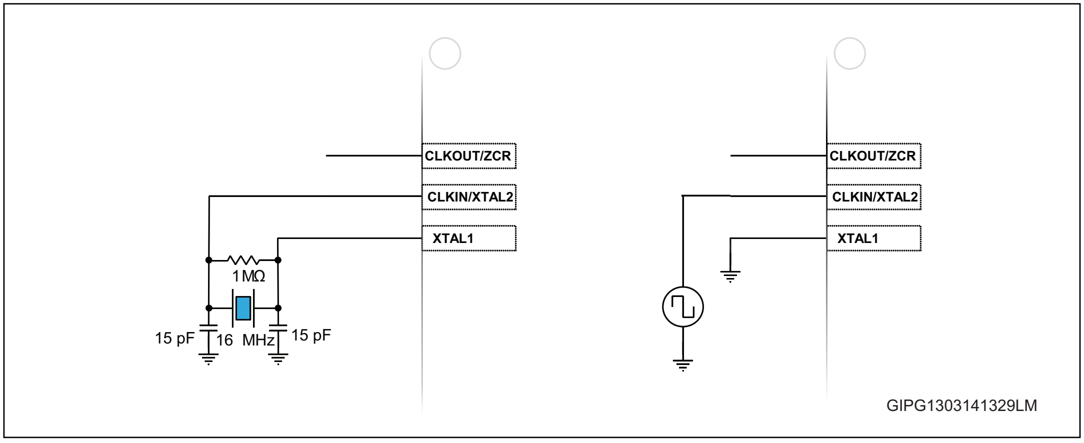
All the internal timing of the STPM3x is based on the input clock signal, namely 16 MHz. This signal can be provided in two different ways:

1. External quartz: the oscillator works with an external crystal
2. External clock: the XTAL2 pin can be fed by an external 16 MHz clock signal

For specific features of crystal oscillator or CLKIN signal please refer to *Table 5*.

The clock generator is powered by the analog supply and is responsible for two tasks. The former delays the turn-on of some function blocks after POR in order to help a smooth start of external power supply circuitry by keeping off all major loads. The latter provides all necessary clocks for analog and digital parts.

Figure 26. Different oscillator circuits (a): with quartz; (b): with external source



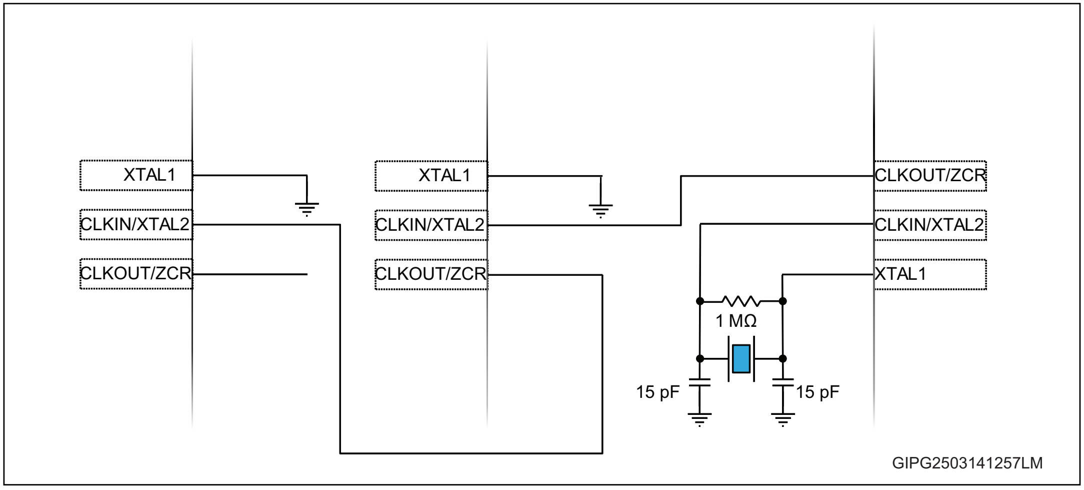
From the external 16 MHz clock, the entire clock tree is generated. All internal clocks have 50% duty cycle.

Table 11. Clock tree

CLK name	Name	Typical value	Description
Input clock	*CLKIN*	16 MHz	External clock
Master clock	*MCLK*	4 MHz	Master root clock
Analog sampling clock	*SCLK*	4 MHz	OSF of sigma-delta modulators
Decimated clock	*DCLK*	7.8125 kHz	Sampling frequency of instantaneous voltage and current values

CLKOUT pin can be used to feed another STPM3x device clock with 16 MHz, when multiple STPM3x are used in cascade as shown in *Figure 27*.

Figure 27. Clock feed for multiple devices

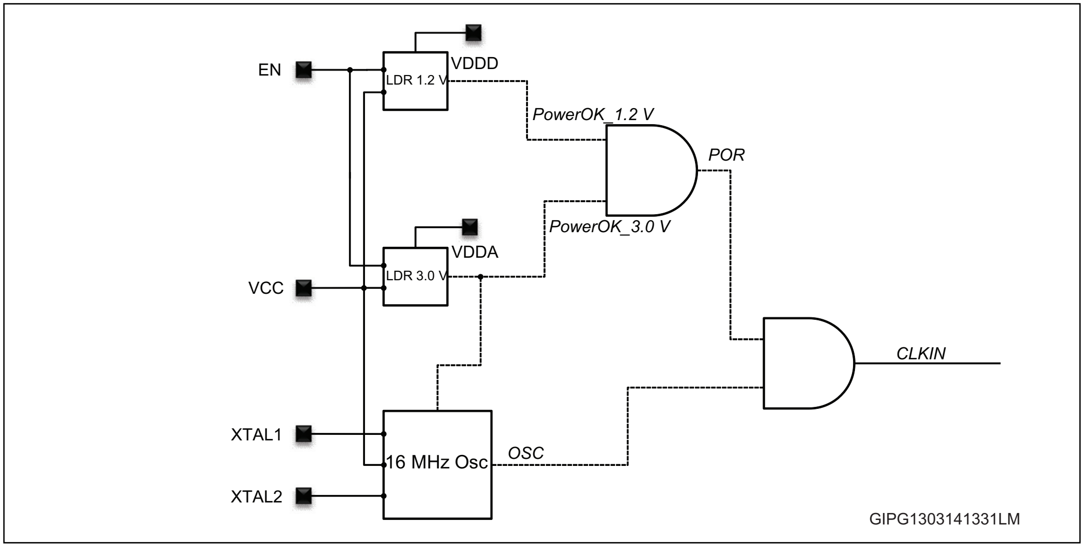


8.2.4 Power-on-reset (POR) and enable (EN)

The STPM3x contains a power-on-reset (POR) circuit which delays the startup of the digital domain about 750 µs. If VCC supply is less than 2.5 V the STPM3x goes to the inactive state, all functions are blocked asserting a reset condition. This is useful to assure the correct device operation during the power-up and power-down.

POR sequence is illustrated in *Figure 28*: after the start of two LDOs and internal *PowerOK* signals are asserted, the analog block first and the digital block after start the processing.

Figure 28. Power-on-reset sequence

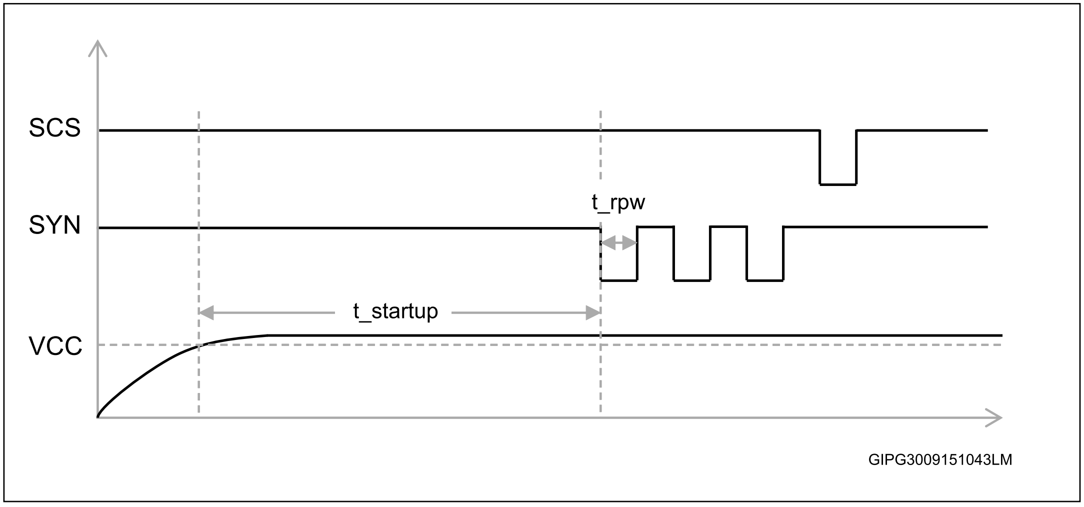


The STPM3x also has an enable pin (EN) which works as follows:

- EN is high: when the power is on and EN pin raises, the device is enabled and starts after POR procedure as above described.
- EN is low: when the power is on and EN pin has a transition high to low, the device is disabled. It stops and the internal digital memory is deleted so a new initialization is needed when EN goes back to high.

After POR, to ensure a correct initialization, it is necessary to perform a reset of DSP and communication peripherals through three SYN pulses (see *Section 8.6.1 on page 68*) and a single SCS pulse, as shown in the figure below. SCS pulse can be performed before or after SYN pulses, but minimum startup time before reset (as indicated in *Table 5 on page 17*) has to be respected.

Figure 29. Global startup reset



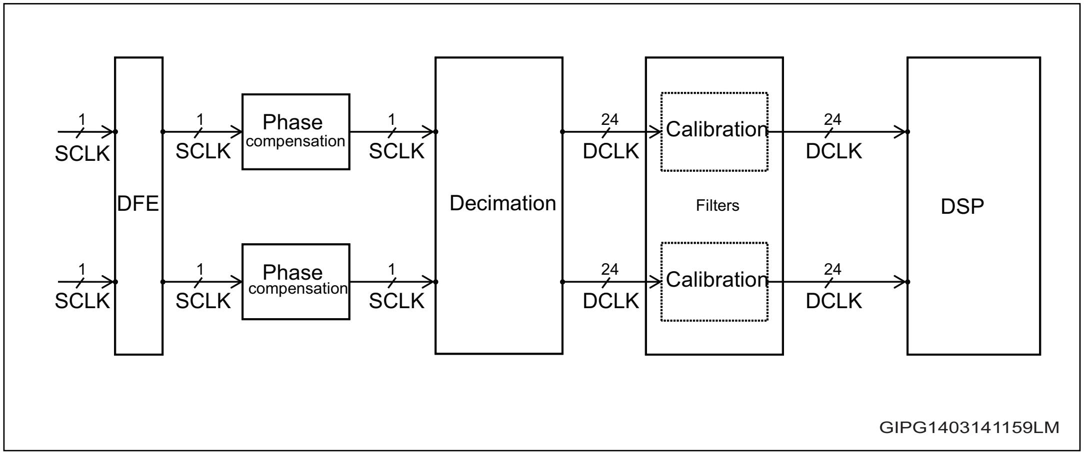
8.3 Functional description of the digital part

Each voltage and current channel has an independent digital signal processing chain, which is composed of:

- Digital front end (DFE)
- Phase compensation
- Decimation
- Filters
- Calibration

The outcoming signals are fed to a common hardwired DSP, which processes the metrology data.

Figure 30. DSP block functional description



8.3.1 Digital front end (SDSx bits)

This block synchronizes and checks the sigma-delta bitstreams of voltage and current signals.

Each channel sigma-delta stream has an SDSx status bit associated, which is cleared if the stream is correct, while it is set if the bitstream is stuck to 0 or 1 (this is the case of an input waveform saturating the dynamic input of the sigma-delta modulator).

To set SDSx bit, sigma-delta (ΣΔ) stream should be stuck to 0 or 1 for a time between:

$t_{\Sigma\Delta stuck} = 2/(MCLK/256) = 128\ \mu s \ldots t_{\Sigma\Delta stuck} = 3/(MCLK/256) = 192\ \mu s$.

Outputs are stored on bit number: 20, 24 of **DSP_SR1,2** and 13, 20 of **DSP_EV1,2**.

If SDSx=1, the instantaneous values of voltage current are set on positive or negative maximum value, according to sigma-delta stream. In this case active powers and energies are calculated with those values of signals.

If sigma-delta stream of voltage channel is stuck, the reactive energy is zero.

8.3.2 Decimation block

The decimation block operates a serial decimation of three sigma-delta serial bitstreams coming from three modulators of voltage, primary and secondary current channels.

The decimation ratio, out of the filter cascade, is 512 so that outputs of this block are parallel 24-bit data at a rated frequency of 7.8125 kHz.

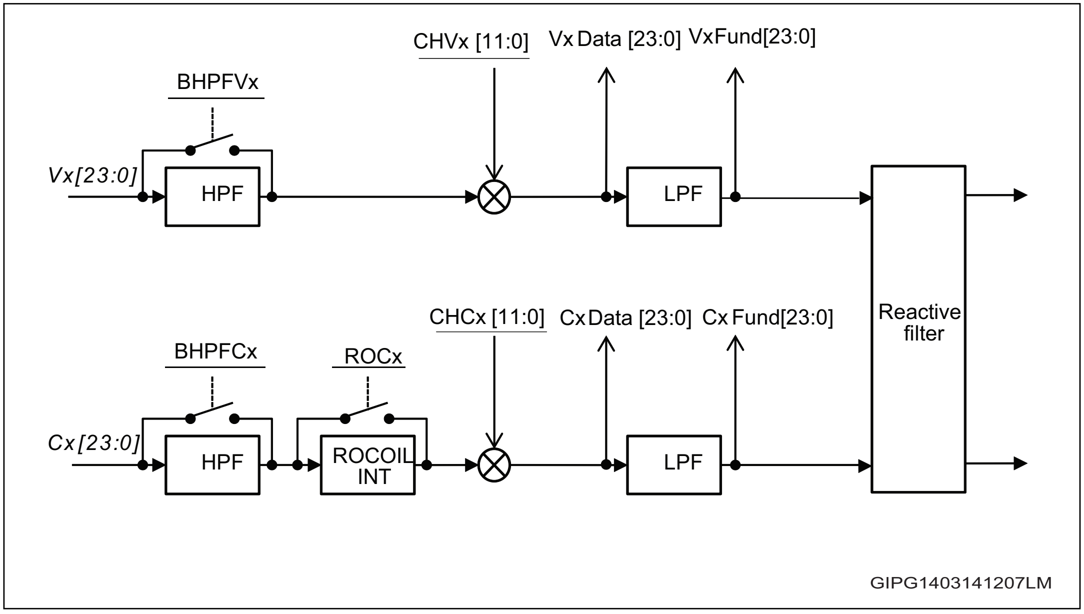
The decimation block has a magnitude response -3 dB band of 3.6 kHz and a 2.0 kHz flat band.

8.3.3 Filter block

The block includes:

- DC cancellation filter (BHPFVx, BHPFCx bits)
- Rogowski coil Integrator (ROCx bit)
- Fundamental harmonic component filter

Figure 31. Filter block diagram



8.3.4 DC cancellation filter

This block removes the DC component of signal from voltage and current signals.

It is a selectable block which can be bypassed in case of particular needs with BHPFVx and BHPFCx bits in **DSP_CR1** and **DSP_CR2**.

The filter has a passband at -3 dB of 8 Hz

BHPFVx = 0: voltage HPF is included for x channel

BHPFVx = 1: voltage HPF is bypassed for x channel

BHPFCx = 0: current HPF is included for x channel

BHPFCx = 1: current HPF is bypassed for x channel

Rogowski coil Integrator

ROCx bit in **DSP_CR1** and **DSP_CR2** selects the type of current sensors (CT, shunt or Rogowski coil):

ROCx = 0: channel x current sensor is CT or shunt

ROCx = 1: channel x current sensor is Rogowski coil

In case of ROCx = 1, integrator filter is included to integrate current signal coming from Rogowski coil current sensor. Rogowski coil integrator is selectable independently for each current channel.

8.3.5 Fundamental component filter

This low-pass filter on the voltage and current signals is used to calculate: zero-crossing, period, phase-angles and fundamental active and reactive energy. Filtered voltage and current components are available on **DSP_REG6**, **DSP_REG7**, **DSP_REG8**, **DSP_REG9** named *VxFund* and *CxFund*.

8.3.6 Reactive filter

Reactive filter introduces a delay in current and voltage streams respectively; these signals are used to calculate reactive power and energy.

Input streams for reactive filter are *VxFund* and *CxFund* signals.

8.4 Functional description of hardwired DSP

From the decimation and filtering block, signals are fed to hardwired DSP to compute the following quantities for primary and secondary channels:

- Active power and energy wideband 0 Hz(4 Hz) -3.6 kHz
- Active power and energy fundamental 45 - 65 Hz
- Reactive power and energy
- Apparent power and energy from RMS data
- Apparent power vectorial calculation
- Signal measurement: RMS, period, zero-crossing, phase-delay, sag and swell, tamper

Each power signal is accumulated in the correspondent energy register every 7.8125 kHz.

Energy registers are up-down counters. The accumulation is signed so that the negative energy is subtracted from the positive energy. When the measured power is positive, the energy register increases its content from 0x00000000 up to the maximum value, 0xFFFFFFFF, then it rolls from 0xFFFFFFFF back to 0x00000000.

Vice versa, when the power is negative, the register decreases its content; from 0x00000000 rolls to 0xFFFFFFFF and continues decreasing till 0x00000000.

To monitor each energy register overflow and power sign, status bits are available on **DSP_SR1** and **DSP_SR2**.

When an energy threshold is reached, a pulse is generated on LED pin.

This pulse is generated by monitoring two consecutive bits of the energy register: the LED signal goes high when the two selected bits commute to 01 and goes low when the bits change to 11.

The configuration bits LPWx[3:0] in **DSP_CR1** and **DSP_CR2** shift the default bits for pulse generation, thus changing the default pulse frequency of a given factor, indicated in *Table 12* for each configuration value. Maximum LED pulse width is anyway fixed to 81.92

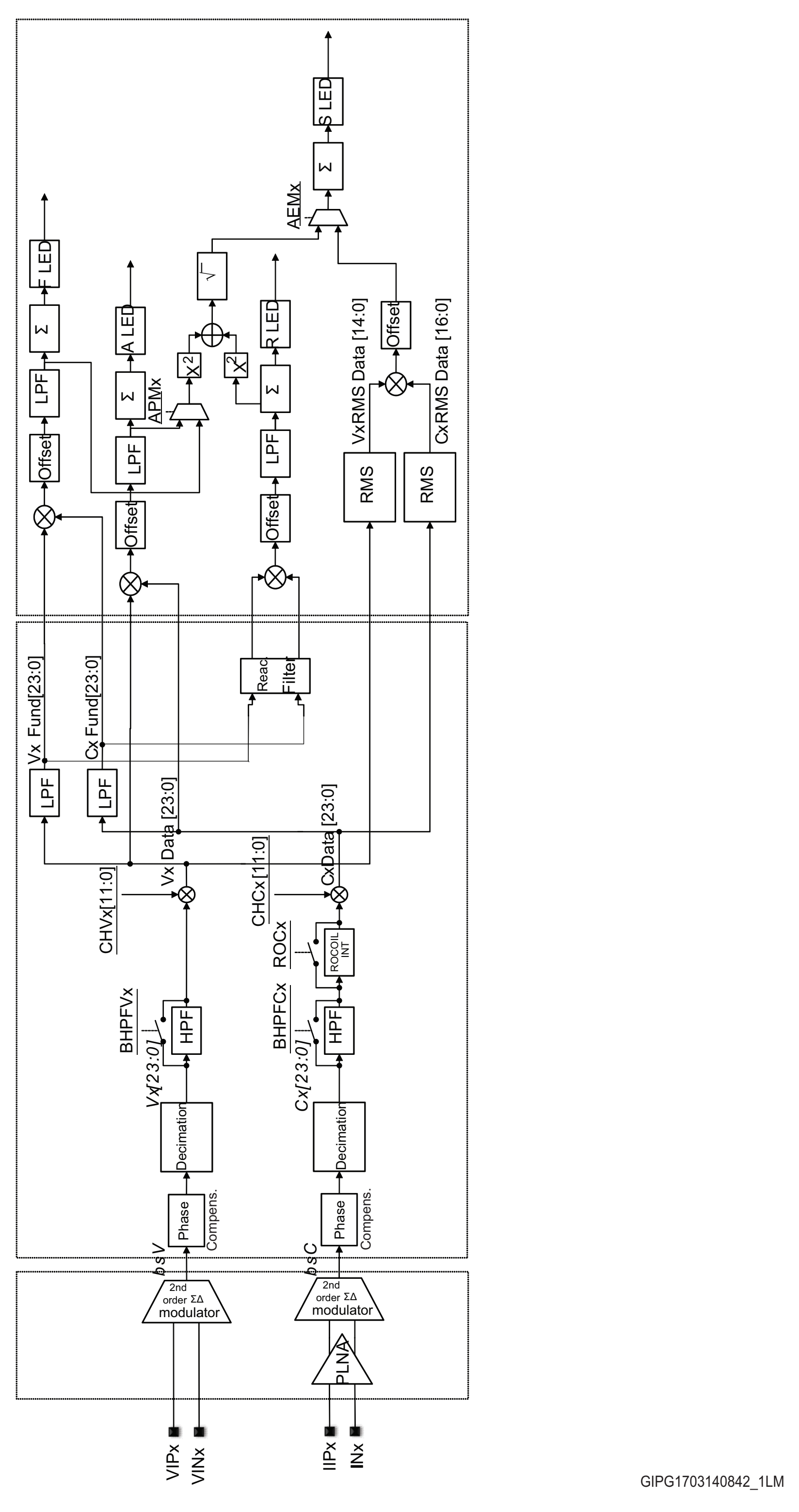
ms (640 periods of 7812.5 Hz clock).

Table 12. LPWx bits

LPWx	LED_PWM
0000	0.0625
0001	0.125
0010	0.25
0011	0.5
0100	1
0101	2
0110	4
0111	8
1000	16
1001	32
1010	64
1011	128
1100	256
1101	512
1110	1024
1111	2048

The signal chain for each power, energy calculations and related frequency conversion are explained in the following section.

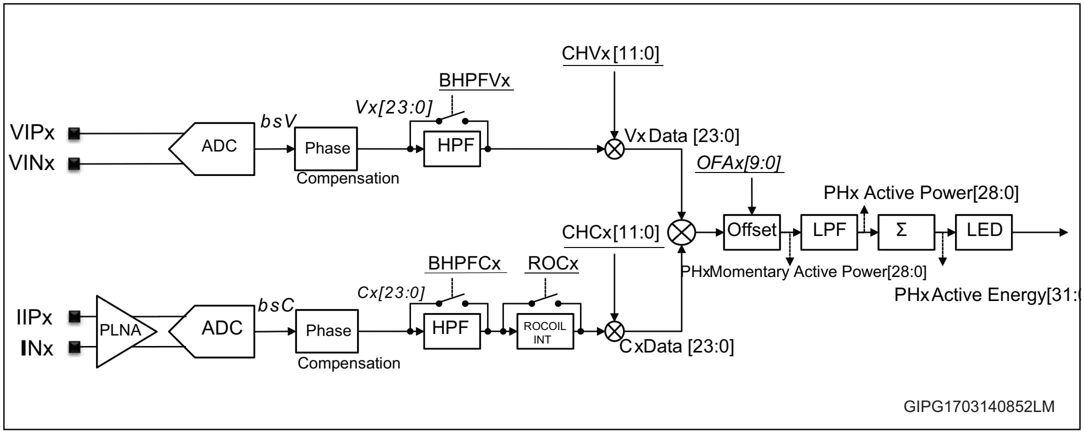
Figure 32. DSP block diagram



8.4.1 Active power and energy calculation

The signal chain for the active power, energy calculations and related frequency conversion are shown in *Figure 33*. The instantaneous power signal *p(t)* is generated by multiplying the current and voltage signals. This value can be compensated by the active power offset calibration block (OFAx[8:0] in **DSP_CR9** and **DSP_CR11** registers). DC component of the instantaneous power signal (average power) is then extracted by LPF (low-pass filter) to obtain the active power information.

Figure 33. Active power and energy calculation block diagram



The active power is calculated simultaneously and independently for primary and secondary current channels.

Results of the calculated quantities are stored in the registers as follows:

EP_1 = primary current channel active energy PH1 ACTIVE Energy[31:0]

P_1 = primary current channel active power PH1 Active Power[28:0]

$p_1(t)$ = primary current channel instantaneous active power PH1 Momentary Active Power[28:0]

EP_2 = secondary current channel active energy PH2 Active Energy[31:0]

P_2 = secondary current channel active power PH2 Active Power[28:0]

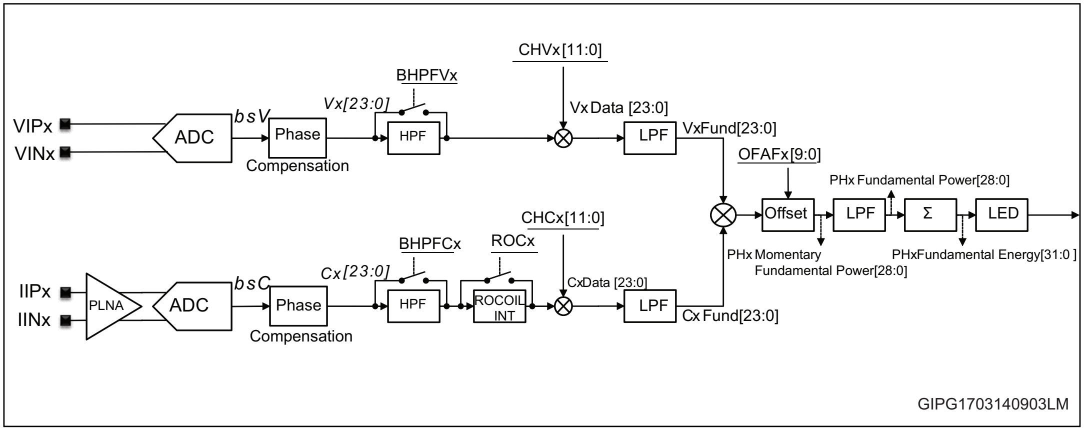
$p_2(t)$ = secondary current channel instantaneous active power PH2 Momentary Active Power[28:0]

Active power measurements have a bandwidth of 3.6 kHz and include the effects of any harmonic within that range.

8.4.2 Fundamental active power and energy calculation

The signal chain for the fundamental active power, energy calculations and related frequency conversion are shown in *Figure 34*. The signal flow is the same as the active energy wideband, but voltage and current waveforms are filtered to remove all harmonic components but the first (45 - 65 Hz). Power value can be compensated by the active power offset calibration block (OFAFx[8:0] in **DSP_CR9** and **DSP_CR11**).

Figure 34. Fundamental active power and energy calculation block diagram



Results of the calculated quantities are stored in the registers as follows:

EF_1 = primary current channel active fundamental energy PH1 Fundamental Energy[31:0]

F_1 = primary current channel active fundamental Power PH1 Fundamental Power[28:0]

$f_1(t)$ = primary current channel instantaneous active fundamental power PH1 Momentary Fundamental Power[28:0]

EF_2 = secondary current channel active fundamental energy PH2 Fundamental Energy[31:0]

F_2 = secondary current channel active fundamental power PH2 Fundamental Power[28:0]

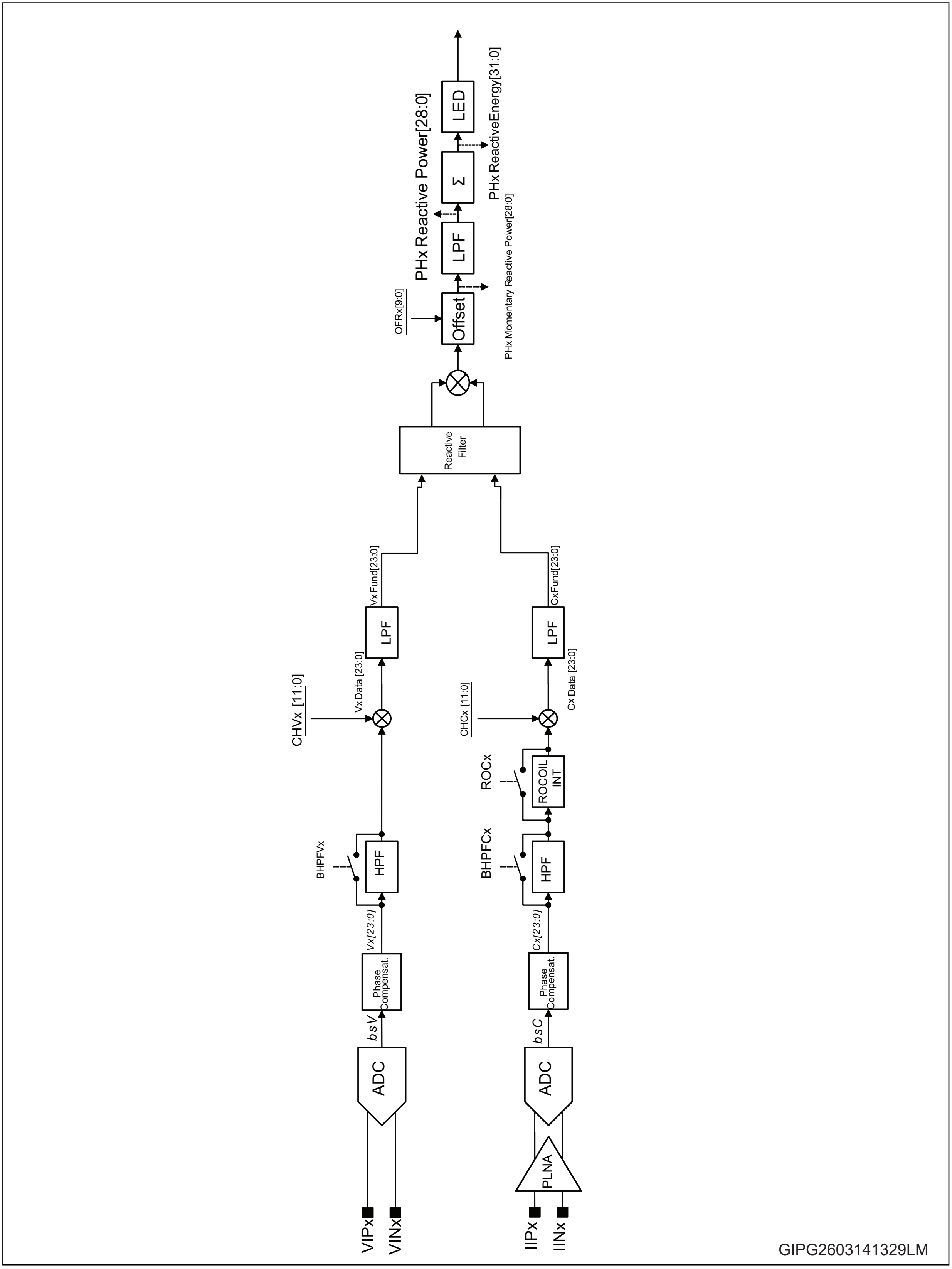
$f_2(t)$ = secondary current channel instantaneous active fundamental power PH2 Momentary Fundamental Power[28:0]

The fundamental active power measurements have a bandwidth of 80 Hz.

8.4.3 Reactive power and energy calculation

The signal chain for the reactive power, energy calculations and related frequency conversion are shown in *Figure 35*. The instantaneous reactive power signal is generated by multiplying the filtered signals of current and voltage. This value can be compensated by the reactive power offset calibration block (OFRx[8:0] in **DSP_CR10** and **DSP_CR12**). The DC component of the instantaneous power signal is extracted from LPF to obtain the reactive power information.

Figure 35. Reactive power and energy calculation block diagram



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Results of the calculated quantities are stored in the registers as follows:

EQ_1 = primary current channel reactive energy PH1 Reactive Energy[31:0]

Q_1 = primary current channel reactive power PH1 Reactive Power[28:0]

$q_1(t)$ = primary current channel instantaneous reactive power PH1 Momentary Reactive Power[28:0]

EQ_2 = secondary current channel reactive energy PH2 Reactive Energy[31:0]

Q_2 = secondary current channel reactive power PH2 Reactive Power[28:0]

$q_2(t)$ = secondary current channel instantaneous active power PH2 Momentary Reactive Power[28:0].

8.4.4 Apparent power and energy calculation

The signal chain for the apparent power, energy calculations and related frequency conversion are shown in *Figure 36*. The apparent power signal S is generated in two ways:

- Vectorial methodology uses the scalar product of active and reactive power. The active power is selectable through the active power mode bit (APMx in **DSP_CR1** and **DSP_CR2**) between wideband or fundamental.

Equation 2

$$S_{vec} = \sqrt{P^2 + Q^2}$$

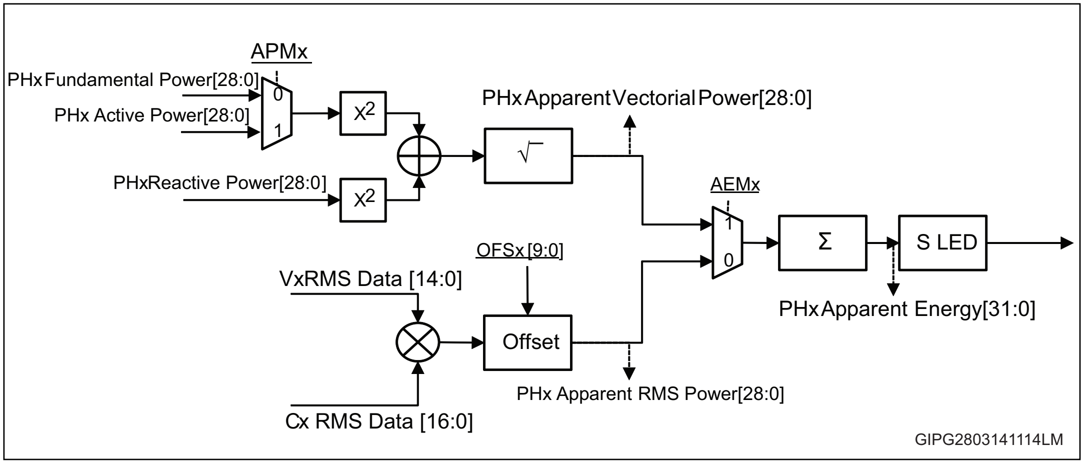
- RMS methodology uses the product of RMS data of voltage and current. This value can be compensated by the apparent power offset calibration block (OFSx[8:0] in **DSP_CR10** and **DSP_CR12**).

Equation 3

$$S_{RMS} = V_{RMS} \cdot I_{RMS}$$

The apparent energy is calculated from vectorial or from RMS apparent power according to AEMx configuration bit in **DSP_CR1** and **DSP_CR2**.

Figure 36. Apparent power and energy calculation block diagram



Results of the calculated quantities are stored in the registers as:

ES_1 = primary current channel apparent energy PH1 Apparent Energy[31:0]

S_{1RMS} = primary current channel apparent RMS power PH1 Apparent RMS Power[28:0]

S_{1vec} = primary current channel apparent vectorial power PH1 Apparent Vectorial Power[28:0]

ES_2 = secondary current channel apparent energy PH2 Apparent Energy[31:0]

S_{2RMS} = primary current channel apparent RMS power PH2 Apparent RMS Power[28:0]

S_{1vec} = primary current channel apparent vectorial power PH2 Apparent Vectorial Power[28:0]

8.4.5 Sign of power

Power measurements are signed calculations. Negative power indicates that energy has been injected into the grid. **DSP_SR1**, **DSP_SR2** status registers and **DSP_EV1**, **DSP_EV2** registers include sign indication bits for each calculated power.

If the sign of power is negative, the sign bit is set.

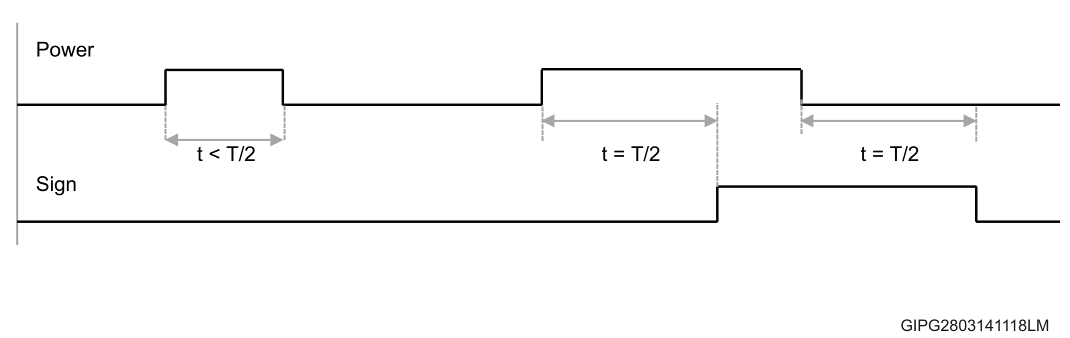
SIGN = 0: positive power

SIGN = 1: negative power

In the calculation of the sign, a delay equal to half line period is included.

If the period of signal is T = 20 ms (f = 50 Hz), the applied delay is 10 ms.

Figure 37. Power sign status bit delay



8.4.6 Calculation of power and energy

In the following section, constant parameters, coming from the device architecture, are used:

Table 13. STPM3x internal parameters

Parameter	Value	
Voltage reference	V_{REF} = 1.18 [V]	
Decimation clock	*DCLK* = 7812.5 [Hz]	
Integrator gain (for Rogowski coil only)	k_{int} = 1	If ROC bit = 0 in **DSP_CR1,2**
	k_{int} = 0.8155773	If ROC bit = 1 in **DSP_CR1,2**

Basic calculations are listed in *Table 14*:

Table 14. STPM3x basic calculations

Parameter	Voltage	Current shunt	Current CT	Current Rogowski coil
Gain	$A_V = 2$	$A_I = 16$	$A_I = 2$	$A_I = 16$
Calibrators(1)	$cal_V = 0.875$	$cal_I = 0.875$		
Sensitivity	$\frac{R_2}{R_1 + R_2}[V/A]$	$k_S = R_{Shunt}\ [\Omega]$	$k_S = \frac{R_b}{N}[V/A]$	$k_S = k_{RoCoil}\ [V/A]$
Voltage at channel inputs	$V_{inV} = \frac{R_2}{R_1 + R_2} \cdot V[V]$	$V_{inC} = k_S \cdot I[V]$		
Integrator gain (for Rogowski coil sensor only)	-	$k_{int} = 1$		$k_{int} = 0.8155773$
ΣΔ bitstream(2)	$V_{\Delta\Sigma} = V_{inV} \cdot \frac{A_V}{V_{ref}}$	$V_{\Delta\Sigma} = V_{inC} \cdot \frac{A_I}{V_{ref}}$		$V_{\Delta\Sigma} = V_{inC} \cdot \frac{A_I}{V_{ref} \cdot K_{int}}$
Input active power	$P_{in} = V \cdot I \cdot \cos\varphi = V \cdot I[W]$			
Active power	$P = V_{\Sigma\Delta} \cdot cal_V \cdot I_{\Sigma\Delta} \cdot cal_C \cdot cos\varphi$			
LED frequency at rated power (3)	$LED_f = \frac{P \cdot DClk}{LED\_PWM \cdot 2}[Hz]$			
Constant pulse	$C_P = \frac{LED_f}{P_{in}}\left[\frac{pulses}{Ws}\right] = \frac{3600000 \cdot LED_f}{P_{in}}\left[\frac{pulses}{kWh}\right]$ $C_P = \frac{1}{2} \cdot \frac{R_2}{R_1 + R_2} \cdot k_{int} \cdot k_S \cdot \frac{A_V \cdot A_I \cdot cal_V \cdot cal_I}{V_{ref}{}^2} \cdot \frac{DClk}{LED\_PWM}\left[\frac{pulses}{Ws}\right]$			
Pulse value	$P_{pulse} = \frac{1}{C_P}\left[\frac{Ws}{pulses}\right]$			
Power register normalized	$p(n)/P_{norm} = \frac{(-1) \cdot 2^{28} \cdot p(n)[28] + p(n)[27:0]}{2^{28}}$			

Table 14. STPM3x basic calculations (continued)

Parameter	Voltage	Current shunt	Current CT	Current Rogowski coil
Power LSB value	$LSB_P = \frac{P_{pulse}}{2^{29}} \cdot DClk = \frac{V_{ref}^2 \cdot (1+R_1/R_2)}{k_{int} \cdot A_V \cdot A_I \cdot k_S \cdot cal_V \cdot cal_I \cdot 2^{28}} \left[\frac{W}{LSB}\right]$			
Energy LSB value	$LSB_E = \frac{P_{pulse}}{2^{18}} = \frac{V_{ref}^2 \cdot (1+R_1/R_2)}{3600 \cdot DClk \cdot k_{int} \cdot A_V \cdot A_I \cdot k_S \cdot cal_V \cdot cal_I \cdot 2^{17}} \left[\frac{Wh}{LSB}\right]$			

1. CHVx and CHCx calibrator bits introduce in the signal processing a correction factor of ±12,5% (with an attenuation from 0,75 to 1). In order to have the maximum available up/down correction range, by default calibrator values are in the middle of their range (0x800) corresponding to an attenuation factor $cal_V = cal_I = 0{,}875$.
2. ΣΔ bitstream should be kept lower than 0.5 (50%) to minimize modulator distortions.
3. LED_PWM is the LED frequency divider that can be set through LPWx bits in DSP_CR1 and DSP_CR2 control registers for primary and secondary current channels respectively. Default value is 1. Please refer to *Table 36 on page 81*.

For each power register, a configurable offset value (default = 0) can be added to the instantaneous power p(n) through OFA[9:0], OFAF[9:0], OFR[9:0], OFAS[9:0] bits in this way:

Equation 4

$$p'(n) = p(n) + (-1)^{OFx[9]} \cdot OFx[8:0] \times 2^2$$

8.4.7 RMS calculation

RMS block calculates RMS values of current and voltage on each phase continuously every 128 µs, as soon as a new sample is available from the ADC, according to the following formulas:

Equation 5

$$V_{RMS} = \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} v(t)^2 dt}$$

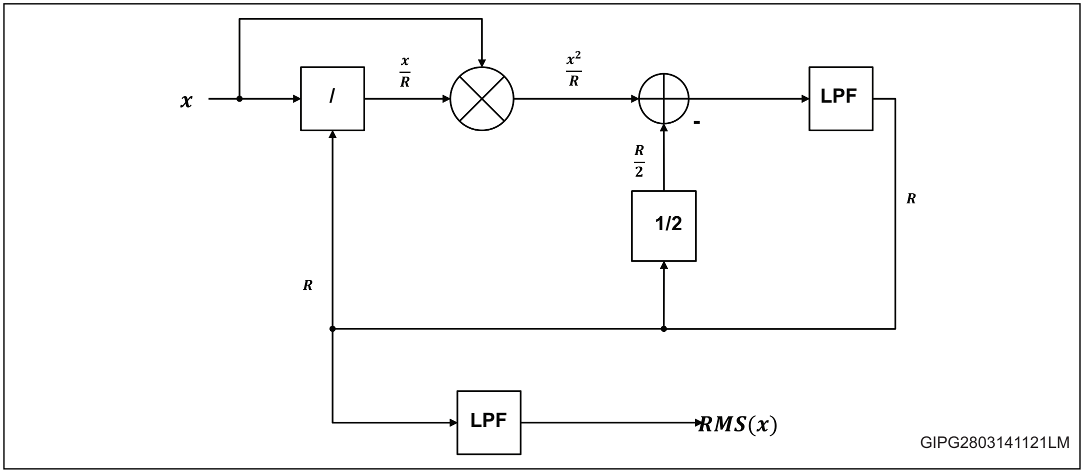
Equation 6

$$I_{RMS} = \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} i(t)^2 dt}$$

with T = 200 ms.

RMS block architecture is shown in *Figure 38*:

Figure 38. RMS block



If the cut-off frequency of an LP filter is set much below the input signal spectrum, it can be considered as an average operator. In this case and according to the figure, the first LP filter averages its input signal which is produced by division and multiplication:

Equation 7

$$R = \overline{\left(\frac{X^2}{R}\right)}$$

By assumption, the feedback signal R is DC type and therefore, it can be extracted from the average operation and the above equation can be rearranged into:

Equation 8

$$R^2 = \overline{(X^2)}$$

By a square-root operation on both sides of previous equation we get:

Equation 9

$$R = \sqrt{\overline{(X^2)}}$$

which is RMS value exact definition.

With an AC input signal:

Equation 10

$$x = x(t) = A\sin(\omega t)$$

$$x^2 = A^2 sin^2(\omega t) = \frac{A^2(1 - \cos(2\omega t))}{2}$$

The LP filter cuts the 2nd harmonic component of input signal multiplying it by a dumping factor α:

Equation 11

$$R = A\sqrt{\frac{1 - \alpha\cos(2\omega t)}{2}} \sim \frac{A}{\sqrt{2}}\left(1 - \frac{\alpha}{2}\cos(\omega t)\right)$$

R result is a DC signal plus the 2nd harmonic ripple with the amplitude of α/2.

For dumping factor | α |<<1:

Equation 12

$$R \sim \frac{A}{\sqrt{2}}$$

RMS updated values are available in **DSP_REG14** and **DSP_REG15** registers every 128 µs.

Raw ADC samples are also available for post-processing by MCU in registers from **DSP_REG2** to **DSP_REG9**.

By taking into account the internal parameters in *Table 13* and the analog front end components in *Table 14*, LSB values of voltage and current registers are the following:

Table 15. STPM3x current voltage LSB values

Parameter	Value
Voltage RMS LSB value	$LSB_{VRMS} = \frac{V_{ref} \cdot (1 + R_1/R_2)}{cal_V \cdot A_V \cdot 2^{15}}[V]$
Current RMS LSB value	$LSB_{IRMS} = \frac{V_{ref}}{cal_I \cdot A_I \cdot 2^{17} \cdot k_S \cdot k_{int}}[A]$
Instantaneous voltage normalized	$v(n)/V_{norm} = \frac{(-1) \cdot 2^{23} \cdot v(n)[23] + v(n)[22:0]}{2^{23}}$

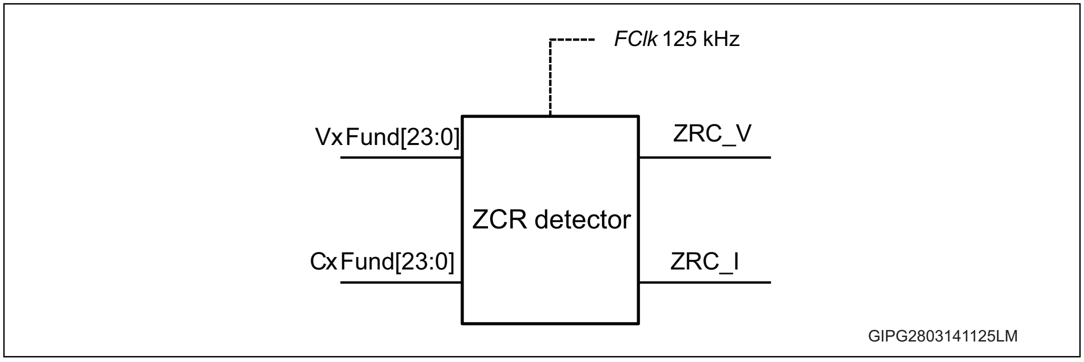
Table 15. STPM3x current voltage LSB values (continued)

Parameter	Value
Instantaneous current normalized	$i(n)/I_{norm} = \frac{(-1) \cdot 2^{23} \cdot i(n)[23] + i(n)[22:0]}{2^{23}}$
Instantaneous voltage LSB value	$LSB_{VMOM} = \frac{V_{ref} \cdot (1 + R_1/R_2)}{cal_V \cdot A_V \cdot 2^{23}} [V]$
Instantaneous current LSB value	$LSB_{IMOM} = \frac{V_{ref}}{cal_I \cdot A_I \cdot 2^{23} \cdot k_S \cdot k_{int}} [A]$

8.4.8 Zero-crossing signal

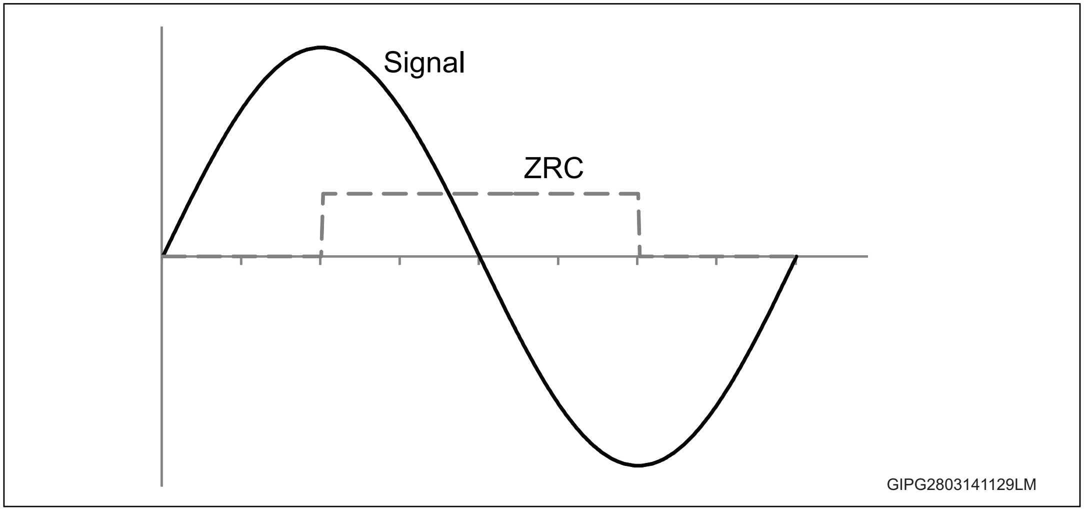
Zero-crossing signals of voltage and current come from fundamental values of voltage and current and output from LPF filter. Resolution of the zero-crossing signal is 8 µs given by F_{CLK} clock = 125 kHz.

Figure 39. Zero-crossing generation



ZRC signal is delayed by an instantaneous voltage current signal: 5.1 ms (typical), as shown in *Figure 40*.

Figure 40. Zero-crossing signal

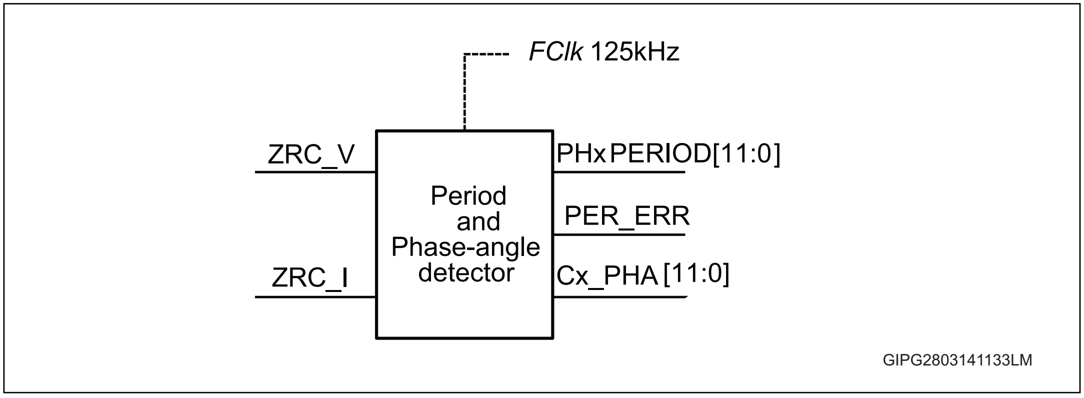


8.4.9 Phase meter

Phase meter detects:

- The period of the voltage line
- The phase-angle delay between voltage and current

Figure 41. Phase meter



Period measurement

Starting from *ZRC* signals, line period and voltage/current phase shift are calculated.

Period information for the two phases is located in **DSP_REG1** register.

The measurement of the period is from *ZRC* signal of voltage channel. The period is calculated like an average of last eight measured periods.

The initial values of period are set on 0x9C4 (2500). LSB of period is 8 µs given by F_{CLK} clock = 125 kHz. Limits to consider the correct period are between 0x600 (1536) and 0x800 (3840) corresponding to a frequency range between 32.55 and 81.38 Hz.

If the voltage signal frequency is out of this range, PER_ERR status bit is set in **DSP_SR1/2**.

PER_ERR = 0: period in the range

PER_ERR = 1: period out of range

PER_ERR bit can be also set when a sag event is detected.

When PER_ERR bit is set, PHx_PERIOD[11:0] is not updated and keeps the previous correct value.

Setting the default line frequency through REF_FREQ bit in register **DSP_CR3** speeds up the period calculation algorithm convergence.

Phase-angle measurement

From the period information, the device calculates phase-delay between voltage and current for the fundamental harmonic.

Cx_PHA[11:0] data for primary and secondary channel are located in **DSP_REG17** and **DSP_REG19** respectively.

Phase-angle φ in degrees can be calculated from the register value as follows:

Equation 13

$$\varphi = \frac{Cx\_PHA[11:0]}{FClk} \cdot f \cdot 360°$$

Resolution at 50 Hz is:

Equation 14

$$\Delta_{PhaseAngle} = \frac{0x001}{125\ kHz} \cdot 50\ Hz \cdot 360° = 0.144°$$

When PER_ERR bit is set, Cx_PHA[11:0] is not updated and keeps the previous correct value.

8.4.10 Sag and swell detection

The device can detect and monitor the undervoltage (also called voltage dip or sag) and the overvoltage or overcurrent events (swell).

A 4-bit event register stores every time that the sag or swell condition is verified. The event history is stored in **DSP_EV1** and **DSP_EV2** registers as SAGx_EV[3:0], SWVx_EV[3:0] and SWCx_EV[3:0]. From the event register, interrupts can be generated, and the event duration is stored in time registers: from **DSP_REG16** to **DSP_REG19**.

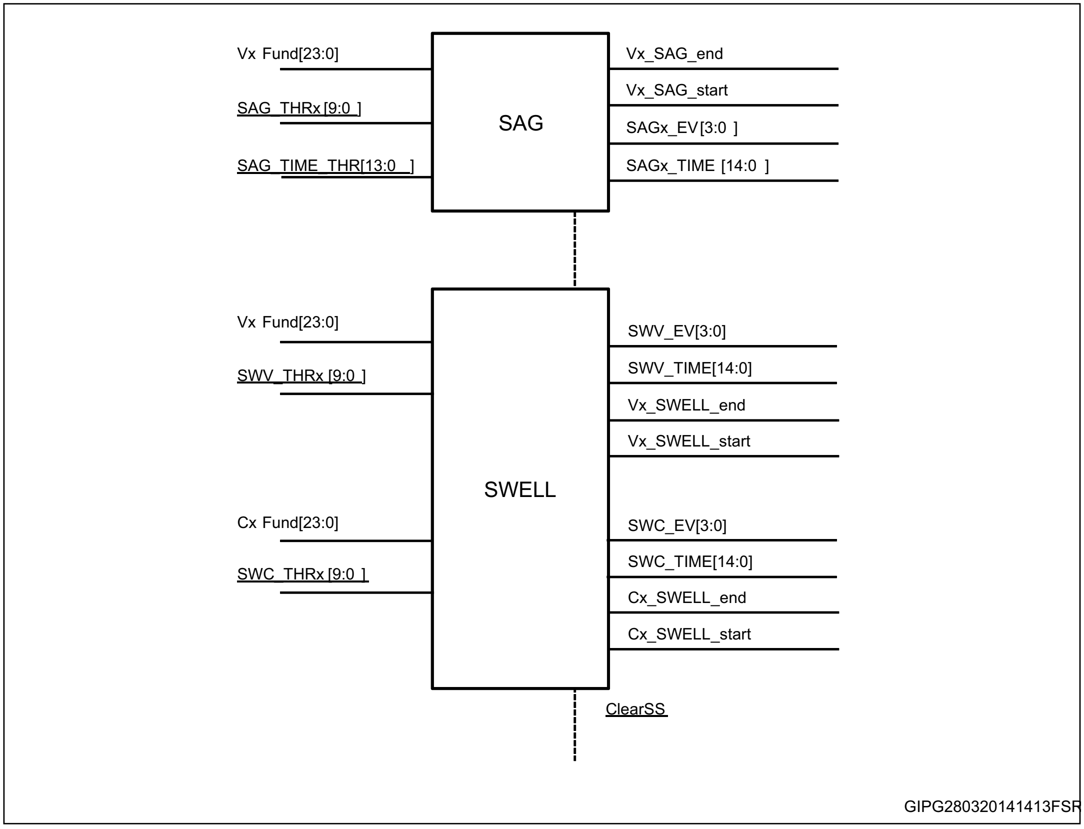
To correctly detect the event, thresholds have to be set from **DSP_CR5** to **DSP_CR8** as explained below.

To clear event history and time registers, once the event has been detected, ClearSS bit in **DSP_CR1**, **DSP_CR2** has to be set. This bit is reset automatically.

To avoid a race condition on digital counters, a time register CLRSS_TO[3:0] (ClearSS reset time) can be set to extend the reset duration of ClearSS bit. LSB of this register is 8 µs.

Status bits are also available in case of sag and swell events in **DSP_SR1** and **DSP_SR2**, they can give the information about the sag/swell event start or end and generate an interrupt if masked in **DSP_IRQ1** and **DSP_IRQ2** registers.

Figure 42. Sag and swell detection blocks



Voltage sag detection

To detect a voltage sag, the fundamental component of voltage is compared to the 10-bit threshold SAG_THRx[9:0] in **DSP_CR5** and **DSP_CR7** for primary and secondary channel respectively.

An internal time counter is incremented until momentary voltage value is below the threshold. Sag event is recorded when the timer counter reaches a programmable value set by SAG_TIME_THR[13:0] bits in **DSP_CR3**. This time threshold is unique for both channels.

When a sag event is detected, LSB of SAGx_EV[3:0] event register and SAG_Start bit are set in the interrupt status register and an interrupt is generated.

If sag event ceases, SAGx_EV register is left shifted and zero is added as LSB, besides, SAG_end bit in the interrupt status register is set as well.

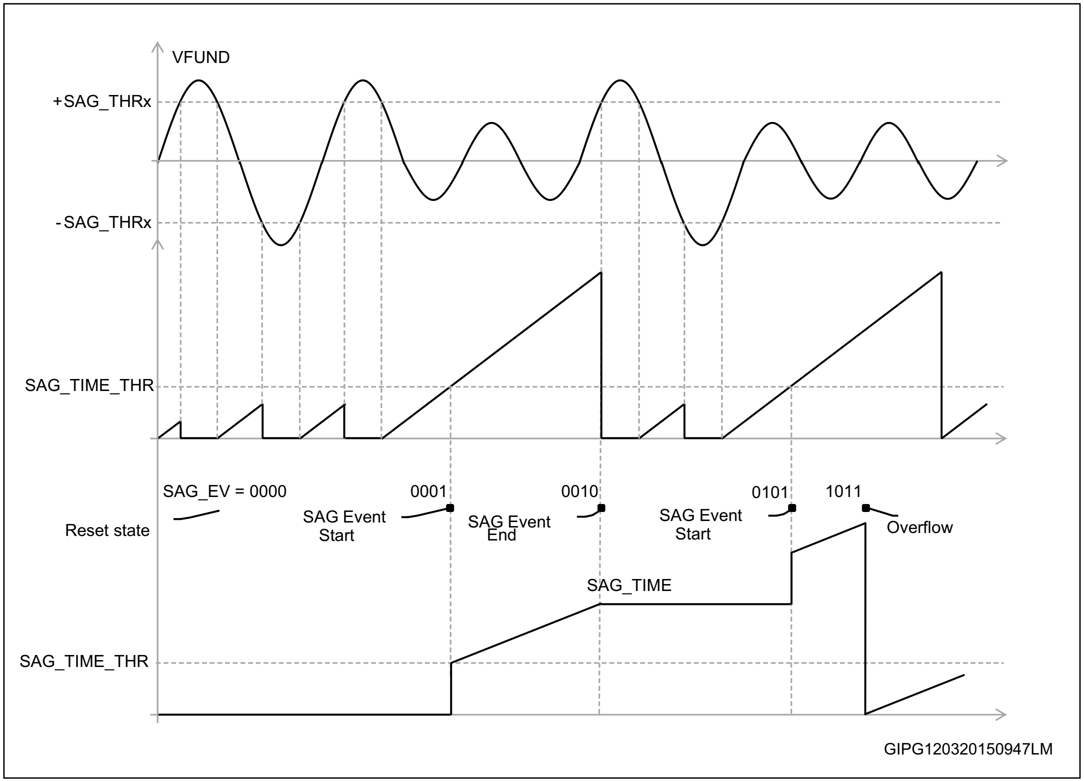
The duration of the event is stored in SAGx_TIME[14:0] in **DSP_REG16** and **DSP_REG18** for primary and secondary voltage channel respectively.

If the overflow of SAG_TIME register occurs, SAGx_EV register is left shifted and its LSB is set, as shown in *Figure 43*.

LSB of time registers is 8 µs.

To disable sag detection, the SAG_THRx register must be set to zero.

Figure 43. Sag detection process



Voltage/current swell detection

To detect a voltage or a current swell, the fundamental component of signal is compared to the 10-bit threshold SWV_THRx[9:0] and SWC_THRx[9:0] in **DSP_CR5**, **DSP_CR6**, **DSP_CR7**, and **DSP_CR8**.

When the signal overcomes the threshold, a swell event is detected and LSB of SWVx_EV[3:0] or SWCx_EV[3:0] event register is set. At the same time, SWELL_Start bit is set in the interrupt status register and an interrupt can be generated.

If the swell event ceases, SWV_EV or SWC_EV register is shifted and its LSB is set to zero, also SWELL_End bit in the interrupt status register is set.

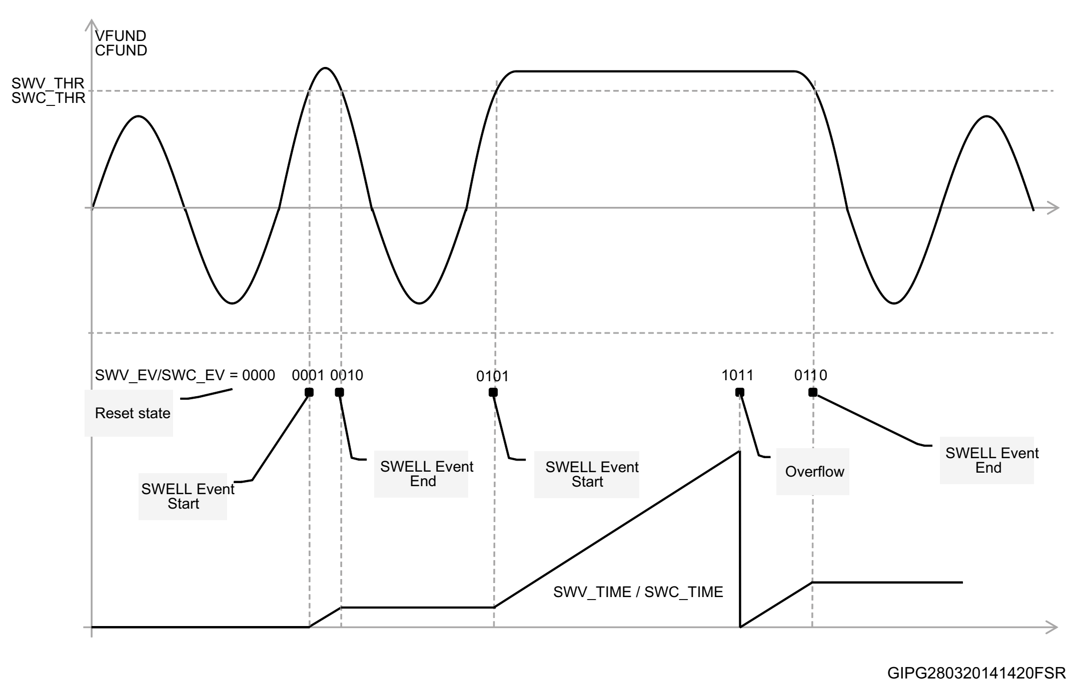
The duration of the event is stored in SWV_TIME[14:0] or SWC_TIME[14:0] in registers from **DSP_REG16** to **DSP_REG19** for primary and secondary voltage and current channel respectively.

If the overflow of SWV_TIME or SWC_TIME register occurs, the related SWVx_EV and SWCx_EV register is left shifted and its LSB is set, as shown in figure below.

LSB of time registers is 8 μs.

To disable swell detection, the registers SWV_THRx and SWC_THRx must have maximum value 0x3FF.

Figure 44. Swell detection process



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Sag and swell threshold calculation

Thresholds for sag voltage detection are calculated below, according to the following input parameters:

V_L: line voltage nominal RMS value

V_{SAG}: target RMS value of sag voltage

R_1, R_2: voltage divider resistors

$A_V = 2$, voltage channel gain

$D_{SAG} = 2^{10}$, length of sag threshold register

$cal_V = 0.875$, calibrator mid value

Table 16. Voltage sag

Parameter	Value
SAG peak voltage	$V_{SAG\_peak} = V_{SAG} * \sqrt{2}$
Input signal	$V_{in\_SAG\_peak} = V_{SAG} * \sqrt{2} * \frac{R2}{R1 + R2}\ [V]$
Percentage of FS input	$V_{in\_SAG\_peak}(FS) = \frac{V_{SAG}}{V_{ref}} \cdot A_V \cdot \sqrt{2} \cdot cal_V \cdot \frac{R_2}{R_1 + R_2}$

Table 16. Voltage sag (continued)

Parameter	Value
Register value	$SAG=\frac{V_{SAG}}{V_{ref}}\cdot A_V\cdot\sqrt{2}\cdot cal_V\cdot\frac{R_2}{R_1+R_2}\cdot D_{SAG}[HEX]$
Register LSB RMS value	$LSB_{SAG}=\frac{(R_1+R_2)\cdot V_{ref}}{A_V\cdot\sqrt{2}\cdot R_2\cdot cal_V\cdot D_{SAG}}[V]$

To calculate the filtering time for the sag event, we consider the time in which the nominal instantaneous voltage is below the sag threshold, that is:

Equation 15

$$time = 2\cdot\arcsin\left(\frac{V_{SAG}}{V_L}\right)\cdot\frac{1000}{2\pi f_L}[ms]$$

To correctly distinguish between normal sinusoidal voltage and sag event, the filtering time should be added to this component, for example half line period (10 ms at 50 Hz). Since LSB of SAG_TIME_THRx register is 8 µs (F_{CLK} = 125 kHz), the value to set is:

Equation 16

$$TIME=\frac{time+dt}{8\ us}\ [HEX]$$

In the same way:

V_{SWELL}: target RMS value of swell voltage

A_V: voltage sensor gain

$D_{SWELL} = 2^{10}$, length of swell threshold register

cal_V = 0.875, calibrator mid value

Following the above calculation we obtain the hexadecimal value of voltage swell threshold:

Table 17. Voltage swell

Parameter	Value
Register value	$SWELL_V=\frac{V_{SWELL}}{V_{ref}}\cdot A_V\cdot\sqrt{2}\cdot\frac{R_2}{R_1+R_2}\cdot cal_V\cdot D_{SWELL}[HEX]$
Register LSB RMS value	$LSB_{SWELL}=\frac{V_{ref}\cdot(R_1+R_2)}{A_V\cdot\sqrt{2}\cdot R_2\cdot cal_V\cdot D_{SWELL}}[V]$

For the current swell, an analogue procedure can be followed:

I_{SWELL}: target RMS value of swell current

k_S: current sensor sensitivity [V/A]

A_I: current sensor gain

$cal_I = 0.875$, calibrator mid value

The swell threshold is:

Table 18. Current swell

Parameter	Value
Register value	$SWELL_C = \frac{I_{SWELL}}{V_{ref}} \cdot A_I \cdot \sqrt{2} \cdot k_S \cdot cal_I \cdot D_{SWELL} [HEX]$
Register LSB RMS value	$LSB_{SWELL} = \frac{V_{ref}}{A_I \cdot \sqrt{2} \cdot k_S \cdot cal_I \cdot D_{SWELL}} [A]$

8.4.11 Tamper detection

The device includes a tamper detection module (the STPM34 and STPM33 only).

To enable this feature, TMP_EN bit and TMP_TOL[1:0] tamper tolerance have to be set in **DSP_CR3**. Tamper detection feature is disabled by default. It is possible to choose among four different tolerances according to *Table 19*:

Table 19. Tamper tolerance setting

TMP_TOL[1:0]	Tamper tolerance
0x00	TOL = 12.5%
0x01	TOL = 8.33%
0x10	TOL = 6.25%
0x11	TOL = 3.125%

Tamper module monitors active energy registers of the two channels. Tamper condition is detected when the absolute value of the difference between the two active energy values is greater than the chosen percentage of the averaged value. This occurs when the following equation is satisfied:

Equation 17

$$|EnergyCH1 - EnergyCH2| > TOL * |EnergyCH1 + EnergyCH2|$$

where TOL is selected according to *Table 19*.

Detection threshold is much higher than the accuracy difference of the current channels, which should be less than 0.2%, but, some headroom should be left for possible transition effect, due to accidental synchronism of load current change at the rate of energy sampling.

Tamper circuit works if energies associated with the two current channels are both positive or negative, if two energies have different sign, a warning flag "TAMPER OR WRONG" in **DSP_SR1** or **DSP_SR2** is set.

The channel with higher energy is signaled by PHx TAMPER status bit in **DSP_SR1** or **DSP_SR2**.

When internal signals are not good enough to perform the calculations, for example line period is out or range or sigma-delta signals from analog section are stuck at high or low logic level, the tamper module is disabled and its state is set to normal.

8.4.12 AH accumulation

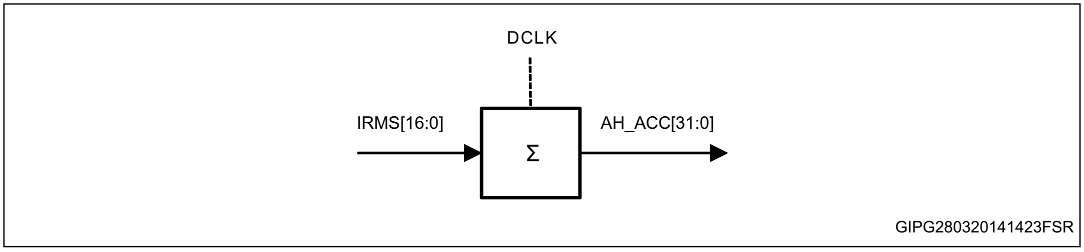
In this particular tamper, the neutral wire is disconnected from the meter and the STPM3x does not sense the voltage anymore, while it keeps sensing the current information. In these conditions, AH accumulator can be used by the microcontroller to regularly calculate the billing based on a nominal voltage value due to the following equation:

Equation 18

$$\text{Energy} = \text{AH\_ACC}[31:0] \cdot \text{LSB}_{\text{AH\_ACC}} \cdot V_{\text{NOM}} \text{ [Wh]}$$

If voltage is too low (sag event detected) or period is wrong (PER_ERR = 1) and RMS value of current is high enough, RMS current is accumulated in the register AH_ACC[31:0]. Value in PHx AH_ACC[31:0] register is increased with a *DCLK* frequency.

Figure 45. AH accumulation block



The accumulation of current values is controlled by AH status bit. AH bit is set when PER_ERR = 1 and real values of current overcome an upper threshold set in AH_UPx[11:0] in **DSP_CR9** and **DSP_CR11**. This bit is cleared when RMS current drops below AH_DOWNx[11:0] threshold in **DSP_CR1**0 and **DSP_CR12**.

To stabilize the current accumulation, SAG event should be monitored by setting some thresholds in the related register.

Figure 46. AH accumulation thresholds

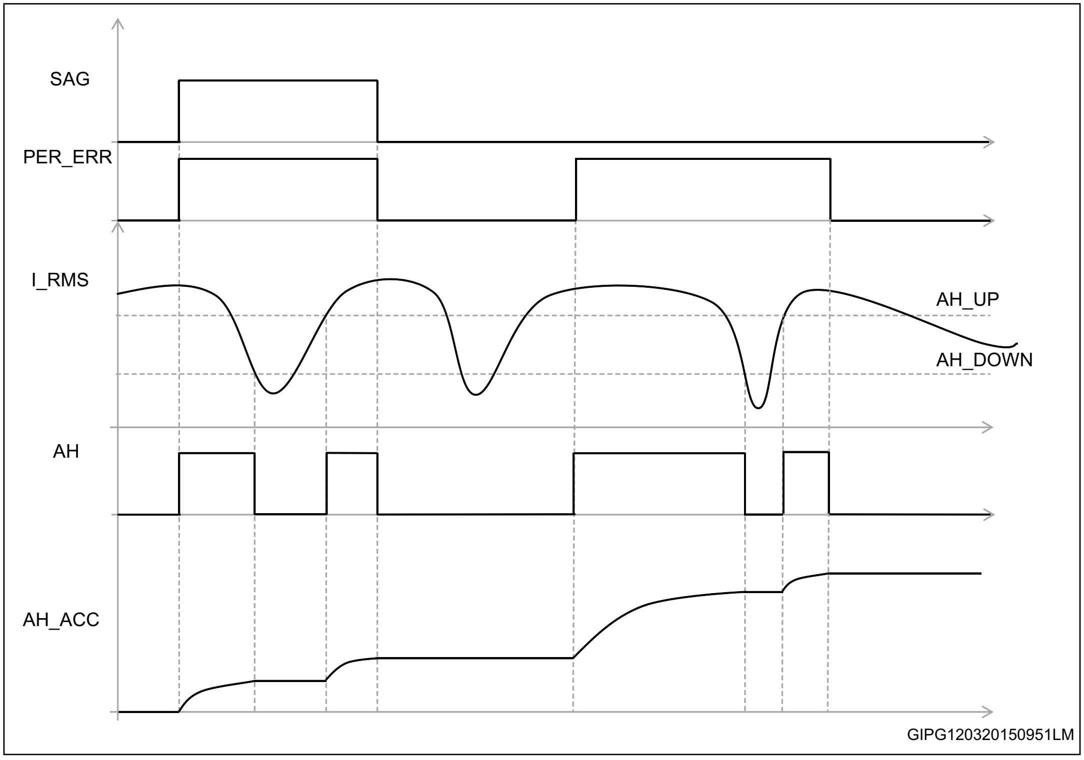


Table 20. AH accumulator LSB

Parameter	Value
AH accumulator register LSB	$LSB_{AH\_ACC} = \frac{LSB_{IRMS} \cdot 2}{3600 \cdot DClk}[Ah]$
AH threshold register LSB	$LSB_{AH\_UP} = LSB_{AH\_DOWN} = LSB_{IRMS} \cdot 2^5[A]$

8.4.13 Status bits, event bits and interrupt masks

The device detects and monitors events like sag and swell, tamper, energy register overflow, power sign and errors, generating an interrupt signal on INTx pins when the masked event is triggered.

When the event is triggered, the correspondent bit is set in two registers:

- Live event register **DSP_EV1,2**
- Status (also called interrupt) register **DSP_SR1,2**

To output the interrupt on INTx pins, the correspondent bit should be set in the interrupt control mask register **DSP_IRQ1,2**

Live event register

In live event registers (**DSP_EV1** and **DSP_EV2**), events are set and cleared by DSP at the sampling rate *DCLK* = 7,8125 kHz.

Table 21. Live events

Bit	Internal signal	Description
0	PH1+PH2 events[1]	Sign total active power
1		Sign total reactive power
2		Overflow total active energy
3		Overflow total reactive energy
4	PHx events	Sign active power
5		Sign active fundamental power
6		Sign reactive power
7		Sign apparent power
8		Overflow active energy
9		Overflow active fundamental energy
10		Overflow reactive energy
11		Overflow apparent power
12	Cx events	Current zero-crossing
13		Current sigma-delta bitstream stuck
14		Current AH accumulation
15		Current swell event history
16		
17		
18		
19	Vx events	Voltage zero-crossing
20		Voltage sigma-delta bitstream stuck
21		Voltage period error (out of range)
22		Voltage swell event history
23		
24		
25		
26		Voltage sag event history
27		
28		
29		
30	-	Reserved
31	-	Reserved

1. Valid for the STPM33 and STPM34 only.

Status interrupt register

When an event is detected, DSP sets the status register (**DSP_SR1** and **DSP_SR2**) bits that remain latched, even if the event ceases, until they are cleared to zero by a write operation.

Table 22. Status register

Bit	Internal signal	Description
0	PH1+PH2 status(1)	Sign total active power
1		Sign total reactive power
2		Overflow total active energy
3		Overflow total reactive energy
4	PH2 IRQ status(1)	Sign secondary channel active power
5		Sign secondary active fundamental power
6		Sign secondary reactive power
7		Sign secondary apparent power
8		Overflow secondary channel active energy
9		Overflow secondary channel active fundamental energy
10		Overflow secondary channel reactive energy
11		Overflow secondary channel apparent energy
12	PH1 IRQ status	Sign primary channel active power
13		Sign primary channel active fundamental power
14		Sign primary channel reactive power
15		Sign primary channel apparent power
16		Overflow primary channel active energy
17		Overflow primary channel active fundamental energy
18		Overflow primary channel reactive energy
19		Overflow primary channel apparent energy
20	Cx IRQ status	Current sigma-delta bitstream stuck
21		AH1 - accumulation of current
22		Current swell detected
23		Current swell end
24	Vx IRQ status	Voltage sigma-delta bitstream stuck
25		Voltage period error
26		Voltage sag detected
27		Voltage sag end
28		Voltage swell detected
29		Voltage swell end

Table 22. Status register (continued)

Bit	Internal signal	Description
30	Tamper status[1]	Tamper
31		Tamper or wrong connection

1. Valid for the STPM33 and STPM34 only.

Interrupt control mask register

Each bit in the status register has a correspondent bit in **DSP_IRQ1**, **DSP_IRQ2** interrupt mask registers. For each bit set, the relative event detection is output on INT1, INT2 pins respectively. In the STPM32, **DSP_IRQ1** is mapped on INT1 pin only.

Status bits can be monitored by an external microcontroller application, in fact when INTx pin triggers, the application reads the relative status register content and clears it.

Note: Power sign status bits generate level interrupts.

8.5 Functional description of communication peripheral

The STPM3x can be interfaced to a control unit through a programmable communication peripheral which can be:

- 4-pin SPI
- 2-pin UART

The serial communication peripherals share same pins so that they cannot be used at the same time.

Interface selection is implemented through an internal detection system that, at the device startup, detects which of the two communication interfaces has to be used. This feature allows communication to be quickly established with minimal initialization.

Auto-detection works at startup, (power-up or EN pin transition from low to high) by monitoring SCS pin status and automatically selecting the communication interface that matches the configuration:

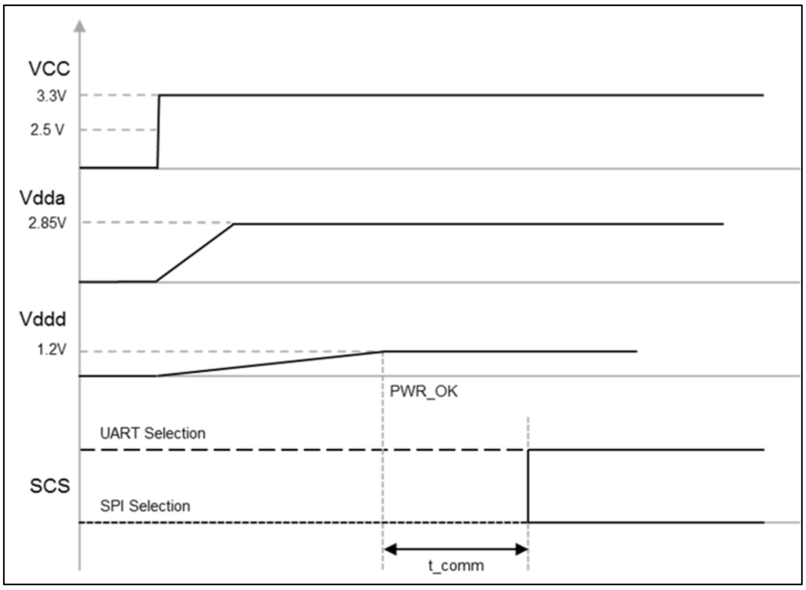
- If SCS pin is held low the communication method is SPI
- If SCS pin is held high the communication interface is UART.

For the communication interface selection the SCS pin must be kept low or high for SPI or UART selection respectively for at least 125ns after the internal clock signal starts.

According to POR sequence in *Figure 28*, only after the regulated voltages are OK the PWR_OK internal signal enables the CLKIN signal to the digital section. After two clock periods, the digital section sets and locks the interface to the selected type. Note that the regulated voltages could be ready later than the Vcc minimum threshold of 2.5 V, because of the capacitance on VDDA and VDDD pins.

Below a timing diagram of startup and interface selection.

Figure 47. Startup interface selection timing



After the selected communication interface is established, the interface is locked to prevent the communication method from changes, and SCS pin is used as chip-select for the device.

Pins used by the serial communication peripheral are listed in *Table 23*.

Table 23. Communication pin description

Name	Function	SPI connection	UART connection
SYN	Synchronization	GPIO (optional), VCC at startup	GPIO (optional), VCC at startup
SCS	Chip-select	-Start-up interface selection at GND -Chip-select at GND	-Start-up interface selection at VCC -Chip-select at VCC
SCL	Clock	SPI CLK	Not used
MOSI/RXD	Data in	SPI MOSI	UART RX
MISO/TXD	Data out	SPI MISO	UART TX

8.6 Communication protocol

A single communication session consists of 4 + 1 (optional CRC) bytes full-duplex data sequence organized as follows:

Table 24. Communication session structures

Byte	Master-side transmitted data	Slave-side transmitted data
1	ADDRESS for 32-bit register to be read	Previously requested data byte LSB
2	ADDRESS for 16-bit register to be written	Previously requested data byte 2 out of 4
3	DATA for 16-bit register to be written, LSB	Previously requested data byte 3 out of 4
4	DATA for 16-bit register to be written, MSB	Previously requested data byte MSB
5 (optional)	Master CRC verification packet	Slave CRC verification packet

The above information is exchanged between master and slave in the same communication session, or transaction. SPI master can issue a read-request and a write-request (optional).

The master initiates the communication sending the STPM3x a frame see *Table 24* (read address - write address - LS data byte - MS data byte - optional CRC).

Two command codes are provided:

- Dummy read address 0xFF increments by one the internal read pointer
- Dummy write address 0xFF specifies that no writing is requested (the two following incoming data frames are ignored)

Upon the reception of a frame, the STPM3x replies to master data sending the 32-bit register addressed during the previous communication session; during the first session the slave sends, by default, the 32-bit data stored into the first (row 0) memory register. Data are organized in 8-bit packets so that the least significant byte is sent first and the most significant byte is sent last.

A final 8-bit CRC packet is sent to master to verify no data corruption has occurred during the transmission from slave to master. The CRC feature, enabled by default, can be controlled by a configuration bit into US_REG1 memory row (read address 0x24, write address 0x24).

If CRC bit in US_REG1 is cleared, the communication consists of 4 bytes only.

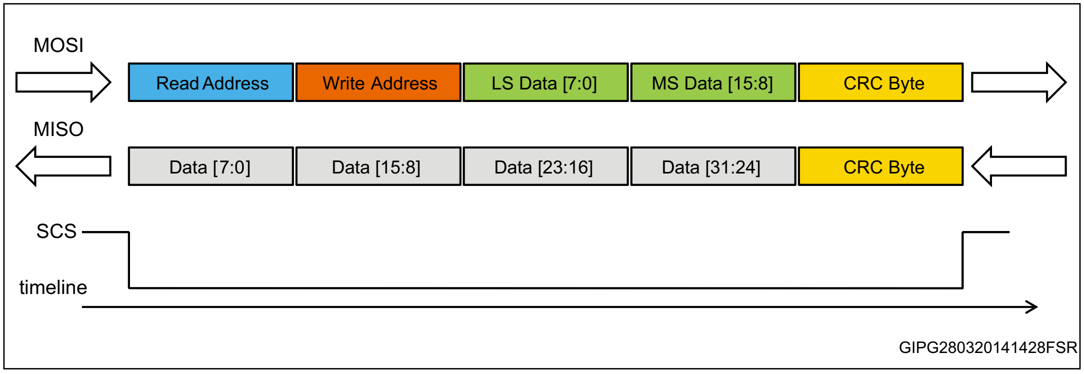
Write-requests are executed immediately after the transaction has completed, while read-requests are fulfilled at the end of the next transaction only, because the sent read-address has just set the internal register pointer to deliver data during the following transaction.

So, while one transaction is enough to write data into memory, at least two transactions are needed to read selected data from memory.

Data bytes are swapped with respect to the order of the byte, since during transmission, the 3rd byte sent to MOSI line is the least-significant (LS) byte (bits [7:0]) and the 4th byte is the most-significant (MS) byte of the data to be written (bits [15:8]).

On MISO line, the first data byte received is the least-significant (LS, bits [7:0]) and the last is the most-significant (MS, bits [31:24]) of the record, as shown below.

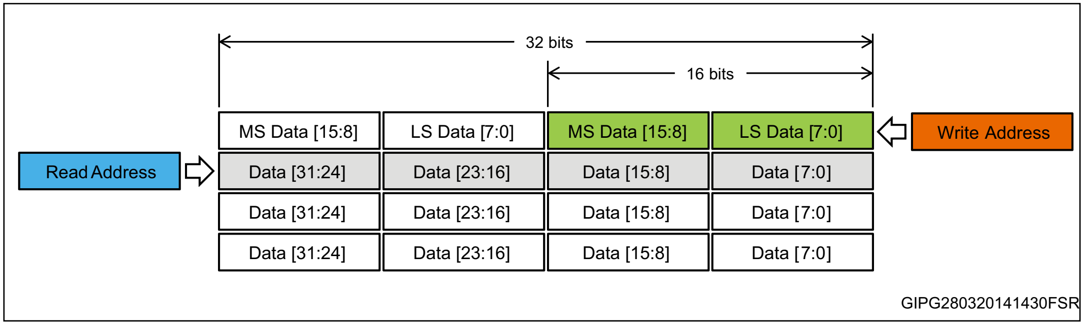
Figure 48. Single communication time frame



Data and configuration registers are organized into 32-bit rows in the internal memory, but can only be accessed 16-bit at a time for writing operations.

The address space is 70 rows wide, so there are 70 32-bit addressable elements for reading operations; since the first 21 configuration registers are writable, there are 42 (= 21 x 2) 16-bit addressable elements for writing operations.

Figure 49. Memory data organization



Two different codes are used for the read address space and write address space, which can be found in the register map.

8.6.1 Synchronization and remote reset functionality

Data into read-only registers are updated internally by DSP with frequency: 7.8125 kHz (clock frequency measure). Latching is used to sample the updated results into transmission latches. The transmission latches are flip-flops holding the data in the communication interface.

Data latching can be implemented in three ways:

- Using SYN and SCS pin
- Writing the channel latch bits before each reading (S/W Latchx in **DSP_CR3**)
- Writing auto-latch bit (S/W Auto Latch in **DSP_CR3**) to automatically latch data registers every clock measure period (128 µs)

The remote reset can be performed in two ways:

- Using SYN and SCS pin
- Writing the reset bit (S/W reset in **DSP_CR3**)

SYN pin: latching, reset and global reset

Latching of internal memory registers can be carried out by producing pulses of a given width on SYN pin while SCS line is high as depicted in *Figure 50*.

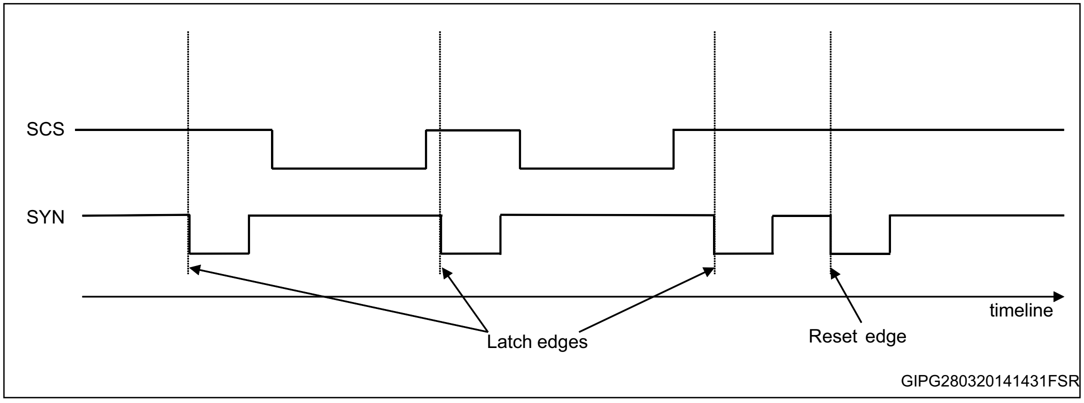
If a single pulse on SYN is detected, latch occurs.

If two consecutive pulses are detected, a reset of measurement registers occurs and the counters are reset, as well.

If three consecutive pulses are detected, a global reset occurs, the configuration is also reset and the chip must be initialized again.

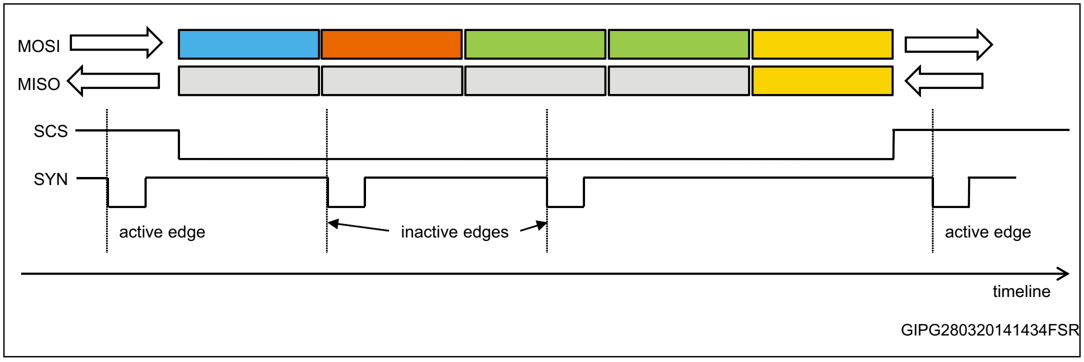
Note: To ensure a correct initialization of DSP, it is recommended to perform a global reset through three SYN pulses at startup and before setting configuration bits.

Figure 50. Latching and reset through SYN pulses



Latch pulse width and other SPI timings are reported in *Table 5 on page 17*.

Figure 51. Latching through SYN pulses



Software latch

Writing S/W Latchx configuration bits of **DSP_CR3** register can latch data into transmission latches. These two bits latch channel 1 and channel 2 data registers respectively; once set, they latch data and are automatically reset. By setting S/W Auto Latch bit, latching is performed automatically at the rate of sampling clock, so data latching, before each reading request, is no longer necessary.

Software reset

Writing SW Reset configuration bit in **DSP_CR3** brings the configuration registers to their default values. Data registers are not reset. This bit is automatically cleared after this action.

8.6.2 SPI peripheral

The device implements a full-duplex communication protocol using MISO, MOSI ports for data exchange, SCL for clock port, SCS port for data exchange activation and SYN for internal register data latching and resetting, when no data activation is set (SCS in off-state). Latching and resetting can also be performed by setting the related bits in **DSP_CR3** register.

With reference to the general SPI protocol, the peripheral is configured to work according to the following settings: cpol=1, cpha=1.

SPI control register

US_REG1 register contains 16-bits with all the configuration parameters of t SPI and UART interfaces of the STPM3x.*Table 25* describes SPI related bits:

Table 25. SPI control register

Bit position in row	Name	Description	Default value
15	LSBfirst	Little(1) or big(0) - endian for bit transmission in data-byte	0
14	CRCenable	Enable/disable CRC feature	1
[7:0]	CRCPolynomial	Polynomial used to validate transmitted and received data	0x07

LSBfirst: endianness of data-byte transmission and reception

CRCenable: enables the optional CRC feature

CRCPolynomial: default polynomial used is 0x07 (x8+x2+x+1)

SPI timings

Any single transaction timing follows the scheme in *Figure 5 on page 13*.

For consecutive writing transactions, a minimum time interval of 4 µs has to be taken into account in order to avoid overrun issues.

For latch and consecutive read transactions a minimum time interval of 4 µs has to be taken into account in order to avoid overrun issues.

Examples

All frames in the following examples do not contain CRC byte, which has to be added just in case the feature has not been disabled previously. After that CRC has been disabled, the frame consists of four bytes only.

To write bits from 31 to 16 (most significant bits) in row 1 with data byte 0xABCD and read row 2 in the following transaction, the first four bytes of the transmission (without CRC) are:

04_03_CD_AB

To receive data from register 04 the master should send the frame:

FF_FF_FF_FF

To write lower (least significant) 16-bits in row 3 with data #AABB and read back from the same row:

06_06_BB_AA

And then

FF_FF_FF_FF

To receive

The sent frame changes according to LSBfirst setting:

Table 26. LSBfirst example

LSBfirst = 0	04_03_CD_AB
LSBfirst = 1	20_C0_B3_D5

MISO line is valid as well. In this case, there is a full-reverse data transmission when LSBfirst=1, since data bit reception order changes as shown in *Table 27*.

Table 27. LSBfirst and MISO line

	Byte[0]	Byte[1]	Byte[2]	Byte[3]
LSBfirst = 0	[7:0]	[15:8]	[23:16]	[31:24]
LSBfirst = 1	[0:7]	[8:15]	[16:23]	[24:31]

LSBfirst can be programmed using the transactions (other configuration bits involved in the transaction are set to their default states):

Table 28. LSBfirst programming

LSBfirst = 1	24_24_07_CO
LSBfirst = 0	24_24_EO_02

The transaction to write LSBfirst = 0 is byte-reversed, since the system has moved from the LSBfirst = 1 condition. The read address is set so to read in the following transaction the content of **US_REG1**.

Following the frames to enable/disable CRC feature:

Table 29. CRCenable programming

CRCenable = 1	24_24_07_40
CRCenable = 0	24_24_07_00

To reset status bits, the following frame should be sent:

28_29_00_00

which resets all 16-bits (SPI and UART status registers). To clear SPI status bits only, SPI-master can send 1 s sequence to UART status bit register. Referring to the previous example, this leads to the following transaction:

28_29_FF_00

Events are associated to interrupts so that, when the correspondent event mask bit in SPI IRQ register is activated, INT line is sensitive to that event.

For example, to activate CRC error interrupt (bit 12, related to status bit 28), the mask 0x1000 has to be written to write address 0x28 by the following transaction:

28_28_00_10

8.6.3 UART peripheral

The STPM3x provides the UART interface, which allows a communication using two single-direction pins only; this reduces the cost of isolated communication, where required, since two low cost opto-isolators are needed for this purpose.

Main features of this interface are:

- Full-duplex, asynchronous communication
- Low-level sequential data exchange protocol (1 start, 8 data, 1 stop)
- NRZ standard format (mark/space)
- Fractional baud rate generator system (to offer a wide range of baud rates)
- Several error detection flags
- Configurable frame length
- Optional configurable CRC checksum
- Optional noise immunity algorithm

TX pin accesses this interface, which transmits data to the microcontroller, and RX pin, which receives data from the microcontroller. A simple master/slave topology is implemented on the UART interface where the STPM3x acts as the slave.

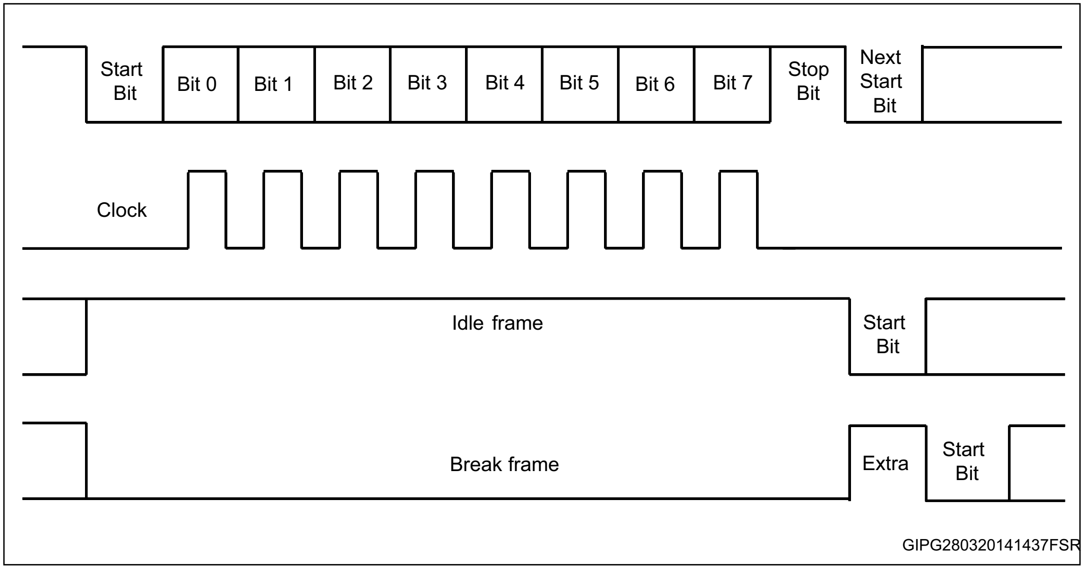
Transmission and reception are driven by a common baud rate generator; the clock for each one is generated only when UART is enabled.

UART transmitting and receiving sections must have the same bit speed, frame length and stop bits.

Chip selection in UART mode requires SCS bit is kept high.

Communication starts when the master sends slave a valid frame (the microcontroller). The format of the frame is shown below.

Figure 52. UART frame



As shown in *Figure 52*, each frame consists of 10 bits. Each bit is sent to a variable rate. All frame data are sent LSBfirst.

If a BREAK frame is received, a break flag is set and the whole packet reception aborts.

The frame receiver can recognize an IDLE frame, but packet processing is not involved.

UART control register

US_REG1 and **US_REG2** registers respectively contain all the configuration parameters of SPI and UART interfaces of the STPM3x. *Table 30* describes UART bits:

Table 30. UART control register US_REG1

Row bit position	Name	Description	Default value
[23:16]	Timeout	Timeout threshold [ms]	0
9	Break on error	Enable/disable the operation to send break frame in case of error	0
8	Noise detection enable	Enable/disable error detection based on noise immunity algorithm	0
[7:0]	CRCPolynomial	Polynomial used to validate transmitted and received data	0x07

- Timeout: any communication session should be completed within this configurable time threshold (ms). If the timeout value is zero this threshold is disabled. If timeout expires, the reception and the transmission processes stop and, if enabled, a BREAK character is transmitted to warn the master about the error. Packet processing can resume only after that BREAK transmission has been completed and an IDLE frame has been received.
- Break on error: if an error occurs (framing/noise/timeout/RX overrun) a BREAK command is transmitted to the master.
- Noise error detection. An oversampling technique is implemented to raise the noise level immunity: received bit value is accomplished taking in account the value of three

samples, and applying to them the majority rule. This noise immunity algorithm is automatically enabled: if “noise detection enable” bit is set, all samples must have the same value to get a valid bit reception. In this case, when noise is detected within a frame, a noise detection error is issued and the whole packet is discarded.

- CRCPolynomial: default polynomial used is 0x07 (x8+x2+x+1).

CRC, in case of UART, has to be calculated on the reversed byte frame, because of the internal structure of UART blocks.

For example, if the frame to transmit is 04_03_CD_AB, CRC should be calculated on the frame:

20_C0_B3_D5 -> CRC = 0x16

The frame to send is: 04_03_CD_AB with the reversed CRC = 68

Note: *For UART peripheral, CRC byte is sent reversed only.*

Table 31. UART control register US_REG2

Row bit position	Name	Description	Default value
[23:16]	Frame delay	TX frame-to-frame delay [bit periods]	0
[15:0]	Baud rate	Fractional baud rate generation	0x0683

- Frame delay: delay (expressed as bit periods) in transmitted frames. The bit period depends on the baud rate divider selection (see below).
- Baud rate: set to 9600 default value, the communication baud rate can be programmed in this configuration register. Theoretical values for configuration register can be calculated according to the following formulas, where a main clock frequency is 16 MHz, BR is the desired baud rate and BRDIV is the theoretical value of fractional divider:

Equation 19

$$BRDIV = \frac{Main\ Clock\ Frequency}{16 * Communication\ Baud\ Rate} = \frac{\cancel{16} * 10^6}{\cancel{16} * BR}$$

Equation 20

$$BRR_I = [BRDIV] = int(BRDIV)$$

Equation 21

$$BRR_F = round(16 * (BRDIV - BRR_I))$$

where BRR_I are bits [15:4] and BRR_F are bits [3:0] of the register.

According to the chosen baud rate divider the bit period is:

Equation 22

$$Bit\ Period = (16 * BRR_I + BRR_F) * MClk\ Period$$

Table 32 summarizes the above calculation of the register value to select some typical baud rates:

Table 32. Baud rate register examples

Baud rate	BRDIV	BRR_I	BRR_F	Register value
2400	416.666667	416 = 0x1A0	11 = 0xB	1A0B
9600	104.166667	104 = 0x68	3 = 0x3	683
19200	52.0833333	52 = 0x34	1 = 0x1	341
57600	17.3611111	17 = 0x11	6 = 0x6	116
115200	8.68055556	8 = 0x8	11 = 0xB	8B
230400	4.34027778	4 = 0x4	5 = 0x5	45
460800	2.17013889	2 = 0x2	3 = 0x3	23

8.6.4 UART/SPI status register and interrupt control register

At row 20, at read address 0x28, the register is responsible for holding the status of UART/SPI peripherals of the STPM3x device. Setting the correspondent bit in IRQ CR the interrupt mask raises an interrupt on both INT1, INT2 pins based on the peripheral status.

Table 33. UART/SPI status and interrupt control register

Register	Bit position	Description	Default value	Access mode
SR	30	SPI RX overrun	0	RW
	29	SPI TX underrun	0	RW
	28	SPI CRC error	0	RW
	27	UART/SPI write address error	0	RW
	26	UART/SPI read address error	0	RW
	25	SPI TX empty	0	RO
	24	SPI RX full	0	RO
	22	UART TX overrun	0	RW
	21	UART RX overrun	0	RW
	20	UART noise error	0	RW
	19	UART frame error	0	RW
	18	UART timeout error	0	RW
	17	UART CRC error	0	RW
	16	UART break	0	RW
IRQ CR	14	mask for SPI RX overrun error status bit	0	RW
	13	mask for SPI TX underrun error status bit	0	RW
	12	mask for SPI CRC error status bit	0	RW
	11	mask for write address error status bit	0	RW
	10	mask for read address error status bit	0	RW
	9	mask for SPI TX empty	0	RW
	8	mask for SPI RX full	0	RW
	6	mask for UART TX overrun	0	RW
	5	mask for UART RX overrun	0	RW
	4	mask for UART noise error	0	RW
	3	mask for UART frame error	0	RW
	2	mask for UART timeout error	0	RW
	1	mask for UART CRC error	0	RW

- SPI RX overrun: occurs when two consecutive write transactions are too fast and close to each other
- SPI TX underrun: occurs when a read-back operation (= write then read the same register) or latch/read is too fast
- SPI CRC error: CRC error detected
- UART/SPI write address error: write address out of range (not write address not writable)

- UART/SPI read address error: read address out of range (not read address not readable)
- SPI TX empty: transmission buffer empty (for SPI diagnostic, not recommended for normal IRQ operations)
- SPI RX full: reception buffer full (for SPI diagnostic, not recommended for normal IRQ operations)
- UART TX overrun: occurs when master and slave have different baud rates and master transmits before reception has ended
- UART RX overrun: active when received data have not been correctly processed
- UART noise error: noisy bit detected
- UART frame error: missing stop bit detected
- UART timeout error: timeout counter expired
- UART CRC error: CRC error detected
- UART break: break frame (all zeros) received

Read-write status bits are set by the occurrence of the related event and are not reset when the event ceases, on contrary master can only reset them transmitting a write sequence addressed to memory location 0x28.

9 Application design and calibration

The choice of external components in the transduction section of the application is a crucial point in the application design, affecting the precision and the resolution of the whole system. A compromise has to be found among the following needs:

1. Maximizing signal-to-noise ratio in the voltage and current channel
2. Choosing current-to-voltage conversion ratio k_S and the voltage divider ratio in a way that calibration can be achieved for a given constant pulse C_P
3. Choosing k_S to take advantage of the whole current dynamic range according to desired maximum current and resolution

In this section, the rules for a good application design are described. After the design phase, any tolerance of the real components from these values or device internal parameter drift can be compensated through calibration.

Please refer to *Section 8.4.6 on page 48* and *Section 8.4.7 on page 50* for device basic calculations.

9.1 Application design

To reach C_P target output constant pulse at default LPW value, the analog front end component choice has to depend on:

- value of R_1 voltage divider resistor, given R_2 and k_S current sensor sensitivity
- k_S given R_1 and R_2 voltage divider resistors

Calculations for these two methods are developed below:

- First method: constant k_S

Given R_2 (smaller voltage divider resistor), k_S (current sensor sensitivity) and the target meter constant pulse C_P (pulses/kWh) as input of the calculations, the value of the voltage divider resistor R_1 comes from the following formula:

Equation 23

$$R_1 = R_2\left(\frac{1800 \cdot k_S \cdot A_V \cdot A_I \cdot cal_V \cdot cal_I \cdot DClk}{V_{ref}^2 \cdot C_P} - 1\right)[\Omega]$$

- Second method: constant R1

Given R_1, R_2 (voltage divider resistors) and C_P target meter constant pulse (pulses/kWh) as input of the calculations, the value of k_S current sensor comes from the following formula:

Equation 24

$$k_S = \frac{V_{ref}^2 \cdot C_P \cdot \left(1 + {}^{R_1}/_{R_2}\right)}{1800 \cdot A_V \cdot A_I \cdot cal_V \cdot cal_I \cdot DClk}\,[mV/A]$$

Note: The resistor (the former) or the current channel sensor sensitivity (the latter) must be chosen as closer as possible to the target; small tolerance is compensated by the calibration, to reach the target constant pulse C_P

With the above external components, the maximum measurable values of RMS voltage and current are:

Equation 25

$$V_{MAX} = \frac{1}{2} \cdot \frac{V_{ref}}{A_V \cdot \sqrt{2}} \cdot \frac{R_1 + R_2}{R_2}\ [V]$$

Equation 26

$$I_{MAX} = \frac{1}{2} \cdot \frac{V_{ref}}{A_I \cdot \sqrt{2}} \cdot \frac{1}{k_S}\ [A]$$

These values are calculated leaving some available room for the input range with the peak value and minimizing modulator distortions.

The current resolution value is equal to 4 times LSB_{IRMS}:

Equation 27

$$I_{MIN} = \frac{V_{ref}}{cal_I \cdot A_I \cdot 2^{15} \cdot k_S \cdot k_{int}}[A]$$

Example: current transformer case

This example shows the correct dimensioning of a meter using a current transformer having the following specification:

Table 34. Example 1 design data

Parameter	Value
V_N nominal voltage	230 V_{RMS}
I_N nominal current	5 A_{RMS}
I_{Max} maximum current	40 A_{RMS}
C_P constant pulses	1000 imp/kWh

The dimension of the voltage channel considers the voltage divider resistor values as 770 kΩ and 470 Ω.

Setting C_P = 64000 pulses/kWh (at LPWx = 1 - device default value) and according to calculation above the following values are:

Table 35. Example 1 calculated data

Parameter	Value
Current sensor sensitivity	$k_S = \frac{V_{ref}^2 \cdot C_P \cdot (1 + R_1/R_2)}{1800 \cdot DClk \cdot A_V \cdot A_I \cdot cal_V \cdot cal_I} = 3.51 mV/A$
LED frequency at P_N	$LED_f = \frac{C_P \cdot V_N \cdot I_N}{3600000} = 20.44 Hz$
V_{MAX}	$V_{MAX} = \frac{1}{2} \cdot \frac{V_{ref}}{A_V \cdot \sqrt{2}} \cdot \frac{R_1 + R_2}{R_2} = 347{,}8V$
I_{MAX}	$I_{MAX} = \frac{1}{2} \cdot \frac{V_{ref}}{A_I \cdot \sqrt{2}} \cdot \frac{1}{k_S} = 60{,}5\ A$
I_{MIN}	$I_{MIN} = \frac{V_{ref}}{cal_I \cdot A_I \cdot 2^{15} \cdot k_S \cdot k_{int}} = 5.97\ mA$
LSB_P	$LSB_P = \frac{V_{ref}^2 \cdot (1 + R_1/R_2)}{k_{int} \cdot A_V \cdot A_I \cdot k_S \cdot cal_V \cdot cal_I \cdot 2^{28}} = 0.818 mW/LSB$
LSB_E	$LSB_E = \frac{V_{ref}^2 \cdot (1 + R_1/R_2)}{3600 \cdot DClk \cdot k_{int} \cdot A_V \cdot A_I \cdot k_S \cdot cal_V \cdot cal_I \cdot 2^{17}} = 0.214 mWs/LSB$

To set the desired LED pulse output, division factor LED_PWM can be set through LPWx[3:0] bits in **DSP_CR1** and **DSP_CR2** configuration registers.

Table 36. LPWx bits, Cp, LED frequency relationships

LPWx	LED_PWM	C_P [imp/kWh]	LED at P_{Nom} [Hz]	Pulse value [Ws]
0000	0.0625	1024000	327.11	3.52
0001	0.125	512000	163.56	7.03
0010	0.25	256000	81.78	14.06
0011	0.5	128000	40.89	28.13
0100	**1**	**64000**	**20.44**	**56.25**
0101	2	32000	10.22	112.50
0110	4	16000	5.11	225
0111	8	8000	2.56	450
1000	16	4000	1.28	900
1001	32	2000	0.64	1800
1010	**64**	**1000**	**0.32**	**3600**
1011	128	500	0.16	7200
1100	256	250	0.08	14400
1101	512	125	0.04	28800
1110	1024	62.5	0.02	57600
1111	2048	31.25	0.01	115200

The closer value to desired C_P is given by setting LPWx divider to 1010.

Any tolerance producing small variation of C_P from 1000 imp/kWh can be compensated by calibration: setting CHV and CHC bits.

9.2 Application calibration

The meter has to be calibrated so to compensate external component tolerances and internal V_{REF} possible drift.

After the calibration, a meter using the STPM3x can reach IEC class 0.2 accuracy, taking into account that the component choice follows the rules explained above, and the layout and signal routing minimize the noise capture.

9.2.1 Voltage and current calibration (CHVx, CHCx bits)

Thanks to the device internal architecture and linearity, all calculated values (RMS, energies and power) can be calibrated in a single point, just calibrating voltage and current streams.

For this purpose, a known nominal voltage V_N and current I_N must be applied to the meter under calibration.

Referring to *Section 9.1* and *Section 5 on page 24*, having R_1 or k_S calculated as stated in the previous section, the target values of voltage and current RMS registers, X_V and X_I respectively are calculated as follows:

Table 37. Calibration target values

Parameter	Value
Voltage register value at V_N	$X_V = \frac{V_N \cdot A_V \cdot cal_V \cdot 2^{15}}{V_{ref} \cdot (1 + R_1 / R_2)}$
Current register value at I_N	$X_I = \frac{I_N \cdot A_I \cdot cal_I \cdot k_S \cdot 2^{17}}{V_{ref}}$

Note: *For the above calculation, the calculated value of the component k_S or R_1 (according to the chosen design method) must be used; the difference of the real component is compensated by calibration as a tolerance.*

To start calibration, the device has to be programmed with the proper gain and current sensor; moreover, to obtain the greatest correction dynamic, calibrators are initially set in the middle of their range (0x800), thus obtaining a calibration range of ± 12.5% per voltage or current channel.

After applying V_N and current I_N to the meter, a certain number of voltage and current RMS samples must be read and averaged (please, refer to averaged register values as V_{AV} and I_{AV}) to calculate voltage and channel calibrators as follows:

Table 38. Calibrator calculation

Parameter	Value	
Calibrator value	$CHV = 14336 \cdot \frac{X_V}{V_{AV}} - 12288$	$CHC = 14336 \cdot \frac{X_I}{I_{AV}} - 12288$
Correction factor	$K_V = 0{,}125 \cdot \frac{CHV}{2048} + 0{,}75$	$K_I = 0{,}125 \cdot \frac{CHI}{2048} + 0{,}75$

The above procedure must be repeated for all voltage/current channels.

9.2.2 Phase calibration (PHVx, PHCx bits)

The STPM3x does not introduce any phase shift between voltage and current channels.

However, the voltage and current signals come from transducers, which could have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a current transformer (CT). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors.

The phase compensation block provides a method of digital phase correction of the phase shifting between voltage and current channels which can be introduced by the external component intrinsic characteristics or by external component mismatch. The amount of phase compensation can be set per each channel, and it is executed delaying the currents and voltage samples using bits of the phase calibration configurators: PHCx[9:0] and PHVx[1:0].

These registers act in the same way by delaying the desired waveform by a certain quantity given from the equations below in degree:

Table 39. Phase-delay

Parameter	Value
Current shift	$\varphi_C = \frac{f_{line}}{\mathrm{SCLK}} \cdot \mathrm{PHCx}[9:0] \cdot 360°$
Voltage shift	$\varphi_V = \frac{f_{line}}{\mathrm{SCLK}} \cdot \mathrm{PHVx}[1:0] \cdot 2^9 \cdot 360°$
Global phase shift	$\varphi = \frac{f_{line}}{\mathrm{SCLK}} \cdot (\mathrm{PHCx}[9:0] - \mathrm{PHVx}[1:0] \cdot 2^9) \cdot 360°$

A capacitive behavior is determined by the current leading the voltage waveform to a certain angle. In this case, there is the compensation by delaying the current waveform by the same angle through PHCx register. For a 50 Hz line the current channel waveform maximum delayed is:

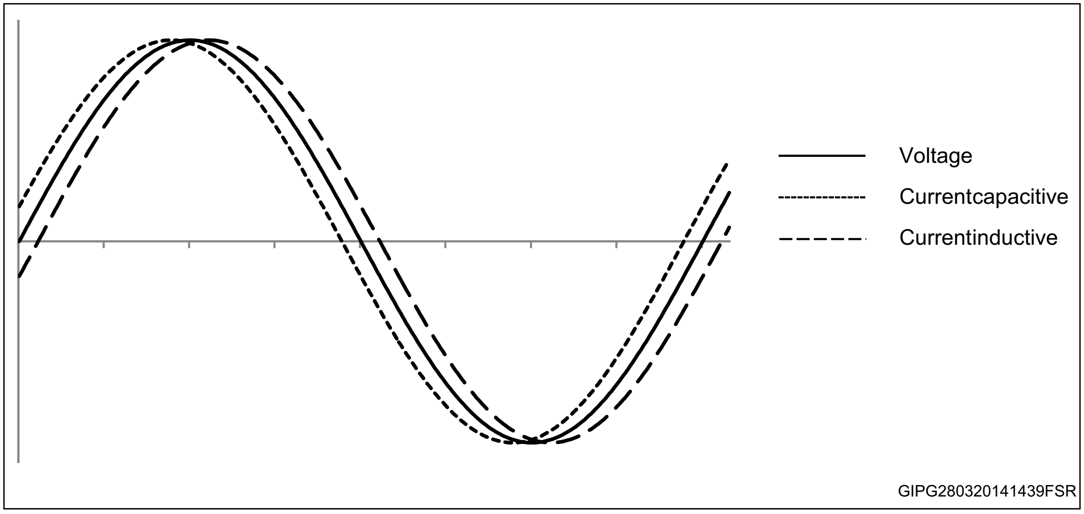
$\varphi_C \leq 4.6035°$ with step $\Delta\varphi_C = 0.0045°$

An inductive behavior has the opposite effect, so that current lags the voltage waveform. In this case, PHV register delays the voltage waveform by the minimum angle to invert the behavior to capacitive and then acting on PHCx register for the fine tuning of the current waveform.

PHV impacts on the calculation of power and energies related to both current channels. For a 50 Hz line, the voltage channel waveform maximum delayed is:

$\varphi_V \leq 6.912°$ with step $\Delta\varphi_V = 2.304°$.

Figure 53. Phase shift error



The θ angle can be measured through the error on active power (from LED) averaged over a certain number of samples (for example 50) at power factor PF = 0,5.

For example, if the error = e, the phase shift between voltage and current is:

Equation 28

$$\theta = \arccos\left(\frac{1+e}{2}\right) - 60°$$

To compensate this error, PHC and PHV bits must be set as below, to introduce a correction factor φ = -θ.

Table 40. Phase compensation

Parameter	Value
$\varphi \ge 0$	PHVx = 0x0 $PHCx = \frac{\varphi \cdot SCLK}{360 \cdot f_{line}}$
$-\frac{f_{line}}{SCLK} \cdot 2^9 \cdot 360° \le \varphi < 0$	PHVx = 0x1 PHCx[9] = 0x0 $PHCx[8:0] = PHVx \cdot 2^9 + \frac{\varphi \cdot SCLK}{360° \cdot f_{line}}$
$-\frac{f_{line}}{SCLK} \cdot 2^{10} \cdot 360° \le \varphi < -\frac{f_{line}}{SCLK} \cdot 2^9 \cdot 360°$	PHVx = 0x2 PHCx[9] = 0 $PHCx[8:0] = PHVx \cdot 2^{10} + \frac{\varphi \cdot SCLK}{360° \cdot f_{line}}$
$-\frac{f_{line}}{SCLK} \cdot 2^9 \cdot 3 \cdot 360° \le \varphi < -\frac{f_{line}}{SCLK} \cdot 2^{10} \cdot 360°$	PHVx = 0x3 PHCx[9] = 0 $PHCx[8:0] = PHVx \cdot 2^9 + \frac{\varphi \cdot SCLK}{360° \cdot f_{line}}$

9.2.3 Power offset calibration (OFAx, OFAFx, OFRx, OFSx bits)

The device has the power offset compensation register for all measured powers (active, active fundamental, reactive and apparent) to compensate, for each channel, the power measured due to noise capture in the application.

Power registers are signed values, (MSB is the sign and negative values are two's complemented); the power offset registers are also signed registers with LSB value equal to 4 times the power LSB:

Table 41. Power offset LSB

Parameter	Value
Power LSB value	$LSB_P = \frac{V_{ref}^2 \cdot (1 + R_1 / R_2)}{K_{int} \cdot A_V \cdot A_I \cdot k_S \cdot cal_V \cdot cal_I \cdot 2^{28}} \left[\frac{w}{LSB}\right]$
Power offset LSB value	$LSB_{PO} = LSB_P \cdot 2^2 = \frac{V_{ref}^2 \cdot (1 + R_1 / R_2)}{K_{int} \cdot A_V \cdot A_I \cdot k_S \cdot cal_V \cdot cal_I \cdot 2^{28}} \cdot 2^2 \left[\frac{w}{LSB}\right]$

Power offset can be compensated by measuring the power value when the current I = 0, if the average value is not null; the value is due to external influences, then an opposite value should be applied to the power offset register.

Register map

There are three types of data register:

- RW: read and written by application (in orange in the picture below)
- RWL: the status bits, set from DSP, must be latched to read updated content, and must be cleared by the application (in orange in the picture below)
- RL: read registers only, they contain measured data and are continuously updated by DSP, so they need to be latched before reading (in blue in the picture below)

The following nomenclature is used in the above registers:

10 Register map

There are three types of data register:

- RW: read and written by application (in orange in the picture below)
- RWL: the status bits, set from DSP, must be latched to read updated content, and must be cleared by the application (in orange in the picture below)
- RL: read registers only, they contain measured data and are continuously updated by DSP, so they need to be latched before reading (in blue in the picture below)

The following nomenclature is used in the above registers:

- A: active wideband
- F: active fundamental
- R: reactive
- S: apparent

10.1 Register map graphical representation

Table 42. Register map

<table>
<tr><th rowspan="4">Row</th><th rowspan="4">Address</th><th rowspan="4">(R)ead
(W)rite
(L)atch</th><th colspan="32">Index</th><th rowspan="4">Names</th><th rowspan="4">Default values</th></tr>
<tr><th colspan="16">MSW [31:16]</th><th colspan="16">LSW [15:0]</th></tr>
<tr><th colspan="8">MSB [31:24]</th><th colspan="8">LSB [23:16]</th><th colspan="8">MSB [15:8]</th><th colspan="8">LSB [7:0]</th></tr>
<tr><th colspan="4">31:28</th><th colspan="4">27:24</th><th colspan="4">23:20</th><th colspan="4">19:16</th><th colspan="4">15:12</th><th colspan="4">11:8</th><th colspan="4">7:4</th><th colspan="4">3:0</th></tr>
<tr><td rowspan="3">0</td><td rowspan="3">00</td><td rowspan="3">RW</td><td colspan="32">DSP control register #1</td><td rowspan="3">dsp_cr1</td><td rowspan="3">040000A0</td></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">LCS1[1:0]</td><td colspan="2">LPS1[1:0]</td><td colspan="4">LPW1 [3:0]</td><td colspan="2"></td><td>ROC1</td><td>BHPFC1</td><td>BHPFV1</td><td>APM1</td><td>AEM1</td><td colspan="8"></td><td colspan="3">TC1[2:0]</td><td>ENVREF1</td><td>ClearSS1</td><td colspan="4">CLRSS1_TO1[3:0]</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">02</td><td rowspan="3">RW</td><td colspan="32">DSP control register #2</td><td rowspan="3">dsp_cr2</td><td rowspan="3">240000A0</td></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">LCS2[1:0]</td><td colspan="2">LPS2[1:0]</td><td colspan="4">LPW2 [3:0]</td><td colspan="2"></td><td>ROC2</td><td>BHPFC2</td><td>BHPFV2</td><td>APM2</td><td>AEM2</td><td colspan="8"></td><td colspan="3">TC2[2:0]</td><td>ENVREF2</td><td>ClearSS2</td><td colspan="4">CLRSS2_TO2[3:0]</td></tr>
</table>

Table 42. Register map (continued)

<table>
<tr><th rowspan="4">Row</th><th rowspan="4">Address</th><th rowspan="4">(R)ead (W)rite (L)atch</th><th colspan="32">Index</th><th rowspan="4">Names</th><th rowspan="4">Default values</th></tr>
<tr><th colspan="16">MSW [31:16]</th><th colspan="16">LSW [15:0]</th></tr>
<tr><th colspan="8">MSB [31:24]</th><th colspan="8">LSB [23:16]</th><th colspan="8">MSB [15:8]</th><th colspan="8">LSB [7:0]</th></tr>
<tr><th colspan="4">31:28</th><th colspan="4">27:24</th><th colspan="4">23:20</th><th colspan="4">19:16</th><th colspan="4">15:12</th><th colspan="4">11:8</th><th colspan="4">7:4</th><th colspan="4">3:0</th></tr>
<tr><td rowspan="3">2</td><td rowspan="3">04</td><td rowspan="3">RW</td><td colspan="32">DSP control register #3</td><td rowspan="3">dsp_cr3</td><td rowspan="3">000004E0</td></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4"></td><td>REF_FREQ</td><td>EN_CUM</td><td>LED_OFF2</td><td>LED_OFF1</td><td>S/W Auto Latch</td><td>S/W latch2</td><td>S/W latch1</td><td>S/W reset</td><td>TMP_EN</td><td colspan="2">TMP_TOL[1:0]</td><td>ZCR_EN</td><td colspan="2">ZCR_SEL[1:0]</td><td colspan="14">SAG_TIME_THR[13:0]</td></tr>
<tr><td>3</td><td>06</td><td>RW</td><td colspan="8"></td><td colspan="2">PHV1[1:0]</td><td colspan="10">PHC1[9:0]</td><td colspan="2">PHV2[1:0]</td><td colspan="10">PHC2[9:0]</td><td>dsp_cr4</td><td>00000000</td></tr>
<tr><td>4</td><td>08</td><td>RW</td><td colspan="10">SAG_THR1 [9:0]</td><td colspan="10">SWV_THR1 [9:0]</td><td colspan="12">CHV1 [11:0]</td><td>dsp_cr5</td><td>003FF800</td></tr>
<tr><td>5</td><td>0A</td><td>RW</td><td colspan="10"></td><td colspan="10">SWC_THR1 [9:0]</td><td colspan="12">CHC1 [11:0]</td><td>dsp_cr6</td><td>003FF800</td></tr>
<tr><td>6</td><td>0C</td><td>RW</td><td colspan="10">SAG_THR2 [9:0]</td><td colspan="10">SWV_THR2 [9:0]</td><td colspan="12">CHV2 [11:0]</td><td>dsp_cr7</td><td>003FF800</td></tr>
<tr><td>7</td><td>0E</td><td>RW</td><td colspan="10"></td><td colspan="10">SWC_THR2 [9:0]</td><td colspan="12">CHC2 [11:0]</td><td>dsp_cr8</td><td>003FF800</td></tr>
<tr><td>8</td><td>10</td><td>RW</td><td colspan="10">OFAF1 [9:0]</td><td colspan="10">OFA1 [9:0]</td><td colspan="12">AH_UP1 [11:0]</td><td>dsp_cr9</td><td>00000FFF</td></tr>
<tr><td>9</td><td>12</td><td>RW</td><td colspan="10">OFS1 [9:0]</td><td colspan="10">OFR1 [9:0]</td><td colspan="12">AH_DOWN1 [11:0]</td><td>dsp_cr10</td><td>00000FFF</td></tr>
</table>

Table 42. Register map (continued)

<table>
<tr><th rowspan="4">Row</th><th rowspan="4">Address</th><th rowspan="4">(R)ead (W)rite (L)atch</th><th colspan="32">Index</th><th rowspan="4">Names</th><th rowspan="4">Default values</th></tr>
<tr><th colspan="16">MSW [31:16]</th><th colspan="16">LSW [15:0]</th></tr>
<tr><th colspan="8">MSB [31:24]</th><th colspan="8">LSB [23:16]</th><th colspan="8">MSB [15:8]</th><th colspan="8">LSB [7:0]</th></tr>
<tr><th colspan="4">31:28</th><th colspan="4">27:24</th><th colspan="4">23:20</th><th colspan="4">19:16</th><th colspan="4">15:12</th><th colspan="4">11:8</th><th colspan="4">7:4</th><th colspan="4">3:0</th></tr>
<tr><td>10</td><td>14</td><td>RW</td><td colspan="10">OFAF2 [9:0]</td><td colspan="10">OFA2 [9:0]</td><td colspan="12">AH_UP2 [11:0]</td><td>dsp_cr11</td><td>00000FFF</td></tr>
<tr><td>11</td><td>16</td><td>RW</td><td colspan="10">OFS2 [9:0]</td><td colspan="10">OFR2 [9:0]</td><td colspan="12">AH_DOWN2 [11:0]</td><td>dsp_cr12</td><td>00000FFF</td></tr>
<tr><td rowspan="3">12</td><td rowspan="3">18</td><td rowspan="3">RW</td><td colspan="32">DFE Control Register 1 [31:0]</td><td rowspan="3">dfe_cr1</td><td rowspan="3">0F270327</td></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4"></td><td colspan="2">GAIN1[1:0]</td><td colspan="9"></td><td>enC1</td><td colspan="15"></td><td>enV1</td></tr>
<tr><td rowspan="3">13</td><td rowspan="3">1A</td><td rowspan="3">RW</td><td colspan="32">DFE Control Register 2 [31:0]</td><td rowspan="3">dfe_cr2</td><td rowspan="3">03270327</td></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4"></td><td colspan="2">GAIN1[2:0]</td><td colspan="9"></td><td>enC2</td><td colspan="15"></td><td>enV2</td></tr>
</table>

Table 42. Register map (continued)

Row	Address	(R)ead (W)rite (L)atch	Index								Names	Default values
			MSW [31:16]				LSW [15:0]					
			MSB [31:24]		LSB [23:16]		MSB [15:8]		LSB [7:0]			
			31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0		
14	1C	RW	DSP IRQ (Interrupt Control Mask) Register #1								dsp_irq1	00000000
			31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0		
			V1 IRQ CR [7:0]		C1 IRQ CR[3:0]	PH1 IRQ CR[7:0]		PH2 IRQ CR [7:0]		PH1+PH2 IRQ CR[3:0]		
15	1E	RW	DSP IRQ (interrupt control mask) register #2								dsp_irq2	00000000
			31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0		
			V2 IRQ CR [7:0]		C2 IRQ CR[3:0]	PH1 IRQ CR [7:0]		PH2 IRQ CR [7:0]		PH1+PH2 IRQ CR[3:0]		

Table 42. Register map (continued)

Row	Address	(R)ead (W)rite (L)atch	Index																																Names	Default values
			MSW [31:16]																LSW [15:0]																	
			MSB [31:24]								LSB [23:16]								MSB [15:8]								LSB [7:0]									
			31:28				27:24				23:20				19:16				15:12				11:8				7:4				3:0					
16	20	RWL	DSP Status Register #1																																dsp_sr1	00000000
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
			TAMPER OR WRONG	PH1 TAMPER	V1						C1				PH1								PH2								PH1+PH2					
					Swell End	Swell Start	Sag End	Sag Start	Per ERR	Signal Stuck	Swell End	Swell Start	Nah	Signal Stuck	Energy Overflow				Power Sign				Energy Overflow				Power Sign				Energy Overflow		Power Sign			
															S	R	F	A	S	R	F	A	S	R	F	A	S	R	F	A	R	A	R	A		

Table 42. Register map (continued)

Row	Address	(R)ead (W)rite (L)atch	Index																																Names	Default values
			MSW [31:16]																LSW [15:0]																	
			MSB [31:24]								LSB [23:16]								MSB [15:8]								LSB [7:0]									
			31:28				27:24				23:20				19:16				15:12				11:8				7:4				3:0					
17	22	RWL	DSP Status Register #2																																dsp_sr2	00000000
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
			TAMPER OR WRONG	PH2 TAMPER	V2						C2				PH1								PH2								PH1+PH2					
					Swell End	Swell Start	Sag End	Sag Start	Per ERR	Signal Stuck	Swell End	Swell Start	Nah	Signal Stuck	Energy Overflow				Power Sign				Energy Overflow				Power Sign				Energy Overflow		Power Sign			
															S	R	F	A	S	R	F	A	S	R	F	A	S	R	F	A	R	A	R	A		

Table 42. Register map (continued)

Row	Address	(R)ead (W)rite (L)atch	Index																																Names	Default values
			MSW [31:16]																LSW [15:0]																	
			MSB [31:24]								LSB [23:16]								MSB [15:8]								LSB [7:0]									
			31:28				27:24				23:20				19:16				15:12				11:8				7:4				3:0					
18	24	RW	UART & SPI Control Register #1																																us_reg1	00004007
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
											Time Out [7:0] (ms)								lsbfirst	crcen					Break on Err	Noise en	CRC Polynomial [7:0]									
19	26	RW	UART & SPI Control Register #2																																us_reg2	00000683
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
											Frame Delay [7:0]								Baud rate (ufix16_en4)																	

Table 42. Register map (continued)

Row	Address	(R)ead (W)rite (L)atch	Index																																Names	Default values
			MSW [31:16]																LSW [15:0]																	
			MSB [31:24]								LSB [23:16]								MSB [15:8]								LSB [7:0]									
			31:28				27:24				23:20				19:16				15:12				11:8				7:4				3:0					
20	28	RW	UART & SPI IRQ Register																																us_reg3	00000000
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
			UART & SPI IRQ Status Register																UART & SPI IRQ Control Register																	
				overrun	underrun	crc error	write error	read error	tx empty	rx full		tx ovr	rx ovr	noise err	frame err	time-out err	crc error	Break		overrun	underrun	crc error	write error	read error	tx empty	rx full		tx ovr	rx ovr	noise err	frame err	time-out err	crcerror			
21	2A	RL	DSP live events #1																																dsp_ev1	00000000
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
					V1											C1							PH1								PH1+PH2					
					SAG1_EV[3:0]				SWV1_EV[3:0]				Per ERR	Signal stuck	ZCR	SWC1_EV[3:0]				Nah	Signal Stuck	ZCR	Energy Overflow				Power Sign				Energy Overflow		Power Sign			
																							S	R	F	A	S	R	F	A	R	A	R	A		

Table 42. Register map (continued)

Row	Address	(R)ead (W)rite (L)atch	Index																																Names	Default values
			MSW [31:16]																LSW [15:0]																	
			MSB [31:24]								LSB [23:16]								MSB [15:8]								LSB [7:0]									
			31:28				27:24				23:20				19:16				15:12				11:8				7:4				3:0					
22	2C	RL	DSP live events #2																																dsp_ev2	00000000
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
					V2											C2							PH2								PH1+PH2					
					SAG2_EV[3:0]				SWV2_EV[3:0]				Per ERR	Signal Stuck	ZCR	SWC2_EV[3:0]				Nah	Signal Stuck	ZCR	Power Sign				Power Sign				Energy Overflow		Power Sign			
																							S	R	F	A	S	R	F	A	R	A	R	A		
23	2E	RL					PH2 Period [11:0]																PH1 Period [11:0]												dsp_reg1	00000000
24	30	RL	Padding								V1 Data [23:0]																								dsp_reg2	00000000
25	32	RL	Padding								C1 Data [23:0]																								dsp_reg3	00000000
26	34	RL	Padding								V2 Data [23:0]																								dsp_reg4	00000000
27	36	RL	Padding								C2 Data [23:0]																								dsp_reg5	00000000
28	38	RL	Padding								V1 Fund [23:0]																								dsp_reg6	00000000

Table 42. Register map (continued)

Row	Address	(R)ead (W)rite (L)atch	Index								Names	Default values
			MSW [31:16]				LSW [15:0]					
			MSB [31:24]		LSB [23:16]		MSB [15:8]		LSB [7:0]			
			31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0		
29	3A	RL	Padding		C1 Fund [23:0]						dsp_reg7	00000000
30	3C	RL	Padding		V2 Fund [23:0]						dsp_reg8	00000000
31	3E	RL	Padding		C2 Fund [23:0]						dsp_reg9	00000000
32	40	RL									dsp_reg10	00000000
33	42	RL									dsp_reg11	00000000
34	44	RL									dsp_reg12	00000000
35	46	RL									dsp_reg13	00000000
36	48	RL	C1 RMS Data [16:0]				V1 RMS Data [14:0]				dsp_reg14	00000000
37	4A	RL	C2 RMS Data [16:0]				V2 RMS Data [14:0]				dsp_reg15	00000000
38	4C	RL	SAG1_TIME [14:0]				SWV1_TIME [14:0]				dsp_reg16	00000000
39	4E	RL		C1_PHA[11:0]			SWC1_TIME [14:0]				dsp_reg17	00000000
40	50	RL	SAG2_TIME [14:0]				SWV2_TIME [14:0]				dsp_reg18	00000000

Table 42. Register map (continued)

Row	Address	(R)ead (W)rite (L)atch	Index								Names	Default values
			MSW [31:16]				LSW [15:0]					
			MSB [31:24]		LSB [23:16]		MSB [15:8]		LSB [7:0]			
			31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0		
41	52	RL		C2_PHA[11:0]			SWC2_TIME [14:0]				dsp_reg19	00000000
42	54	RL	PH1 Active Energy								ph1_reg1	00000000
43	56	RL	PH1 Fundamental Energy								ph1_reg2	00000000
44	58	RL	PH1 Reactive Energy								ph1_reg3	00000000
45	5A	RL	PH1 Apparent Energy								ph1_reg4	00000000
46	5C	RL	PH1 Active Power[28:0]								ph1_reg5	00000000
47	5E	RL	PH1 Fundamental Power[28:0]								ph1_reg6	00000000
48	60	RL	PH1 Reactive Power[28:0]								ph1_reg7	00000000
49	62	RL	PH1 Apparent RMS Power[28:0]								ph1_reg8	00000000
50	64	RL	PH1 Apparent Vectorial Power[28:0]								ph1_reg9	00000000
51	66	RL	PH1 Momentary Active Power[28:0]								ph1_reg10	00000000
52	68	RL	PH1 Momentary Fundamental Power[28:0]								ph1_reg11	00000000
53	6A	RL	PH1 AH_ACC								ph1_reg12	00000000

Table 42. Register map (continued)

Row	Address	(R)ead (W)rite (L)atch	Index								Names	Default values
			MSW [31:16]				LSW [15:0]					
			MSB [31:24]		LSB [23:16]		MSB [15:8]		LSB [7:0]			
			31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0		
54	6C	RL	PH2 Active Energy								ph2_reg1	00000000
55	6E	RL	PH2 Fundamental Energy								ph2_reg2	00000000
56	70	RL	PH2 Reactive Energy								ph2_reg3	00000000
57	72	RL	PH2 Apparent Energy								ph2_reg4	00000000
58	74	RL	PH2 Active Power[28:0]								ph2_reg5	00000000
59	76	RL	PH2 Fundamental Power[28:0]								ph2_reg6	00000000
60	78	RL	PH2 Reactive Power[28:0]								ph2_reg7	00000000
61	7A	RL	PH2 Apparent RMS Power[28:0]								ph2_reg8	00000000
62	7C	RL	PH2 Apparent Vectorial Power[28:0]								ph2_reg9	00000000
63	7E	RL	PH2 Momentary Active Power[28:0]								ph2_reg10	00000000
64	80	RL	PH2 Momentary Fundamental Power[28:0]								ph2_reg11	00000000
65	82	RL	PH2 AH_ACC								ph2_reg12	00000000
66	84	RL	Total Active Energy								tot_reg1	00000000

Table 42. Register map (continued)

Row	Address	(R)ead (W)rite (L)atch	Index								Names	Default values
			MSW [31:16]				LSW [15:0]					
			MSB [31:24]		LSB [23:16]		MSB [15:8]		LSB [7:0]			
			31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0		
67	86	RL	Total Fundamental Energy								tot_reg2	00000000
68	88	RL	Total Reactive Energy								tot_reg3	00000000
69	8A	RL	Total Apparent Energy								tot_reg4	00000000

Table 43. Register map legend

Read/Write bit	RESERVED	Read	Active Energy/Power	Fundamental Energy/Power	Reactive Energy/Power	Apparent Energy/Power
■	□	🟦	A	F	R	S

10.2 Configuration register

Table 44. Row 0, DSP control register 1 (DSP_CR1)

Bit	Internal signal	Description	Default
[3:0]	CLRSS_TO1	Set duration of primary channel reset signal to clear sag and swell registers	0x0
4	ClearSS1	Clear sag and swell time register and history bits for primary channel, auto-reset to '0'	0x0
5	ENVREF1	Enable internal voltage reference for primary channel: 0: reference disabled – external V_{REF} required 1: reference enabled	0x1
[8:6]	TC1	Temperature compensation coefficient selection for primary channel voltage reference V_{REF1} (see *Table 9 on page 32*)	0x2
[16:9]	-	Reserved	0x0
17	AEM1	Apparent energy mode for primary channel: 0: use apparent RMS power 1: use apparent vectorial power	0x0
18	APM1	Apparent vectorial power mode for primary channel: 0: use fundamental power 1: use active power	0x0
19	BHPFV1	Bypass hi-pass filter for primary voltage channel: 0: HPF enabled 1: HPF bypassed	0x0
20	BHPFC1	Bypass hi-pass filter for primary current channel: 0: HPF enabled 1: HPF bypassed	0x0
21	ROC1	Add Rogowski integrator to primary current channel filtering pipeline: 0: integrator bypassed 1: integrator enabled	0x0
[23:22]	-	Reserved	0x0
[27:24]	LPW1	LED1 speed dividing factor: 0x0 = 2^(-4), 0xF = 2^11 Default 0x4 = 1	0x4
[29:28]	LPS1	LED1 pulse-out power selection: LPS1 [1:0]: 00,01,10,11 LED1 output: active, fundamental, reactive, apparent	0x0
[31:30]	LCS1	**LED1 pulse-out channel selection:** LCS1 [1:0]: 00,01,10,11 LED1: primary channels, secondary channels, cumulative, sigma-delta bitstream	0x0

Table 45. Row 1, DSP control register 2 (DSP_CR2)

Bit	Internal signal	Description	Default
[3:0]	CLRSS_TO2	Set duration of secondary channel reset signal to clear sag and swell registers	0x0
4	ClearSS2	Clear sag and swell time register and history bits for secondary channel, auto-reset to 0	0x0
5	ENVREF2	Enable internal voltage reference for secondary channel: 0: reference disabled – external V_{REF} required 1: reference enabled	0x1
[8:6]	TC2	Temperature compensation coefficient selection for secondary channel voltage reference V_{REF2} (see *Table 9 on page 32*)	0x2
[16:9]	-	Reserved	0x0
17	AEM2	Apparent energy mode for secondary channel: 0: use apparent RMS power 1: use apparent vectorial power	0x0
18	APM2	Apparent vectorial power mode for secondary channel: 0: use fundamental power 1: use active power	0x0
19	BHPFV2	Bypass hi-pass filter for secondary voltage channel: 0: HPF enabled 1: HPF bypassed	0x0
20	BHPFC2	Bypass hi-pass filter for secondary current channel: 0: HPF enabled 1: HPF bypassed	0x0
21	ROC2	Add Rogowski integrator to secondary current channel filtering pipeline: 0: integrator bypassed 1: integrator enabled	0x0
[23:22]	-	Reserved	0x0
[27:24]	LPW2	LED2 speed dividing factor: 0x0 = 2^(-4), 0xF = 2^11 Default 0x4 = 1	0x4
[29:28]	LPS2	**LED2 pulse-out power selection:** LPS2 [1:0]: 00,01,10,11 LED2: output, active, fundamental, reactive, apparent	0x2
[31:30]	LCS2	**LED2 pulse-out channel selection:** LCS2 [1:0]: 00,01,10,11 LED2: secondary channels, algebraic, sigma-delta bitstream	0x0

Table 46. Row 2, DSP control register 3 (DSP_CR3)

Bit	Internal signal	Description	Default
[13:0]	TIME_VALUE	Time counter threshold for voltage sag detection	0x4E0
[15:14]	ZCR_SEL	Selection bit for ZCR/CLK pin, (output depends on ZCR/CLK enable bit): **ZCR_SEL[1:0]**: 00, 01, 10, 11 **ZCR**: V1, C1, V2, C2 **CLK**: 7.8125 kHz, 4 MHz, 4 MHz, 50% duty cycle, 16 MHz	0x0
16	ZCR_EN	ZCR/CLK pin output: 0: CLK 1: ZCR	0x0
[18:17]	TMP_TOL	Selection bits for tamper tolerance: **TMP_TOL[1:0]:** 00, 01, 10, 11 **Tolerance:** 12.5%, 8.33%, 6.25%, 3.125%	0x0
19	TMP_EN	Enable tampering feature: 0: tamper disable 1: tamper enable	0x0
20	S/W reset	SW reset brings the configuration registers to default This bit is set to zero after this action automatically	0
21	S/W latch1	Primary channel measurement register latch This bit is set to zero after this action automatically	0
22	S/W latch2	Secondary channel measurement register latch his bit is set to zero after this action automatically	0
23	S/W Auto Latch	Automatic measurement register latch at 7.8125 kHz	0
24	LED1OFF	LED1 pin output disable 0: LED1 output on 1: LED1 output disabled When the LED output is disabled the pin is set at low-state	0
25	LED2OFF	LED2 pin output disable 0: LED2 output on 1: LED2 output disabled When the LED output is disabled the pin is set at low-state	0
26	EN_CUM	Cumulative energy calculation 0: cumulative is the sum of channel energies 1: total is the difference of energies	0
27	REF_FREQ	Reference line frequency: 0: 50 Hz 1: 60 Hz	0
[31:28]	-	Reserved	0

Table 47. Row 3, DSP control register 4 (DSP_CR4)

Bit	Internal signal	Description	Default
[9:0]	PHC2	Secondary current channel phase compensation register	0x0
[11:10]	PHV2	Secondary voltage channel phase compensation register	0x0
[21:12]	PHC1	Primary current channel phase compensation register	0x0
[23:22]	PHV1	Primary voltage channel phase compensation register	0x0
[31:24]	-	Reserved	0x0

Table 48. Row 4, DSP control register 5 (DSP_CR5)

Bit	Internal signal	Description	Default
[11:0]	CHV1	Calibration register of primary voltage channel	0x800
[21:12]	SWV_THR1	Swell threshold of primary voltage channel	0x3FF
[31:22]	SAG_THR1	Sag threshold of primary voltage channel	0x0

Table 49. Row 5, DSP control register 6 (DSP_CR6)

Bit	Internal signal	Description	Default
[11:0]	CHC1	Calibration register of primary current channel	0x800
[21:12]	SWC_THR1	Swell threshold of primary current channel	0x3FF
[31:22]	-	Reserved	0x0

Table 50. Row 6, DSP control register 7 (DSP_CR7)

Bit	Internal signal	Description	Default
[11:0]	CHV2	Calibration register of secondary voltage channel	0x800
[21:12]	SWV_THR2	Swell threshold of secondary voltage channel	0x3FF
[31:22]	SAG_THR2	Sag threshold of secondary voltage channel	0x0

Table 51. Row 7, DSP control register 8 (DSP_CR8)

Bit	Internal signal	Description	Default
[11:0]	CHC2	Calibration register of secondary current channel	0x800
[21:12]	SWC_THR2	Swell threshold of secondary current channel	0x3FF
[31:22]	-	Reserved	0x0

Table 52. Row 8, DSP control register 9 (DSP_CR9)

Bit	Internal signal	Description	Default
[11:0]	AH_UP1	Primary channel RMS upper threshold (for AH)	0xFFF
[21:12]	OFA1	Offset for primary channel active power	0x0
[31:22]	OFAF1	Offset for primary channel fundamental active power	0x0

Table 53. Row 9, DSP control register 10 (DSP_CR10)

Bit	Internal signal	Description	Default
[11:0]	AH_DOWN1	Primary channel RMS lower threshold (for AH)	0xFFF
[21:12	OFR1	Offset for primary channel reactive power	0x0
[31:22]	OFS1	Offset for primary channel apparent power	0x0

Table 54. Row 10, DSP control register 11 (DSP_CR11)

Bit	Internal signal	Description	Default
[11:0]	AH_UP2	Secondary channel RMS upper threshold (for AH)	0xFFF
[21:12]	OFA2	Offset for secondary channel active power	0x0
[31:22]	OFAF2	Offset for secondary channel fundamental active power	0x0

Table 55. Row 11, DSP control register 12 (DSP_CR12)

Bit	Internal signal	Description	Default
[11:0]	AH_DOWN2	Secondary channel RMS lower threshold (for AH)	0xFFF
[21:12]	OFR2	Offset for secondary channel reactive power	0x0
[31:22]	OFS2	Offset for secondary channel apparent power	0x0

Table 56. Row 12, digital front end control register 1 (DFE_CR1)

Bit	Internal signal	Description	Default
0	enV1	Enable for primary voltage channel	0x1
[15:1]	-	Reserved	0x193
[16]	enC1	Enable for primary current channel	0x1
[17:25]	-	Reserved	0x193
[27:26]	GAIN1	Gain selection of primary current channel: **GAIN1[1:0]:** 00, 01, 10, 11 **GAIN**: x2, x4, x8, x16	0x3
[31:28]	-	Reserved	0x0

Table 57. Row 13, digital front end control register 2 (DFE_CR2)

Bit	Internal signal	Description	Default
0	enV2	Enable for secondary voltage channel	0x1
[15:1]	-	Reserved	0x193
[16]	enC2	Enable for secondary current channel	0x1
[17:25]	-	Reserved	0x193
[27:26]	GAIN2	Gain selection of secondary current channel: **GAIN2 [1:0]:** 00, 01, 10, 11 **GAIN**: x2, x4, x8, x16	0x0
[31:28]	-	Reserved	0x0

Table 58. Row 14, DSP interrupt control mask register 1 (DSP_IRQ1)

Bit	Internal signal	Description	Default
0	PH1+PH2 IRQ CR	Sign total active power	0
1		Sign total reactive power	0
2		Overflow total active energy	0
3		Overflow total reactive energy	0
4	PH2 IRQ CR	Sign secondary channel active power	0
5		Sign secondary channel active fundamental power	0
6		Sign secondary channel reactive power	0
7		Sign secondary channel apparent power	0
8		Overflow secondary channel active energy	0
9		Overflow secondary channel active fundamental energy	0
10		Overflow secondary channel reactive energy	0
11		Overflow secondary channel apparent energy	0
12	PH1 IRQ CR	Sign primary channel active power	0
13		Sign primary channel active fundamental power	0
14		Sign primary channel reactive power	0
15		Sign primary channel apparent power	0
16		Overflow primary channel active energy	0
17		Overflow primary channel active fundamental energy	0
18		Overflow primary channel reactive energy	0
19		Overflow primary channel apparent energy	0
20	C1 IRQ CR	Primary current sigma-delta bitstream stuck	0
21		AH1 - accumulation of primary channel current	0
22		Primary current swell detected	0
23		Primary current swell end	0

Table 58. Row 14, DSP interrupt control mask register 1 (DSP_IRQ1) (continued)

Bit	Internal signal	Description	Default
24	V1 IRQ CR	Primary voltage sigma-delta bitstream stuck	0
25		Primary voltage period error	0
26		Primary voltage sag detected	0
27		Primary voltage sag end	0
28		Primary voltage swell detected	0
29		Primary voltage swell end	0
30	Tamper	Tamper on primary	0
31		Tamper or wrong connection	0

Table 59. Row 15, DSP interrupt control mask register 2 (DSP_IRQ2)

Bit	Internal signal	Description	Default
0	PH1+PH2 IRQ CR	Sign total active power	0
1		Sign total reactive power	0
2		Overflow total active energy	0
3		Overflow total reactive energy	0
4	PH2 IRQ CR	Sign secondary channel active power	0
5		Sign secondary channel active fundamental power	0
6		Sign secondary channel reactive power	0
7		Sign secondary channel apparent power	0
8		Overflow secondary channel active energy	0
9		Overflow secondary channel active fundamental energy	0
10		Overflow secondary channel reactive energy	0
11		Overflow secondary channel apparent energy	0
12	PH1 IRQ CR	Sign primary channel active power	0
13		Sign primary channel active fundamental power	0
14		Sign primary channel reactive power	0
15		Sign primary channel apparent power	0
16		Overflow primary channel active energy	0
17		Overflow primary channel active fundamental energy	0
18		Overflow primary channel reactive energy	0
19		Overflow primary channel apparent energy	0
20	C2 IRQ CR	Secondary current sigma-delta bitstream stuck	0
21		AH1 - accumulation of secondary channel current	0
22		Secondary current swell detected	0
23		Secondary current swell end	0

Table 59. Row 15, DSP interrupt control mask register 2 (DSP_IRQ2) (continued)

Bit	Internal signal	Description	Default
24	V2 IRQ CR	Secondary voltage sigma-delta bitstream stuck	0
25		Secondary voltage period error	0
26		Secondary voltage sag detected	0
27		Secondary voltage sag end	0
28		Secondary voltage swell detected	0
29		Secondary voltage swell end	0
30	Tamper	Tamper on secondary	0
31		Tamper or wrong connection	0

Table 60. Row 16, DSP status register 1 (DSP_SR1)

Bit	Internal signal	Description	Default
0	PH1+PH2 status	Sign total active power	0
1		Sign total reactive power	0
2		Overflow total active energy	0
3		Overflow total reactive energy	0
4	PH2 IRQ status	Sign secondary channel active power	0
5		Sign secondary channel active fundamental power	0
6		Sign secondary channel reactive power	0
7		Sign secondary channel apparent power	0
8		Overflow secondary channel active energy	0
9		Overflow secondary channel active fundamental energy	0
10		Overflow secondary channel reactive energy	0
11		Overflow secondary channel apparent energy	0
12	PH1 IRQ status	Sign primary channel active power	0
13		Sign primary channel active fundamental power	0
14		Sign primary channel reactive power	0
15		Sign primary channel apparent power	0
16		Overflow primary channel active energy	0
17		Overflow primary channel active fundamental energy	0
18		Overflow primary channel reactive energy	0
19		Overflow primary channel apparent energy	0
20	C1 IRQ status	Primary current sigma-delta bitstream stuck	0
21		AH1 - accumulation of primary channel current	0
22		Primary current swell detected	0
23		Primary current swell end	0

Table 60. Row 16, DSP status register 1 (DSP_SR1) (continued)

Bit	Internal signal	Description	Default
24	V1 IRQ status	Primary voltage sigma-delta bitstream stuck	0
25		Primary voltage period error	0
26		Primary voltage sag detected	0
27		Primary voltage sag end	0
28		Primary voltage swell detected	0
29		Primary voltage swell end	0
30	Tamper	Tamper on primary	0
31		Tamper or wrong connection	0

Table 61. Row 17, DSP status register 2 (DSP_SR2)

Bit	Internal signal	Description	Default
0	PH1+PH2 status	Sign total active power	0
1		Sign total reactive power	0
2		Overflow total active energy	0
3		Overflow total reactive energy	0
4	PH2 status	Sign secondary channel active power	0
5		Sign secondary channel active fundamental power	0
6		Sign secondary channel reactive power	0
7		Sign secondary channel apparent power	0
8		Overflow secondary channel active energy	0
9		Overflow secondary channel active fundamental energy	0
10		Overflow secondary channel reactive energy	0
11		Overflow secondary channel apparent energy	0
12	PH1 status	Sign primary channel active power	0
13		Sign primary channel active fundamental power	0
14		Sign primary channel reactive power	0
15		Sign primary channel apparent power	0
16		Overflow primary channel active energy	0
17		Overflow primary channel active fundamental energy	0
18		Overflow primary channel reactive energy	0
19		Overflow primary channel apparent energy	0
20	C2 status	Secondary current sigma-delta bitstream stuck	0
21		AH1 - accumulation of secondary channel current	0
22		Secondary current swell detected	0
23		Secondary current swell end	0

Table 61. Row 17, DSP status register 2 (DSP_SR2) (continued)

Bit	Internal signal	Description	Default
24	V2 status	Secondary voltage sigma-delta bitstream stuck	0
25		Secondary voltage period error	0
26		Secondary voltage sag detected	0
27		Secondary voltage sag end	0
28		Secondary voltage swell detected	0
29		Secondary voltage swell end	0
30	Tamper	Tamper on secondary	0
31		Tamper or wrong connection	0

10.3 UART/SPI registers

Table 62. Row 18, UART/SPI control register 1 (US_REG1)

Bit	Internal signal	Description	Default
[7:0]	CRCpolynomial	UART/SPI polynomial for CRC calculus (SMBus default polynomial used: x^8+x^2+x+1)	0x07
8	Noise detection enable	UART noise immunity feature enabled	0x0
9	Break on error	UART break feature enabled	0x0
[13:10]	-	Reserved	0x0
14	CRCenable	8-bit CRC enable (5th packet required in each transmission)	0x1
15	LSBfirst	0: big-endian, 1: little-endian	0x0
[23:16]	Time out	Time out (ms)	0x0
[31:24]	-	Reserved	0x0

Table 63. Row 19, UART/SPI control register 2 (US_REG2)

Bit	Internal signal	Description	Default
[15:0]	Baud rate	Defaulted to 9600 baud	0x683
[23:16]	Frame delay	Frame delay	0x0
[31:24]	-	Reserved	0x0

Table 64. Row 20, UART/SPI control register 3 (US_REG3)

Bit	Internal signal	Description	Default
0		Reserved	0
1	UART CRC error	Activate IRQ on both INT1, INT2 for selected signals	0
2	UART timeout error	Activate IRQ on both INT1, INT2 for selected signals	0
3	UART framing error	Activate IRQ on both INT1, INT2 for selected signals	0
4	UART noise error	Activate IRQ on both INT1, INT2 for selected signals	0
5	UART RX overrun	Activate IRQ on both INT1, INT2 for selected signals	0
6	UART TX overrun	Activate IRQ on both INT1, INT2 for selected signals	0
7	-	Reserved	0
8	SPI RX full	Activate IRQ on both INT1, INT2 for selected signals	0
9	SPI TX empty	Activate IRQ on both INT1, INT2 for selected signals	0
10	UART/SPI read error	Activate IRQ on both INT1, INT2 for selected signals	0
11	UART/SPI write error	Activate IRQ on both INT1, INT2 for selected signals	0
12	SPI CRC error	Activate IRQ on both INT1, INT2 for selected signals	0
13	SPI TX underrun	Activate IRQ on both INT1, INT2 for selected signals	0
14	SPI RX overrun	Activate IRQ on both INT1, INT2 for selected signals	0
15	-	Reserved	0
16	UART break	Break frame (all zeros) received	0
17	UART CRC error	CRC error detected	0
18	UART timeout error	Timeout counter expired	0
19	UART framing error	Missing stop bit detected	0
20	UART noise error	Noisy bit detected	0
21	UART RX overrun	Active when received data have not been correctly processed	0
22	UART TX overrun	Occurs when master and slave have different baud rates and master transmits before reception has ended	0
23	-	Reserved	0
24	SPI RX full	Reception buffer full (for SPI diagnostic, not recommended for normal IRQ operations)	0
25	SPI TX empty	Transmission buffer empty (for SPI diagnostic, not recommended for normal IRQ operations)	0
26	UART/SPI read address error	Read address out of range	0
27	UART/SPI write address error	Write address out of range	0
28	SPI CRC error	CRC error detected	0

Table 64. Row 20, UART/SPI control register 3 (US_REG3) (continued)

Bit	Internal signal	Description	Default
29	SPI TX underrun	Occurs when a read-back operation (= write then read the same register) or latch + read is too fast	0
30	SPI RX overrun	Occurs when two consecutive write transactions are too fast and close to each other	0
31	-	Reserved	0

10.4 Data registers

Table 65. Row 21, DSP live event 1 (DSP_EV1)

Bit	Internal signal	Description	Default
0	PH1+PH2 events	Sign total active power	0
1		Sign total reactive power	0
2		Overflow total active energy	0
3		Overflow total reactive energy	0
4	PH1 events	Sign primary channel active power	0
5		Sign primary channel active fundamental power	0
6		Sign primary channel reactive power	0
7		Sign primary channel apparent power	0
8		Overflow primary channel active energy	0
9		Overflow primary channel active fundamental energy	0
10		Overflow primary channel reactive energy	0
11		Overflow primary channel apparent energy	0
12	C1 events	Primary current zero-crossing	0
13		Primary current sigma-delta bitstream stuck	0
14		Primary current AH accumulation	0
15		Primary current swell event history	0
16			0
17			0
18			0
19	V1 events	Primary voltage zero-crossing	0
20		Primary voltage sigma-delta bitstream stuck	0
21		Primary voltage period error (out of range)	0
22		Primary voltage swell event history	0
23			0
24			0
25			0
26		Primary voltage sag event history	0
27			0
28			0
29			0
30	-	Reserved	0
31	-	Reserved	0

Table 66. Row 22, DSP live event 2 (DSP_EV2)

Bit	Internal signal	Description	Default
0	PH1+PH2 events	Sign total active power	0
1		Sign total reactive power	0
2		Overflow active energy total	0
3		Overflow reactive energy total	0
4	PH2 events	Sign secondary channel active power	0
5		Sign secondary channel active fundamental power	0
6		Sign secondary channel reactive power	0
7		Sign secondary channel apparent power	0
8		Overflow secondary channel active energy	0
9		Overflow secondary channel active fundamental energy	0
10		Overflow secondary channel reactive energy	0
11		Overflow secondary channel apparent energy	0
12	C2 events	Secondary current zero-crossing	0
13		Secondary current sigma-delta bitstream stuck	0
14		Secondary current AH accumulation	0
15		Secondary current swell event history	0
16			0
17			0
18			0
19	V2 events	Secondary voltage zero-crossing	0
20		Secondary voltage sigma-delta bitstream stuck	0
21		Secondary voltage period error (out of range)	0
22		Secondary voltage swell event history	0
23			0
24			0
25			0
26		Secondary voltage sag event history	0
27			0
28			0
29			0
30	-	Reserved	0
31	-	Reserved	0

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

11.1 QFN24L (4x4x1) 0.5 pitch package information

Figure 54. QFN24L (4x4x1) 0.5 pitch package outline

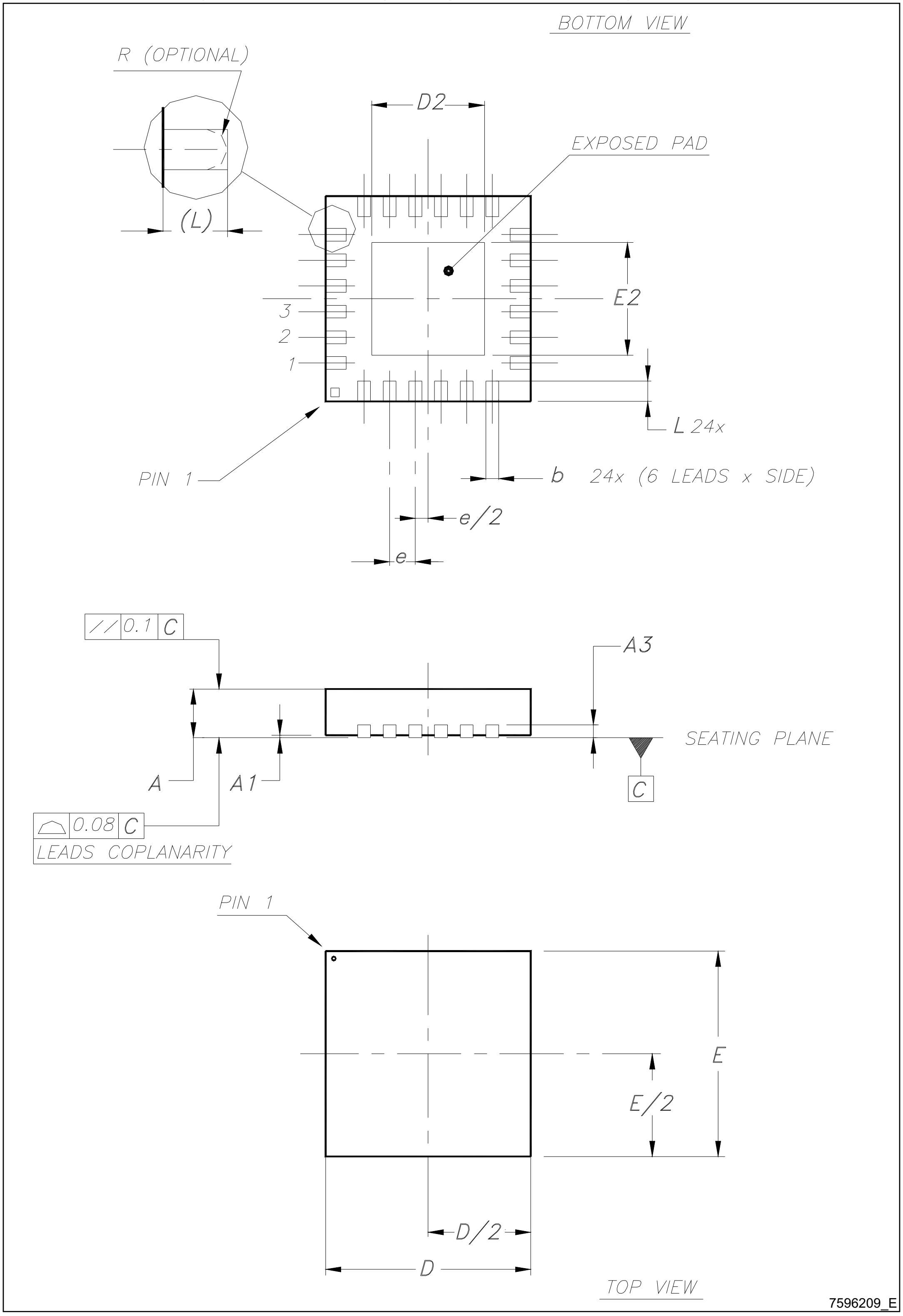
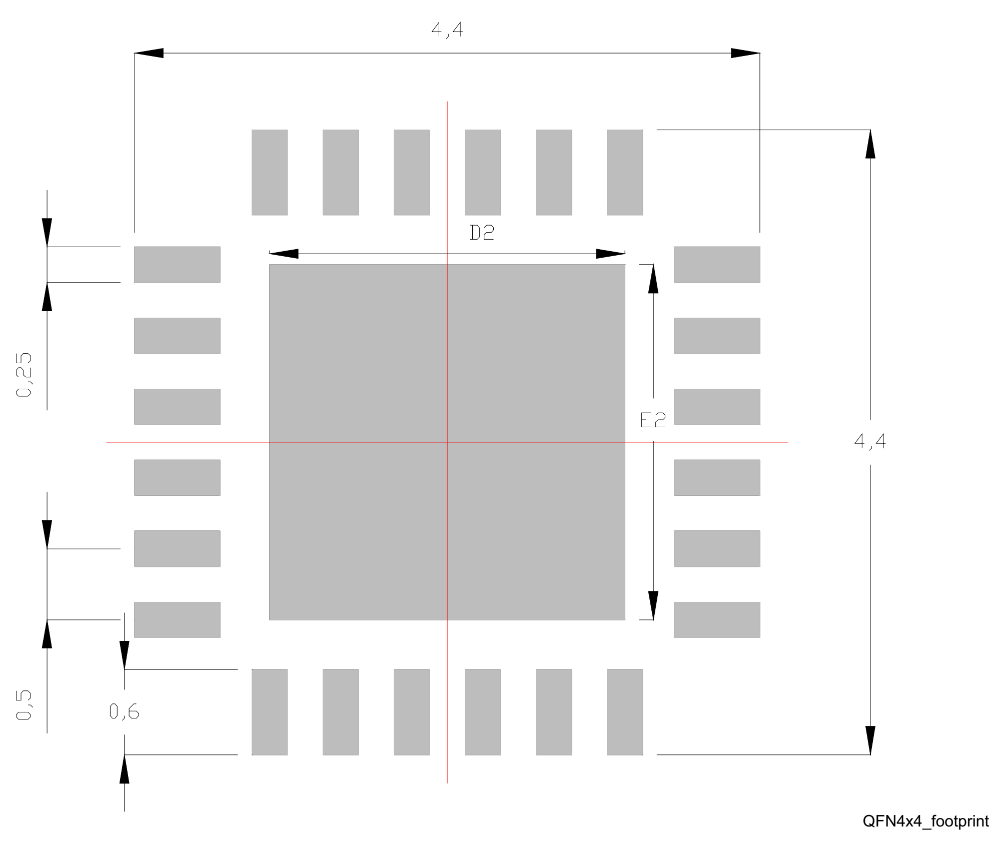


Table 67. QFN24L (4x4x1) 0.5 pitch package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.30	2.45	2.55
E	3.90	4.00	4.10
E2	2.30	2.45	2.55
e	0.45	0.50	0.55
K	0.20	-	-
L	0.30	0.40	0.50

Figure 55. QFN24L (4x4x1) 0.5 pitch recommended footprint



11.2 QFN32L (5x5x1) 0.5 pitch package information

Figure 56. QFN32L (5x5x1) 0.5 pitch package outline

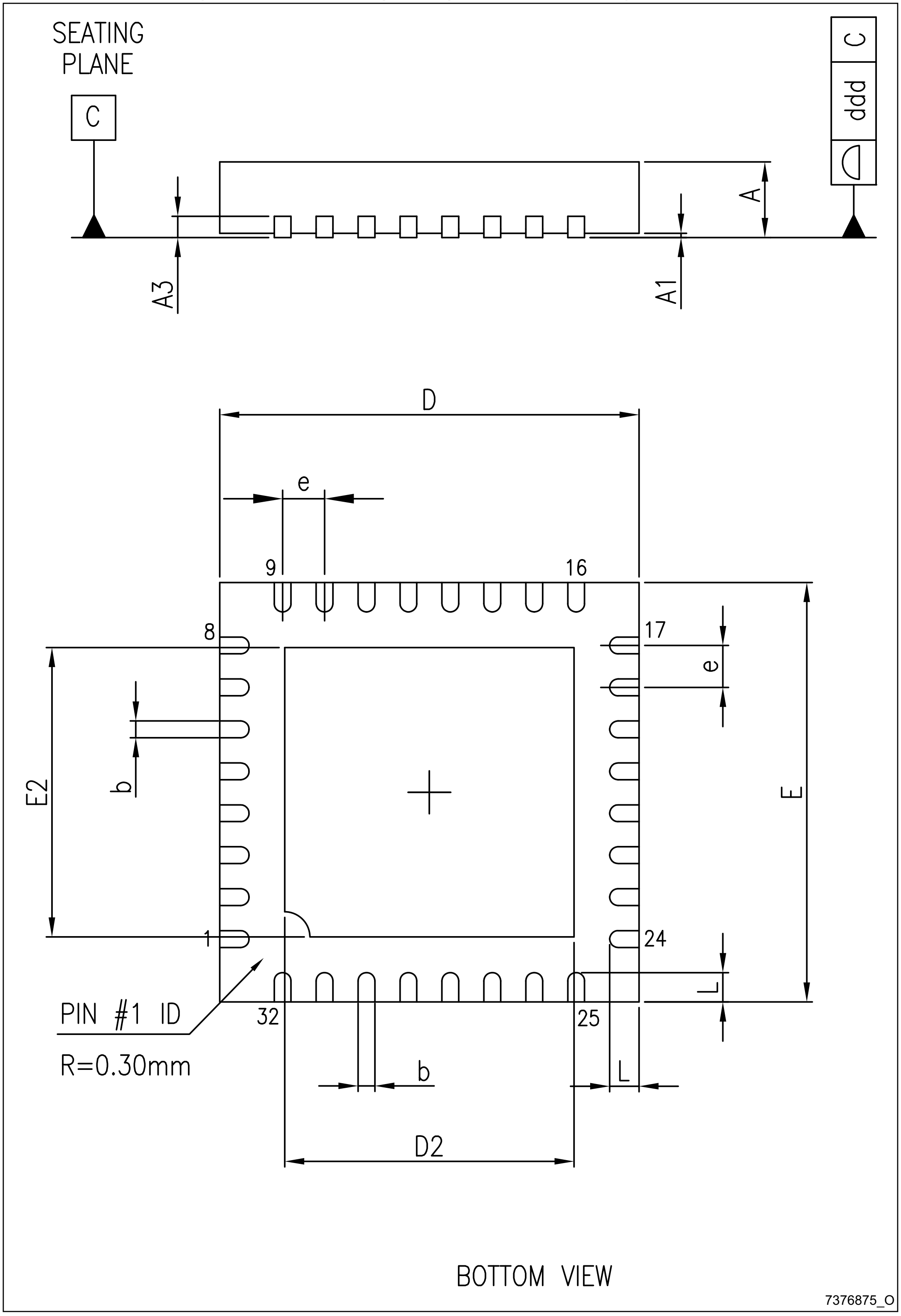
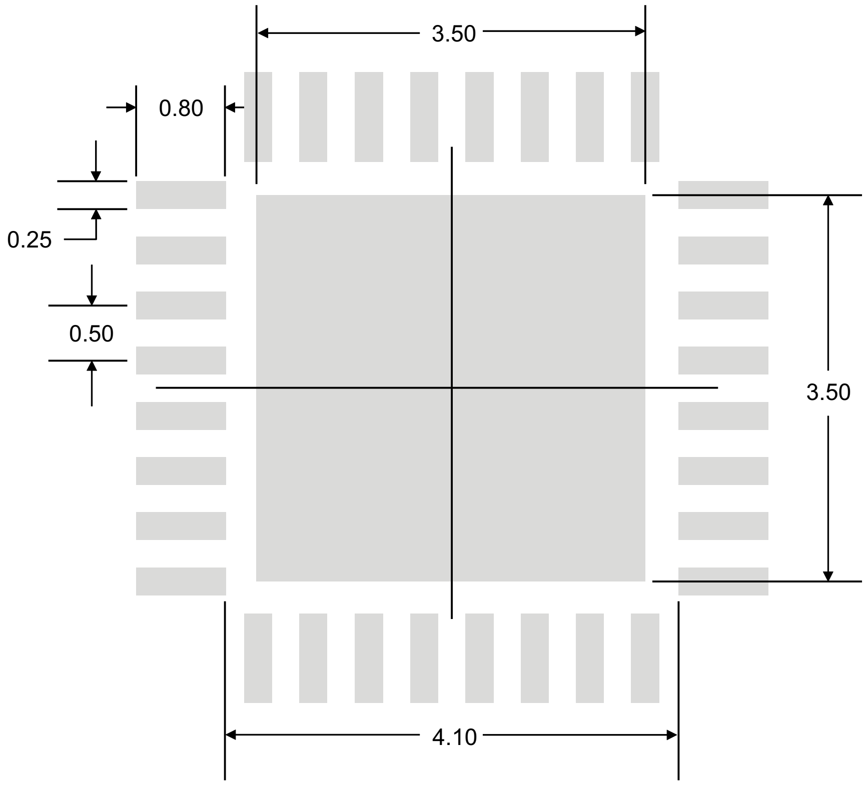


Table 68. QFN32L (5x5x1) 0.5 pitch package mechanical data

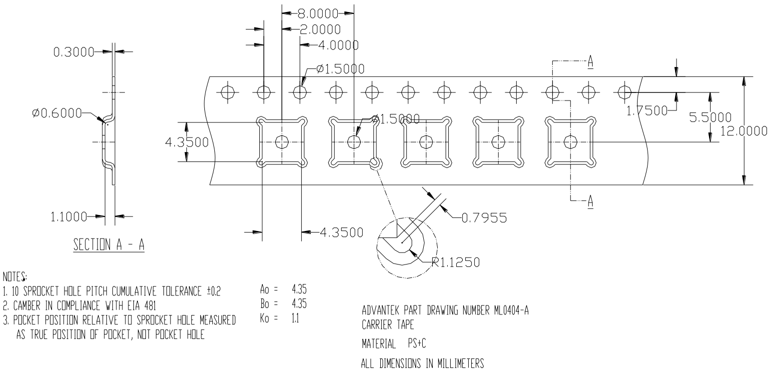
Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	-	0.20	-
b	0.18	0.25	0.30
D	4.85	5.00	5.15
D2	3.40	3.45	3.50
E	4.85	5.00	5.15
E2	3.40	3.45	3.50
e	0.45	0.50	0.55
L	0.30	0.40	0.50
Ddd	-	-	0.08

Figure 57. QFN32L (5x5x1) 0.5 pitch recommended footprint



11.3 QFN24L (4x4x1) packing information

Figure 58. QFN24L (4x4x1) carrier tape outline



11.4 QFN32L (5x5x1) packing information

Figure 59. QFN32L (5x5x1) carrier tape outline

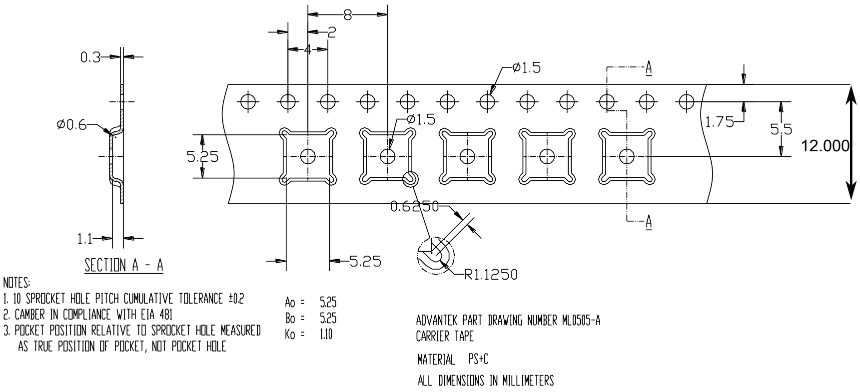
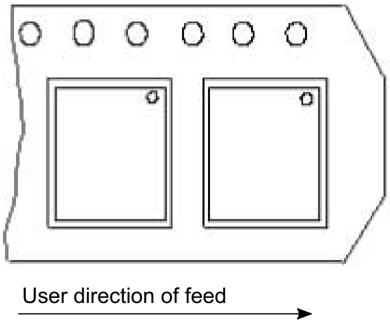


Figure 60. Feed direction of square QFN24L and QFN32L reel



12 Revision history

Table 69. Document revision history

Date	Revision	Changes
31-Mar-2014	1	Initial release.
16-Oct-2014	2	Updated *Features*. Updated *Table 2*, from *Table 14*, to *Table 18*, from *Table 21*, to *Table 23*; updated *Table 33*, *Table 35*, *Table 36*, *Table 40*, *Table 41* and from *Table 44* to *Table 66*. Changed title of *Figure 15*. Updated *Figure 22*, *Figure 31*. Updated *Section 8.2.1*, *Section 8.2.3*, *Section 8.3.1*, *Section 8.4.12*, *Section 8.6.3*. Minor text changes.
01-Oct-2015	3	Updated *Features*. Updated *Section 8.2.1*, *Section 8.3.3*, *Section 8.3.6*, *Section 8.4*, *Section 8.4.3*, *Section 8.4.4*, *Section 8.4.12*, *Section 8.4.13*, *Period measurement*, *Sag and swell threshold calculation*. Added note to *Interrupt control mask register*. Updated *Table 5*, *Table 22*, *Table 42*, *Table 44*, *Table 45*, *Table 56*,*Table 57*, *Table 58*, *Table 59*, *Table 60*, *Table 61*. Updated equations in *Table 14*, *Table 15*, *Table 16*, *Table 17*, *Table 18*, *Table 20*, *Table 35*, *Table 37*, *Table 39*, *Table 40*. Updated *Equation 29*. Added *Figure 8*, *Figure 9*, *Figure 10* and *Figure 29*. Updated *Figure 26*, *Figure 27*, *Figure 28*, *Figure 31*, *Figure 32*, *Figure 35*, *Figure 36*, *Figure 45*. Changed *Figure 46*.
31-Aug-2016	4	Added *Figure 56: QFN32L 5x5x1 mm 0.5 pitch recommended footprint*. Minor text changes.
02-Nov-2016	5	Updated *Table 5*, *Table 9* and changed *Figure 23*. Added *Section 11.3: QFN24L (4x4x1) packing information* and *Section 11.4: QFN32L (5x5x1) packing information*.
11-Sep-2017	6	Updated *Table 5*, *Table 14*, *Table 42*, *Table 48* and *Table 60*.
12-Jan-2018	7	Updated *Table 3 on page 16* and *Table 5 on page 17*. Minor modifications throughout document.
14-Dec-2018	8	Updated *Table 5*, *Table 44*, and *Table 45*. Changed *Figure 23* and amended *Section 8.4* and *Section 8.4.10*