Single Inverter with Schmitt-Trigger Input

MC74HC1G14

The MC74HC1G14 is a high speed CMOS inverter with Schmitt−Trigger input fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The MC74HC1G14 output drive current is 1/2 compared to MC74HC series.

Features

- High Speed: t_{PD} = 7 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- High Noise Immunity
- Balanced Propagation Delays ($t_{pLH} = t_{pHL}$)
- Symmetrical Output Impedance ($I_{OH} = I_{OL}$ = 2 mA)
- Chip Complexity: < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

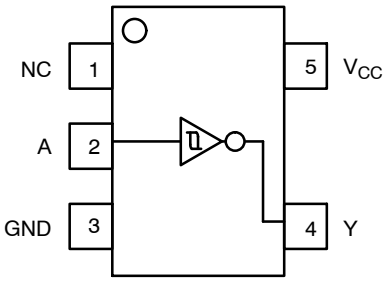

Figure 1. Pinout

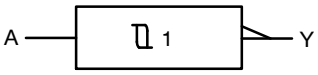

Figure 2. Logic Symbol

PIN ASSIGNMENT	
1	N/C
2	A
3	GND
4	Y
5	V_{CC}

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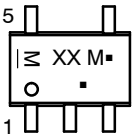
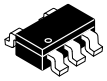
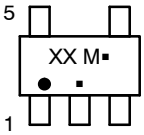
MARKING DIAGRAMS

SC−88A
DF SUFFIX
CASE 419A





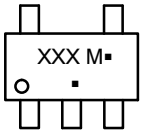
TSOP−5
DT SUFFIX
CASE 483



XX = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

SC−74A
DBV SUFFIX
CASE 318BQ



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Input	Output
A	**Y**
L	H
H	L

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage	SC−88A (NLV), TSOP−5 SC−88A, SC−74A	−0.5 to +7.0 −0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±20	mA
I_{OUT}	DC Output Source/Sink Current		±12.5	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±25	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SC70−5/SC−88A/SOT−353 SOT23−5/TSOP−5/SC59−5 SC−74A	659 555 555	°C/W
P_D	Power Dissipation in Still Air at 85°C	SC70−5/SC−88A/SOT−353 SOT23−5/TSOP−5/SC59−5 SC−74A	190 225 225	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 1000	V
$I_{LATCHUP}$	Latchup Performance (Note 3)	SC−88A (NLV), TSOP−5 SC−88A, SC−74A	±500 ±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 20 ounce copper trace with no air flow.
2. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued per JEDEC/JEP172A.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	6.0	V
V_{IN}	DC Input Voltage		0.0	V_{CC}	V
V_{OUT}	DC Output Voltage		0.0	V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_r , t_f	Input Rise and Fall Time	SC−88A (NLV), TSOP−5			ns/V
		V_{CC} = 2.0 V	−	No Limit	
		V_{CC} = 3.0 V	−	No Limit	
		V_{CC} = 4.5 V	−	No Limit	
		V_{CC} = 6.0 V	−	No Limit	
	Input Rise and Fall Time	SC−88A, SC−74A			
		V_{CC} = 2.0 V	−	No Limit	
		V_{CC} = 2.3 V to 2.7 V	−	No Limit	
		V_{CC} = 3.0 V to 3.6 V	−	No Limit	
		V_{CC} = 4.5 V to 6.0 V	−	No Limit	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

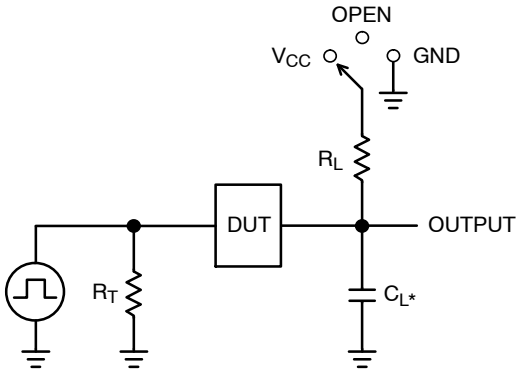
Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		−55°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	Positive Threshold Voltage		3.0	−	2.0	2.20	−	2.20	−	2.20	V
			4.5	−	3.0	3.15	−	3.15	−	3.15	
			5.5	−	3.6	3.85	−	3.85	−	3.85	
V_{T-}	Negative Threshold Voltage		3.0	0.9	1.5	−	0.9	−	0.9	−	V
			4.5	1.35	2.3	−	1.35	−	1.35	−	
			5.5	1.65	2.9	−	1.65	−	1.65	−	
V_H	Hysteresis Voltage		3.0	0.30	0.57	1.20	0.30	1.20	0.30	1.20	V
			4.5	0.40	0.67	1.40	0.40	1.40	0.40	1.40	
			5.5	0.50	0.74	1.60	0.50	1.60	0.50	1.60	
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	1.9	−	V
			3.0	2.9	3.0	−	2.9	−	2.9	−	
			4.5	4.4	4.5	−	4.4	−	4.4	−	
			6.0	5.9	6.0	−	5.9	−	5.9	−	
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −2 mA	4.5	4.18	4.31	−	4.13	−	4.08	−	
		I_{OH} = −2.6 mA	6.0	5.68	5.80	−	5.63	−	5.58	−	
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	−	0.1	V
			3.0	−	0.0	0.1	−	0.1	−	0.1	
			4.5	−	0.0	0.1	−	0.1	−	0.1	
			6.0	−	0.0	0.1	−	0.1	−	0.1	
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 2 mA	4.5	−	0.17	0.26	−	0.33	−	0.40	
		I_{OL} = 2.6 mA	6.0	−	0.18	0.26	−	0.33	−	0.40	
I_{IN}	Input Leakage Current	V_{IN} = 6.0 V or GND	6.0	−	−	±0.1	−	±1.0	−	±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	6.0	−	−	1.0	−	10	−	40	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$			$-40°C \le T_A \le 85°C$		$-55°C \le T_A \le 125°C$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, Input A or B to Y	V_{CC} = 5.0 V C_L = 15 pF	–	3.5	15	–	20	–	25	ns
		V_{CC} = 2.0 V C_L = 50 pF	–	19	100	–	125	–	155	
		V_{CC} = 3.0 V	–	10.5	27	–	35	–	90	
		V_{CC} = 4.5 V	–	7.5	20	–	25	–	35	
		V_{CC} = 6.0 V	–	6.5	17	–	21	–	26	
t_{TLH}, t_{THL}	Output Transition Time	V_{CC} = 5.0 V C_L = 15 pF	–	3	10	–	15	–	20	ns
		V_{CC} = 2.0 V C_L = 50 pF	–	25	125	–	155	–	200	
		V_{CC} = 3.0 V	–	16	35	–	45	–	60	
		V_{CC} = 4.5 V	–	11	25	–	31	–	38	
		V_{CC} = 6.0 V	–	9	21	–	26	–	32	
C_{IN}	Input Capacitance		–	5	10	–	10	–	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 4)	10	pF

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.



Test	Switch Position	C_L, pF	R_L, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	X
t_{TLH} / t_{THL} (Note 5)	Open		X
t_{PLZ} / t_{PZL}	V_{CC}		1 k
t_{PHZ} / t_{PZH}	GND		1 k

X – Don't Care

*C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 W)
f = 1 MHz

Figure 3. Test Circuit

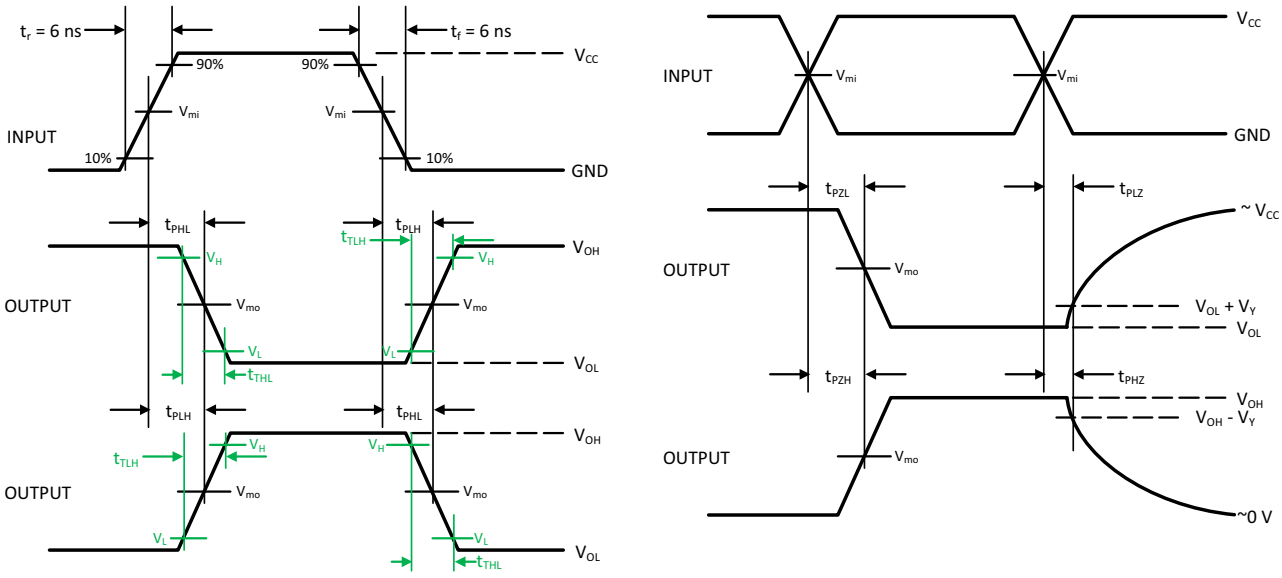


Figure 4. Switching Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V		V_L, V	V_H, V	V_Y, V
		t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}			
3.0 to 3.6	V_{CC}/2	(V_{OH} – V_{OL})/2	V_{CC}/2	V_{OL} + 0.1 (V_{OH} – V_{OL})	V_{OL} + 0.9 (V_{OH} – V_{OL})	0.3
4.5 to 5.5	V_{CC}/2	(V_{OH} – V_{OL})/2	V_{CC}/2	V_{OL} + 0.1 (V_{OH} – V_{OL})	V_{OL} + 0.9 (V_{OH} – V_{OL})	0.3

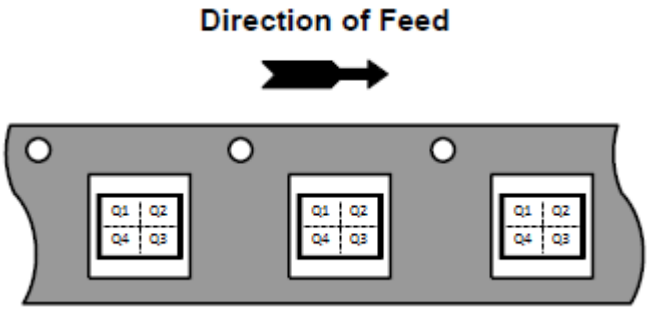
5. t_{TLH} and t_{THL} are measured from 10% to 90% of (V_{OH} – V_{OL}), and 90% to 10% of (V_{OH} – V_{OL}), respectively.

ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping†
MC74HC1G14DFT1G	SC−88A	HA	Q2	3000 / Tape & Reel
NLVHC1G14DFT1G*	SC−88A	HA	Q2	3000 / Tape & Reel
MC74HC1G14DFT2G	SC−88A	HA	Q4	3000 / Tape & Reel
NLVHC1G14DFT2G*	SC−88A	HA	Q4	3000 / Tape & Reel
MC74HC1G14DTT1G	TSOP−5	HA	Q4	3000 / Tape & Reel
NLV74HC1G14DTT1G*	TSOP−5	HAR	Q4	3000 / Tape & Reel
MC74HC1G14DBVT1G	SC−74A	HA	Q4	3000 / Tape & Reel

†For complete information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel

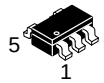


MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

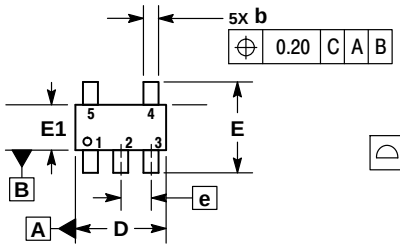
ON Semiconductor®

SC−74A
CASE 318BQ
ISSUE B

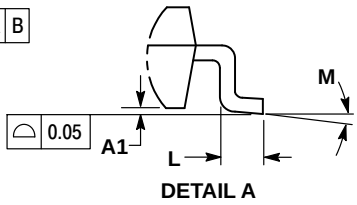
DATE 18 JAN 2018



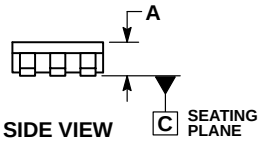
SCALE 2:1



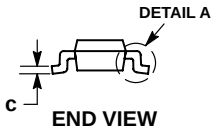
TOP VIEW



DETAIL A



SIDE VIEW

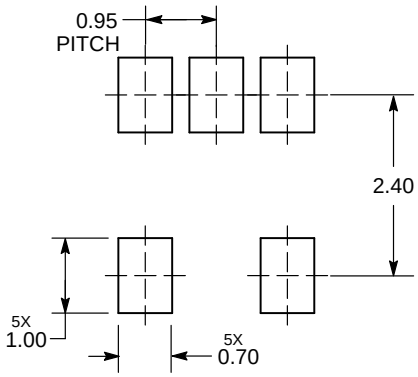


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0 °	10 °

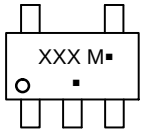
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

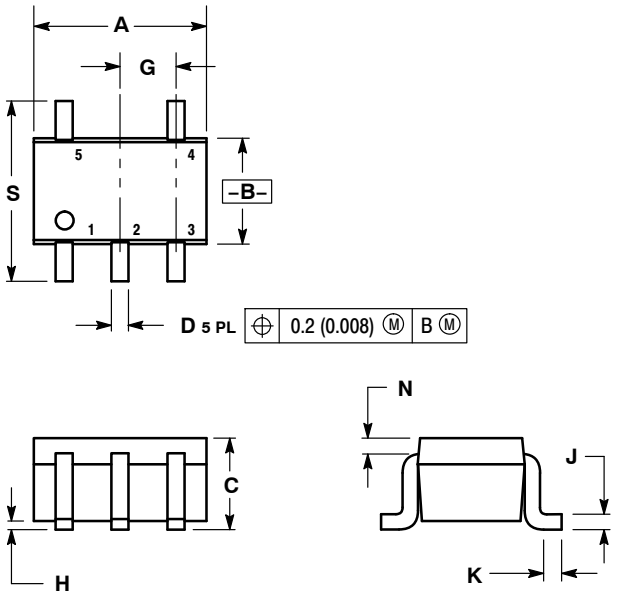
DOCUMENT NUMBER:	**98AON66279G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
STATUS:	**ON SEMICONDUCTOR STANDARD**		
NEW STANDARD:			
DESCRIPTION:	**SC−74A**		**PAGE 1 OF 2**

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ BY I. HYLAND.	27 JUN 2017
A	CORRECTED MARKING DIAGRAM FROM 6 TO 5−LEAD. REQ BY I. HYLAND.	20 SEP 2017
B	CORRECTED SOLDERING FOOTPRINT PITCH FROM 3.40MM TO 2.40MM. REQ. BY I. HYLAND.	18 JAN 2018

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

SCALE 2:1

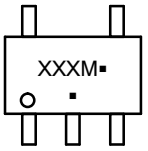
DATE 17 JAN 2013



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

GENERIC MARKING DIAGRAM*

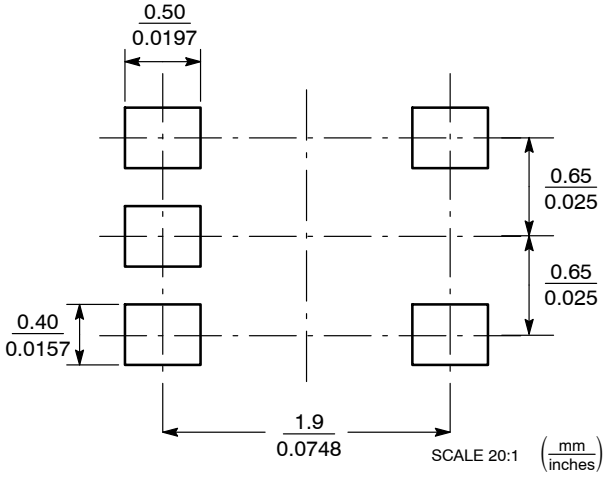


XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This infomration is generic. Please refer to device data sheet for actual part marking.

SOLDER FOOTPRINT



STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

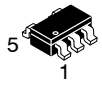
STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

ISSUE	REVISION	DATE
C	CONVERTED FROM PAPER DOCUMENT TO ELECTRONIC. REQ. BY N LAFEBRE.	20 JUN 1998
D	CONVERTED FROM MOTOROLA TO ON SEMICONDUCTOR. ADDED STYLE 5. REQ. BY E. KIM.	24 JUL 2000
E	ADDED STYLES 6 & 7. REQ. BY S. BACHMAN.	03 AUG 2000
F	DELETED DIMENSION V, WAS 0.3−0.44MM/0.012−0.016IN. REQ. BY G. KWONG.	14 JUN 2001
G	ADDED STYLE 8, REQ. BY S. CHANG; ADDED STYLE 9, REQ. BY S. BACHMAN; ADDED NOTE 4, REQ. BY S. RIGGS	25 JUN 2003
H	CHANGED STYLE 6. REQ. BY C. LIM	28 APR 2005
J	CHANGED TITLE DESCRIPTION. REQ. BY B. LOFTS.	31 AUG 2005
K	CORRECTED TITLE AND DESCRIPTION TO SC−88A (SC−70−5/SOT−353). CORRECTED MARKING DIAGRAM. REQ. BY D. TRUHITTE.	13 JUL 2010
L	ADDED SOLDER FOOTPRINT. REQ. BY I. MARIANO.	17 JAN 2013

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

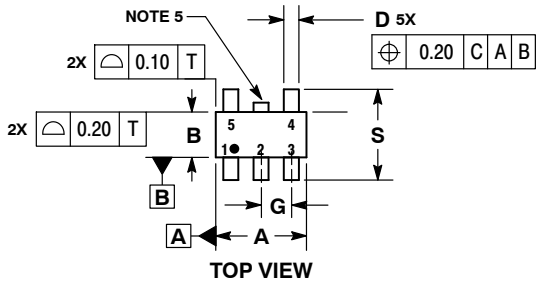
ON Semiconductor®



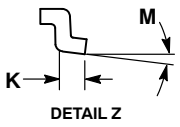
SCALE 2:1

TSOP−5
CASE 483
ISSUE N

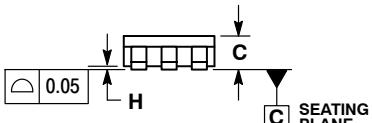
DATE 12 AUG 2020



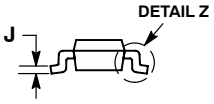
TOP VIEW



DETAIL Z



SIDE VIEW

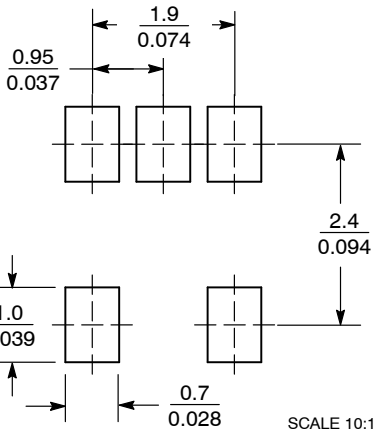


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

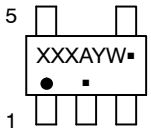
SOLDERING FOOTPRINT*



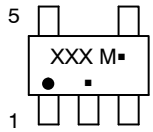
SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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