# CD54HC165, CD74HC165, CD54HCT165, CD74HCT165

Data sheet acquired from Harris Semiconductor
SCHS156C

February 1998 - Revised October 2003

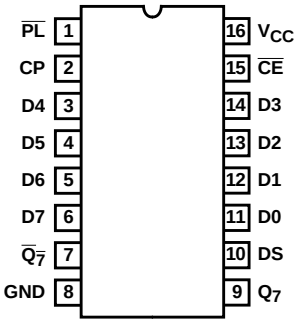
## High-Speed CMOS Logic 8-Bit Parallel-In/Serial-Out Shift Register

### Features

- **Buffered Inputs**
- **Asynchronous Parallel Load**
- **Complementary Outputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^{o}$C to 125$^{o}$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

### Pinout

**CD54HC165, CD54HCT165**
**(CERDIP)**
**CD74HC165, CD74HCT165**
**(PDIP, SOIC)**
TOP VIEW




### Description

The ’HC165 and ’HCT165 are 8-bit parallel or serial-in shift registers with complementary serial outputs ($Q_7$ and $\overline{Q_7}$) available from the last stage. When the parallel load ($\overline{PL}$) input is LOW, parallel data from the D0 to D7 inputs are loaded into the register asynchronously. When the $\overline{PL}$ is HIGH, data enters the register serially at the DS input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by typing the $Q_7$ output to the DS input of the succeeding device.

For predictable operation the LOW-to-HIGH transition of $\overline{CE}$ should only take place while CP is HIGH. Also, CP an d $\overline{CE}$ should be LOW before the LOW-to-HIGH transition of PL to prevent shifting the data when $\overline{PL}$ goes HIGH.

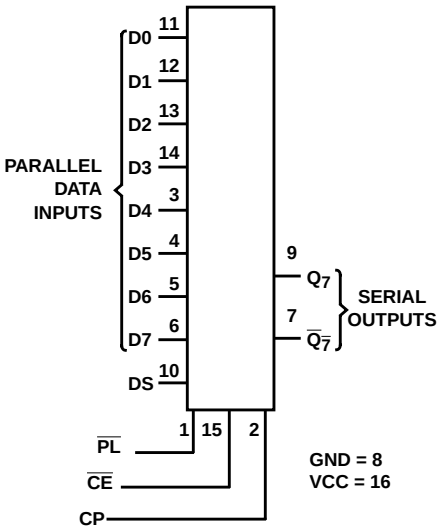
### Ordering Information

| PART NUMBER | TEMP. RANGE ($^{o}$C) | PACKAGE |
|---|---|---|
| CD54HC165F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT165F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC165E | -55 to 125 | 16 Ld PDIP |
| CD74HC165M | -55 to 125 | 16 Ld SOIC |
| CD74HC165MT | -55 to 125 | 16 Ld SOIC |
| CD54HC165M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT165E | -55 to 125 | 16 Ld PDIP |
| CD74HCT165M | -55 to 125 | 16 Ld SOIC |
| CD74HCT165MT | -55 to 125 | 16 Ld SOIC |
| CD54HCT165M96 | -55 to 125 | 16 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

## Functional Diagram




**TRUTH TABLE**

| OPERATING MODE | INPUTS | | | | | $Q_n$ REGISTER | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{PL}$ | $\overline{CE}$ | CP | DS | D0 - D7 | $Q_0$ | $Q_1$ - $Q_6$ | $Q_7$ | $\overline{Q}_7$ |
| Parallel Load | L | X | X | X | L | L | L-L | L | H |
| | L | X | X | X | H | H | H-H | H | L |
| Serial Shift | H | L | ↑ | l | X | L | $q_0$ - $q_5$ | $q_6$ | $\overline{q}_6$ |
| | H | L | ↑ | h | X | H | $q_0$ - $q_5$ | $q_6$ | $\overline{q}_6$ |
| Hold Do Nothing | H | H | X | X | X | $q_0$ | $q_1$ - $q_6$ | $q_7$ | $\overline{q}_7$ |

H =High Voltage Level
h = High Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition
l = Low Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition
L = Low Voltage Level
X = Don't Care
↑ = Transition from Low to High Level
$q_n$ = Lower Case Letters Indicate The State Of the Reference Output Clock Transition

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Drain Current per Output, IO
For $V_O$ < -0.5V $V_O$ > $V_{CC}$ + 0.5V . . . . . ±25mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| E (PDIP) Package | 67 |
| M (SOIC) Package | 73 |

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

2. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| DS, D0 to D7 | 0.35 |
| CP, $\overline{PL}$ | 0.65 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

## Prerequisite For Switching Specifications

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | |
| CP Pulse Width | $t_{WL}$, $t_{WH}$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |

**Prerequisite For Switching Specifications** **(Continued)**

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $\overline{PL}$ Pulse Width | $t_{WL}$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Set-up Time DS to CP | $t_{SU}$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| $\overline{CE}$ to CP | $t_{SU(L)}$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| D0-D7 to $\overline{PL}$ | $t_{SU}$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Hold Time DS to CP or $\overline{CE}$ | $t_H$ | 2 | 35 | - | 45 | - | 55 | - | ns |
| | | 4.5 | 7 | - | 9 | - | 11 | - | ns |
| | | 6 | 6 | - | 8 | - | 9 | - | ns |
| $\overline{CE}$ to CP | $t_H$ | 2 | 0 | - | 0 | - | 0 | - | ns |
| | | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| | | 6 | 0 | - | 0 | - | 0 | - | ns |
| Recovery Time $\overline{PL}$ to CP | $t_{REC}$ | 2 | 100 | - | 125 | - | 150 | - | ns |
| | | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| | | 6 | 17 | - | 21 | - | 26 | - | ns |
| Maximum Clock Pulse Frequency | $f_{MAX}$ | 2 | 6 | - | 5 | - | 4 | - | MHz |
| | | 4.5 | 30 | - | 24 | - | 20 | - | MHz |
| | | 6 | 35 | - | 28 | - | 24 | - | MHz |
| **HCT TYPES** | | | | | | | | | |
| CP Pulse Width | $t_{WL}$, $t_{WH}$ | 4.5 | 18 | - | 23 | - | 27 | - | ns |
| $\overline{PL}$ Pulse Width | $t_{WL}$ | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| Set-up Time DS to CP | $t_{SU}$ | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| $\overline{CE}$ to CP | $t_{SU(L)}$ | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| D0-D7 to $\overline{PL}$ | $t_{SU}$ | 6 | 20 | - | 25 | - | 30 | - | ns |
| Hold Time DS to CP or $\overline{CE}$ | $t_H$ | 4.5 | 7 | - | 9 | - | 11 | - | ns |
| $\overline{CE}$ to CP | $t_S$, $t_H$ | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| Recovery Time $\overline{PL}$ to CP | $t_{REC}$ | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| Maximum Clock Pulse Frequency | $f_{MAX}$ | 4.5 | 27 | - | 22 | - | 18 | - | MHz |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | MAX | MAX | |
| **HC TYPES** | | | | | | | | |
| Propagation Delay | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 165 | 205 | 250 | ns |
| CP or $\overline{CE}$ to $Q_7$ or $\overline{Q_7}$ | | | 4.5 | - | 33 | 41 | 50 | ns |
| | | $C_L$ = 15pF | 5 | 13 | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | 28 | 35 | 43 | ns |
| $\overline{PL}$ to $Q_7$ or $\overline{Q_7}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | 30 | 37 | 45 | ns |
| D7 to $Q_7$ or $\overline{Q_7}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | 26 | 33 | 38 | ns |
| Output Transition Times | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | 75 | 95 | 110 | ns |
| | | | 4.5 | - | 15 | 19 | 22 | ns |
| | | | 6 | - | 13 | 16 | 19 | ns |
| Input Capacitance | $C_{IN}$ | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | - | 5 | 17 | - | - | - | pF |
| **HCT TYPES** | | | | | | | | |
| Propagation Delay | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 40 | 50 | 60 | ns |
| CP or $\overline{CE}$ to $Q_7$ or $\overline{Q_7}$ | | $C_L$ = 15pF | 5 | 17 | - | - | - | ns |
| $\overline{PL}$ to $Q_7$ or $\overline{Q_7}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 40 | 50 | 60 | ns |
| | | $C_L$ = 15pF | 5 | 17 | - | - | - | ns |
| D7 to $Q_7$ or $\overline{Q_7}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 35 | 44 | 53 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| Output Transition Times | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | 15 | 19 | 22 | ns |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | - | 5 | 24 | | - | - | pF |

NOTES:

3. $C_{PD}$ is used to determine the dynamic power consumption, per package.
4. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_O)$ where $f_i$ = Input Frequency, $f_O$ = Output Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## Test Circuits and Waveforms

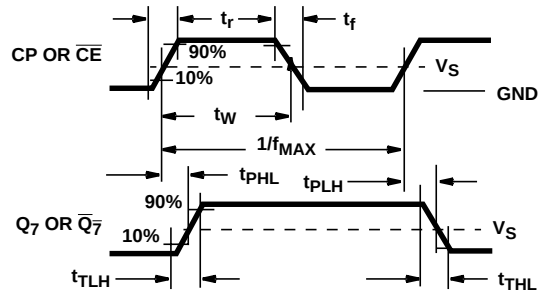



FIGURE 3. SERIAL-SHIFT MODE

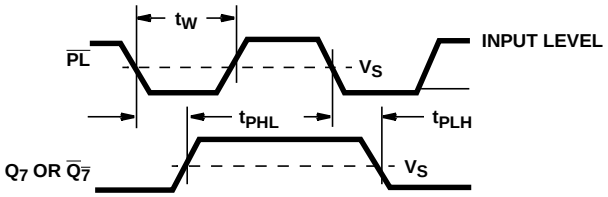



FIGURE 4. PARALLEL-LOAD MODE

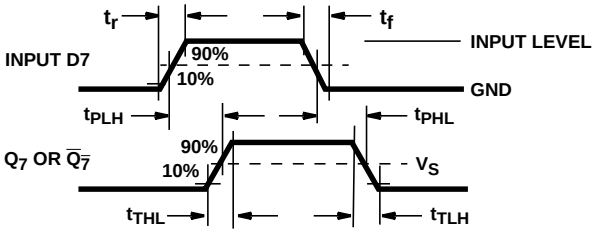



FIGURE 5. PARALLEL-LOAD MODE

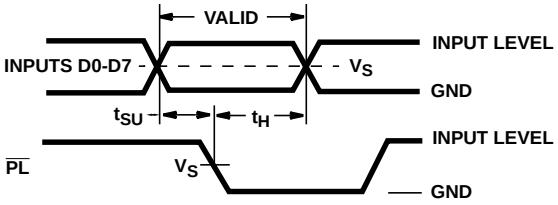



FIGURE 6. PARALLEL-LOAD MODE

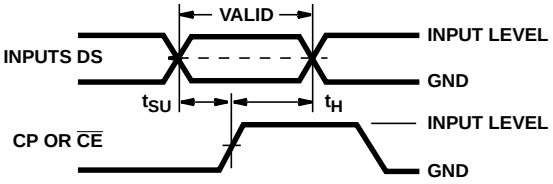



FIGURE 7. SERIAL-SHIFT MODE

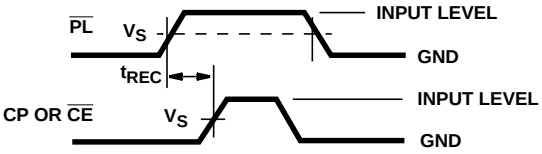



FIGURE 8. SERIAL-SHIFT MODE

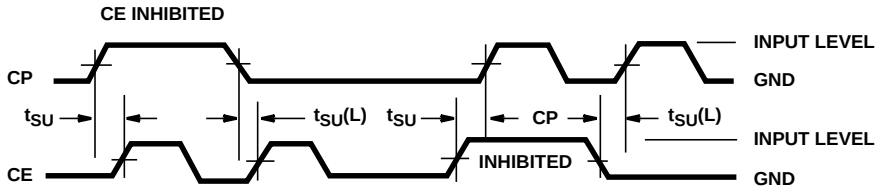



FIGURE 9. SERIAL-SHIFT, CLOCK-INHIBIT MODE

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8685501EA | ACTIVE | CDIP | J | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8685501EA CD54HCT165F3A | Samples |
| CD54HC165F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 8409501EA CD54HC165F3A | Samples |
| CD54HCT165F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8685501EA CD54HCT165F3A | Samples |
| CD74HC165E | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC165E | Samples |
| CD74HC165EE4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC165E | Samples |
| CD74HC165M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC165M | Samples |
| CD74HC165M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC165M | Samples |
| CD74HC165M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC165M | Samples |
| CD74HC165ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC165M | Samples |
| CD74HC165MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC165M | Samples |
| CD74HC165MTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC165M | Samples |
| CD74HCT165E | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT165E | Samples |
| CD74HCT165EE4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT165E | Samples |
| CD74HCT165M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT165M | Samples |
| CD74HCT165M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-1-260C-UNLIM | -55 to 125 | HCT165M | Samples |
| CD74HCT165M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT165M | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HCT165M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT165M | Samples |
| CD74HCT165ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT165M | Samples |
| CD74HCT165MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT165M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF CD54HC165, CD54HCT165, CD74HC165, CD74HCT165 :**

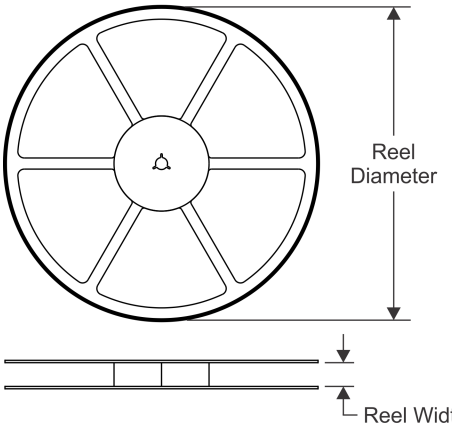
- Catalog: CD74HC165, CD74HCT165
- Military: CD54HC165, CD54HCT165

NOTE: Qualified Version Definitions:

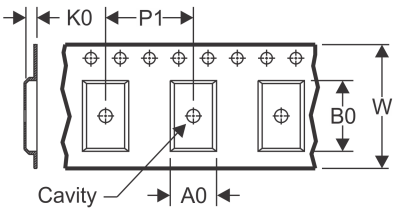
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

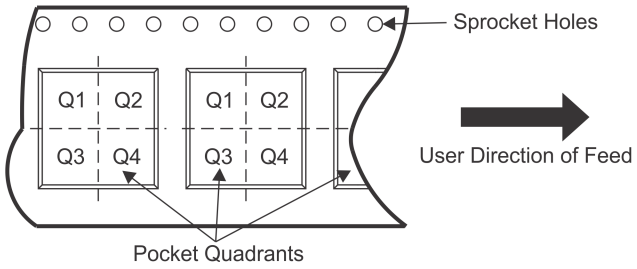



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

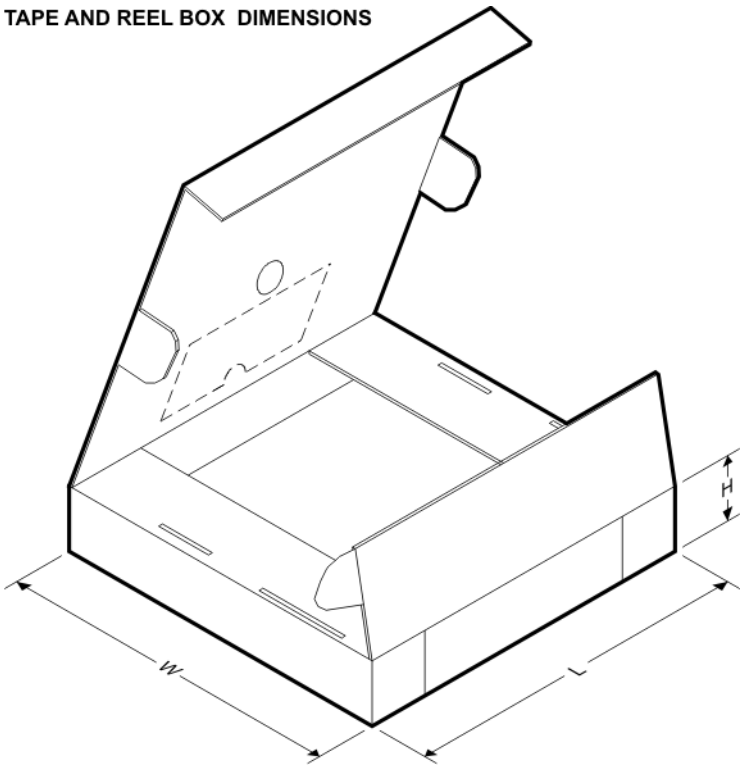
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC165M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC165M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT165M96 | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT165M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT165M96G4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

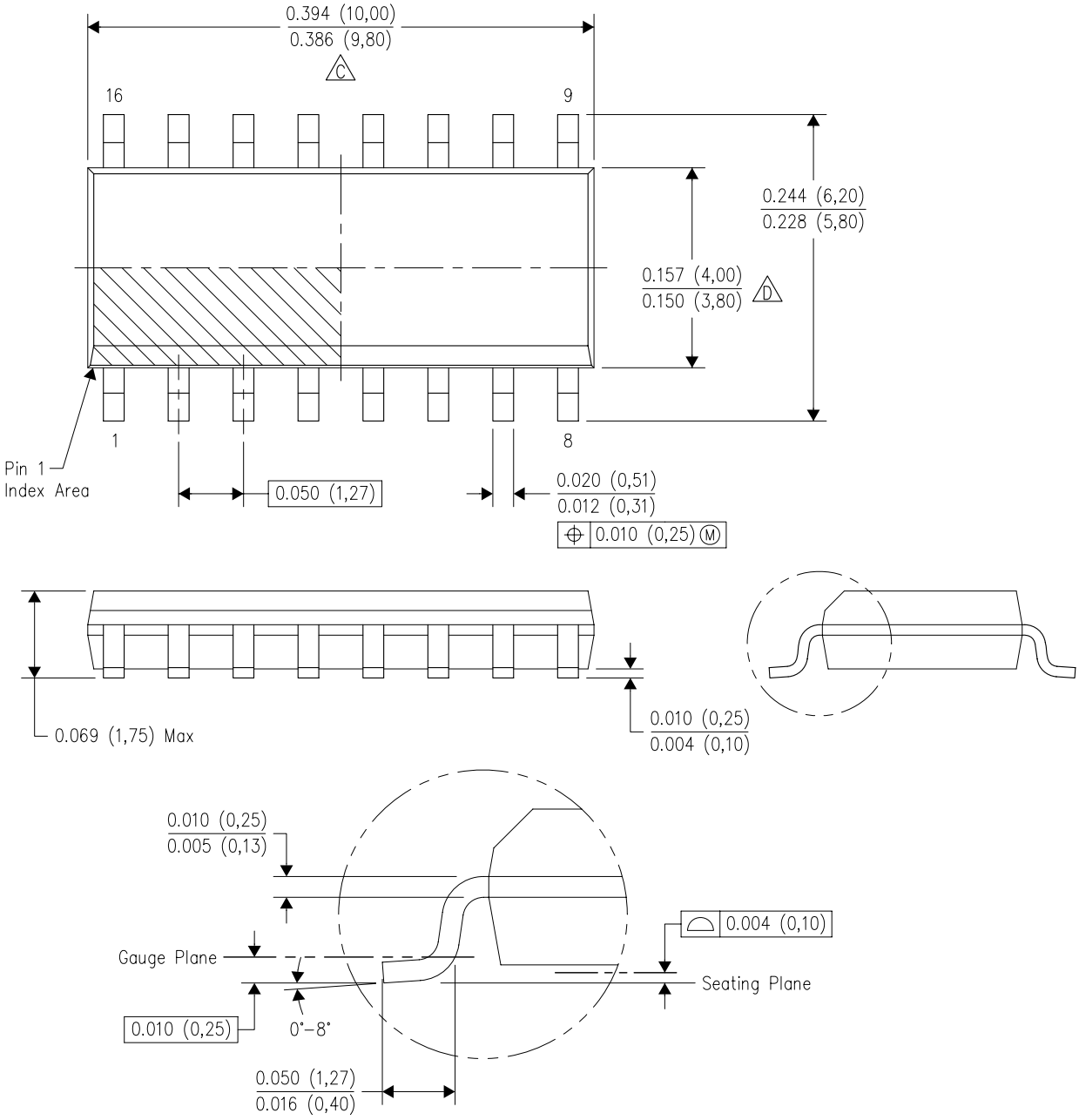
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

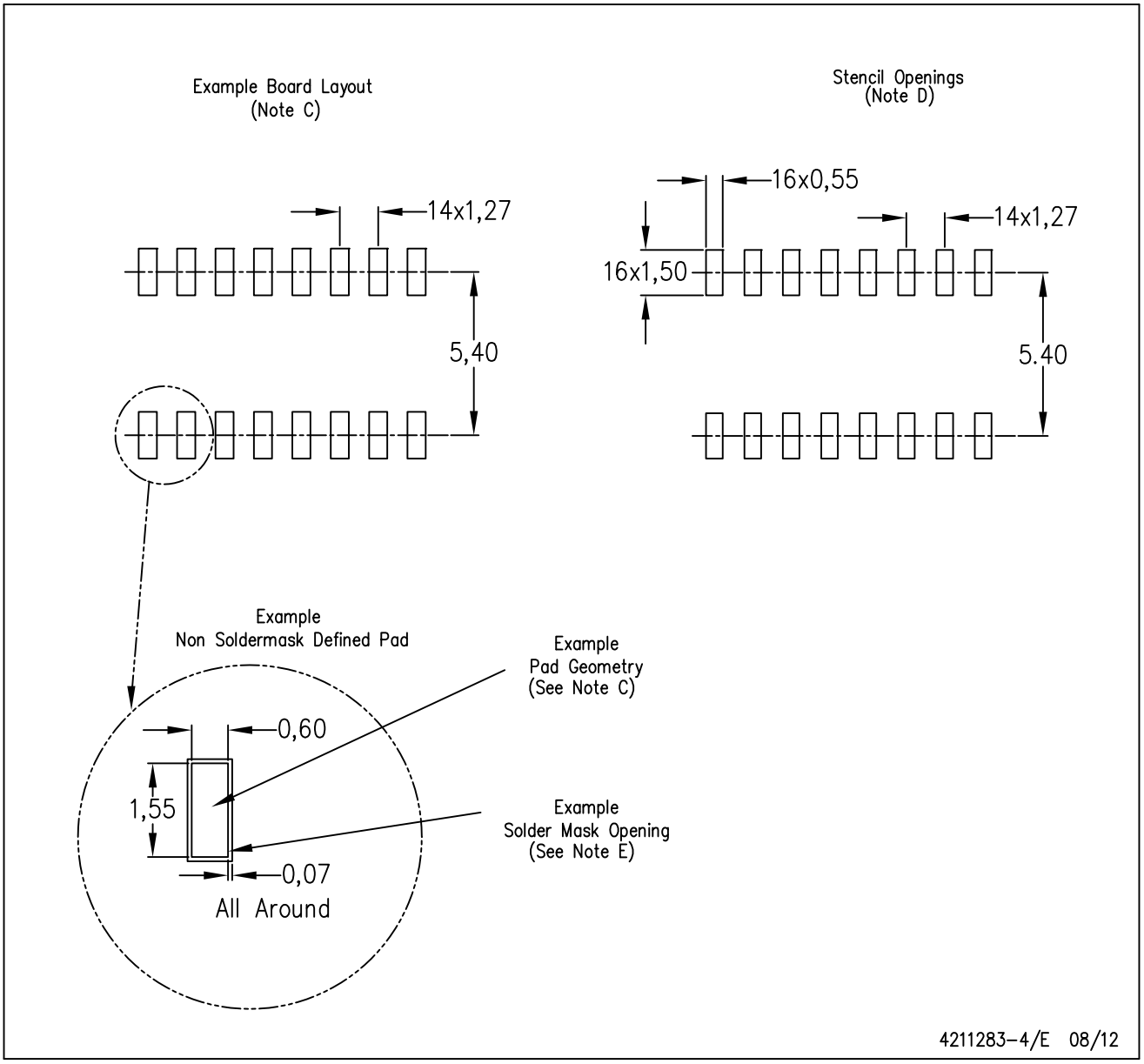
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC165M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HC165M96 | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| CD74HCT165M96 | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| CD74HCT165M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HCT165M96G4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

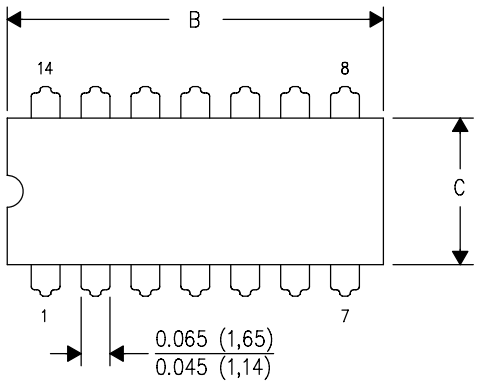



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

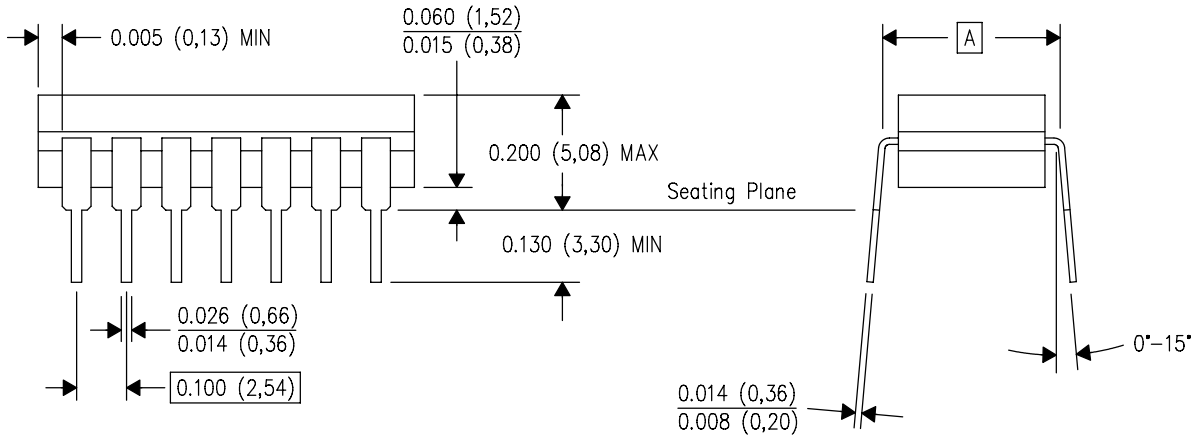
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



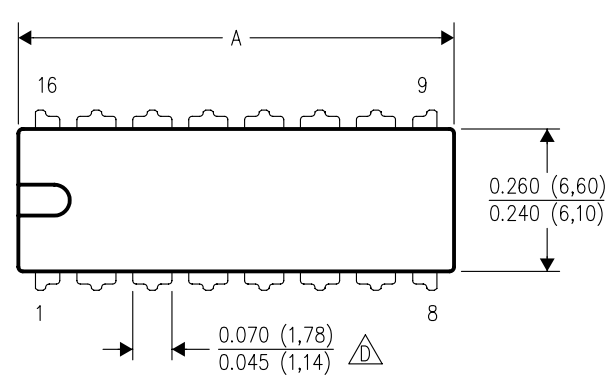

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

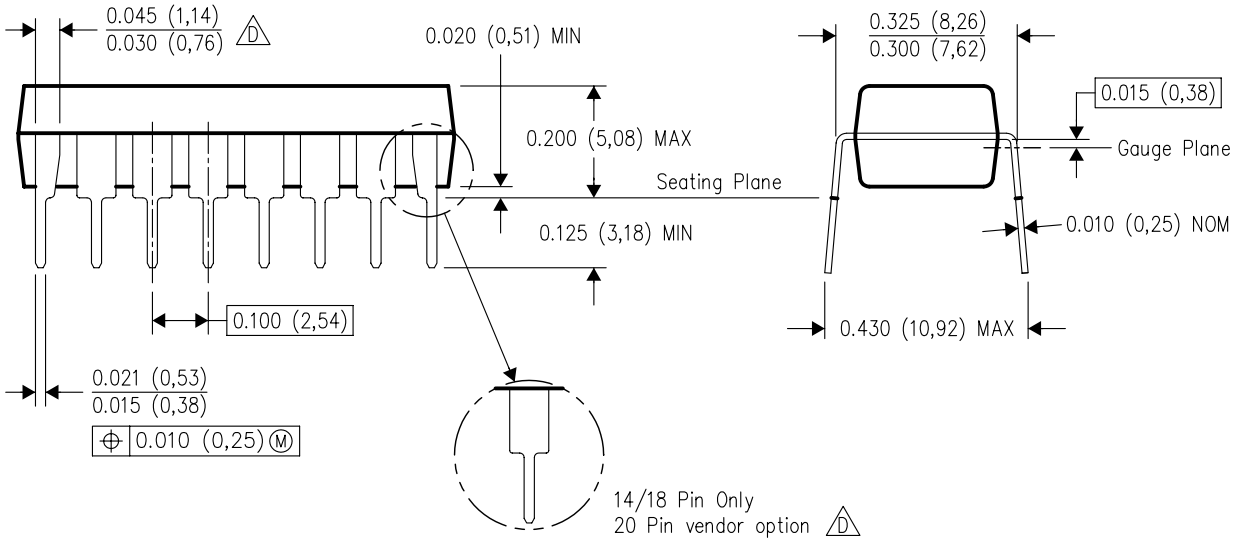
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265