VCA821 Ultra-Wideband, > 40-dB Gain Adjust Range, Linear in dB Variable Gain Amplifier

1 Features

- 710-MHz Small-Signal Bandwidth (G = +2 V/V)
- 320 MHz, 4 V_{PP} Bandwidth (G = +10 V/V)
- 0.1-dB Gain Flatness to 135 MHz
- 2500 V/µs Slew Rate
- > 40-dB Gain Adjust Range
- High Gain Accuracy: 20 dB ±0.3 dB
- High Output Current: ±90 mA

2 Applications

- AGC Receivers With RSSI
- Differential Line Receivers
- Pulse Amplitude Compensation
- Variable Attenuators
- Voltage-Tunable Active Filters

3 Description

The VCA821 device is a DC-coupled, wideband, linear in dB, continuously variable, voltage-controlled gain amplifier. It provides a differential input to single-ended conversion with a high-impedance gain control input used to vary the gain down 40 dB from the nominal maximum gain set by the gain resistor (R_G) and feedback resistor (R_F).

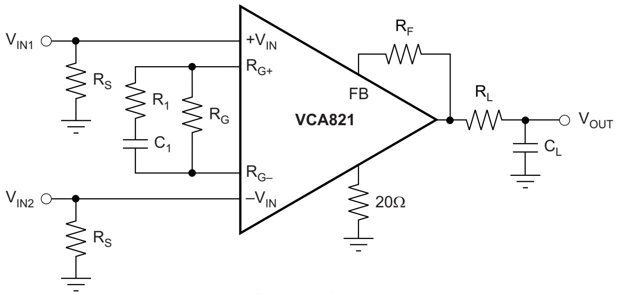
The VCA821 device internal architecture consists of two input buffers and an output current feedback amplifier stage integrated with a multiplier core to provide a complete variable gain amplifier (VGA) system that does not require external buffering. The maximum gain is set externally with two resistors, providing flexibility in designs. The maximum gain is intended to be set between 6 dB and 32 dB. Operating from ±5-V supplies, the gain control voltage for the VCA821 device adjusts the gain linearly in dB as the control voltage varies from 0V to +2 V. For example, set at a maximum gain of 20 dB, the VCA821 device provides 20 dB, at V_G = +2 V, to less than –20 dB at V_G = 0 V. The VCA821 device offers excellent gain linearity. For a 20-dB maximum gain, and a gain-control input voltage varying between +1 V and +2 V, the gain does not deviate by more than ±0.3 dB (maximum at +25°C).

Device Information[(1)]

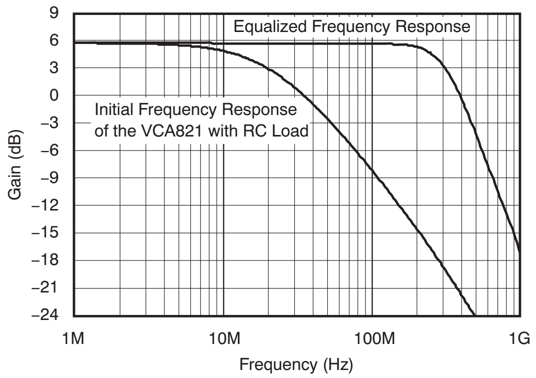
PART NUMBER	PACKAGE	BODY SIZE (NOM)
VCA821	SOIC (14)	8.65 mm × 3.91 mm
	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Differential Equalizer



Differential Equalization of an RC Load



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2015) to Revision D	Page
• Changed Output voltage swing values	8
• Changed Output current values	8

Changes from Revision B (December 2008) to Revision C	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table	1

Changes from Revision A (August 2008) to Revision B	Page
• Revised second paragraph in *Wideband Variable Gain Amplifier Operation* section describing pin 9	29

Changes from Original (December 2007) to Revision A	Page
• Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C	5

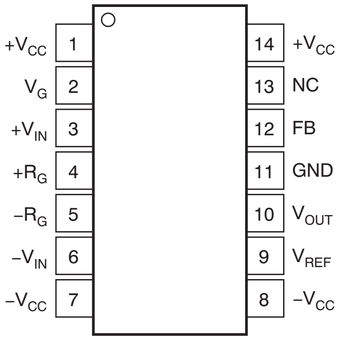
5 Device Comparison Table

VCA821 Related Products

SINGLES	DUALS	GAIN ADJUST RANGE (dB)	INPUT NOISE (nV/√Hz)	SIGNAL BANDWIDTH (MHz)
VCA810	—	80	2.4	35
—	VCA2612	45	1.25	80
—	VCA2613	45	1	80
—	VCA2615	52	0.8	50
—	VCA2617	48	4.1	50
VCA820	—	40	8.2	150
VCA821	—	40	6.0	420
VCA822	—	40	8.2	150
VCA824	—	40	6.0	420

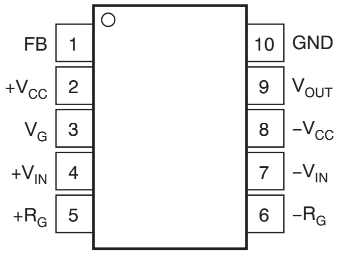
6 Pin Configuration and Functions

D Package
14-Pin SOIC
Top View



NC = No Connection

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC	VSSOP		
FB	12	1	I	Feedback Resistor Input
GND	11	10	—	Ground
NC	13	—	—	No Connection
+R_G	4	5	I	Gain Set Resistor
–R_G	5	6	I	Gain Set Resistor
+V_{CC}	1, 14	2	P	Positive Supply
–V_{CC}	7, 8	8	P	Negative Supply
+V_{IN}	3	4	I	Gain Control
–V_{IN}	6	7	I	Inverting Input
V_G	2	3	I	Noninverting Input
V_{OUT}	10	9	O	Output
V_{REF}	9	—	I	Output Voltage Reference

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power Supply		±6.5	V
Internal Power Dissipation	See *Thermal Information*		
Input Voltage		±V_S	V
Lead Temperature (soldering, 10 s)		260	°C
Junction Temperature (T_J)		150	°C
Junction Temperature (T_J) Maximum Continuous Operation		140	°C
Storage Temperature (T_{stg})	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating voltage	7	10	12	V
Operating temperature	–40	25	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		VCA821 D [SOIC] 14 PINS	VCA821 DGS [VSSOP] 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.3	173.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.8	46.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.9	94.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.8	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.6	92.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: V_S = ±5 V

At A_{VMAX} = 20 dB, R_F = 402 Ω, R_G = 80 Ω, R_L = 100 Ω, unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (1)
AC PERFORMANCE							
Small-signal bandwidth	G = 6dB, V_O = 500mV_{PP} G = 20dB, V_O = 500mV_{PP} G = 40dB, V_O = 500mV_{PP}			710		MHz	C
				420		MHz	C
				170		MHz	C
Large-signal bandwidth	G = 20dB, V_O = 4V_{PP}			320		MHz	C
Gain control bandwidth	V_O = 200mV_{PP}	+25° C (2)	240	330		MHz	B
		0° C to 70° C (3)	235				
		–40° C to +85° C (3)	235				
Bandwidth for 0.1dB flatness	G = 20dB, V_O = 200mV_{PP}			135		MHz	C
Slew rate	G = 20dB, V_O = 5V Step	+25° C (2)	1800	2500		V/µs	B
		0° C to 70° C (3)	1700				
		–40° C to +85° C (3)	1700				
Rise-and-fall time	G = 20dB, V_O = 5V Step	+25° C (2)		1.5	1.8	ns	B
		0° C to 70° C (3)			1.9		
		–40° C to +85° C (3)			1.9		
Settling time to 0.01%	G = 20dB, V_O = 5V Step			11		ns	C
Harmonic distortion, 2nd-harmonic	V_O = 2V_{PP}, f = 20MHz	+25° C (2)	–64	–66		dBc	B
		0° C to 70° C (3)	–64				
		–40° C to +85° C (3)	–64				
Harmonic distortion, 3rd -harmonic	V_O = 2V_{PP}, f = 20MHz	+25° C (2)	–61	–63		dBc	B
		0° C to 70° C (3)	–61				
		–40° C to +85° C (3)	–61				
Input voltage noise	f > 100kHz			6.0		nV/√Hz	C
Input current noise	f > 100kHz			2.6		pA/√Hz	C
GAIN CONTROL							
Absolute gain error	G_{MAX} = 20dB, V_G = 2V	+25° C (2)		±0.1	±0.4	dB	A
		0° C to 70° C (3)			±0.5		
		–40° C to +85° C (3)			±0.6		
V_{ctrl0}				0.85		V	C
V_{Slope}				0.09		V	C
Absolute gain error	G_{MAX} = 20dB, V_G = 1V, (G = 18.06 dB)	+25° C (2)		±0.3	±0.4	dB	A
		0° C to 70° C (3)			±0.5		
		–40° C to +85° C (3)			±0.6		
Gain at V_G = 0.2V	Relative to max gain	+25° C (2)		–26	–24	dB	A
		0° C to 70° C (3)			–24		
		–40° C to +85° C (3)			–23		
Gain control bias current	+25° C (2)			10	16	µA	A
	0° C to 70° C (3)				16.6		
	–40° C to +85° C (3)				16.7		
Average gain control bias current drift	0° C to 70° C (3)				±12	nA/°C	B
	–40° C to +85° C (3)				±12		
Gain control input impedance				1.5 || 0.6		MΩ || pF	C
DC PERFORMANCE							
Input offset voltage	G = 20dB, V_{CM} = 0V, V_G = 1V	+25° C (2)		±4	±17	mV	A
		0° C to 70° C (3)			±17.8		
		–40° C to +85° C (3)			±19		
Average input offset voltage drift	G = 20dB, V_{CM} = 0V, V_G = 1V	0° C to 70° C (3)			30	µV/°C	B
		–40° C to +85° C (3)			30		

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(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(2) Junction temperature = ambient for +25°C tested specifications.

(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.

Electrical Characteristics: V_S = ±5 V (continued)

At A_{VMAX} = 20 dB, R_F = 402 Ω, R_G = 80 Ω, R_L = 100 Ω, unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL[1]
Input bias current	G = 20dB, V_{CM} = 0V, V_G = 1V	+25° C [2]		19	25	μA	A
		0° C to 70° C [3]			29		
		–40° C to +85° C [3]			31		
Average input bias current drift	G = 20dB, V_{CM} = 0V, V_G = 1V	0° C to 70° C [3]			90	nA/°C	B
		–40° C to +85° C [3]			90		
Input offset current	G = 20dB, V_{CM} = 0V, V_G = 1V	+25° C [2]		±0.5	±2.5	μA	A
		0° C to 70° C [3]			±3.2		
		–40° C to +85° C [3]			±3.5		
Average input offset current drift	G = 20dB, V_{CM} = 0V, V_G = 1V	0° C to 70° C [3]			±16	nA/°C	B
		–40° C to +85° C [3]			±16		
$I_{RG\ MAX}$ Max current through gain resistance	+25° C [2]			±2.6	±2.55	mA	B
	0° C to 70° C [3]				±2.55		
	–40° C to +85° C [3]				±2.5		
INPUT							
Most positive common mode input voltage	R_L = 100Ω	+25° C [2]	+1.6	+1.6		V	A
		0° C to 70° C [3]	+1.6				
		–40° C to +85° C [3]	+1.6				
Most negative common mode input voltage	R_L = 100Ω	+25° C [2]		–2.1	-2.1	V	A
		0° C to 70° C [3]			–2.1		
		–40° C to +85° C [3]			–2.1		
Common-mode rejection ratio	V_{CM} = ±0.5V	+25° C [2]	65	80		dB	A
		0° C to 70° C [3]	60				
		–40° C to +85° C [3]	60				
Input impedance, differential				0.9 || 0.6		MΩ || pF	C
Input impedance, common-mode				1 || 2		MΩ || pF	C

Electrical Characteristics: V_S = ±5 V (continued)

At A_{VMAX} = 20 dB, R_F = 402 Ω, R_G = 80 Ω, R_L = 100 Ω, unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL[1]
OUTPUT							
Output voltage swing	R_L = 1kΩ	+25° C [2]	±3.6	±3.9		V	A
		0° C to 70° C [3]	±3.4				
		–40° C to +85° C [3]	±3.3				
	R_L = 100Ω	+25° C [2]	±3.5	–3.3/+3.6	–3.2	V	A
		0° C to 70° C [3]	+3.3		–3.0		
		–40° C to +85° C [3]	+3.2		–2.9		
Output current	V_O = 0V, R_L = 10Ω	+25° C [2]	+60	–55/+90	–50	mA	A
		0° C to 70° C [3]	+50		–42		
		–40° C to +85° C [3]	+45		–38		
Output impedance	G = +10V/V, f > 100kHz			0.01		Ω	C
POWER SUPPLY							
Specified operating voltage				±5		V	C
Minimum operating voltage				±3.5		V	C
Maximum operating voltage	+25° C [2]				±6	V	A
	0° C to 70° C [3]				±6		
	–40° C to +85° C [3]				±6		
Maximum quiescent current	V_G = 1V	+25° C [2]		34	35	mA	A
		0° C to 70° C [3]			35.5		
		–40° C to +85° C [3]			36		
Minimum quiescent current	V_G = 1V	+25° C [2]		34	32.5	mA	A
		0° C to 70° C [3]			32		
		–40° C to +85° C [3]			31.5		
–PSRR Power-supply rejection ratio	+25° C [2]		–61	–68		dB	A
	0° C to 70° C [3]		–59				
	–40° C to +85° C [3]		–58				
THERMAL CHARACTERISTICS							
Specified operating range, D package				–40 to +85		°C	C
θ_{JA} Junction-to-ambient thermal resistance	VSSOP-10 (DGS)			130		°C/W	C
	SOIC-14 (D)			80		°C/W	C

7.6 Typical Characteristics: V_S = ±5 V, DC Parameters

At T_A = +25°C, R_L = 100 Ω, V_G = +2 V, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

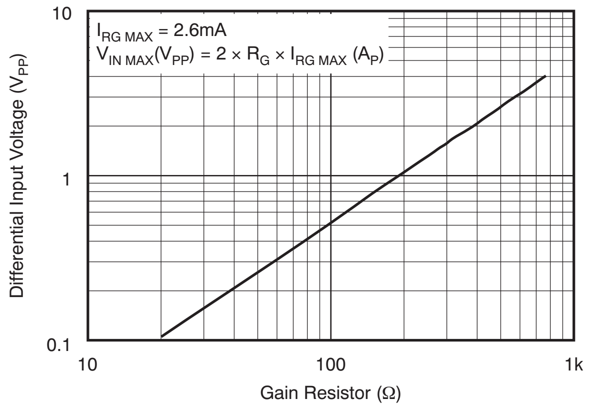

Figure 1. Maximum Differential Input Voltage vs R_G

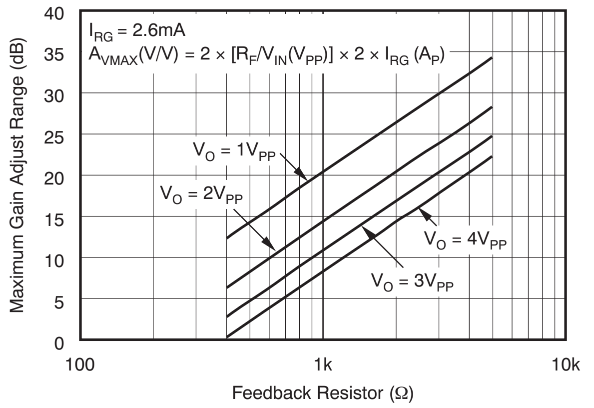

Figure 2. Maximum Gain Adjust Range vs R_F

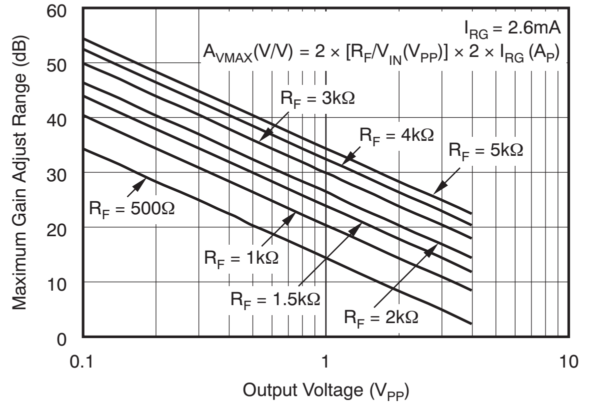

Figure 3. Maximum Gain Adjust Range vs Peak-to-Peak Output Voltage

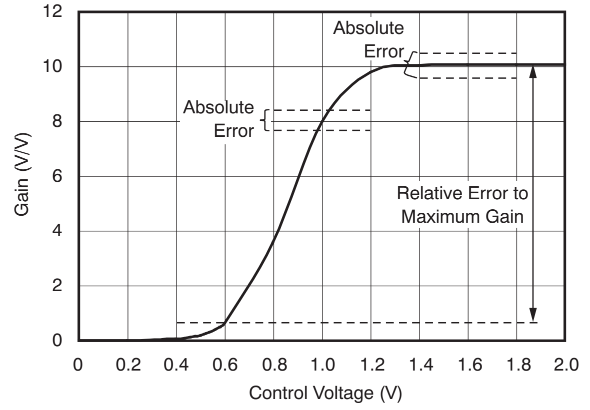

Figure 4. Gain Error Band vs Gain Control Voltage

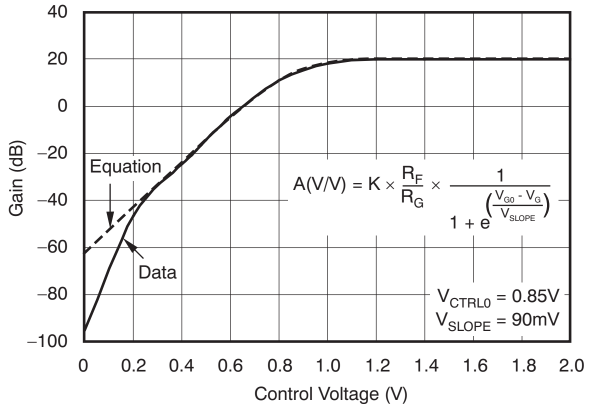

Figure 5. Gain Error Band vs Gain Control Voltage

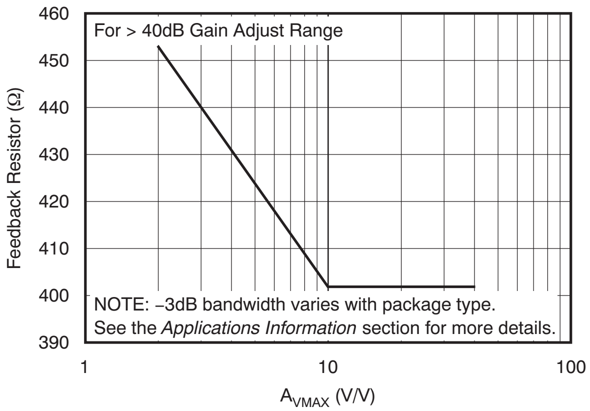

Figure 6. Recommended R_F vs A_{VMAX}

7.7 Typical Characteristics: V_S = ±5 V, DC and Power-Supply Parameters

At T_A = +25°C, R_L = 100 Ω, V_G = +2 V, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

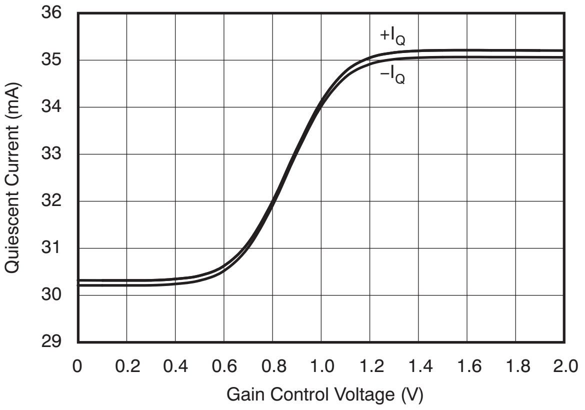

Figure 7. Supply Current vs Control Voltage (A_{VMAX} = 6 dB)

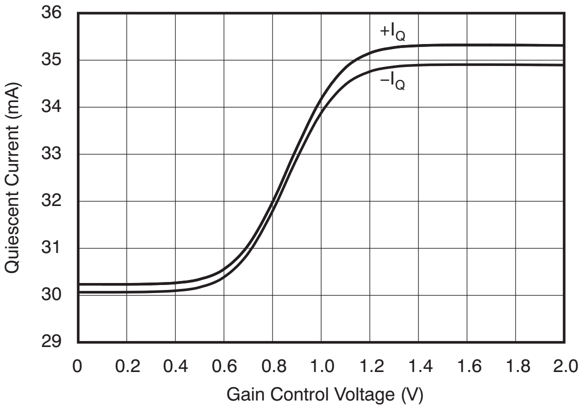

Figure 8. Supply Current vs Control voltage (A_{VMAX} = 20 dB)

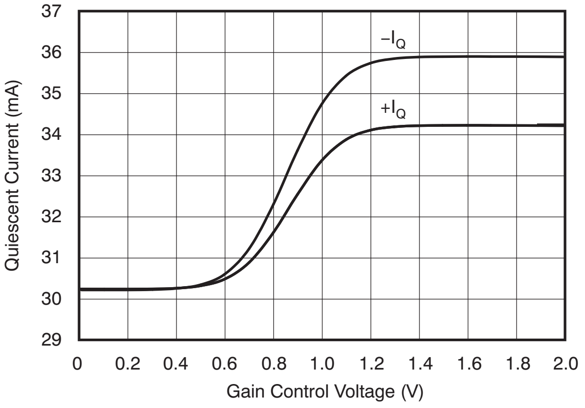

Figure 9. Supply Current vs Control Voltage (A_{VMAX} = 32 dB)

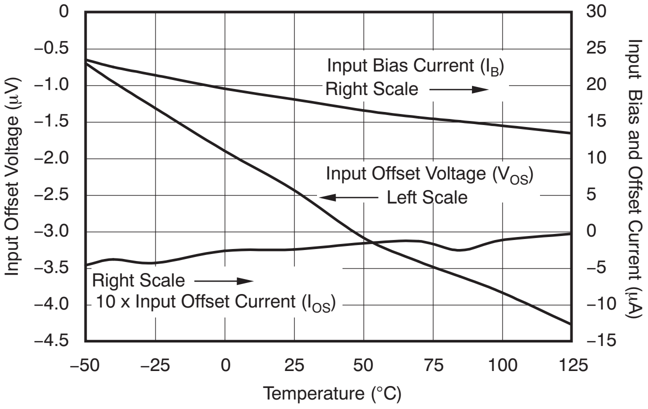

Figure 10. Typical DC Drift vs Temperature

7.8 Typical Characteristics: V_S = ±5 V, A_{VMAX} = 6 dB

At T_A = 25°C, R_L = 100 Ω, R_F = 453 Ω, R_G = 453 Ω, V_G = 2 V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SOIC package, unless otherwise noted.

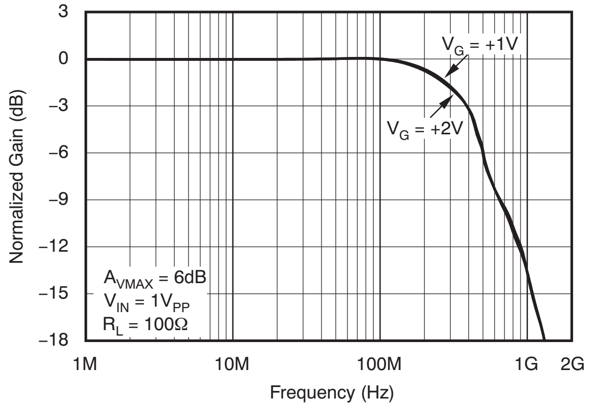

Figure 11. Small-Signal Frequency Response

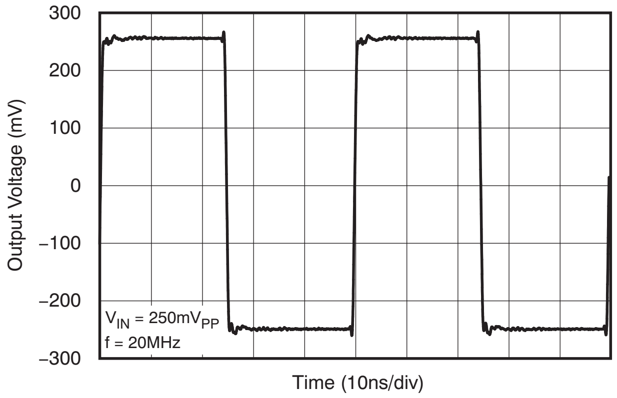

Figure 12. Small-Signal Pulse Response

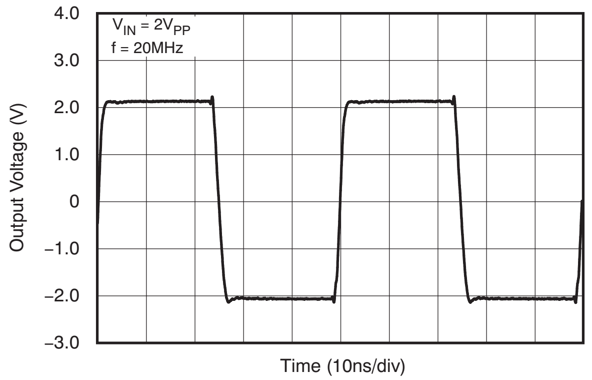

Figure 13. Large-Signal Pulse Response

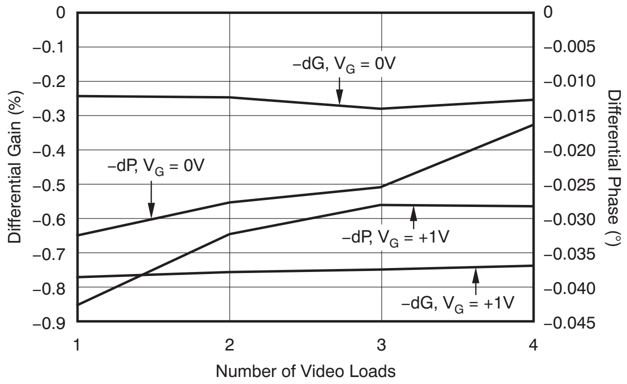

Figure 14. Composite Video dG/dP

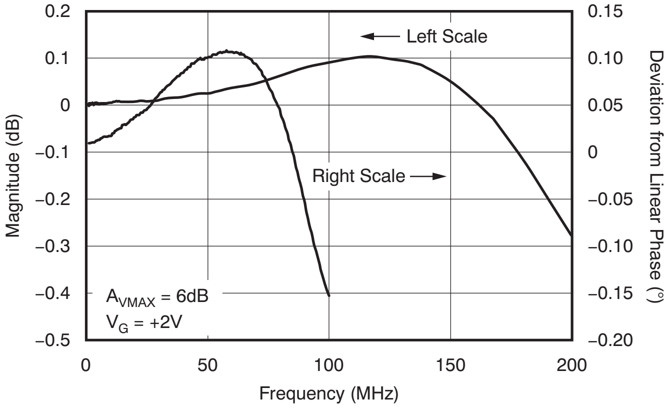

Figure 15. Gain Flatness, Deviation From Linear Phase

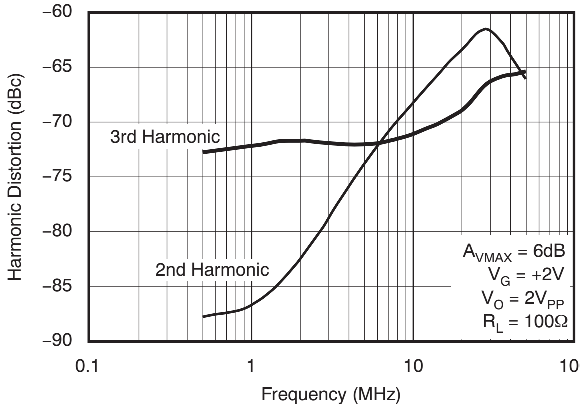

Figure 16. Harmonic Distortion vs Frequency

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 6 dB (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 453 Ω, R_G = 453 Ω, V_G = 2 V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SOIC package, unless otherwise noted.

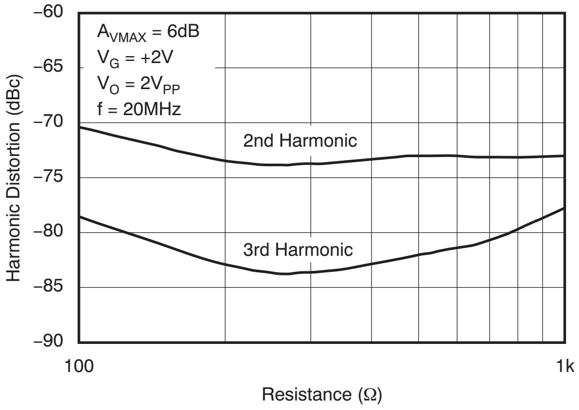

Figure 17. Harmonic Distortion vs Load Resistance

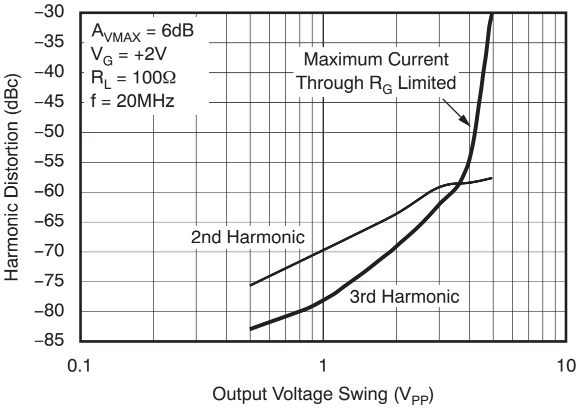

Figure 18. Harmonic Distortion vs Output Voltage

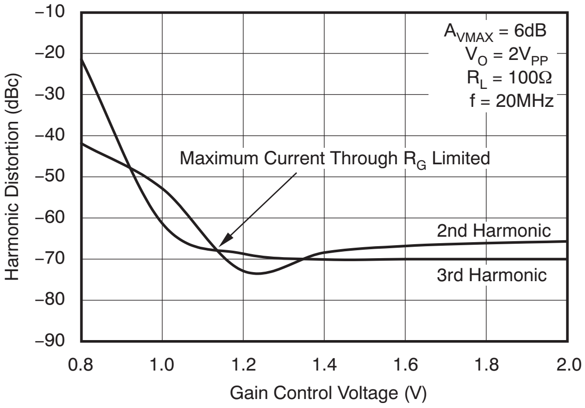

Figure 19. Harmonic Distortion vs Gain Control Voltage

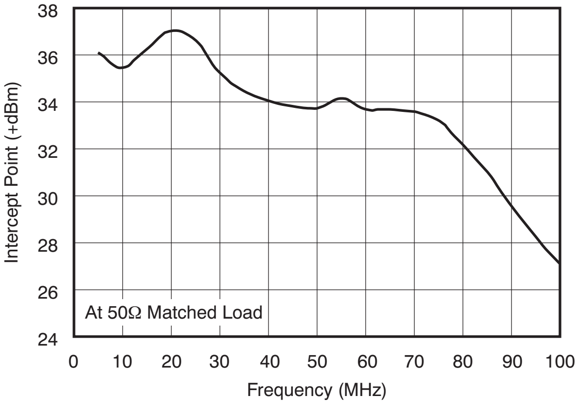

Figure 20. Two-Tone, Third-Order Intermodulation Intercept

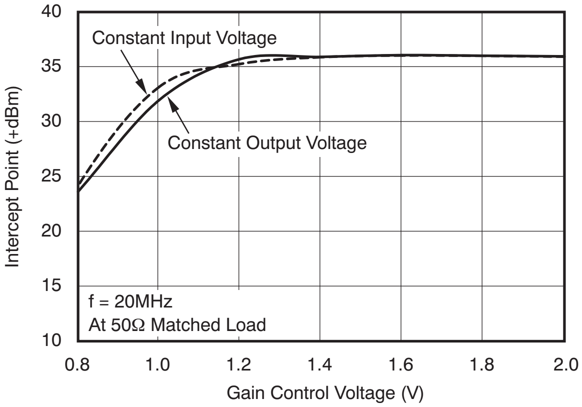

Figure 21. Two-Tone, Third-Order Intermodulation Intercept vs Gain Control Voltage

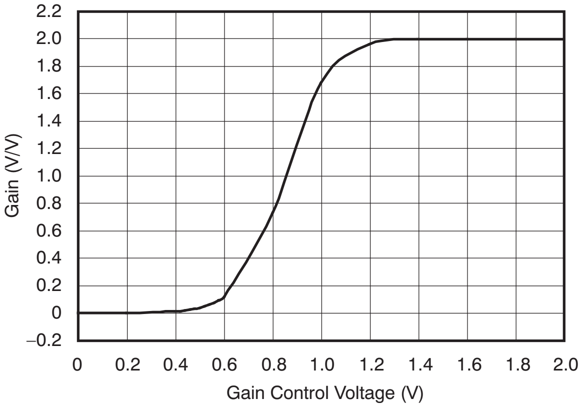

Figure 22. Gain vs Gain Control Voltage

Typical Characteristics: $V_S = \pm5$ V, $A_{VMAX} = 6$ dB (continued)

At $T_A = 25°C$, $R_L = 100\ \Omega$, $R_F = 453\ \Omega$, $R_G = 453\ \Omega$, $V_G = 2$ V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SOIC package, unless otherwise noted.

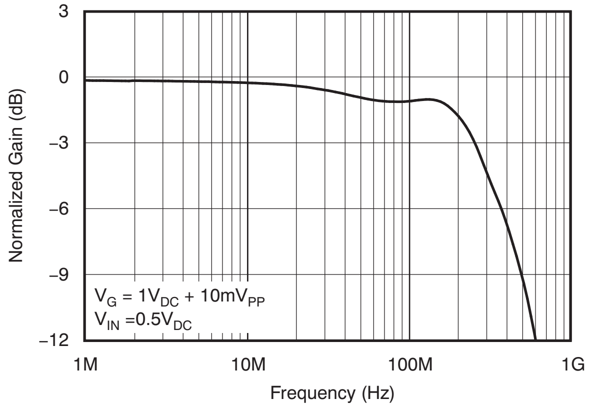

Figure 23. Gain Control Frequency Response

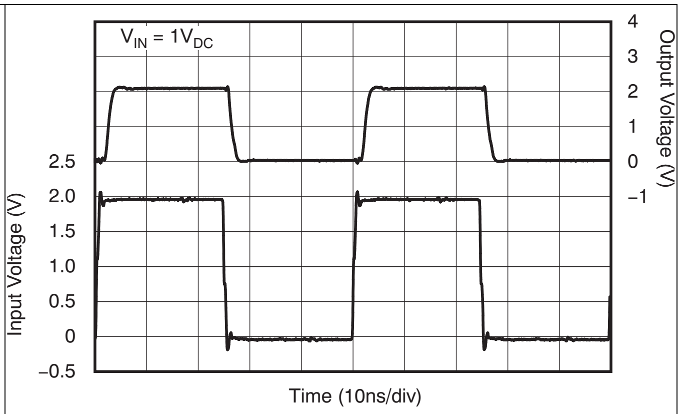

Figure 24. Gain Control Pulse Response

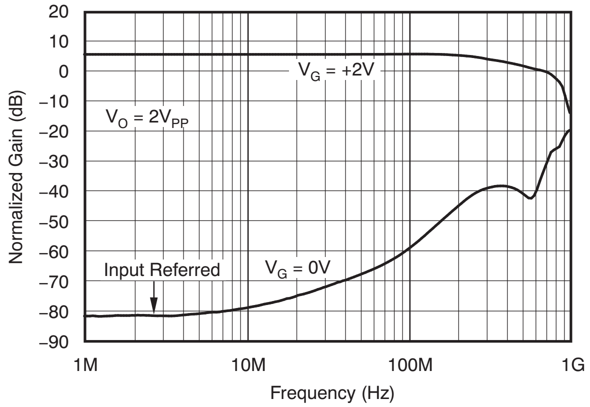

Figure 25. Fully-Attenuated Response

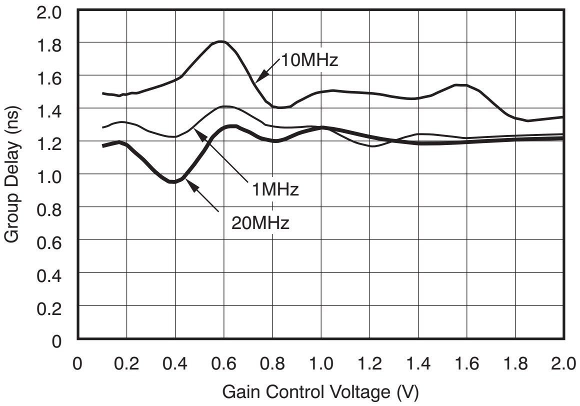

Figure 26. Group Delay vs Gain Control Voltage

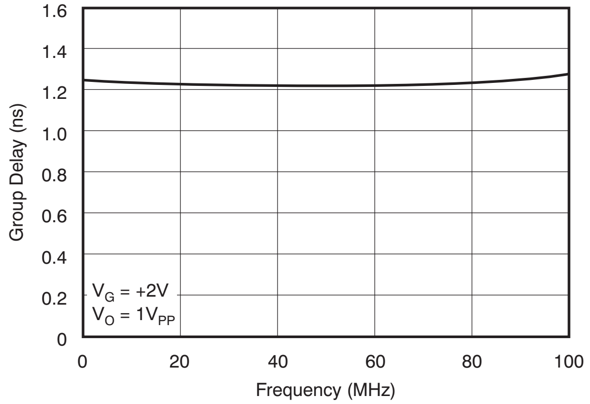

Figure 27. Group Delay vs Frequency

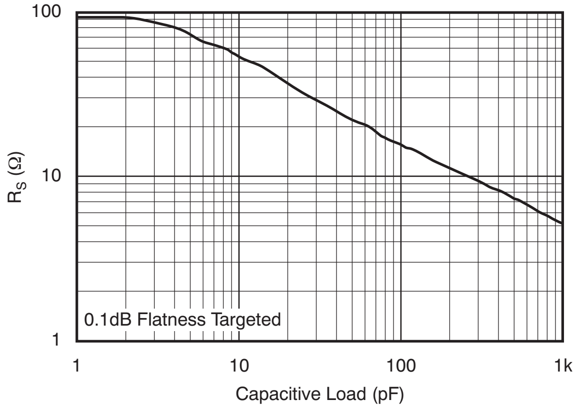

Figure 28. Recommended R_S vs Capacitive Load

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 6 dB (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 453 Ω, R_G = 453 Ω, V_G = 2 V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SOIC package, unless otherwise noted.

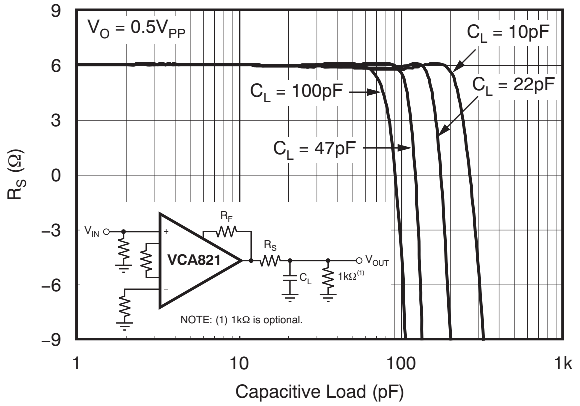

Figure 29. Frequency Response vs Capacitive Load

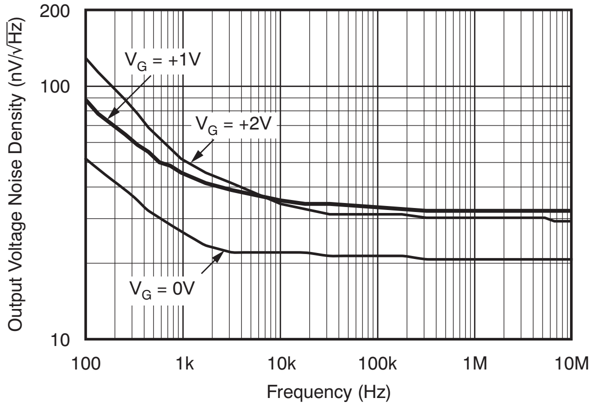

Figure 30. Output Voltage Noise Density

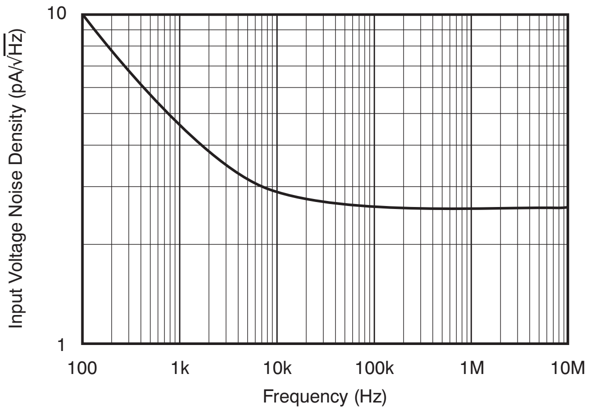

Figure 31. Input Current Noise Density

7.9 Typical Characteristics: $V_S = \pm 5$ V, $A_{VMAX} = 20$ dB

At $T_A = +25°C$, $R_L = 100\ \Omega$, $R_F = 402\ \Omega$, $R_G = 80\ \Omega$, $V_G = +2$ V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

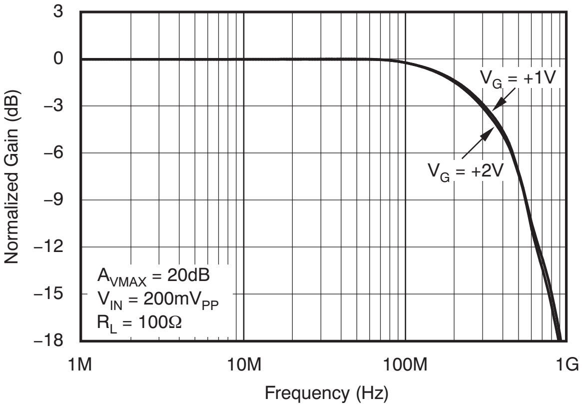

Figure 32. Small-Signal Frequency Response

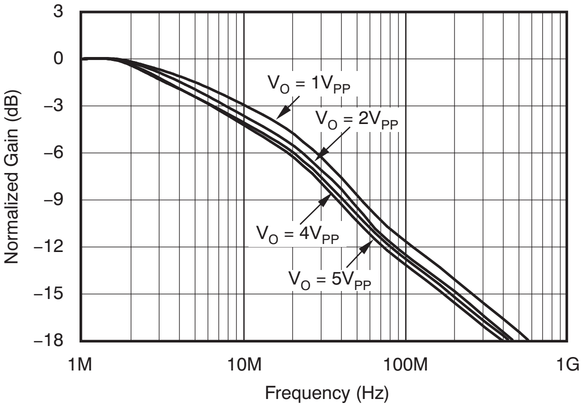

Figure 33. Large-Signal Frequency Response

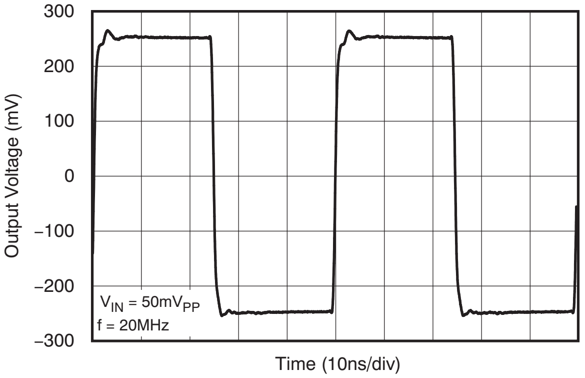

Figure 34. Small-Signal Pulse Response

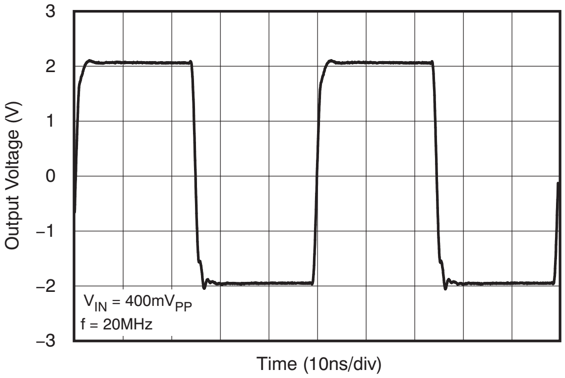

Figure 35. Large-Signal Pulse Response

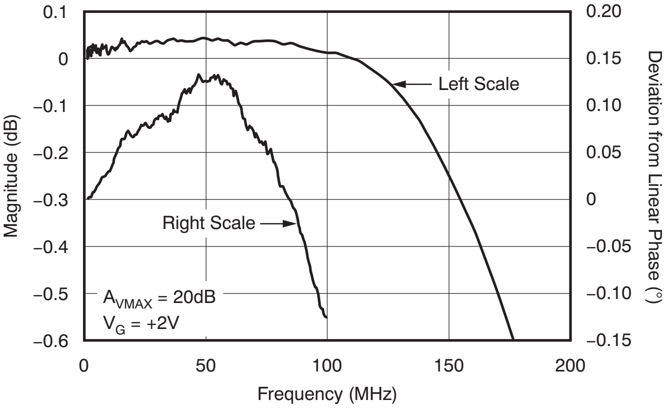

Figure 36. Gain Flatness, Deviation From Linear Phase

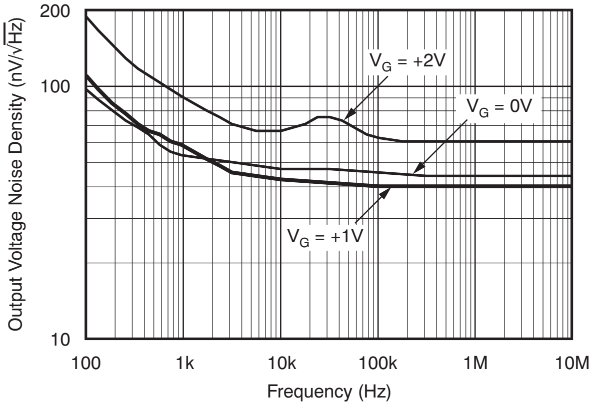

Figure 37. Output Voltage Noise Density

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 20 dB (continued)

At T_A = +25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 80 Ω, V_G = +2 V, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

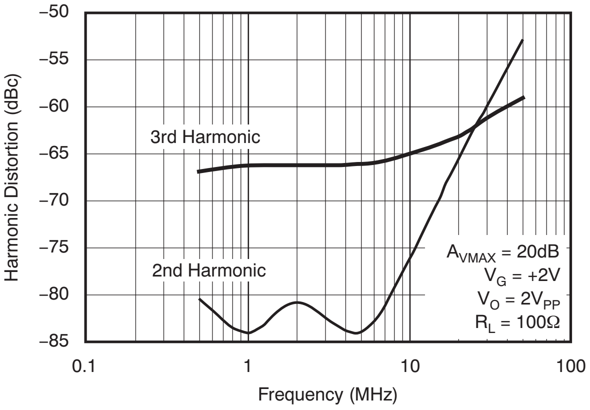

Figure 38. Harmonic Distortion vs Frequency

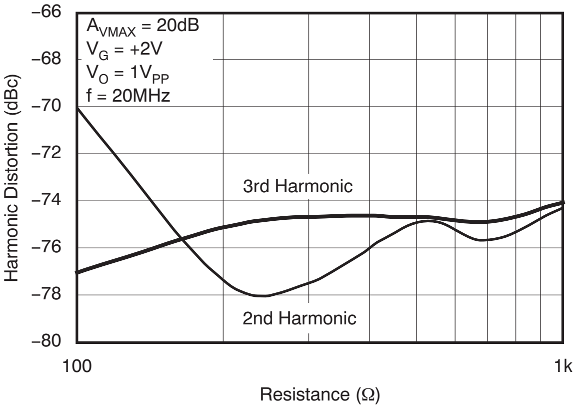

Figure 39. Harmonic Distortion vs Load Resistance

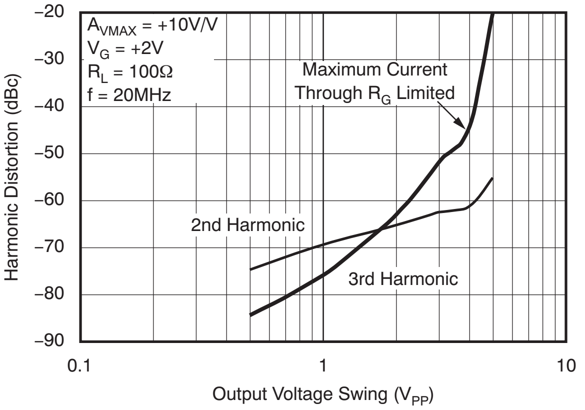

Figure 40. Harmonic Distortion vs Output Voltage

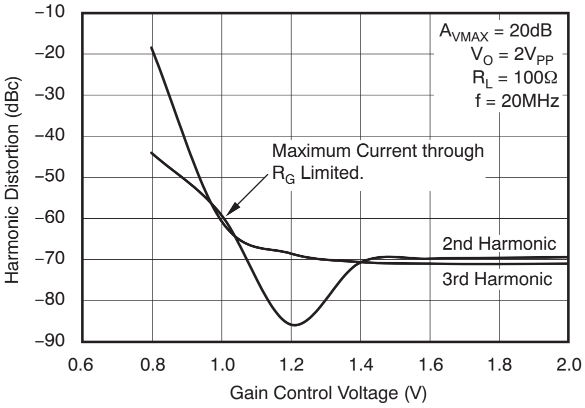

Figure 41. Harmonic Distortion vs Gain Control Voltage

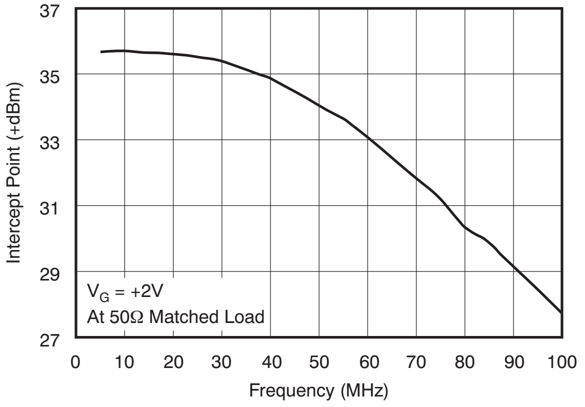

Figure 42. Two-Tone, Third-Order Intermodulation Intercept

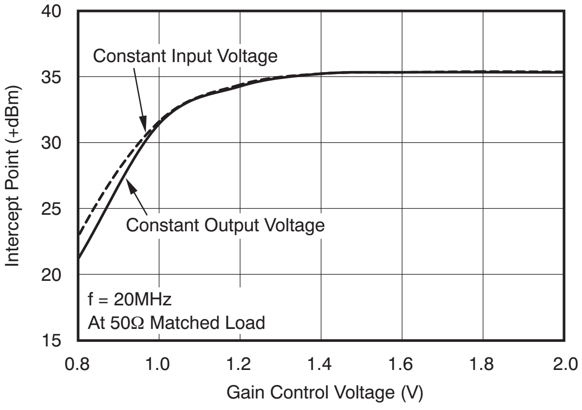

Figure 43. Two-Tone, Third-Order Intermodulation Intercept vs Gain Control Voltage

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 20 dB (continued)

At T_A = +25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 80 Ω, V_G = +2 V, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

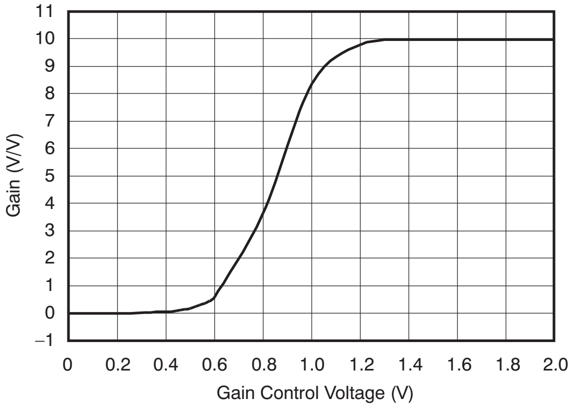

Figure 44. Gain vs Gain Control Voltage

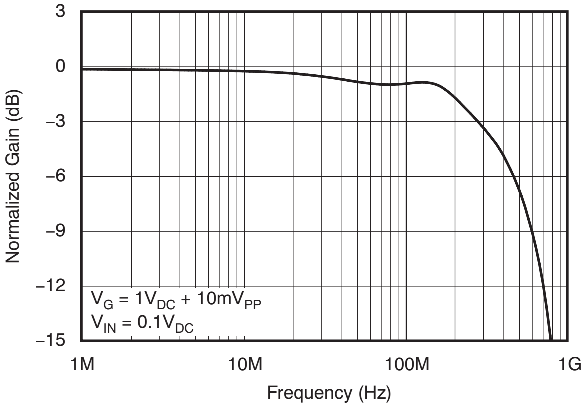

Figure 45. Gain Control Frequency Response

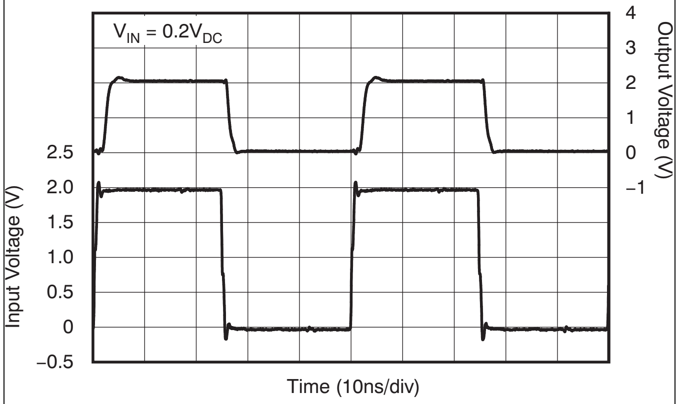

Figure 46. Gain Control Pulse Response

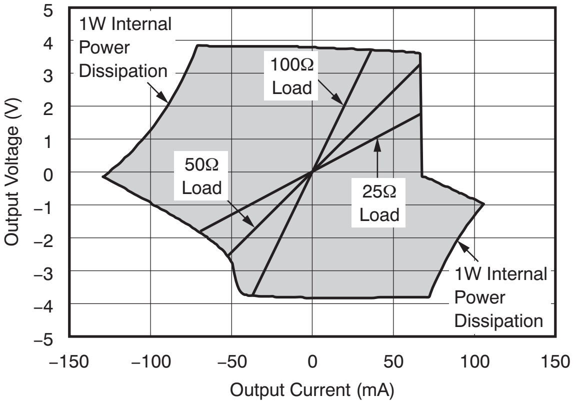

Figure 47. Output Voltage and Current Limitations

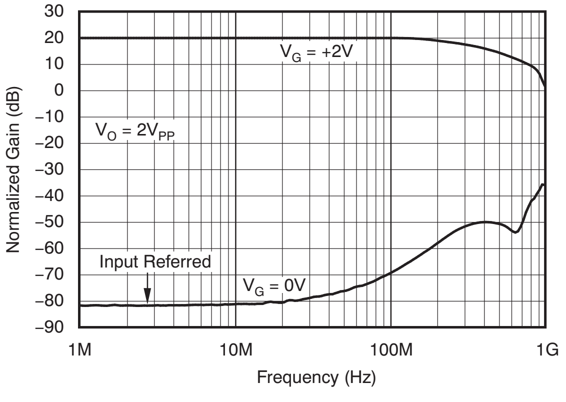

Figure 48. Fully-Attenuated Response

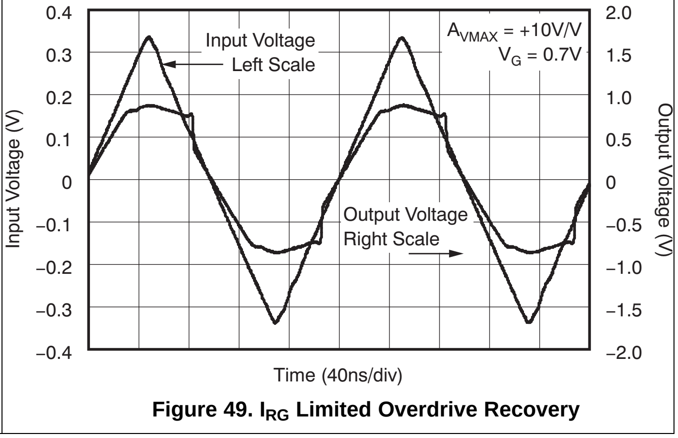

Figure 49. I_{RG} Limited Overdrive Recovery

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 20 dB (continued)

At T_A = +25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 80 Ω, V_G = +2 V, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

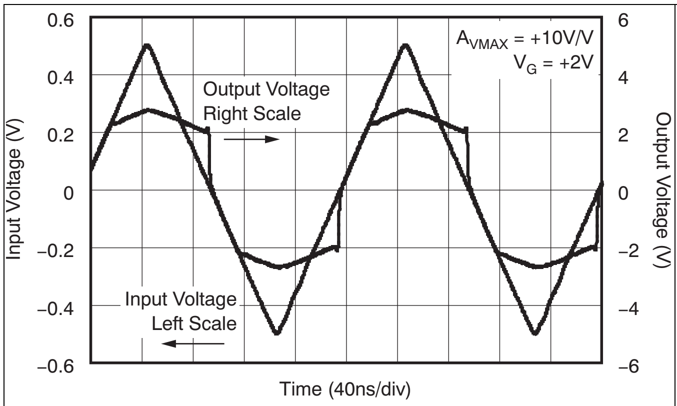

Figure 50. Output Limited Overdrive Recovery

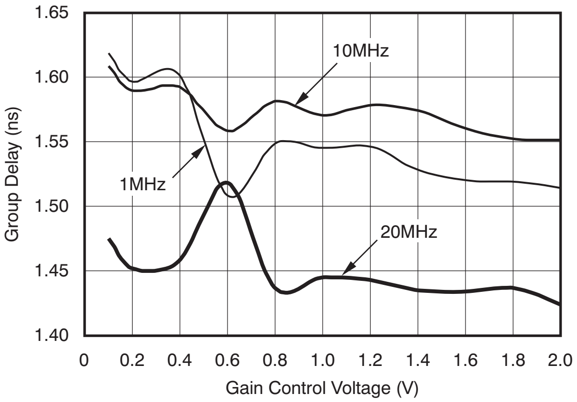

Figure 51. Group Delay vs Gain Control Voltage

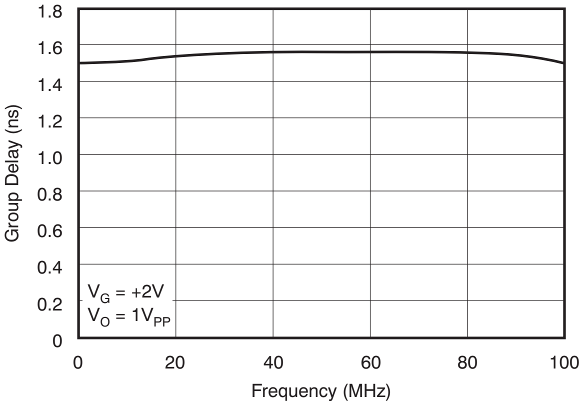

Figure 52. Group Delay vs Frequency

7.10 Typical Characteristics: V_S = ±5 V, A_{VMAX} = 32 dB

At T_A = +25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 18 Ω, V_G = +2 V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SOIC package, unless otherwise noted.

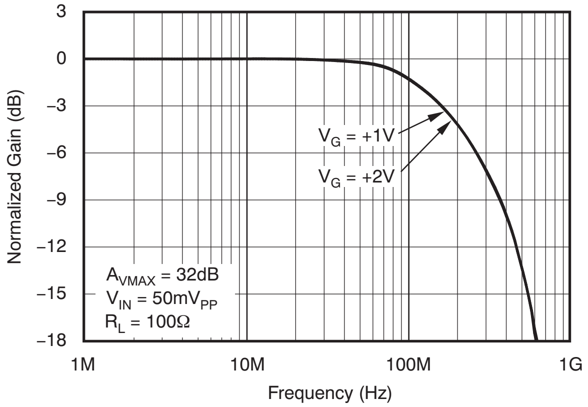

Figure 53. Small-Signal Frequency Response

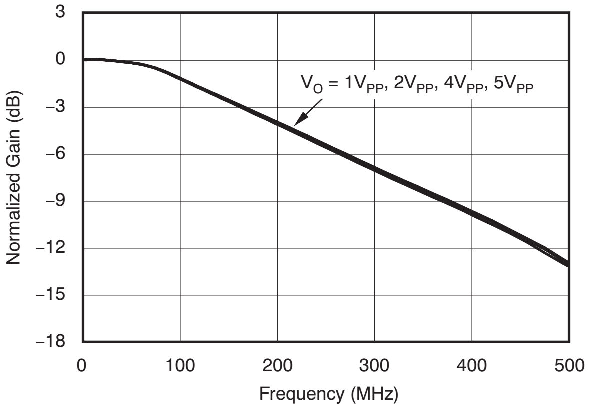

Figure 54. Large-Signal Frequency Response

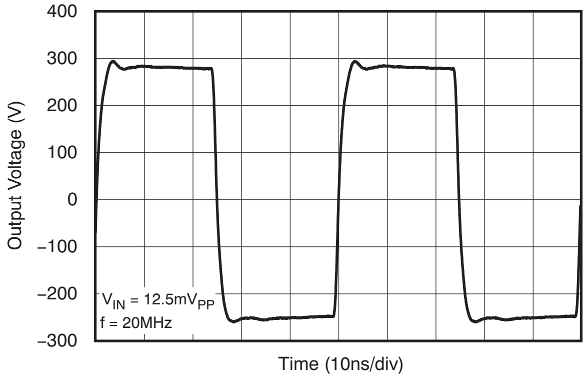

Figure 55. Small-Signal Pulse Response

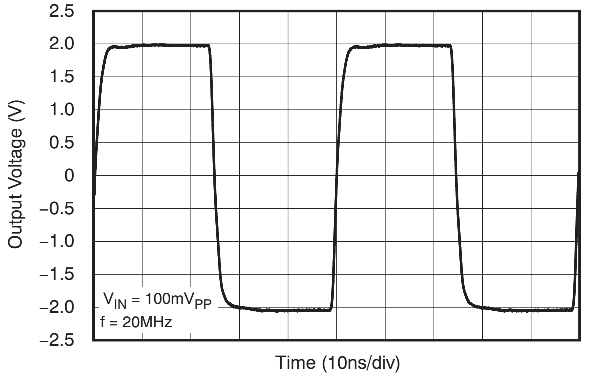

Figure 56. Large-Signal Pulse response

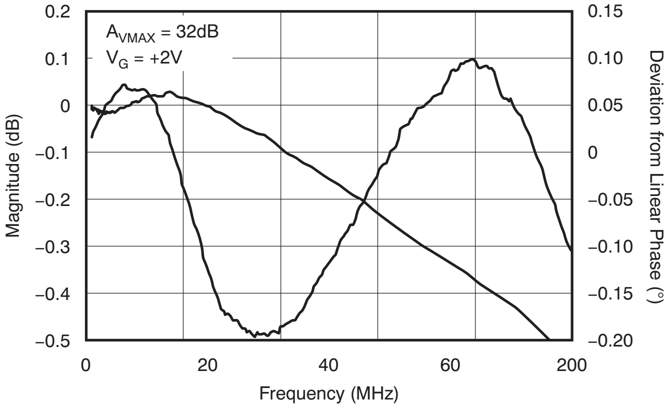

Figure 57. Gain Flatness, Deviation From Linear Phase

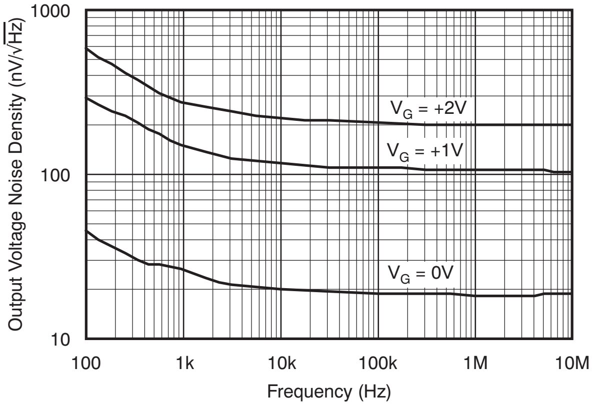

Figure 58. Output Voltage Noise Density

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 32 dB (continued)

At T_A = +25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 18 Ω, V_G = +2 V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SOIC package, unless otherwise noted.

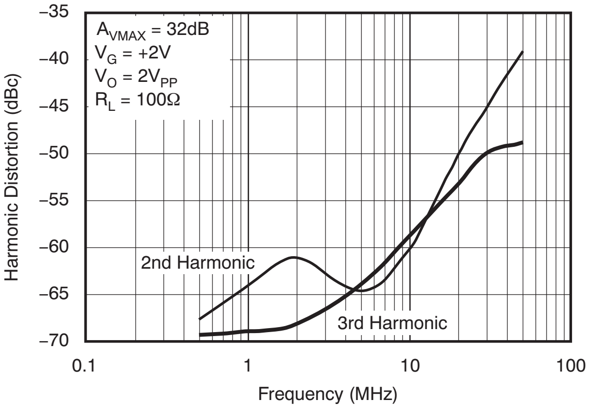

Figure 59. Harmonic Distortion vs Frequency

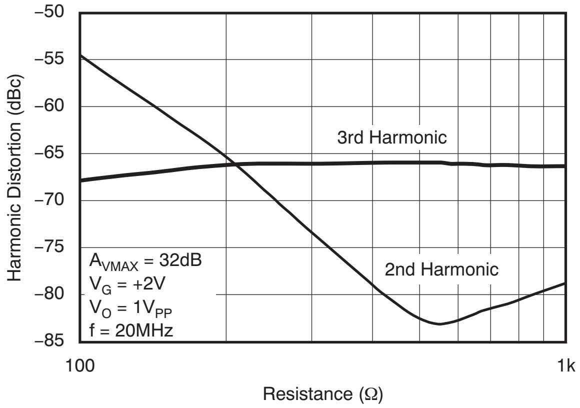

Figure 60. Harmonic Distortion vs Load Resistance

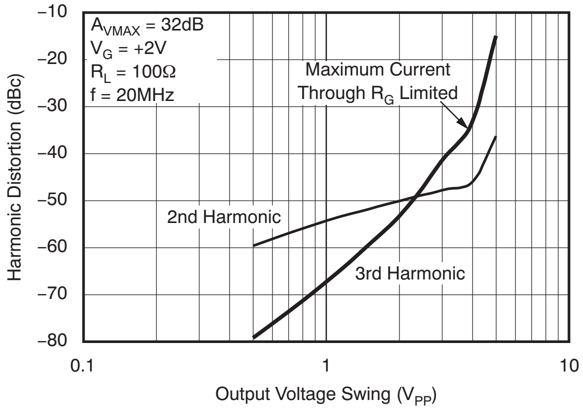

Figure 61. Harmonic Distortion Output Voltage

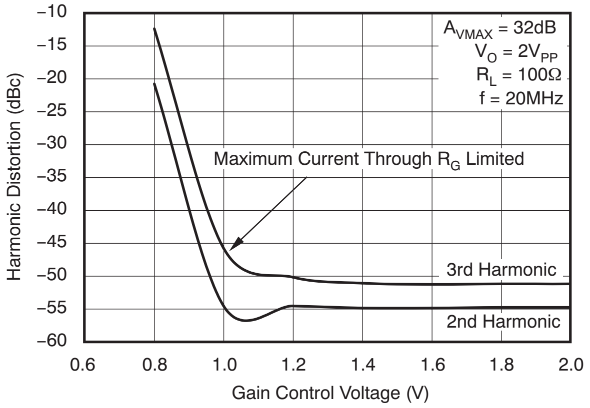

Figure 62. Harmonic Distortion vs Gain Control Voltage

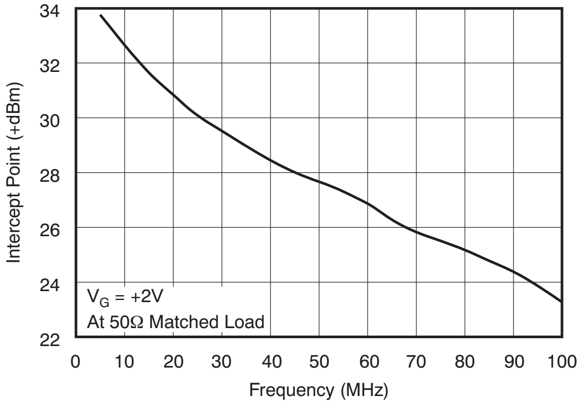

Figure 63. Two-Tone, Third-Order Intermodulation Intercept

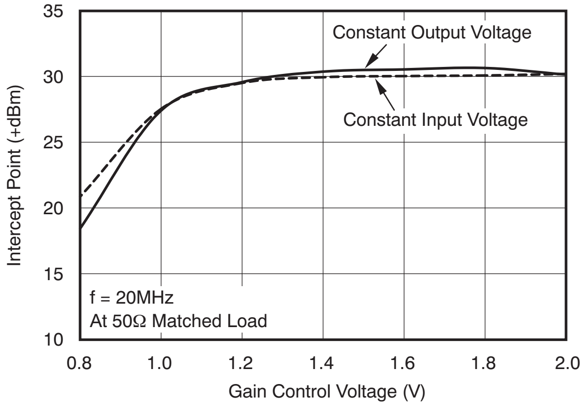

Figure 64. Two-Tone, Third-Order Intermodulation Intercept vs Gain Control Voltage

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 32 dB (continued)

At T_A = +25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 18 Ω, V_G = +2 V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SOIC package, unless otherwise noted.

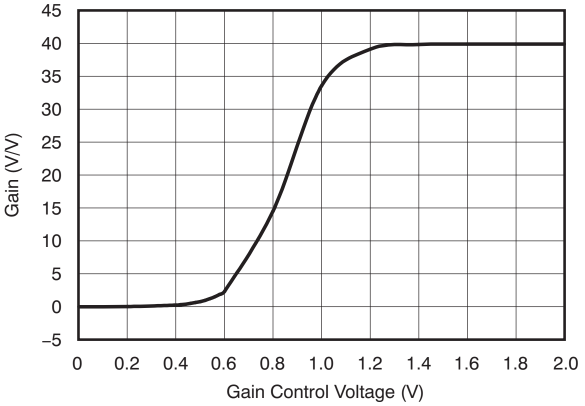

Figure 65. Gain vs Gain Control Voltage

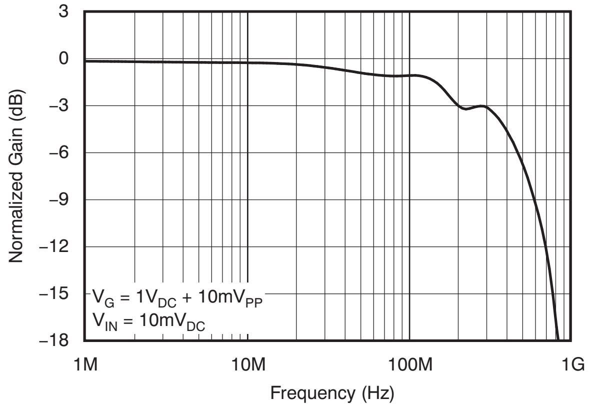

Figure 66. Gain Control Frequency Response

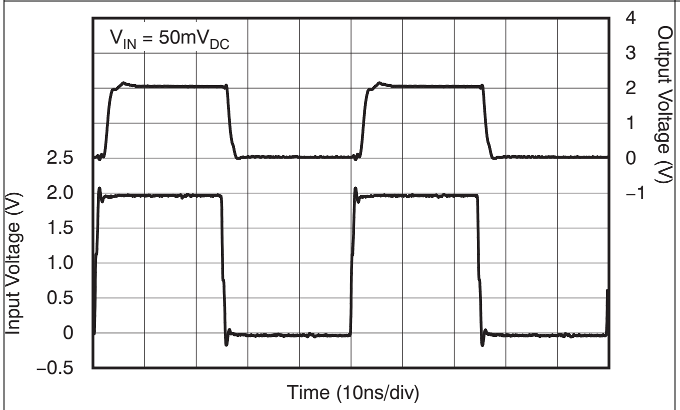

Figure 67. Gain Control Pulse Response

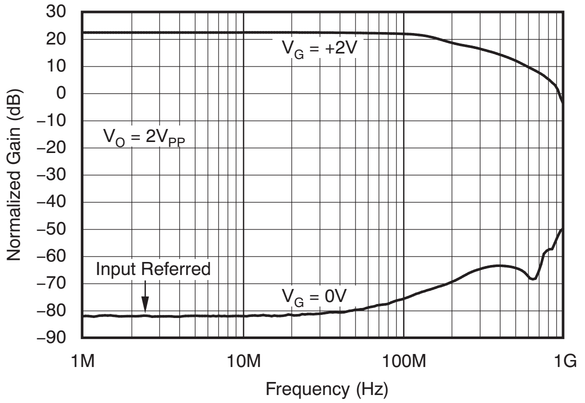

Figure 68. Fully Attenuated Response

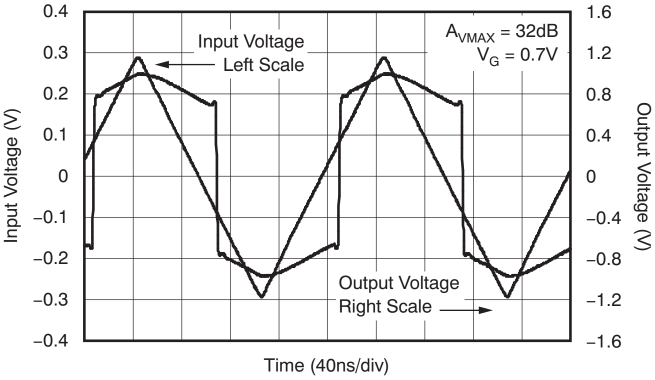

Figure 69. I_{RG} Limited Overdrive Recovery

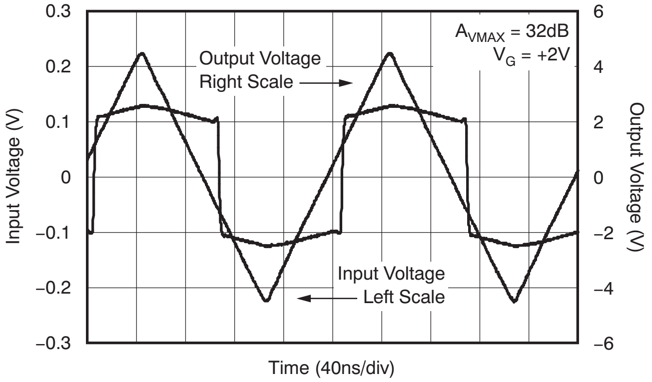

Figure 70. Output Limited Overdrive Recovery

Typical Characteristics: $V_S = \pm 5$ V, $A_{VMAX} = 32$ dB (continued)

At T_A = +25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 18 Ω, V_G = +2 V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SOIC package, unless otherwise noted.

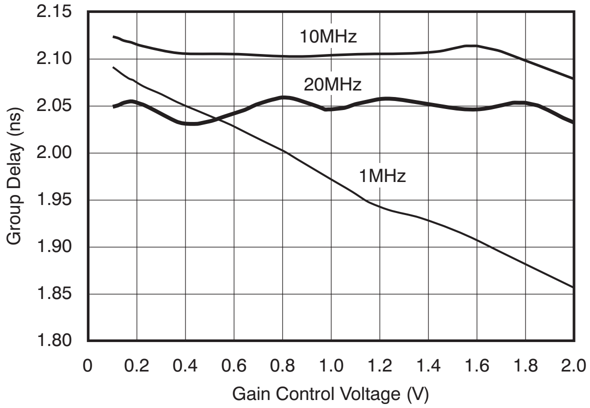

Figure 71. Group Delay vs Gain Control Voltage

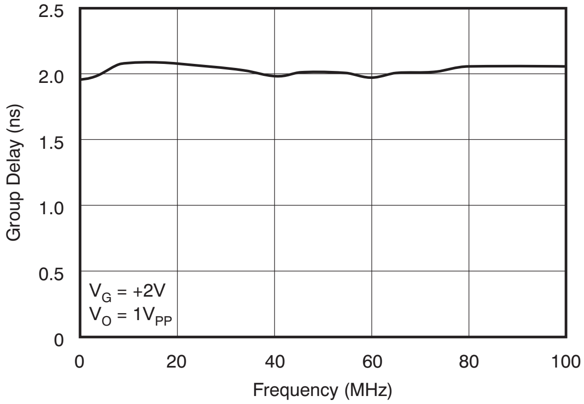

Figure 72. Group Delay vs Frequency

8 Parameter Measurement Information

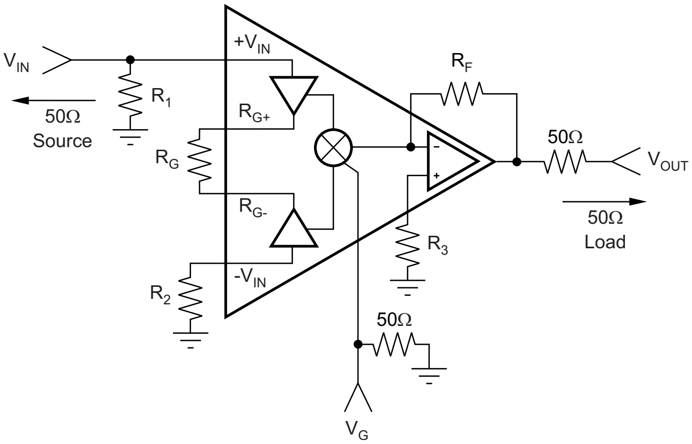

Figure 73. Test Circuit

9 Detailed Description

9.1 Overview

The VCA821 is a voltage controlled variable gain amplifier with differential inputs and a single ended output. The maximum gain is set by external resistors while the gain range is controlled by an external analog voltage. The maximum gain is designed for gains of 2 V/V up to 100 V/V and the analog control allows a gain range of over 40 dB. The VCA821 Input consists of two buffers which, together create a fully symmetrical, high impedance differential input with a typical common mode rejection of 80 dB. The gain set resistor is connected between the two input buffer output pins, so that the input impedance is independent of the gain settings. The bipolar inputs have a input voltage range of +1.6 V and –2.1 V on ±5 V supplies. The amplifier maximum gain is set by external resistors, but the internal gain control circuit is controlled by a continuously variable, analog voltage. The gain control is a multiplier stage which is linear in dB. The gain control input pin operates over a voltage range of 0 V to 2 V. The VCA821 contains a high speed, high current output buffer. The output stage can typically swing ±3.9 V and source/sink ±90 mA. The VCA821 can be operated over a voltage range of ±3.5 V to ±6 V.

9.2 Feature Description

The VCA821 can be operated with both single ended or differential input signals. The inputs present consistently high impedance across all gain configurations. By using an analog control signal the amplifier gain is continuously variable for smooth, glitch free gain changes. With a large signal bandwidth of 320 MHz and a slew rate of 2500 V/us the VCA821 offers linear performance over a wide range of signal amplitudes and gain settings. The low impedance/high current output buffer can drive loads ranging from low impedance transmission lines to high-impedance, switched-capacitor analog to digital converters. By using closely matched internal components the VCA821 offers gain accuracy of ±0.3 dB.

9.3 Device Functional Modes

The VCA821 functions as a differential input, single-ended output variable gain amplifier. This functional mode is enabled by applying power to the amplifier supply pins and is disabled by turning the power off.

The gain is continuously variable through the analog gain control input. While the gain range is fixed the maximum gain is set by two external components, Rf and Rg as shown in the *Figure 73*. The maximum gain is equal to 2x (Rf / Rg). This gain is achieved with a 2-V voltage on the gain adjust pin VG. As the voltage decreases on the VG pin, the gain decreases in a linear in dB fashion with over 40 dB of gain range from 2-V to 0-V control voltage.

As with most other differential input amplifiers, inputs can be applied to either one or both of the amplifier inputs. The amplifier gain is controlled through the gain control pin.

Device Functional Modes (continued)

9.3.1 Maximum Gain of Operation

This section describes the use of the VCA821 device in a fixed-gain application in which the V_G control pin is set at V_G = +1 V. The tradeoffs described here are with bandwidth, gain, and output voltage range.

In the case of an application that does not make use of the V_{GAIN} but requires some other characteristic of the VCA821 device, the R_G resistor must be set so that the maximum current flowing through the resistance I_{RG} is less than ±2.6 mA typical, or 5.2 mA_{PP} as defined in the *Electrical Characteristics* table and must follow Equation 1.

$$I_{RG} = \frac{V_{OUT}}{A_{VMAX} \times R_G} \tag{1}$$

As Equation 1 illustrates, when the output dynamic range and maximum gain are defined, the gain resistor is set. This gain setting in turn affects the bandwidth because to achieve the gain (and with a set gain element), the feedback element of the output stage amplifier is set as well. Keeping in mind that the output amplifier of the VCA821 device is a current-feedback amplifier, the larger the feedback element, the lower the bandwidth because the feedback resistor is the compensation element.

Limiting the discussion to the input voltage only and ignoring the output voltage and gain, Figure 1 illustrates the tradeoff between the input voltage and the current flowing through the gain resistor.

9.3.2 Output Current and Voltage

The VCA821 device provides output voltage and current capabilities that are unsurpassed in a low-cost monolithic VCA. Under no-load conditions at +25°C, the output voltage typically swings closer than 1 V to either supply rails; the +25°C swing limit is within 1.2 V of either rails. Into a 15-Ω load (the minimum tested load), it is tested to deliver more than ±90 mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or *V-I product*, that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot (Figure 47) in the *Typical Characteristics: V_S = ±5 V, A_{VMAX} = 20 dB*. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the VCA821 device output drive capabilities, noting that the graph is bounded by a *aafe operating area* of 1-W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the VCA821 device can drive ±2.5 V into 25 Ω or ±3.5 V into 50 Ω without exceeding the output capabilities or the 1-W dissipation limit. A 100-Ω load line (the standard test circuit load) shows the full ±3.9-V output swing capability, as shown in the *Typical Characteristics*.

The minimum specified output voltage and current over-temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup do the output current and voltage decrease to the numbers shown in the *Electrical Characteristics* table. As the output transistors deliver power, the respective junction temperatures increase, thereby increasing the available output voltage swing and output current.

In steady-state operation, the available output voltage and current are always greater than the temperature shown in the over-temperature specifications because the output stage junction temperatures are higher than the specified operating ambient.

9.3.3 Input Voltage Dynamic Range

The VCA821 device has a input dynamic range limited to +1.6 V and –2.1 V. Increasing the input voltage dynamic range can be done by using an attenuator network on the input. If the VCA821 device is trying to regulate the amplitude at the output, such as in an AGC application, the input voltage dynamic range is directly proportional to Equation 2.

$$V_{IN(PP)} = R_G \times I_{RG(PP)} \tag{2}$$

As such, for unity-gain or under-attenuated conditions, the input voltage must be limited to the CMIR of ±1.6 V ($3.2V_{PP}$) and the current (I_{RQ}) must flow through the gain resistor, ±2.6 mA ($5.2mA_{PP}$). This configuration sets a minimum value for R_E such that the gain resistor must be greater than Equation 3.

Device Functional Modes (continued)

$$R_{GMIN} = \frac{3.2V_{PP}}{5.2mA_{PP}} = 615.4\Omega \quad (3)$$

Values lower than 615.4 Ω are gain elements that result in reduced input range, as the dynamic input range is limited by the current flowing through the gain resistor R_G (I_{RG}). If the I_{RG} current limits the performance of the circuit, the input stage of the VCA821 device goes into overdrive, resulting in limited output voltage range. Such I_{RG}-limited overdrive conditions are shown in Figure 49 for the gain of 20 dB and Figure 69 for the 32-dB gain.

9.3.4 Output Voltage Dynamic Range

With its large output current capability and its wide output voltage swing of ±3.9-V typical on 100-Ω load, it is easy to forget other types of limitations that the VCA821 device can encounter. For these limitations, careful analysis must be done to avoid input stage limitation: either voltage or I_{RG} current.

NOTE

If control pin V_G varies, the gain limitation may affect other aspects of the circuit.

9.3.5 Bandwidth

The output stage of the VCA821 device is a wideband current-feedback amplifier. As such, the feedback resistance is the compensation of the last stage. Reducing the feedback element and maintaining the gain constant limits the useful range of I_{RG}, and therefore, reduces the gain adjust range. For a given gain, reducing the gain element limits the maximum achievable output voltage swing.

9.3.6 Offset Adjustment

As a result of the internal architecture used on the VCA821 device, the output offset voltage originates from the output stage and from the input stage and multiplier core. Figure 74 shows how to compensate both sources of the output offset voltage. Use this procedure to compensate the output offset voltage: starting with the output stage compensation, set V_G = –1 V to eliminate all offset contribution of the input stage and multiplier core. Adjust the output stage offset compensation potentiometer. Finally, set V_G = +1 V to the maximum gain and adjust the input stage and multiplier core potentiometer. This procedure effectively eliminates all offset contribution at the maximum gain. Because adjusting the gain modifies the contribution of the input stage and the multiplier core, some residual output offset voltage remains.

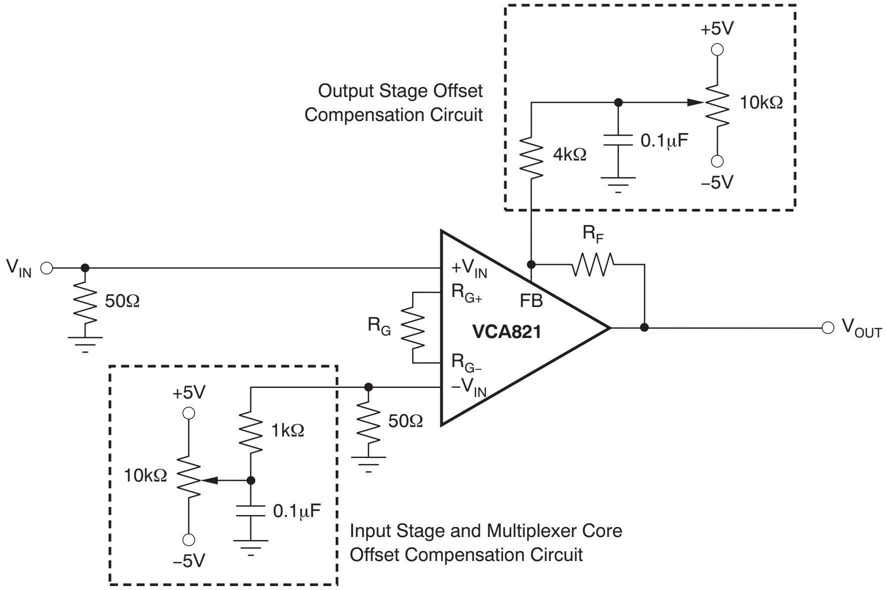

Figure 74. Adjusting the Input and Output Voltage Sources

Device Functional Modes (continued)

9.3.7 Noise

The VCA821 device offers 6 nV/√Hz input-referred voltage noise density at a gain of 20 dB and 2.6 pA/√Hz input-referred current noise density. The input-referred voltage noise density considers that all noise terms (except the input current noise but including the thermal noise of both the feedback resistor and the gain resistor) are expressed as one term.

This model is formulated in Equation 4 and Figure 88.

$$e_O = A_{VMAX} \times \sqrt{2 \times (R_S \times i_n)^2 + e_n^2 + 2 \times 4kTR_S} \qquad (4)$$

A more complete model is shown in Figure 89. For additional information on this model and the actual modeled noise terms, please contact the High-Speed Product Application Support team at www.ti.com.

9.3.7.1 Input and ESD Protection

The VCA821 device is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table.

All pins on the VCA821 device are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply, as shown in Figure 75. These diodes begin to conduct when the pin voltage exceeds either power supply by about 0.7 V. This situation can occur with loss of the amplifier power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30 mA without destruction. To ensure long-term reliability, however, diode current should be externally limited to 10 mA whenever possible.

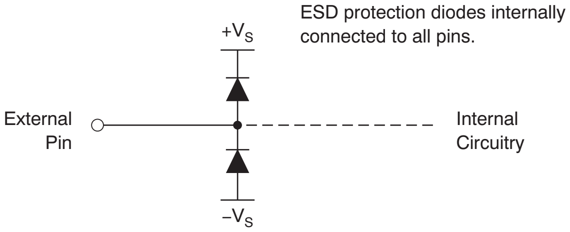

Figure 75. Internal ESD Protection

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The VCA821 has flexible maximum gain which is set by the Rf and Rg resistors shown in *Figure 73*. The maximum gain is equal to 2x (Rf / Rg). This gain is achieved with a 2-V voltage on the gain adjust pin VG. As the voltage decreases on the VG pin, the gain decreases in a linear in dB fashion with over 40 dB of gain range from 2-V to 0-V control voltage.

10.1.1 Design-In Tools

10.1.1.1 Demonstration Boards

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the VCA821 device in the two package options. Both of these are offered free of charge as unpopulated PCBs that are delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. EVM Ordering Information

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE NUMBER
VCA821ID	SOIC-14	DEM-VCA-SO-1B	SBOU050
VCA821IDGS	VSSOP-10	DEM-VCA-VSSOP-1A	SBOU051

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the VCA821 device product folder.

10.1.1.2 Macromodels and Applications Support

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This principle is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role in circuit performance. A SPICE model for the VCA821 device is available through the TI web page. The applications group is also available for design assistance. The models available from TI predict typical small-signal ac performance, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the relevant product data sheet.

10.1.1.3 Operating Suggestions

Operating the VCA821 optimally for a specific application requires trade-offs between bandwidth, input dynamic range and the maximum input voltage, the maximum gain of operation and gain, output dynamic range and the maximum input voltage, the package used, loading, and layout and bypass recommendations. The *Typical Characteristics* have been defined to cover as much ground as possible to describe the VCA821 operation. There are four sections in the *Typical Characteristics*:

- V_S = ±5 V *DC Parameters* and V_S = ±5V *DC and Power-Supply Parameters*, which include DC operation and the intrinsic limitation of a VCA821 device design
- V_S = ±5 V, A_{VMAX} = 6 dB *Gain of 6dB Operation*
- V_S = ±5 V, A_{VMAX} = 20 dB *Gain of 20dB Operation*
- V_S = ±5 V, A_{VMAX} = 32 dB *Gain of 32dB Operation*

Where the Typical Characteristics describe the actual performance that can be achieved by using the amplifier properly, the following sections describe in detail the trade-offs needed to achieve this level of performance.

Application Information (continued)

10.1.1.4 Package Considerations

The VCA821 device is available in both SOIC-14 and VSSOP-10 packages. Each package has, for the different gains used in the typical characteristics, different values of R_F and R_G in order to achieve the same performance detailed in the *Electrical Characteristics* table.

Figure 76 shows a test gain circuit for the VCA821 device. Table 2 lists the recommended configuration for the SOIC-14 and VSSOP-10 packages.

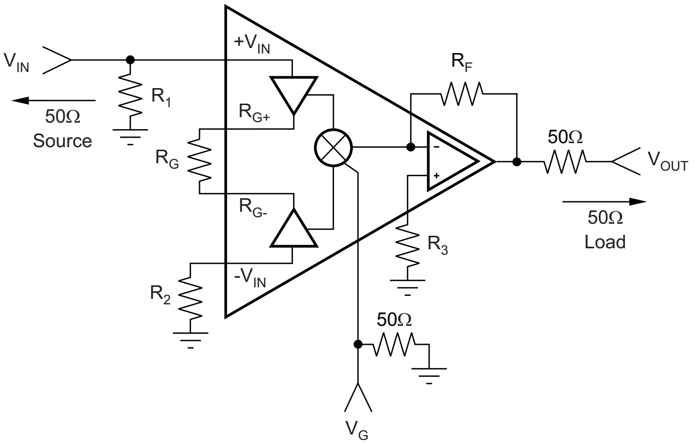

Figure 76. Test Circuit

Table 2. SOIC-14 and VSSOP-10 R_F and R_G Configurations

	G = 2	G = 10	G = 40
R_F	453 Ω	402 Ω	402 Ω
R_G	453 Ω	80 Ω	18 Ω

There are no differences between the packages in the recommended values for the gain and feedback resistors. However, the bandwidth for the VCA821IDGS (VSSOP-10 package) is lower than the bandwidth for the VCA821ID (SOIC-14 package). This difference is true for all gains, but especially true for gains greater than 5 V/V, as can be seen in Figure 77 and Figure 78.

NOTE

The scale must be changed to a linear scale to view the details.

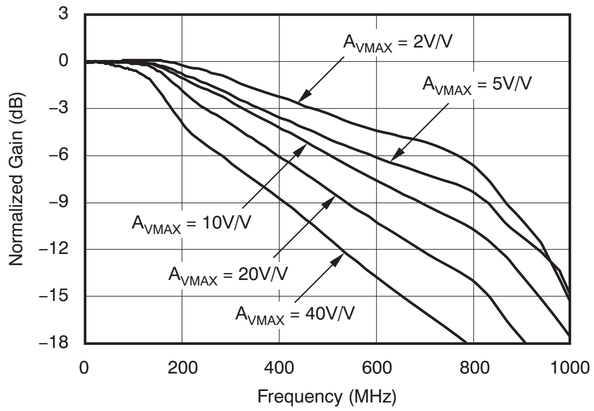

Figure 77. SOIC-14 Recommended R_F and R_G vs A_{VMAX}

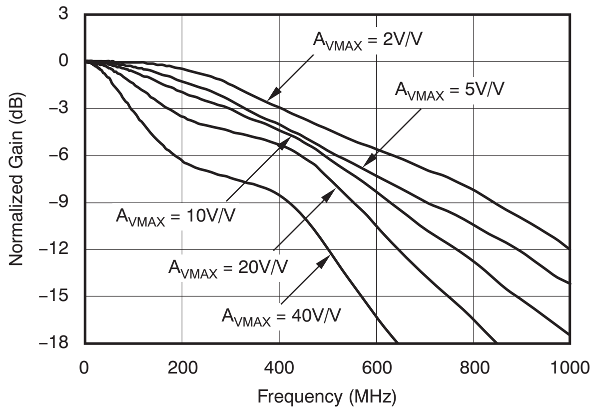

Figure 78. VSSOP-10 Recommended R_F and R_G vs A_{VMAX}

10.2 Typical Applications

10.2.1 Wideband Variable-Gain Amplifier Operation Application

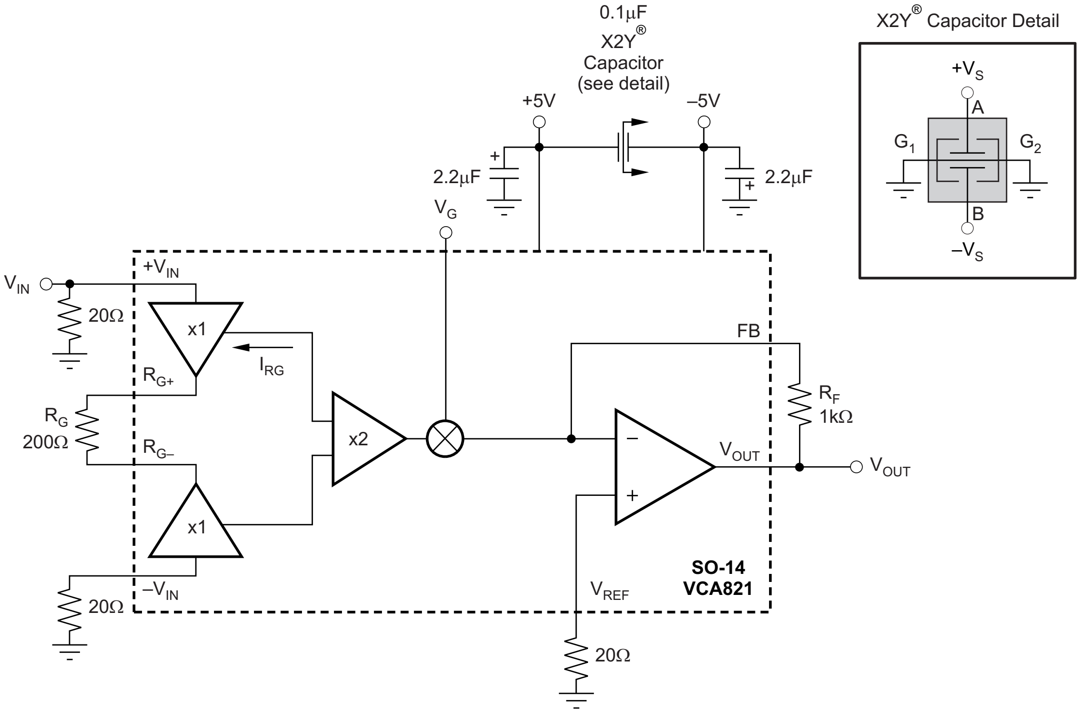

Figure 79. DC-Coupled, A_{VMAX} = 20 dB, Bipolar Supply Specification and Test Circuit

10.2.1.1 Design Requirements

The design shown in Figure 79 requires a single-ended input, continuously variable gain control and a single-ended output. This configuration is used to achieve the best performance with a bipolar supply. This circuit also requires a maximum gain of 10 V/V and low noise.

10.2.1.2 Detailed Design Procedure

The VCA821 device provides an exceptional combination of high output power capability with a wideband, greater than 40-dB gain adjust range, linear in dB variable gain amplifier. The VCA821 device input stage places the transconductance element between two input buffers, using the output currents as the forward signal. As the differential input voltage rises, a signal current is generated through the gain element. This current is then mirrored and gained by a factor of two before reaching the multiplier. The other input of the multiplier is the voltage gain control pin, V_G. Depending on the voltage present on V_G, up to two times the gain current is provided to the transimpedance output stage. The transimpedance output stage is a current-feedback amplifier providing high output current capability and high slew rate, 2500 V/µs. This exceptional full-power performance comes at the price of relatively high quiescent current (34 mA), but low input voltage noise for this type of architecture (6 nV/$\sqrt{\text{Hz}}$).

Figure 79 shows the DC-coupled, gain of +10 V/V, dual power-supply circuit used as the basis of the ±5-V *Electrical Characteristics* and *Typical Characteristics*. For test purposes, the input impedance is set to 50 Ω with a resistor to ground and the output impedance is set to 50 Ω with a series output resistor. Voltage swings reported in the *Electrical Characteristics* table are taken directly at the input and output pins, while output power (dBm) is at the matched 50-Ω load. For the circuit in Figure 79, the total effective load is 100 Ω ∥ 1 kΩ.

Typical Applications (continued)

NOTE

For the SOIC-14 package, there is a voltage reference pin, V_{REF} (pin 9). For the SOIC-14 package, this pin must be connected to ground through a 20-Ω resistor in order to avoid possible oscillations of the output stage. In the VSSOP-10 package, this pin is internally connected and does not require such precaution.

An X2Y® capacitor has been used for power-supply bypassing. The combination of low inductance, high resonance frequency, and integration of three capacitors in one package (two capacitors to ground and one across the supplies) enables the VCA821 device to achieve the low second-harmonic distortion reported in the *Electrical Characteristics* table. More information on how the VCA821 device operates can be found in the *Operating Suggestions* section.

10.2.1.3 Application Curve

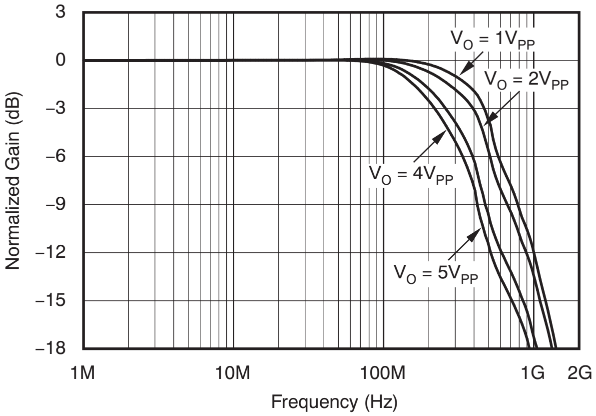

Figure 80. Large-Signal Frequency Response

10.2.2 Difference Amplifier Application

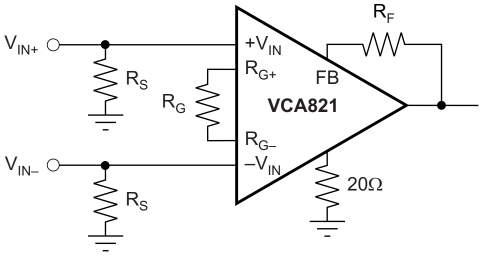

Figure 81. Difference Amplifier

10.2.2.1 Design Requirements

For a difference amplifier, the design requirements are differential voltage gain, common mode rejection, and load drive capability. This circuit delivers differential gain of 2* (Rf/Rg), and CMRR as shown in Figure 82.

10.2.2.2 Detailed Design Procedure

Because both inputs of the VCA821 device are high-impedance, a difference amplifier can be implemented without any major problem. Figure 81 shows this implementation. This circuit provides excellent common-mode rejection ratio (CMRR) as long as the input is within the CMRR range of –2.1 V to +1.6 V.

Typical Applications (continued)

NOTE

This circuit does not make use of the gain control pin, V_G. Also, it is recommended to choose R_S such that the pole formed by R_S and the parasitic input capacitance does not limit the bandwidth of the circuit.

Figure 82 shows the common-mode rejection ratio for this circuit implemented in a gain of 20 dB for V_G = +2 V.

NOTE

Because the gain control voltage is fixed and is normally set to +2 V, the feedback element can be reduced to increase the bandwidth. When reducing the feedback element, make sure that the VCA821 device is not limited by common-mode input voltage, the current flowing through R_G, or any other limitation described in this data sheet.

10.2.2.3 Application Curve

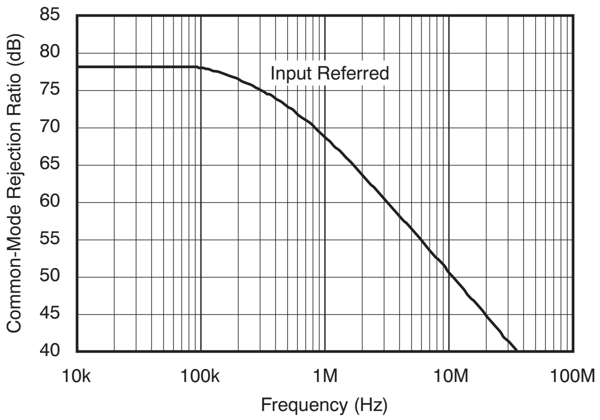

Figure 82. Common-Mode Rejection Ratio

10.2.3 Differential Equalizer Application

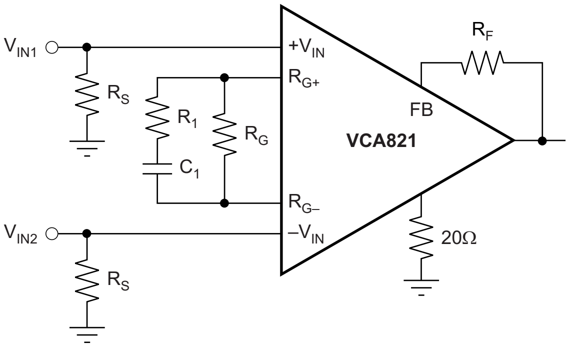

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Figure 83. Differential Equalizer

10.2.3.1 Design Requirements

Signals that travel over a length of cable experience an attenuation that is proportional to the square root of the frequency. For this reason, a fixed bandwidth amplifier will not restore the original signal. To replicate the original signal, the higher frequency signal components require more gain. The circuit in Figure 83 has one stage of frequency shaping to help restore a signal transmitted along a cable. If needed, additional frequency shaping stages can be added as shown in Figure 84.

Typical Applications (continued)

10.2.3.2 Detailed Design Procedure

If the application requires frequency shaping (the transition from one gain to another), the VCA821 device can be used advantageously because its architecture allows the application to isolate the input from the gain setting elements. Figure 83 shows an implementation of such a configuration. The transfer function is shown in Equation 5.

This transfer function has one pole, P_1 (located at R_GC_1), and one zero, Z_1 (located at R_1C_1). When equalizing an RC load, R_L and C_L, compensate the pole added by the load located at R_LC_L with the zero Z_1. Knowing R_L, C_L, and R_G allows the user to select C_1 as a first step and then calculate R_1. Using R_L = 75 Ω, C_L = 100 pF and wanting the VCA821 device to operate at a gain of +2 V/V (which gives $R_F = R_G$ = 453 Ω) allows the user to select C_1 = 15.5 pF to ensure a positive value for the resistor R_1. With all these values known, to achieve greater than 300-MHz bandwidth, R_1 can be calculated to be 20 Ω. Figure 84 shows the frequency response for both the initial, unequalized frequency response and the resulting equalized frequency response.

$$G = 2 \times \frac{R_F}{R_G} \times \frac{1 + sR_GC_1}{1 + sR_1C_1} \tag{5}$$

10.2.3.3 Application Curve

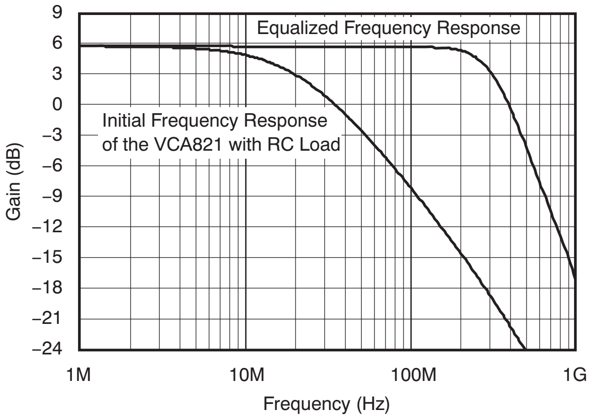


Figure 84. Differential Equalization of an RC Load

10.2.4 Differential Cable Equalizer Application

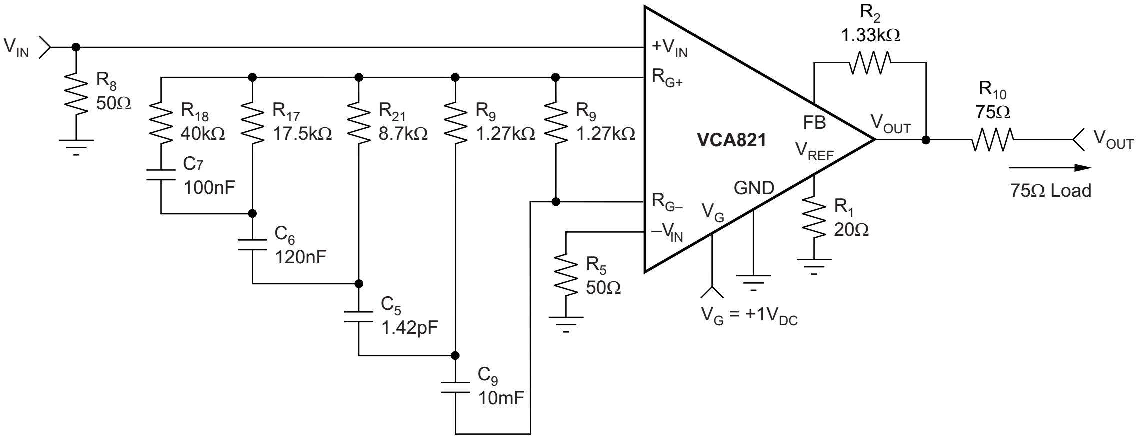


Figure 85. Differential Cable Equalizer

Typical Applications (continued)

10.2.4.1 Design Requirements

Signals that travel over a length of cable experience an attenuation that is proportional to the square root of the frequency. For this reason, a fixed bandwidth amplifier will not restore the original signal. To replicate the original signal, the higher frequency signal components require more gain. The circuit in Figure 85 has multiple stages of frequency shaping to help restore a signal transmitted along a cable. This circuit is similar to the one shown in Figure 83, but is much more accurate in replicating the 1/(sqrt(f)) frequency response shape.

10.2.4.2 Detailed Design Procedure

A differential cable equalizer can easily be implemented using the VCA821 device. An example of a cable equalization for 100 feet of Belden cable 1694F is illustrated in Figure 84, with Figure 86 showing the result for this implementation. This implementation has a maximum error of 0.2 dB from DC to 70 MHz.

NOTE

This implementation shows the cable attenuation side-by-side with the equalization in the same plot.

For a given frequency, the equalization function realized with the VCA821 device matches the cable attenuation. The circuit in Figure 85 is a driver circuit. To implement a receiver circuit, the signal is received differentially between the $+V_{IN}$ and $–V_{IN}$ inputs.

10.2.4.3 Application Curve

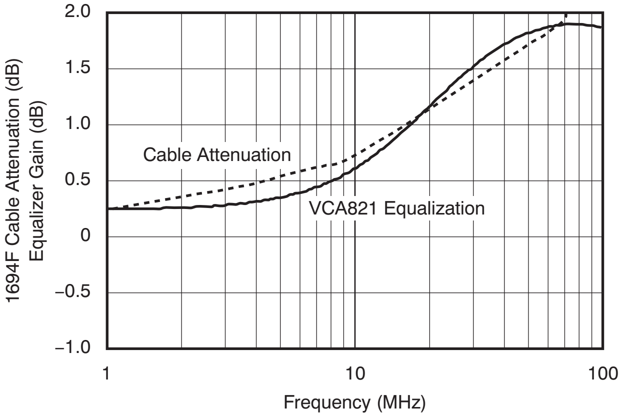


Figure 86. Cable Attenuation vs Equalizer Gain

Typical Applications (continued)

10.2.5 AGC Loop Application

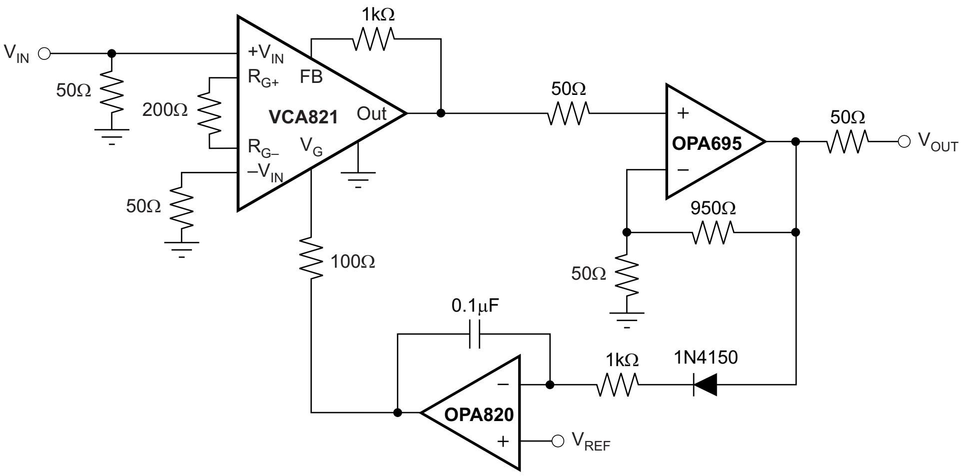


Figure 87. AGC Loop

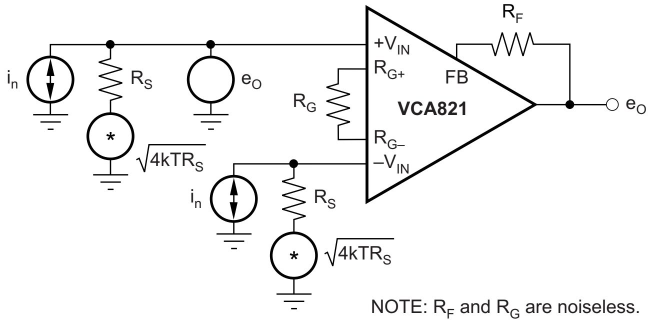
10.2.5.1 Design Requirements

When dynamic signal amplitude correction is required, an AGC loop will provide real-time gain control. The requirements for this circuit are fast gain control response and linear in dB gain control. The time constant of the loop is set with the 0.1-µF capacitor and the 1-kΩ resistor. The OPA695 provides additional load driving capability.

10.2.5.2 Detailed Design Procedure

In the typical AGC loop shown in Figure 87, the OPA695 device follows the VCA821 device to provide 40 dB of overall gain. The output of the OPA695 device is rectified and integrated by an OPA820 device to control the gain of the VCA821 device. When the output level exceeds the reference voltage (V_{REF}), the integrator ramps down reducing the gain of the AGC loop. Conversely, if the output is too small, the integrator ramps up increasing the net gain and the output voltage.

10.3 System Examples



NOTE: R_F and R_G are noiseless.

Figure 88. Simple Noise Model

System Examples (continued)

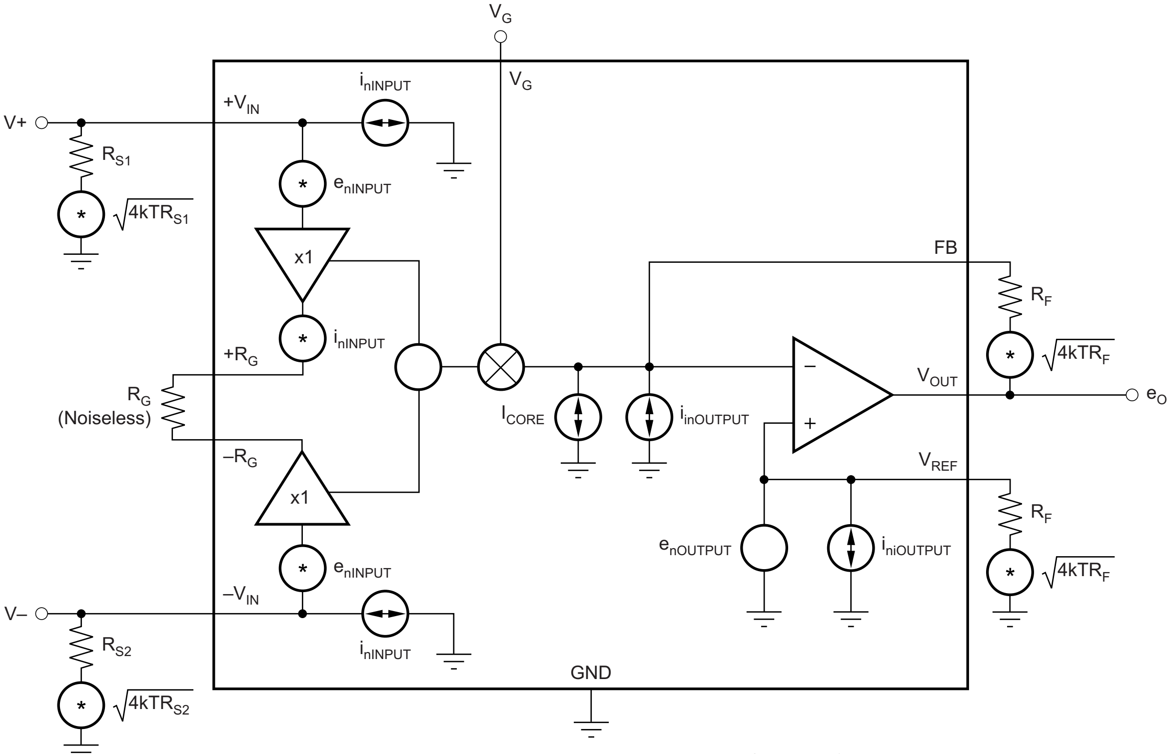


Figure 89. Full Noise Model

11 Power Supply Recommendations

High-speed amplifiers require low inductance power supply traces and low ESR bypass capacitors. The power supply voltage should be centered on the desired amplifier output voltage, so for ground referenced output signals, split supplies are required. The power supply voltage should be from 7 V to 12 V.

12 Layout

12.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the VCA821 device requires careful attention to printed circuit board (PCB) layout parasitics and external component types. Recommendations to optimize performance include the following:

1. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. This recommendation includes GND (pin 2). Parasitic capacitance on the output can cause instability on both the inverting input and the noninverting input, and it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins must be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. Place a small series resistance (greater than 25 Ω) with the input pin connected to ground to help decouple package parasitics.
2. **Minimize the distance** (less than 0.25 inches, or 6.3 mm) from the power-supply pins to high-frequency 0.1-μF decoupling capacitors. At the device pins, the ground and power plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger decoupling capacitors (2.2 μF to 6.8 μF), effective at lower frequencies, must also be used on the main supply pins. These capacitors can be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.
3. **Careful selection and placement** of external components preserves the high-frequency performance of the VCA821 device. Resistors must be a very low-reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Because the output pin is the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as inverting or noninverting input termination resistors, must also be placed close to the package.
4. **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils, or 1.27 mm to 2.54 mm) must be used, preferably with ground and power planes opened up around them.
5. **Socketing a high-speed part like the VCA821 device is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the VCA821 device onto the board.

12.2 Layout Example

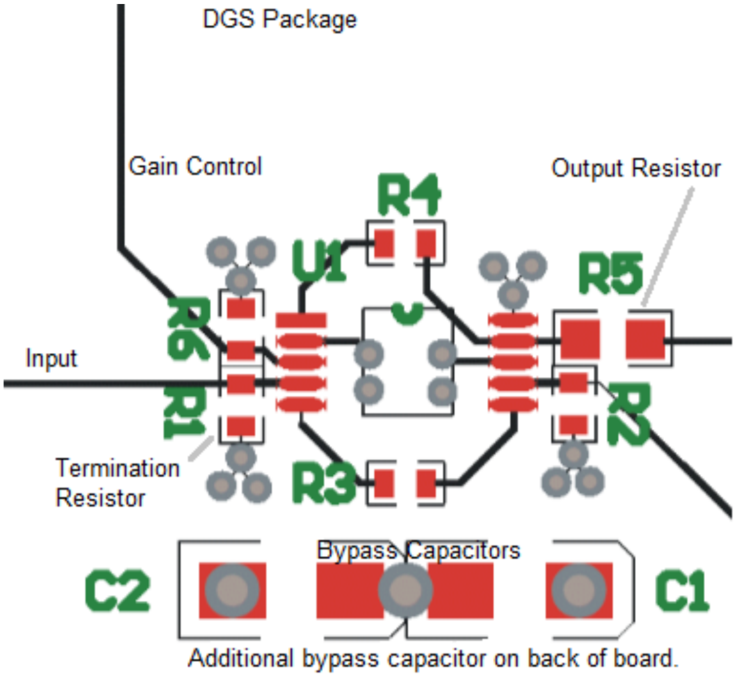


Figure 90. Layout Recommendations

12.3 Thermal Considerations

The VCA821 device does not require heat sinking or airflow in most applications. The maximum desired junction temperature sets the maximum allowed internal power dissipation as described in this section. The maximum junction temperature must not exceed 150°C.

Operating junction temperature (T_J) is given by Equation 6.

$$T_J = T_A + P_D \times \theta_{JA} \tag{6}$$

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load; however, it is at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S{}^2 / (4 \times R_L)$, where R_L is the resistive load.

NOTE

It is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using a VCA821ID (SOIC-14 package) in the circuit of Figure 79 operating at maximum gain and at the maximum specified ambient temperature of 85°C.

$$P_D = 10V(36mA) + 5^2/(4 \times 100\Omega) = 422.5mW \tag{7}$$

$$\text{Maximum } T_J = +85°C + (0.443W \times 80°C/W) = 120.5°C \tag{8}$$

This maximum operating junction temperature is well below most system level targets. Most applications must be lower because an absolute worst-case output stage power was assumed in this calculation of V_{CC} / 2, which is beyond the output voltage range for the VCA821 device.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
X2Y is a registered trademark of X2Y Attenuators LLC.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VCA821ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA821ID	Samples
VCA821IDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BOR	Samples
VCA821IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA821ID	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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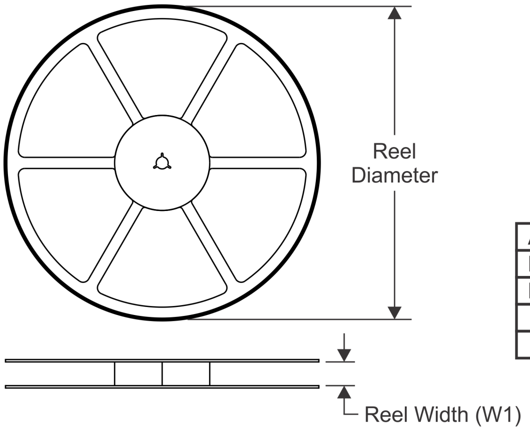
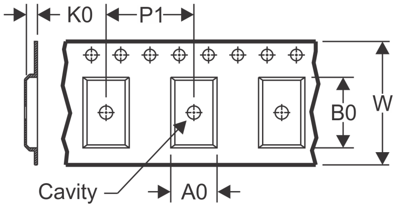
TAPE AND REEL INFORMATION

REEL DIMENSIONS

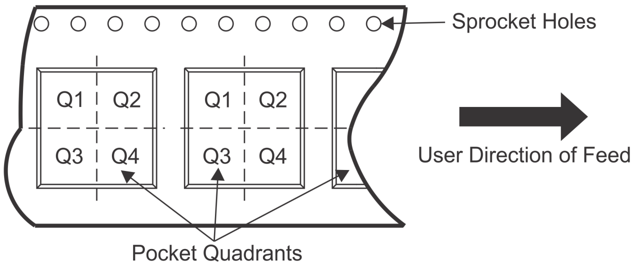


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

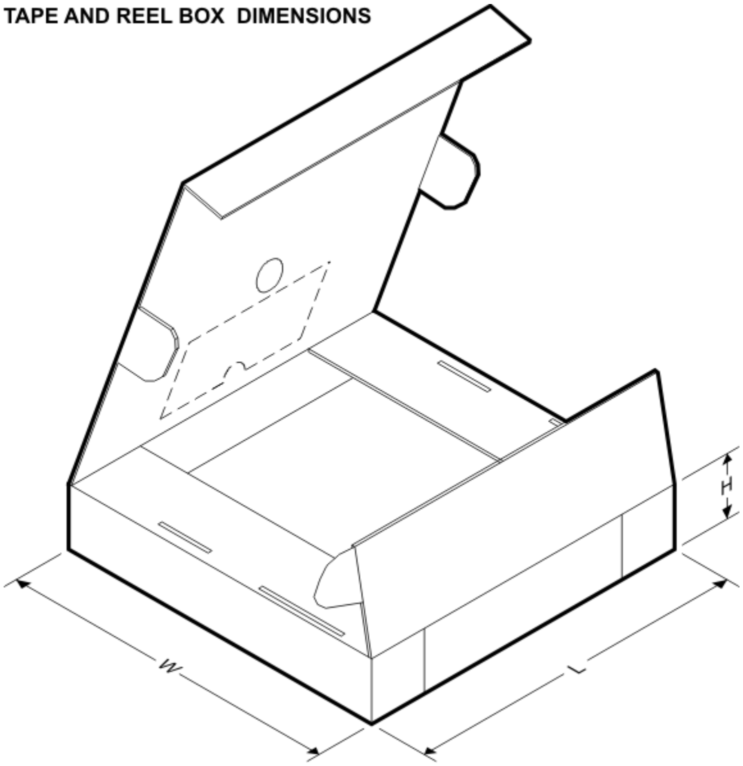
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VCA821IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
VCA821IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

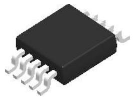
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VCA821IDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
VCA821IDR	SOIC	D	14	2500	367.0	367.0	38.0

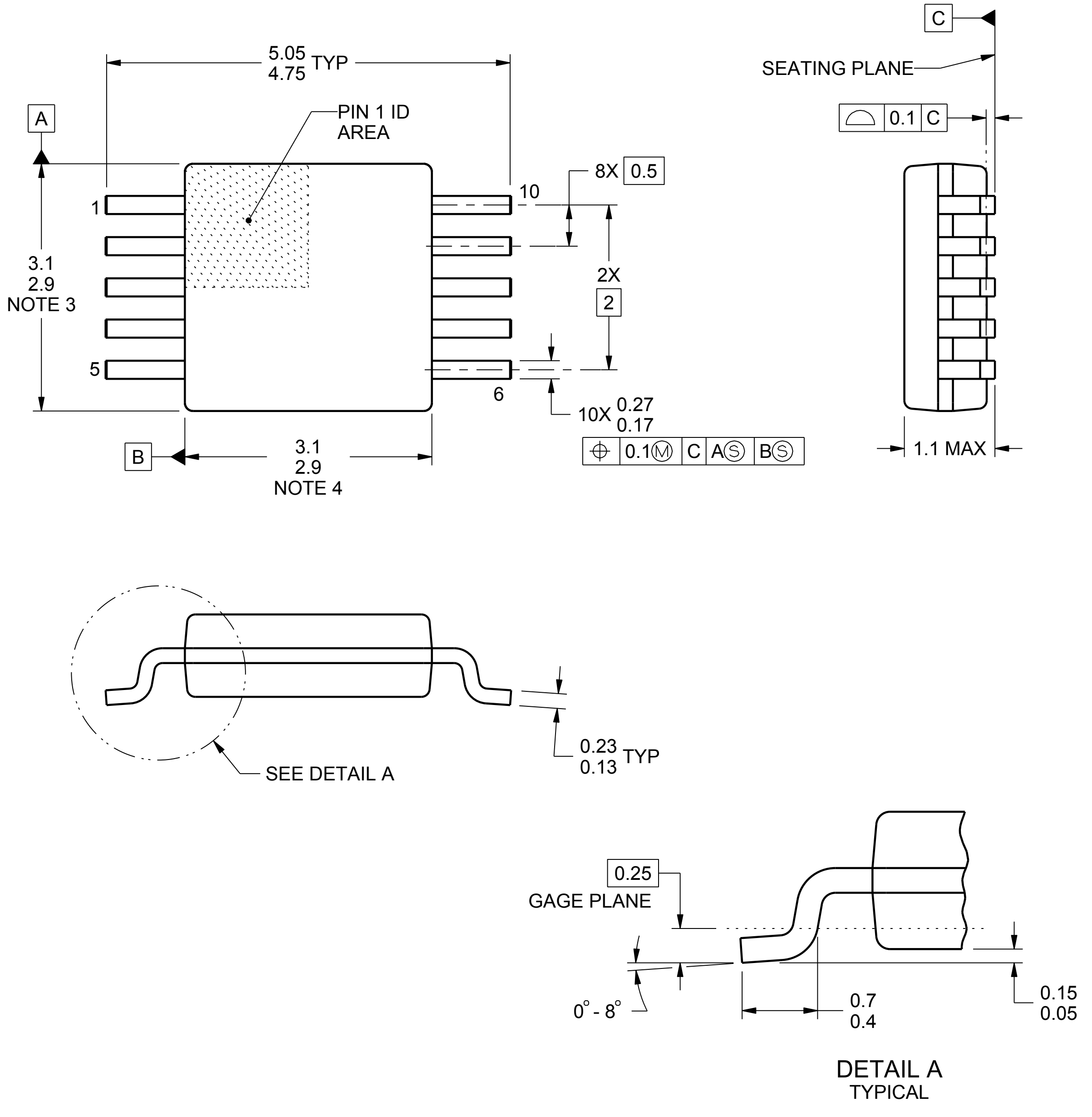
PACKAGE OUTLINE



DGS0010A

VSSOP - 1.1 mm max height

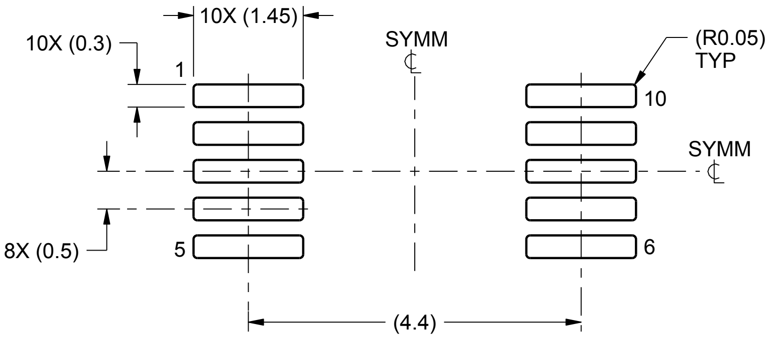
SMALL OUTLINE PACKAGE



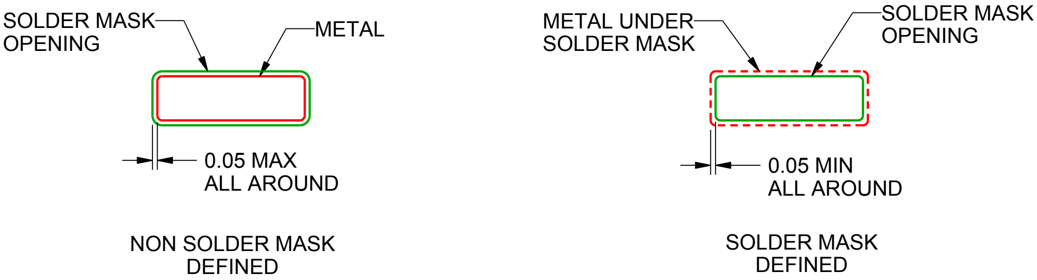
4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

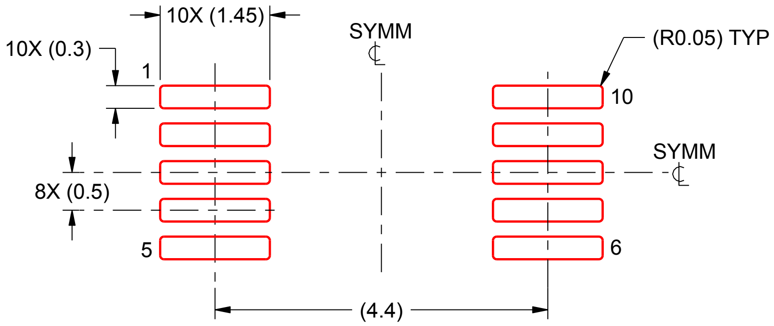


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

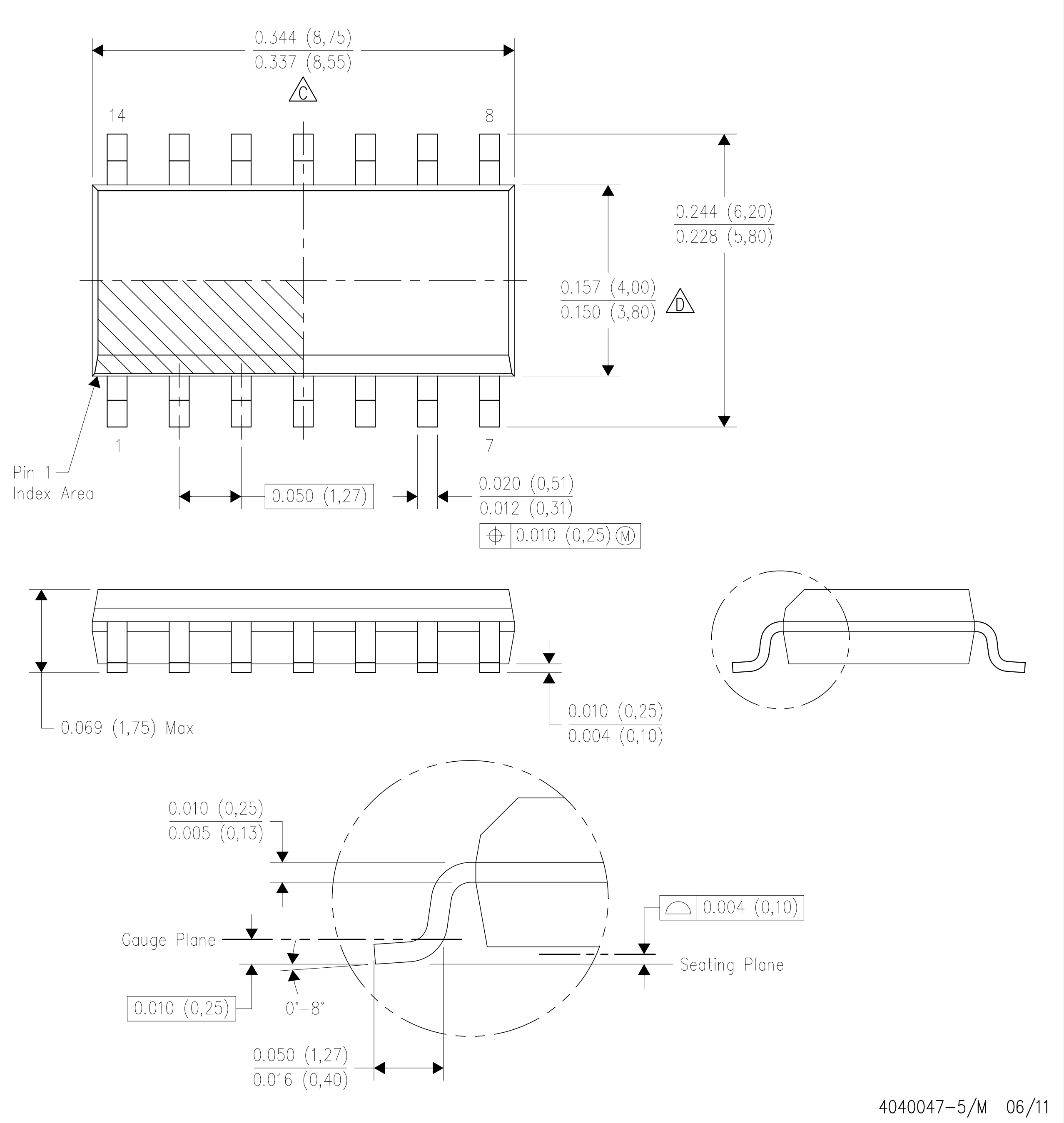


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

NOTES: (continued)

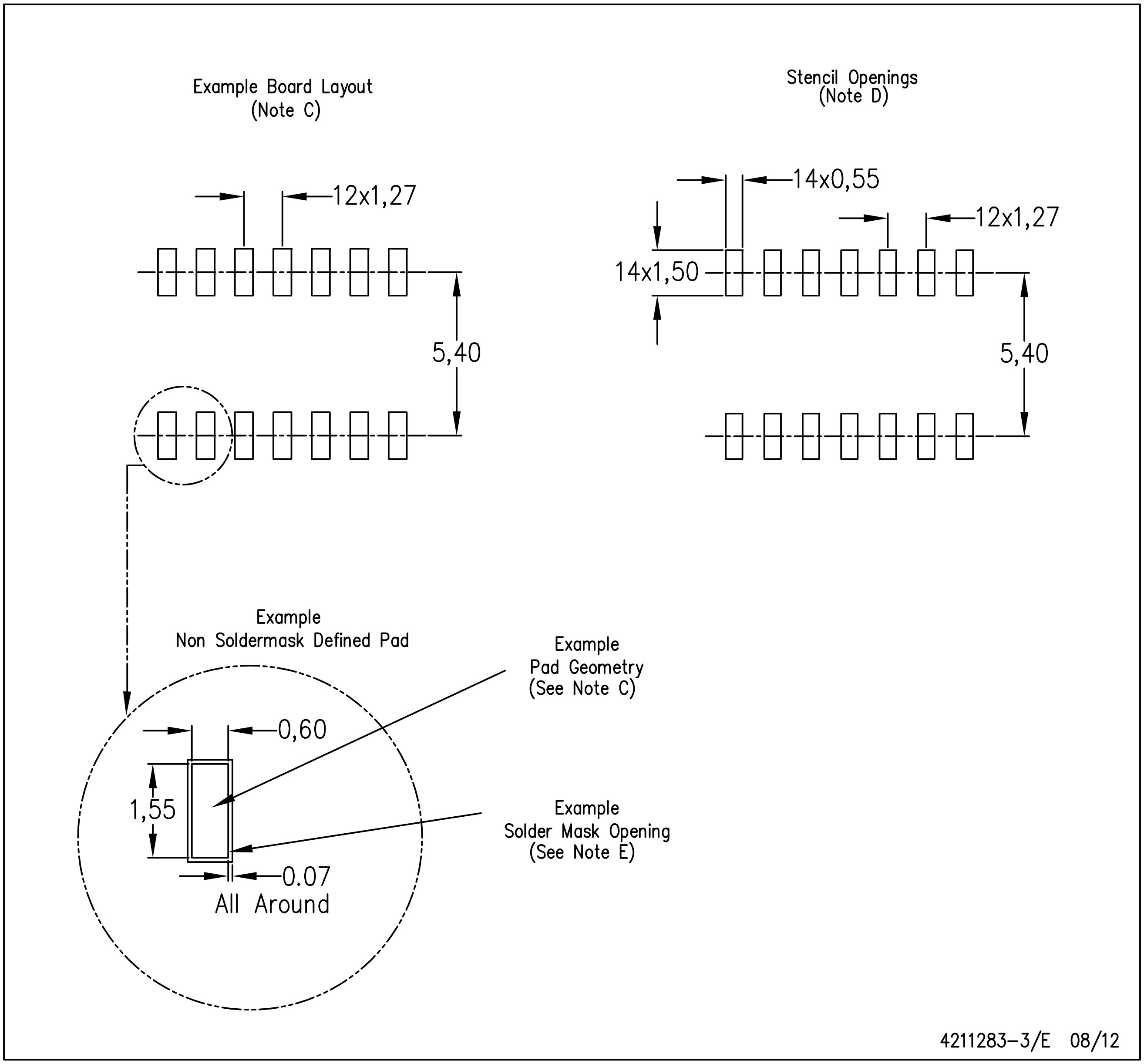
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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