Boost LED Driver with Low-side LED Wiring Fault Detection

Features

- Switch mode controller for boost LED driver
- High output current accuracy
- Constant frequency operation
- Hiccup mode protection for both short circuit and open circuit conditions
- LED wiring fault detection

Applications

- RGB or white LED backlighting

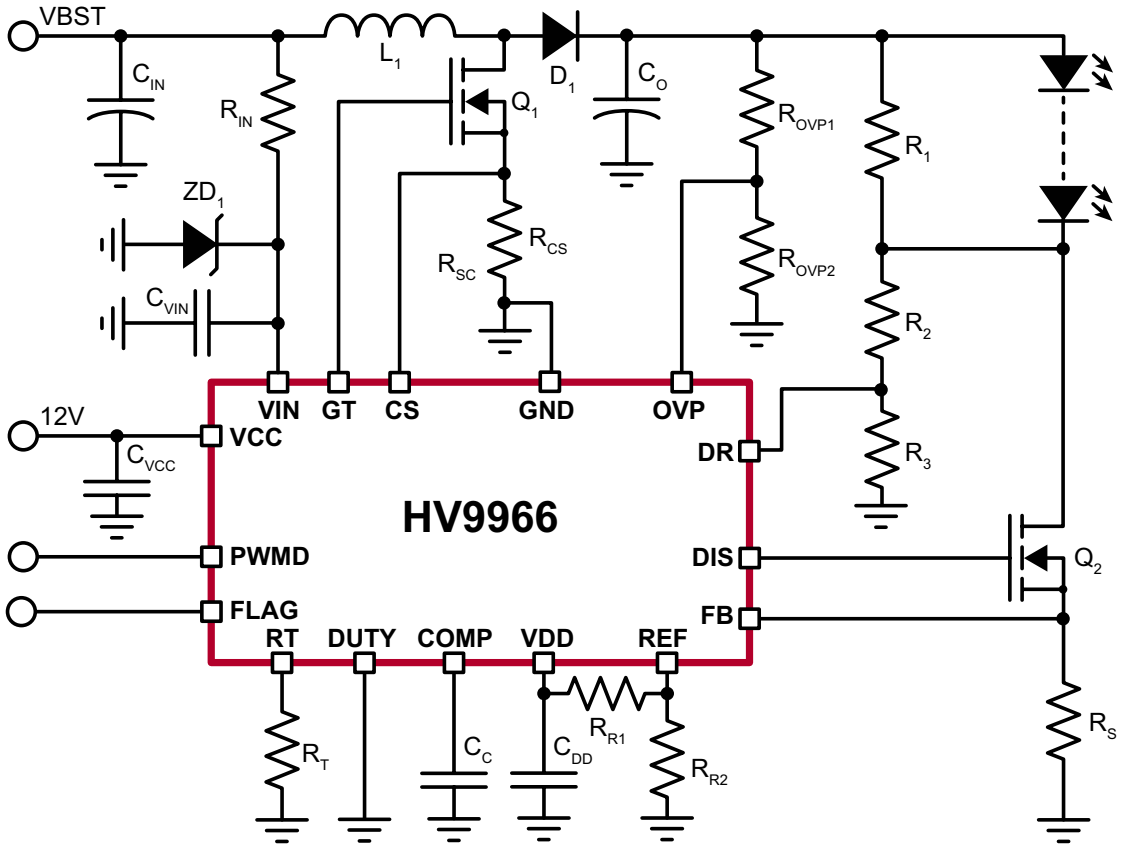
General Description

The HV9966 is a current mode control LED driver IC designed to control a boost LED driver in constant frequency mode. The controller uses a peak current-mode control scheme (with programmable slope compensation) and includes an internal transconductance amplifier to accurately control the output current over all line and load conditions. The IC also provides a disconnect switch gate drive output, which can be used to achieve good PWM rise and fall times for the LED current using an external disconnect FET.

The HV9966 also provides a TTL compatible, low-frequency PWM dimming input that can accept an external control signal with a duty ratio of 0-100% and a frequency of up to a few kilohertz.

The HV9966 includes LED wiring fault detection function which turns off the boost converter and sends a shutdown signal to the external power supply in case the cathode of the LED string (or any tap in the LED string) is shorted to ground. A dedicated power supply input keeps the wiring fault detection circuitry armed even in the absence of the V_{CC} supply.

Typical Boost Application Circuit



Ordering Information

Part Number	Package Option	Packing
HV9966NG-G	16-Lead SOIC (Narrow Body)	45/Tube
HV9966NG-G M934	16-Lead SOIC (Narrow Body)	2500/Reel

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

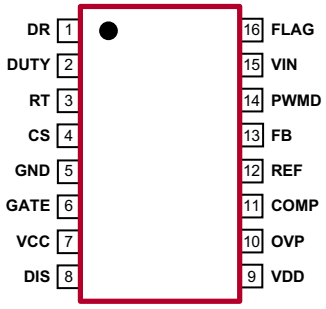
Parameter	Value
VDD to GND	-0.5V to +16V
GATE, DIS to GND	-0.3V to (V_{CC} +0.3V)
VDD to GND	-0.3V to +3.8V
VIN to GND	-0.3V to +3.8V
DR, RT, FLAG to GND	-0.3V to (V_{IN} +0.3V)
REF to GND	-0.3V to +1.5V
All other pins to GND	-0.3V to (V_{DD} +0.3V)
Junction temperature	+150°C
Storage ambient temperature range	-65°C to +150°C
Continuous power dissipation (T_A = +25°C)	1000mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Thermal Resistance

Package	θ_{j-a}
16-Lead SOIC	83°C/W

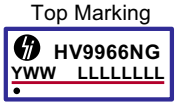
Pin Description



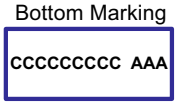
16-Lead SOIC (NG)
(top view)

Product Marking

Top Marking



Bottom Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging
**May be part of top marking*

Package may or may not include the following marks: Si or

16-Lead SOIC (NG)

Electrical Characteristics

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{CC} = 12V, C_{VCC} = 1.0µF, C_{DD} = 1.0µF, C_{GATE} = 1.0nF, C_{FLT} = 500pF, R_T = 374kΩ, DUTY = GND unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Unit	Conditions
Input							
V_{CCDC}	Input DC supply voltage range	-	10	12	14	V	DC input voltage
I_{CCSD}	Shut-down mode supply current	-	-	-	1.5	mA	PWMD to GND
$UVLO_{RISE,VCC}$	V_{CC} under-voltage lockout threshold	*	9.0	-	9.5	V	V_{CC} rising
$UVLO_{HYST,VCC}$	V_{CC} under-voltage hysteresis	-	-	1.0	-	V	V_{CC} falling
Internal Low Voltage Regulator							
V_{DD}	Internally regulated voltage	-	3.23	3.30	3.37	V	PWMD = V_{DD}; f_s = 300kHz; I_{VDD_EXT} = 0 -500µA
$UVLO_{RISE,VDD}$	V_{DD} under-voltage lockout threshold	*	3.03	3.10	3.17	V	V_{CC} rising
$UVLO_{HYST,VDD}$	V_{DD} under-voltage hysteresis	-	-	0.20	-	V	V_{CC} falling

Note:
 # Denotes specifications guaranteed by design

Electrical Characteristics *(cont.)*

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{CC} = 12V, C_{VCC} = 1.0µF, C_{DD} = 1.0µF, C_{GATE} = 1.0nF, C_{FLT} = 500pF, R_T = 374kΩ, DUTY = GND unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Unit	Conditions
PWM Dimming							
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	1.0	V	---
$V_{PWMD(hi)}$	PWMD input high voltage	*	2.0	-	-	V	---
R_{PWMD}	PWMD pull down resistor	-	50	100	100	kΩ	$V_{PWMD} = V_{DD}$
Boost FET Driver							
I_{SOURCE}	GATE short circuit current, sourcing	*	0.25	-	-	A	V_{GATE} = 0V
I_{SINK}	GATE sinking current	*	0.50	-	-	A	$V_{GATE} = V_{CC}$
T_{RISE}	GATE output rise time	-	-	-	70	ns	---
T_{FALL}	GATE output fall time	-	-	-	35	ns	---
Disconnect FET Driver							
$I_{SOURCE,DIS}$	GATE short circuit current, sourcing	*	0.02	-	-	A	V_{GATE} = 0V
$I_{SINK,DIS}$	GATE sinking current	*	0.04	-	-	A	$V_{GATE} = V_{CC}$
$T_{RISE,DIS}$	GATE output rise time	-	-	-	300	ns	---
$T_{FALL,DIS}$	GATE output fall time	-	-	-	150	ns	---
Oscillator							
f_{OSC1}	Oscillator frequency	-	88	100	112	kHz	R_T = 374kΩ
f_{OSC2}	Oscillator frequency	-	220	250	280	kHz	R_T = 249kΩ
F_{OSC}	Output frequency range	#	80	-	300	kHz	---
D_{MAX}	Maximum duty cycle at GATE output	*	87	-	93	%	DUTY = GND
		-	67	-	73	%	DUTY = V_{DD}
Current Sense							
T_{BLANK}	Leading edge blanking	*	100	-	250	ns	---
T_{PROP_DELAY1}	Delay to Gate falling	-	-	-	200	ns	COMP = V_{DD}; 50mV overdrive at CS
R_{DIV}	Internal resistor divider ratio – COMP to CS	#	-	0.167	-	-	---
V_{OFFSET}	Comparator offset voltage	#	-10	-	10	mV	---
$R_{PULLDOWN}$	Pull down FET resistance	*	-	-	100	Ω	---
Over Voltage Protection							
$V_{OVP,RISING}$	Over voltage rising trip point	*	1.94	2.00	2.06	V	OVP rising
$V_{OVP,HYST}$	Over voltage hysteresis	-	-	0.2	-	V	OVP falling
T_{PROP_DELAY}	Propagation delay time	-	-	-	200	ns	50mV overdrive

Note:

 # Denotes specifications guaranteed by design

Electrical Characteristics *(cont.)*

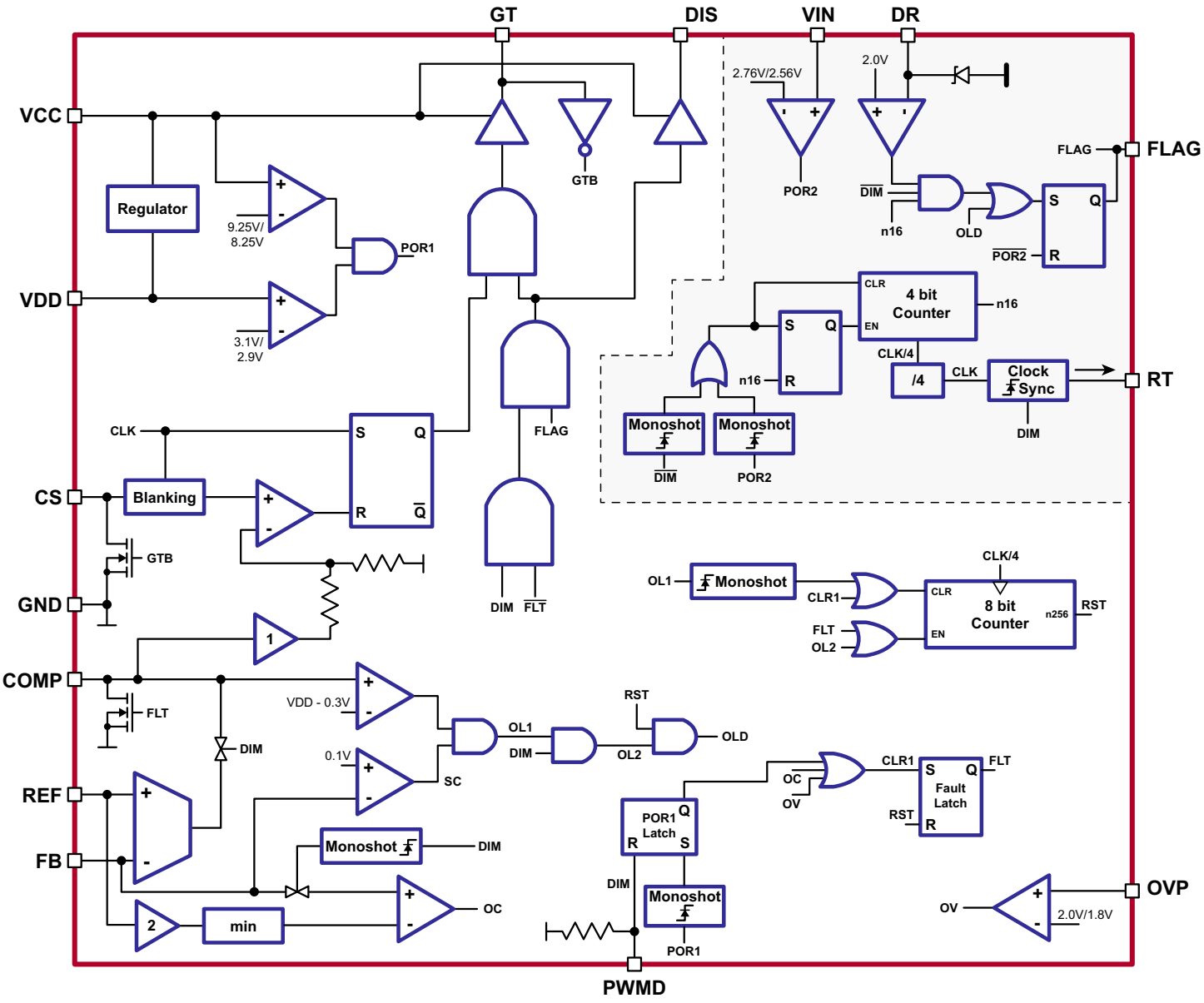
*((The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{CC} = 12V, C_{VCC} = 1.0µF, C_{DD} = 1.0µF, C_{GATE} = 1.0nF, C_{FLT} = 500pF, R_T = 374kΩ, DUTY = GND unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Unit	Conditions
Internal Transconductance Opamp							
GB	Gain-bandwidth product	#	-	1.0	-	MHz	75pF capacitance at COMP pin
A_V	Open loop DC gain	-	65	-	-	dB	Output open
V_{CM}	Input common-mode range	#	-0.3	-	1.5	V	---
V_O	Output voltage range	#	0.7	-	V_{DD}-0.7	V	A_V ≥ 65dB
G_m	Transconductance	-	-	500	-	µA/V	---
V_{OFFSET}	Input offset voltage	*	-3.0	-	3.0	mV	---
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
$I_{COMP,DIS}$	Discharging current with pull down FET	-	10	-	-	mA	V_{COMP} = 2.0V
$I_{COMP,LKG}$	COMP leakage current	*	-	-	10	nA	PWMD = GND; COMP = 2.0V
GB_{BUFFER}	Gain-bandwidth of the buffer	#	20	-	-	kHz	---
VIN Pin							
$UV_{LO\_RISE,VIN}$	V_{IN} under voltage lockout threshold	*	2.62	2.76	2.90	V	V_{IN} rising
$UV_{LO\_HYST,VIN}$	V_{IN} under voltage hysteresis	-	-	0.20	-	V	V_{IN} falling
DR and FLAG pins							
V_{REF}	Comparator reference voltage	*	1.58	1.75	1.92	V	---
T_{PROP_DELAY}	Propagation delay time	-	-	-	200	ns	V_{DR} = V_{REF} +0.1V
$V_{CLAMP,DR}$	Clamp Voltage at DR pin	*	2.00	-	2.50	V	Current into DR pin = 50µA
		*	2.75	-	3.20	V	Current into DR pin = 1mA
$I_{SOURCE,FLAG}$	Source current from FLAG pin	-	10	-	-	mA	FLAG = GND
$I_{SINK,FLAG}$	Sink current into FLAG pin	-	10	-	-	mA	FLAG = GND
$T_{RISE,FLAG}$	GATE output rise time	-	-	-	40	ns	C_{FLAG} = 500pF
$T_{FALL,FLAG}$	GATE output fall time	-	-	-	40	ns	C_{FLAG} = 500pF
Wiring Fault Detection (PWMD high)							
V_{REF1}	COMP rail comparator detect threshold	-	-	V_{DD}-0.3	-	V	---
V_{REF2}	FB low comparator threshold	-	-	0.1	-	V	---
T_{PROP_DELAY}	Propagation delay time	-	-	-	200	ns	50mV overdrive
Over Current Protection							
K_{OCP}	Multiplication factor for over-current protection	*	1.95	2.00	2.05	-	---
V_{OCP}	Minimum voltage at output of gain stage	*	0.22	-	0.24	V	REF = GND
$T_{BLANK,OCP}$	Blanking time for OCP	*	500	-	900	ns	---
T_{PROP_DELAY}	Propagation delay time	*	-	-	200	ns	50mV overdrive

Note:

 # Denotes specifications guaranteed by design

Functional Block Diagram



Note:

Circuit in shaded area is powered off the VIN pin; rest of the circuit is powered off the VDD regulator (powered off VCC for the gate drivers)

VCC, VDD and Gate Drivers

The external voltage applied at VCC is used to power the IC. The voltage at this pin is typically 12V+/-15% with a 16V abs max rating.

An internal linear regulator is used to generate 3.3V at VDD pin which is used to power the low voltage analog circuit. The voltage at VDD pin can also be used as a reference to set the LED current using a resistor divider from VDD to the REF pin.

Both VCC and VDD have built-in UVLO to disable the IC in case the voltages at the pins are lower than expected.

The gate drivers are powered off directly from the VCC pin. The switching gate driver currents are supplied from the low ESR capacitor connected externally at the VCC pin.

G_M Amplifier and PWM dimming

The G_M amplifier is used to control the LED current. The current level is set by the voltage at the REF pin and the LED current is sensed by a current sense resistor and the voltage across the sense resistor is fed into the FB pin. The compensation capacitor is connected between COMP and GND.

When PWMD is high, the OTA is allowed to control the voltage at the COMP pin. When PWMD is low, the OTA is disconnected from the COMP pin. The leakage current at the COMP pin due to all circuitry connected to it (ESD protection, pull down transistor and disconnect switch) should be less than 10nA.

The pull down FET at the COMP pin is used to discharge the COMP capacitor at startup and during fault conditions.

Boost FET current sense

The current sense pin has a built in 100 - 250ns blanking time. It also has a pull down FET which is turned on whenever the GT is off. This is to facilitate slope compensation using an external resistor/capacitor network. Although most applications with this IC are expected to be DCM boost circuits which do not need slope compensation, the pull-down FET is included for to make the part usable for CCM boost converters as well.

Hiccup timer

Hiccup timing is achieved by using an internal 8-bit counter which counts 1024 clock cycles. This makes the hiccup time dependent on the switching frequency.

Startup

When power is initially applied to the IC, POR1 goes high. At this point, two latches – Fault latch and POR1 latch – are set and FLT goes high. The POR1 latch output will be high untill the first PWM pulse is applied at PWMD. This keeps the counter cleared and enabled till the PWMD pulse is applied. Once the first PWM dimming pulse is applied, the counter is allowed to count to 256, at which point the gate drivers and COMP pin are released, and the converter can start regulating the LED current.

Over-Voltage and Over-Current Fault

Over-voltage is detected using the voltage at the OVP pin. When the voltage at OVP exceeds 2.0V, over-voltage is triggered and the over-voltage condition is said to exist untill the voltage at OVP drops below 1.8V (10% lower).

Over-current condition is detected by the over-current comparator, which compares the voltage at the FB pin with two-times the voltage at the REF pin.

As long as these fault conditions exist, they set the Fault latch, which turns off the gate drivers and clears the 8-bit counter and keeps the counter cleared. Once the fault disappers, the counter is allowed to count and the operation of the IC is identical to the startup case.

Short Circuit to Chassis Condition

A wiring fault condition occurs during the manufacturing process involving large LED strings. Consider a case of three LED light bars connected in series and driven from the same boost converter. The input to the boost converter is typically about 120V. Assume each LED light bar has a forward drop of about 80V (25 LEDs with 3.2V/per LED). If one of the connections between the LED light bars is shorted to ground (see Fig.1), then the boost converter looses the feedback signal since all the current flows through the short bypassing the sense resistor.

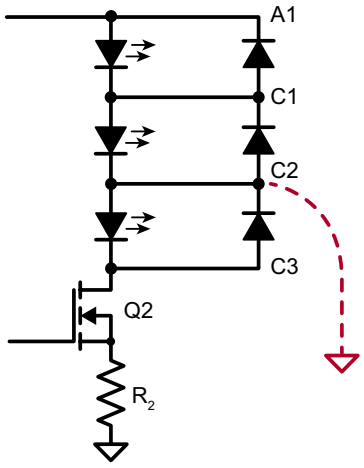


Fig.1 : Short Circuit to Chassis

In this case, COMP will rail to VDD and the boost converter will operate at its maximum power limit. This excessive current through the first two light bars could damage the LEDs.

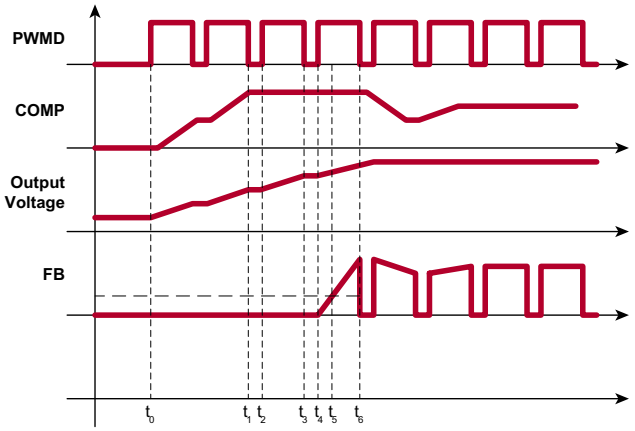
This situation needs to be detected and prevented. Note that turning off the boost converter might not be sufficient in all cases. For example, if C1 was shorted in ground in Fig.1, the LED string voltage (one string; 80V) is lower than the input voltage (120V) and turning off the boost converter will not prevent the short circuit current. Hence, the main solution – besides turning off the boost converter – is to signal the 120V power supply to turn off. This is achieved by means of the FLAG output.

In the HV9966, a short cathode condition is detected by sensing the drain voltage of the disconnect FET. However, the drain voltage of the disconnect FET is zero when PWMD is high. So, the detection is separated into two cases – PWMD high and PWMD low – and each case is detected differently.

Detection of Short Circuit to Chassis when PWMD is High

When a wiring fault condition occurs while the boost converter is running, FB will go to zero and COMP will rail to VDD. This is the condition that is used to detect a short circuit to chassis. However, this condition is also likely to happen at startup.

If the COMP capacitor is low (to achieve a fast transient response) and the output capacitor is large, the startup waveforms may look as shown below (Fig. 2).



In Fig.2, the first PWMD pulse is applied at t_0.

t_0-t_1: Since FB is zero, COMP voltage starts ramping up. Given the large output capacitor, COMP hits VDD before the output capacitor voltage can meet the LED string voltage.

t_1-t_2: At this point, COMP = V_{DD} and FB<0.1V. This sets signal OL1. This resets the counter and the counter is ready to count when PWMD is high.

t_2-t_3: In this time interval, both OLP1 and OLP2 are high and the counter is counting.

t_3-t_4: In this interval, OLP2 = 0 and counter is disabled and so holds its previous state. Enabling the counter only when PWMD is high ensures that the delay time is measured only when PWMD is high, effectively scaling the delay time by the PWMD duty cycle. If the converter were started with a low PWM dimming duty cycle, not scaling the delay time would cause a false detection since the counter would have reached 256 long before COMP can respond (since COMP responds only when PWMD is HI).

t_4-t_5: At t_5, FB = 0.1V and counter has not yet reached 256.

The programmed delay helps to avoid false detection of an open circuit condition at startup or due to a transient condition as described above. Thus, once the condition is detected, the IC waits for the programmed time and if the counter goes all the way to 256, then the IC turns off and pulls FLAG down. The IC can be turned on only by cycling the voltage at V_{IN}.

Detection of Short Circuit to Chassis when PWMD is Low

When PWMD is off, or VCC is not applied, the wiring fault is detected by sensing the voltage at the drain pin of the disconnect FET. This part of the IC is powered by the voltage at the VIN pin and not through the VCC pin. This makes the fault detection independent of the power sequence of the various supplies (VCC, VIN and PWMD).

For the scheme to work, one of two things is required – either one diode per LED light bar (as shown in Fig.1) or a parallel Zener diode across each LED (which typically exist in many LEDs used for backlighting applications).

During normal operation (no short to chassis), the drain of the disconnect FET is pulled to ground when PWMD is high. When PWMD goes low, this FET is turned off. At that time, the parasitic capacitance at the drain node (node C3 in Fig. 1), is charged to the output voltage through resistor R_1. The voltage at the drain is then sensed through resistor divider R_2/R_3 (which may or may not be used).

There is a built in delay which is equal to 64 switching cycles (about 640us at 100kHz switching frequency). Resistor R_1 is programmed such that the voltage at DR pin exceeds 2.0V within this delay time.

Case 1: Short circuit to chassis condition occurs during normal operation

Assuming the antiparallel diodes are used, if there is a wiring fault condition, then the current through R_1 will flow through the antiparallel diodes into the short and the drain node will not exceed one or two diode drops above ground. Thus, a fault condition is detected and it is flagged.

Note: If the PWM dimming duty cycle is large enough that the dimming off-time is less than the delay, then this method of fault detection will not work. However, the detection will occur under PWMD high.

Case 2: Short circuit to chassis condition occurs when VCC is off

In this case, when the 120V boost power supply comes on, the voltage at VIN is regulated to 4.7V using the external Zener diode. Once the voltage at VIN is stabilized, the IC waits for 64 cycles of the clock. Once the timer has run out, if the DR pin is still below 2.0V, then the IC FLAGs a fault.

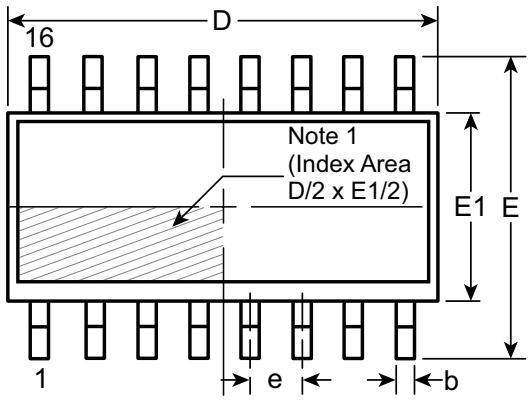
Note: For ESD protection, back to back diodes are needed between the VIN and VDD pins. When V_{CC} is applied, the 4.7V at VIN pin combined with the 5.0V at VDD ensure that the external Zener diode will not be powered through VDD. When V_{CC} is not applied, the voltage at VDD will be 4.7 – 0.6V = 4.1V, which is lower than its UVLO setting. This will keep the IC off and ensure that it is not powered on through the VIN pin.

Pin Description (16-Lead SOIC)

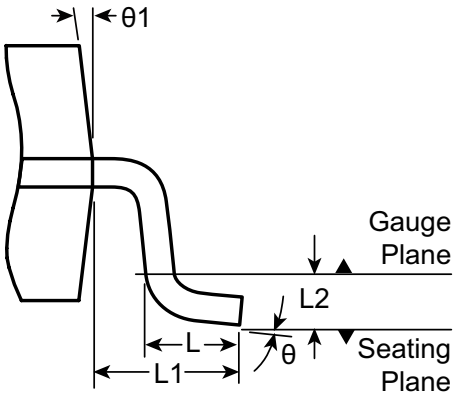
Pin #	Name	Description
1	DR	This pin is connected to the drain of the disconnect FET through a resistor divider and is used to detect a short circuit to chassis wiring fault.
2	DUTY	This pin sets the duty cycle output for the IC. Connecting DUTY to GND programs the maximum duty cycle to 90%, whereas connecting it to VDD programs the maximum duty cycle to 70%.
3	RT	This pin sets the frequency of the power circuit. A resistor between RT and GND will program the circuit in constant frequency mode. The switching frequency is synchronized to the PWMD turn on edge.
4	CS	This pin is used to sense the source current of the external power FET. It includes a built-in 100ns (min) blanking time.
5	GND	Ground return for all the low power analog internal circuitry as well as the gate drivers. This pin must be connected to the return path from the input.
6	GATE	This is the GATE driver output for the switching FET.
7	VCC	This pin is the power supply input to the IC.
8	DIS	This pin is used to drive an external disconnect FET which disconnects the load from the circuit during a fault condition or during PWM dimming to achieve a very high dimming ratio.
9	VDD	This pin is the output of the low voltage regulator. A low ESR capacitor should be connected from this pin to GND.
10	OVP	This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 2.0V, the gate output of the HV9966 is turned off and DIS goes low. The IC will turn on when the voltage at the pin goes below 1.8V.
11	COMP	Stable closed loop control can be accomplished by connecting a compensation network between COMP and GND.
12	REF	The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the VDD pin.
13	FB	This pin provides output current feedback to the HV9966 by using a current sense resistor.
14	PWMD	When this pin is pulled to GND (or left open), switching of the HV9966 is disabled. Then an external TTL high level is applied to it, switching will resume.
15	VIN	This pin is powered from the input of the boost power supply so that the logic powered by the VCC pin is enabled even if there is no VCC at the IC. This pin is used to power the wiring fault detection circuit in the IC. An external 3.0V or 3.3V Zener diode is typically used.
16	FLAG	This is an active-low, open drain pin which is used to disable the boost power supply in case of a wiring fault.

16-Lead SOIC (Narrow Body) Package Outline (NG)

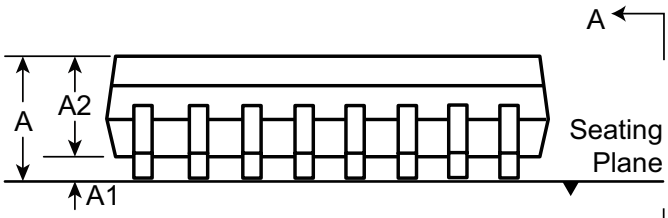
9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



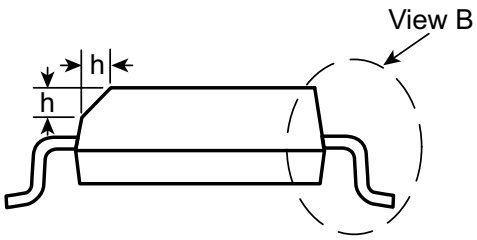
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0^O	5^O
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8^O	15^O

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-16SONG, Version G041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:

HV9966NG-G HV9966NG-G M934